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SL3145

1.6GHz NPN TRANSISTOR ARRAYS

The SL3145 is a monolithic array of five high frequency low current NPN transistors. The SL3145 consists of 3 isolated transistors and a differential pair in a 14 lead SO package The transistors exhibit typical f_{TS} of 1.6GHz and wideband noise figures of 3.0dB The device is pin compatible with the CA3046.

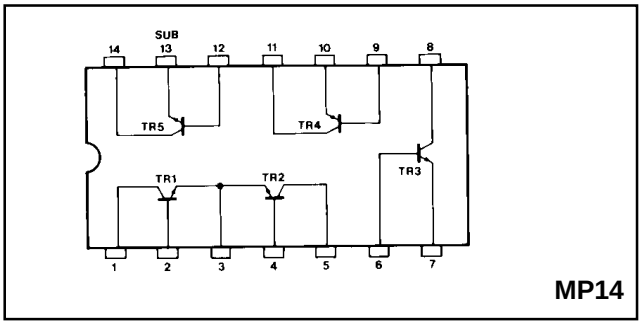

Fig.1 Pin connections SL3145

FEATURES

- f_T Typically 1.6GHz
- Wideband Noise Figure 3.0dB
- V_{BE} Matching Better Than 5mV

APPLICATIONS

- Wide Band Amplifiers
- PCM Regenerators
- High Speed Interface Circuits
- High Performance Instrumentation Amplifiers
- High Speed Modems

ORDERING INFORMATION

SL3145 C MP

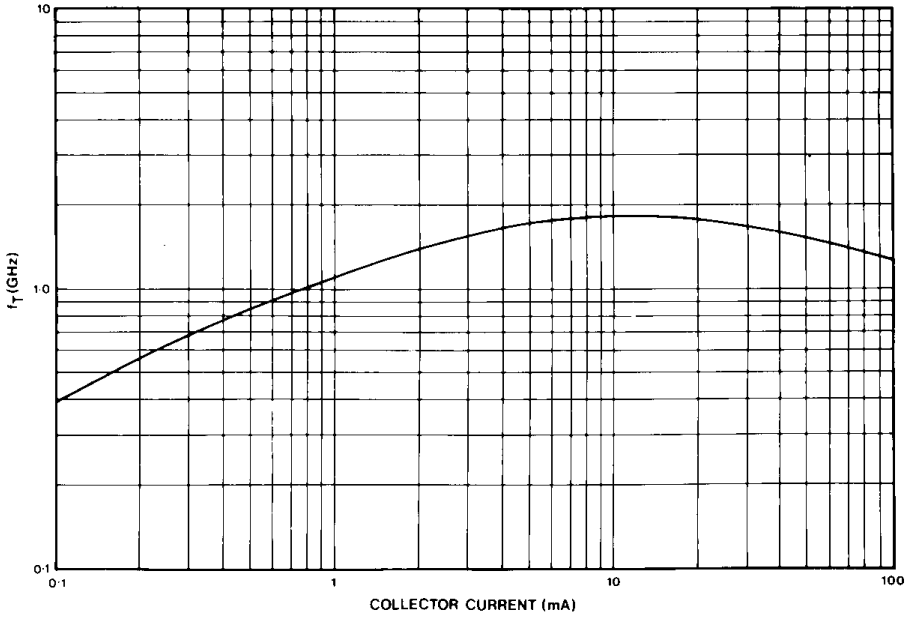

Fig.2 Transition frequency (f_T) v. collector current (V_{CB}= 2V, f=200MHz)

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following test conditions (unless otherwise stated)

T_{amb} = 22°C ± 2°C

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Static characteristic						
Collector base breakdown	BV_{CBO}	20	30		V	I_C = 10µA, I_E = 0
Collector emitter breakdown	LV_{CEO}	15	18		V	I_C = 1mA, I_B = 0
Collector substrate breakdown (isolation)	BV_{CIO}	20	55		V	I_C = 10µA, I_R = I_E = 0
Base to isolation breakdown	BV_{BIO}	10	20		V	I_B = 10µA, I_C = I_E = 0
Base emitter voltage	V_{BE}	0.64	0.74	0.84	V	V_{CE} = 6V, I_C = 1mA
Collector emitter saturation voltage	V_{CE}(SAT)		0.26	0.5	V	I_C = 10mA, I_B = 1mA
Emitter base leakage current	I_{EBO}		0.1	1	µA	V_{EB} = 4V
Base emitter saturation voltage	V_{BE}(SAT)		0.95		V	I_C = 10mA, I_B = 1mA
Base emitter voltage difference, all transistors expect TR1, TR2	ΔV_{BE}		0.45	5	mV	V_{CE} = 6V, I_C = 1mA
Base emitter voltage difference TR1, TR2	ΔV_{BE}		0.35	5	mV	V_{CE} = 6V, I_C = 1mA
Input offset current (except for TR1, TR2)	ΔI_B		0.2	3	µA	V_{CE} = 6V, I_C = 1mA
Input offset current TR1, TR2	ΔI_B		0.2	2	µA	V_{CE} = 6V, I_C = 1mA
Temperature coefficient of ΔV_{BE}	$\frac{\partial \Delta V_{BE}}{\partial T}$		2.0		µV/°C	
Temperature coefficiient of V_{BE}	$\frac{\partial V_{BE}}{\partial T}$		-1.6		mV/°C	V_{CE} = 6V, I_C = 1mA
Static forward current ratio	H_{FE}	40	100			V_{CE} = 6V, I_C = 1mA
Collector base leakage	I_{CBO}		0.3		nA	V_{CB} = 16V
Collector isolation leakage	I_{CIO}		0.6		nA	V_{CI} = 20V
Base isolation leakage	I_{BIO}		100		nA	V_{BI} = 5V
Emitter base capacitance	C_{EB}		0.4		pF	V_{EB} = 0V
Collector base capacitance SL3145	C_{CB}		0.4		pF	V_{CB} = 0V
Collector isolation capacitance	C_{CI}		0.8		pF	V_{CI} = 0V
Dynamic characteristics						
Transition frequency SL3145	f_T		1.6		GHz	V_{CE} = 6V, I_C = 5mA
Wideband noise figure	NF		3.0		dB	V_{CE} = 2V, R_S = 1kΩ I_C = 100µA, f = 60MHz
Knee of 1/f noise curve			1		KHz	V_{CE} = 6V, R_S = 200Ω I_C = 2mA

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

All electrical ratings apply to individual transistors. Thermal ratings apply to the total package.

The isolation pin (substrate) must be connected to the most negative voltage applied to the package to maintain electrical isolation.

V_{CB} = 20 volt
V_{EB} = 4.0 volt
V_{CE} = 15 volt
V_{CI} = 20 volt
I_C = 20 mA

Maximum individual transistor dissipation 200 mWatt
Storage temperature -55°C to 150°C
Max junction temperature 150°C

Package thermal resistance (°C/watt):-

Package Type	**MP14**
Chip to case	45°C/W
Chip to ambient	123°C/W

NOTE:
If all the power is being dissipated in one transistor, these thermal resistance figures should be increased by 100°C/watt

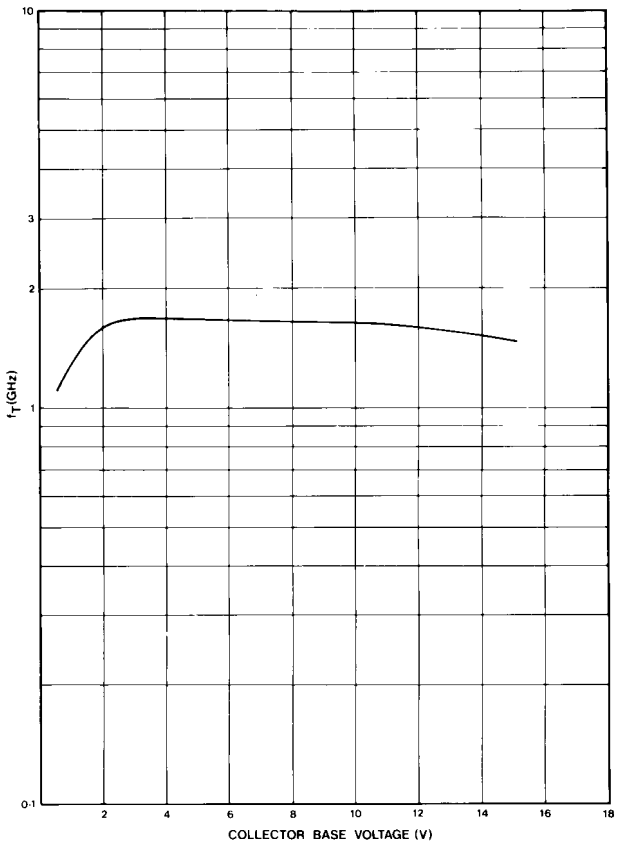

Fig.3 Transition frequency (f_T) v. collector base voltage (I_C = 5mA, Frequency = 200MHz)

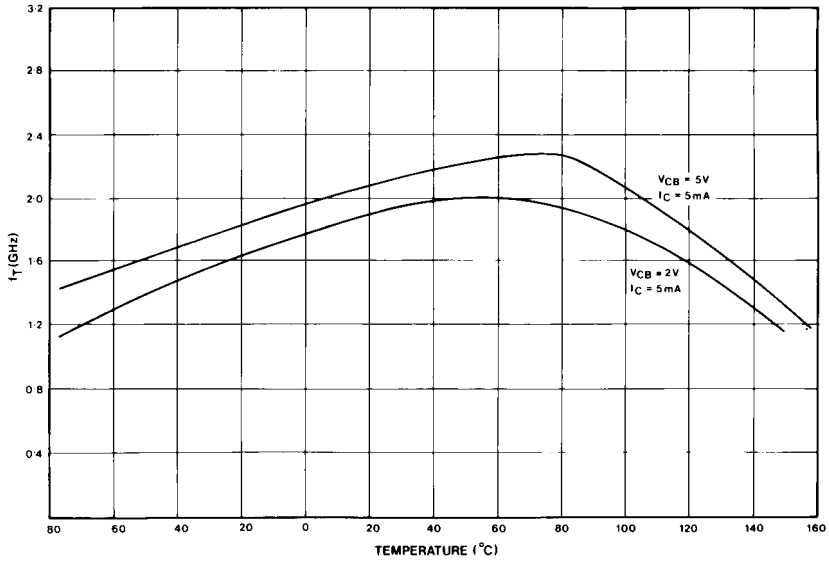

Fig.4 Variation of transition frequency (f_T) with temperature

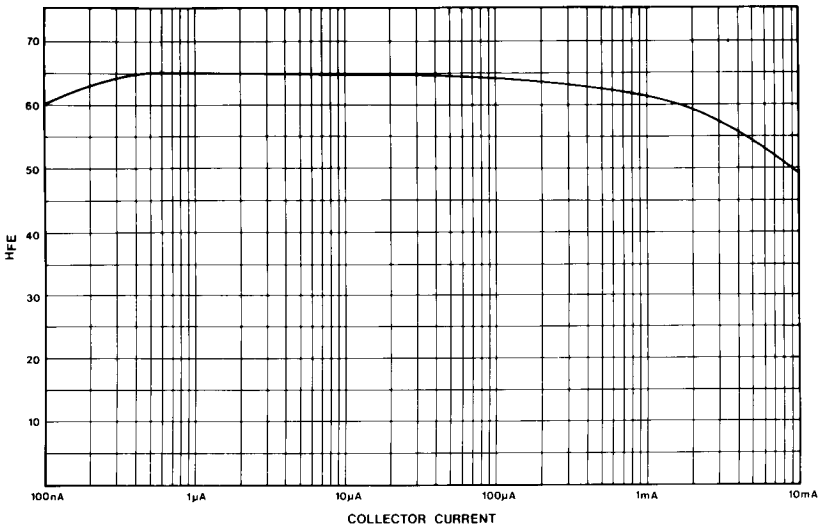

Fig.5 DC current gain v. collector current

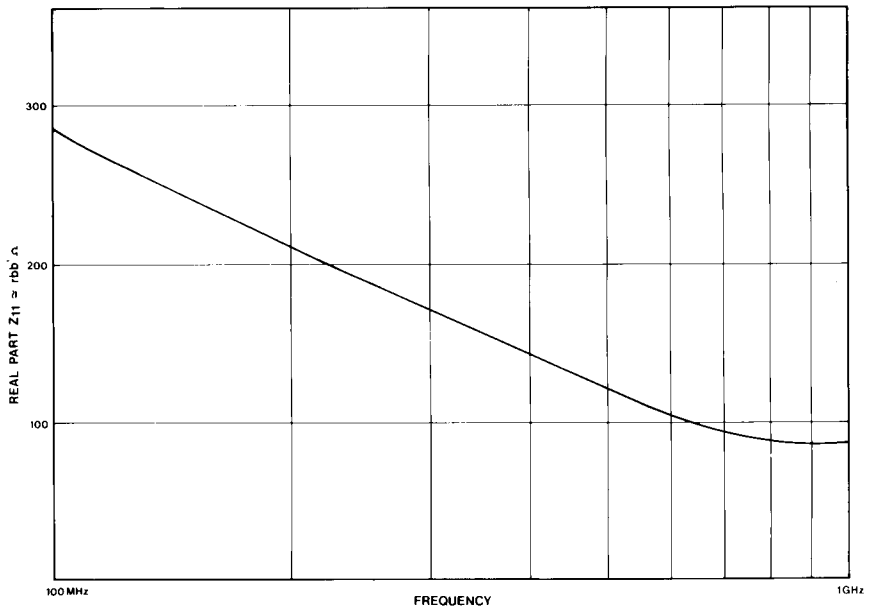

Fig.6 Z_{11} (derived from scattering parameters) v. frequency ($Z_{11} \backsim r_{bb}$)

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