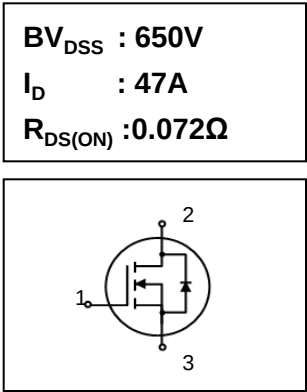
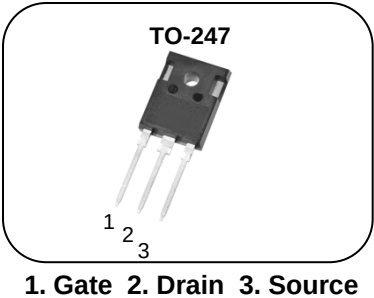


N-Channel Super Junction Power MOSFET

Features

- High ruggedness
- $R_{DS(ON)}$ (Max0.072 Ω)@ $V_{GS}=10V$
- Gate Charge (Typical 152nC)
- Improved dv/dt Capability
- 100% Avalanche Tested



Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DSS}	Drain to Source Voltage	650	V
I_D	Continuous Drain Current (@ $T_C=25^{\circ}C$)	47*	A
	Continuous Drain Current (@ $T_C=100^{\circ}C$)	29.6*	A
I_{DM}	Drain current pulsed (note 1)	188	A
V_{GS}	Gate to Source Voltage	± 30	V
E_{AS}	Single pulsed Avalanche Energy (note 2)	1200	mJ
E_{AR}	Repetitive Avalanche Energy (note 1)	150	mJ
dv/dt	Peak diode Recovery dv/dt (note 3)	5	V/ns
P_D	Total power dissipation (@ $T_C=25^{\circ}C$)	328.9	W
	Derating Factor above 25°C	2.6	W/°C
T_{STG}, T_J	Operating Junction Temperature & Storage Temperature	-55 ~ + 150	°C
T_L	Maximum Lead Temperature for soldering purpose, 1/8 from Case for 5 seconds.	300	°C

*. Drain current is limited by junction temperature.

Thermal characteristics

Symbol	Parameter	Value	Unit
R_{thjc}	Thermal resistance, Junction to case	0.38	°C/W
R_{thcs}	Thermal resistance, Case to Sink		°C/W
R_{thja}	Thermal resistance, Junction to ambient	34.9	°C/W

Electrical characteristic ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Off characteristics						
BV_{DSS}	Drain to source breakdown voltage	$V_{GS}=0V, I_D=250\mu A$	650			V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown voltage temperature coefficient	$I_D=250\mu A$, referenced to 25°C		0.62		$V/^\circ\text{C}$
I_{DSS}	Drain to source leakage current	$V_{DS}=650V, V_{GS}=0V$			1	μA
		$V_{DS}=520V, T_C=125^\circ\text{C}$			50	μA
I_{GSS}	Gate to source leakage current, forward	$V_{GS}=30V, V_{DS}=0V$			100	nA
	Gate to source leakage current, reverse	$V_{GS}=-30V, V_{DS}=0V$			-100	nA
On characteristics						
$V_{GS(TH)}$	Gate threshold voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2		5	V
$R_{DS(ON)}$	Drain to source on state resistance	$V_{GS}=10V, I_D = 23A$		60	72	m Ω
G_{fs}	Forward Transconductance	$V_{DS} = 30V, I_D = 23A$	32			S
Dynamic characteristics						
C_{iss}	Input capacitance	$V_{GS}=0V, V_{DS}=25V, f=1\text{MHz}$		5700		pF
C_{oss}	Output capacitance			3990		
C_{rss}	Reverse transfer capacitance			30		
$t_{d(on)}$	Turn on delay time	$V_{DS}=325V, I_D=47A, R_G=25\Omega$ (note 4, 5)		70		ns
t_r	Rising time			99		
$t_{d(off)}$	Turn off delay time			302		
t_f	Fall time			84		
Q_g	Total gate charge	$V_{DS}=520V, V_{GS}=10V, I_D=47A$ (note 4, 5)		152		nC
Q_{gs}	Gate-source charge			48		
Q_{gd}	Gate-drain charge			66		

Source to drain diode ratings characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Continuous source current	Integral reverse p-n Junction diode in the MOSFET			47	A
I_{SM}	Pulsed source current				188	A
V_{SD}	Diode forward voltage drop.	$I_S=47A, V_{GS}=0V$			1.26	V
T_{rr}	Reverse recovery time	$I_S=20A, V_{GS}=0V,$		1584		ns
Q_{rr}	Reverse recovery Charge	$di_F/dt=100A/\mu s$		31		μC

※. Notes

1. Repeative rating : pulse width limited by junction temperature.
2. $L = 37.2\text{mH}, I_{AS} = 8A, V_{DD} = V, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 20A, di/dt = 100A/\mu s, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse Width $\leq 300\mu s$, duty cycle $\leq 2\%$
5. Essentially independent of operating temperature.

Fig. 1. On-state characteristics

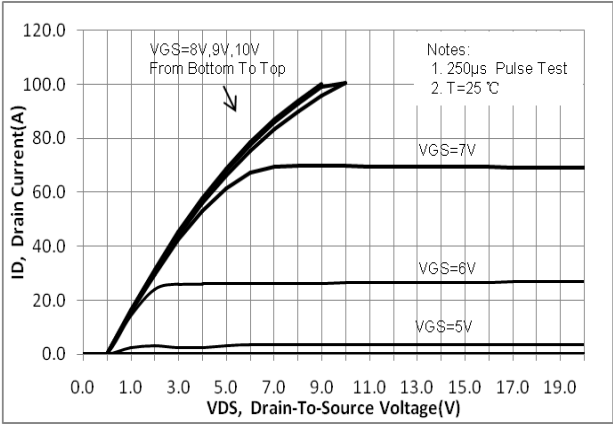


Fig. 2. On-resistance variation vs. drain current and gate voltage

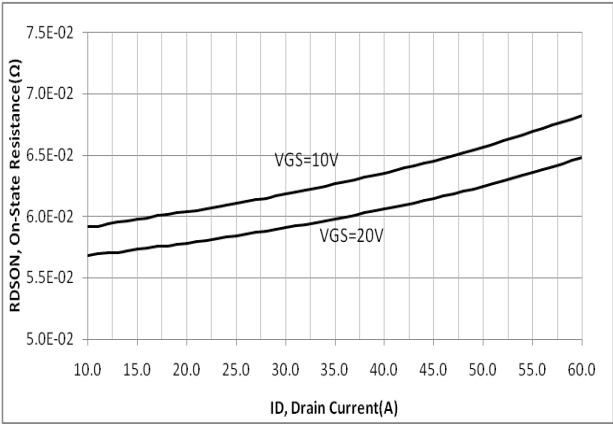


Fig. 3. Gate charge characteristics

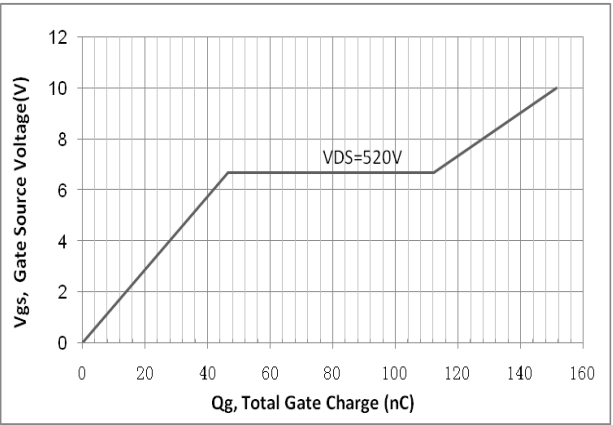


Fig. 4. On state current vs. diode forward voltage

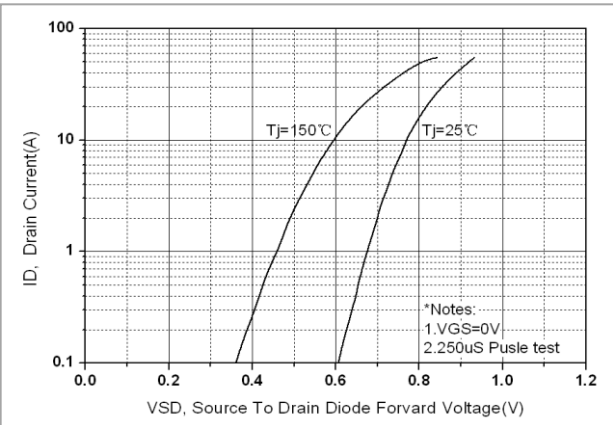


Fig 5. Breakdown Voltage Variation vs. Junction Temperature



Fig. 6. On resistance variation vs. junction temperature

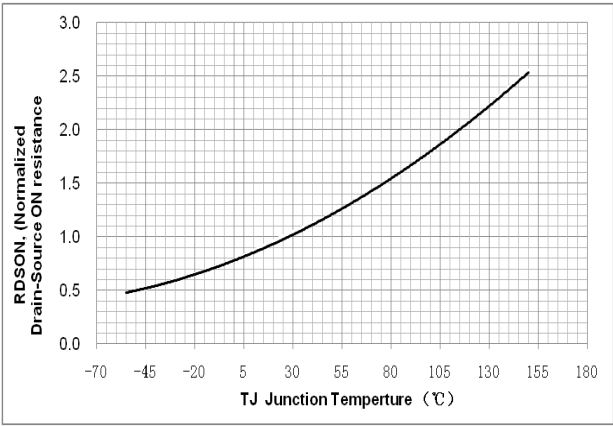


Fig. 7. Maximum safe operating area

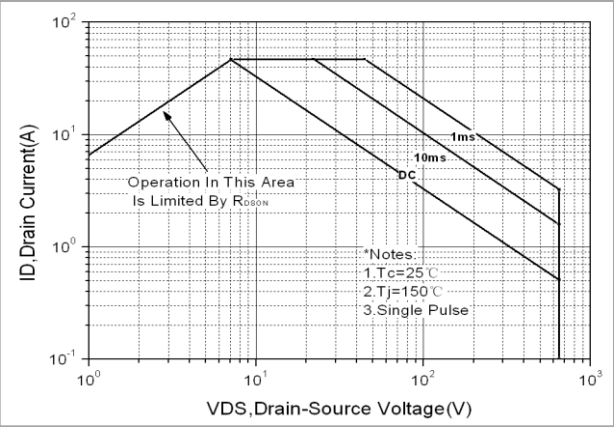


Fig. 8. Transient thermal response curve

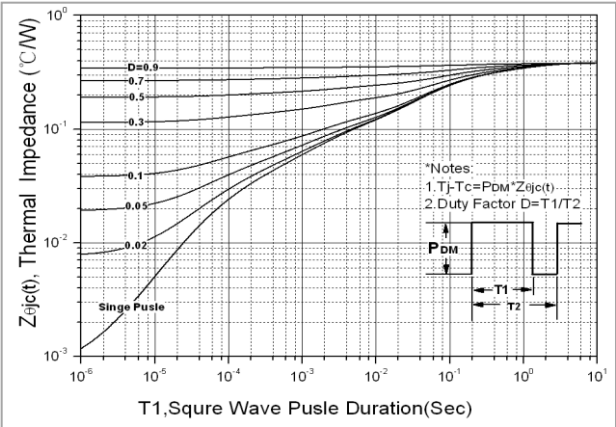


Fig. 9. Capacitance Characteristics

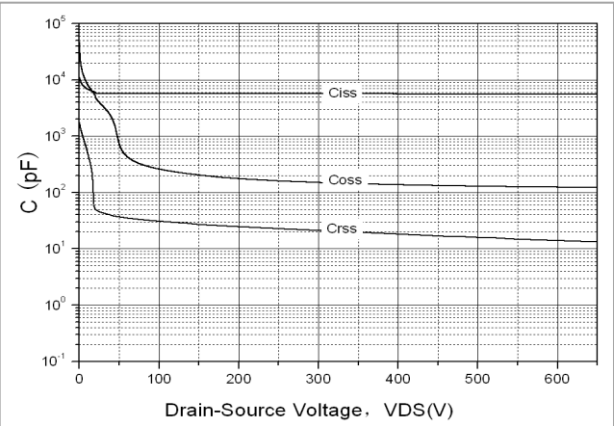


Fig. 10. Gate charge test circuit & waveform

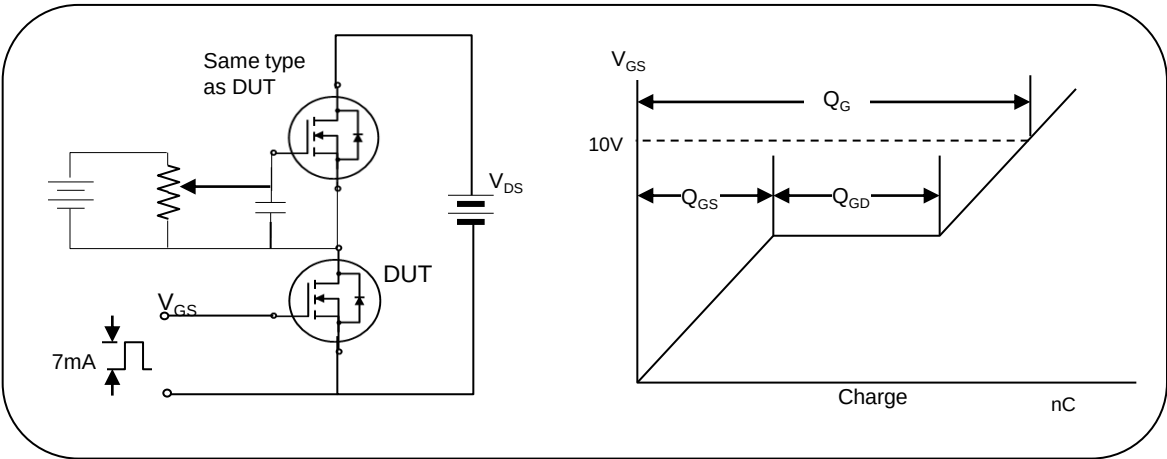


Fig. 11. Switching time test circuit & waveform

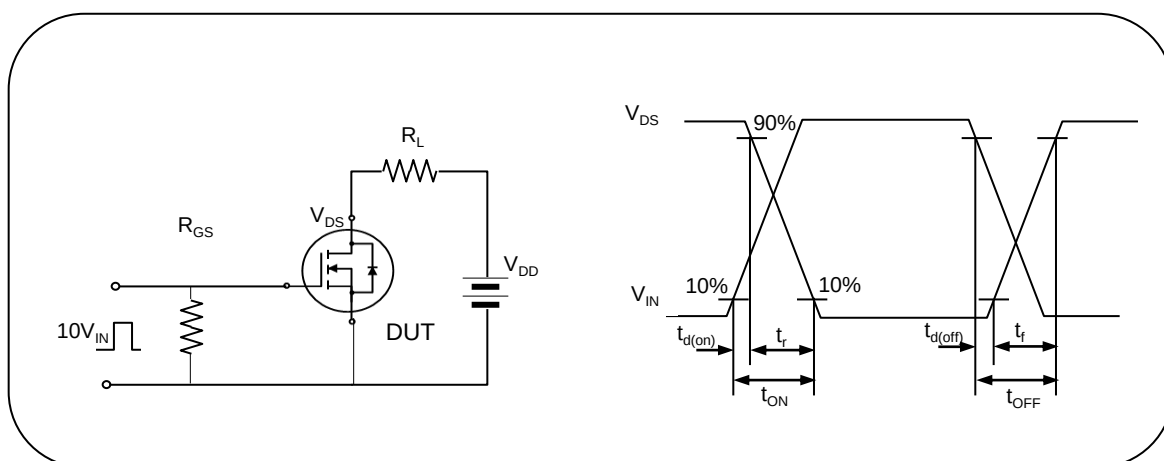


Fig. 12. Unclamped Inductive switching test circuit & waveform

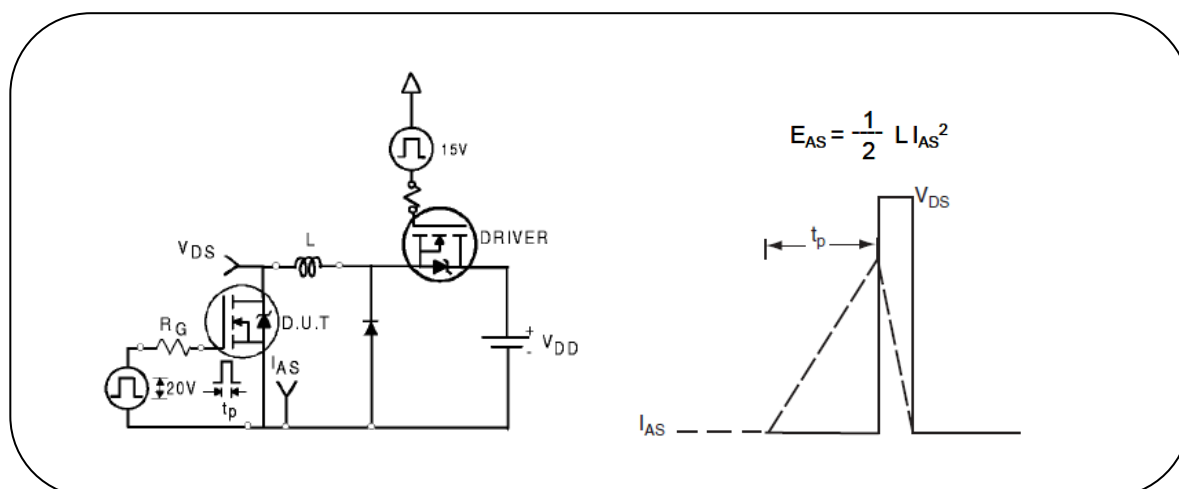


Fig. 13. Peak diode recovery dv/dt test circuit & waveform

