

SL531C

250MHz TRUE LOG IF AMPLIFIER

T-73-43

The SL531C is a wide band amplifier designed for use in logarithmic IF amplifiers of the true log type. The input and log output of a true log amplifier are at the same frequency i.e. detection does not occur. In successive detection log amplifiers (using SL521, SL1521 types) the log output is detected.

The small signal gain is 10dB and bandwidth is over 500MHz. At high signal levels the gain of a single stage drops to unity. A cascade of such stages give a close approximation to a log characteristic at centre frequencies between 10 and 200MHz.

An important feature of the device is that the phase shift is nearly constant with signal level. Thus any phase information on the input signal is preserved through the strip.

The device is also available as the SL531AC which has guaranteed operation over the full Military Temperature Range and is screened to MIL-STD-883C Class B. Data is available separately.

FEATURES

- Low Phase Shift vs Amplitude
- On-Chip Supply Decoupling
- Low External Components Count

APPLICATIONS

True Log Strips with:—

- Log Range 70 dB
- Centre frequencies 10 – 200 MHz
- Phase Shift ± 0.5 degrees / 10 dB

ABSOLUTE MAXIMUM RATINGS

Supply voltage	+12 volts
Storage temperature range	-55°C to +150°C
Operating temperature range	-55°C to +125°C
	See operating notes
Max junction temperature	150°C
Junction — ambient thermal resistance	220°C/Watt
Junction — case thermal resistance	80°C/Watt

CIRCUIT DESCRIPTION

The SL531 transfer characteristic has two regions. For small input signals it has a nominal gain of 10 dB, at large signals the gain falls to unity (see Fig 7). This is achieved by operating a limiting amplifier and a unity gain amplifier in parallel (see Fig 3). Tr1 and Tr4 comprise the long tailed pair limiting amplifier, the tail current being supplied by Tr5, see Fig 2. Tr2 and Tr3 form the unity gain amplifier the gain of which is defined by the emitter resistors. The outputs of both stages are summed in the 300 ohm resistor and Tr7 acts as an emitter follower output buffer. Important features are the amplitude and phase linearity of the unity gain stage which is achieved by the use of 5GHz transistors with carefully optimised geometries.

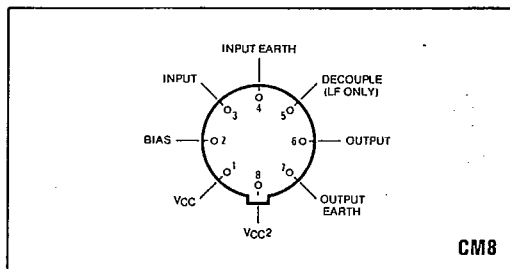


Fig. 1 Pin connections

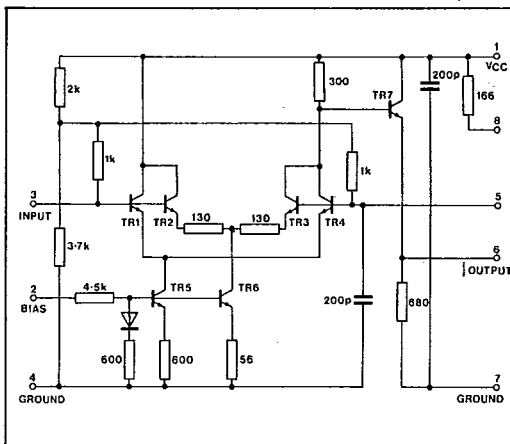


Fig. 2 Circuit diagram

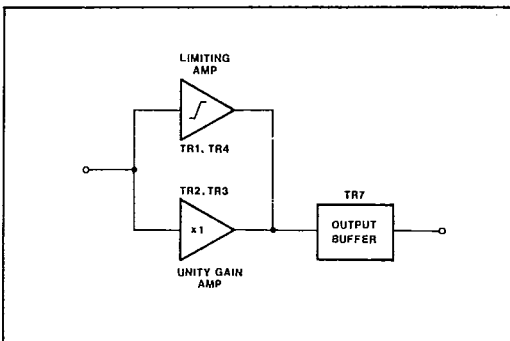


Fig. 3 Block diagram

ELECTRICAL CHARACTERISTICS

PLESSEY SEMICONDUCTORS

Test Conditions (unless otherwise stated):

Test circuit Fig (4)
Frequency 60 MHz
Supply voltage 9 volts
Ambient temperature $22 \pm 2^\circ\text{C}$

Characteristic	Value			Units	Conditions
	Min	Typ	Max		
Small signal voltage gain	8	10	12	dB	$V_{in} = -30 \text{ dBm}$
High level slope gain	-1	0	+1	dB	
Upper cut off frequency	250	500		MHz	-3dB w.r.t. $\pm 60 \text{ MHz}$
Lower cut off frequency		3	10	MHz	
Supply current		17	25	mA	
Phase change with input amplitude		1.1	3	degrees	$-V_{in} = 30 \text{ dBm to } +10 \text{ dBm}$
Input impedance	2.5pF parallel with 1k Ω				$f = 10 - 200 \text{ MHz}$
Output impedance	15 Ω series with 25nH				

OPERATING NOTES

1. Supply Voltage Options

An on chip resistor is provided which can be used to drop the supply voltage instead of the external 180 ohms shown in the test circuit. The extra dissipation in this resistor reduces the maximum ambient operating temperature to 100°C . It is also possible to use a 6 volt supply connected directly to pins 1 and 2. Problems with feedback on the supply line etc may occur in this connection and RF chokes may be required in the supply line between stages.

2. Layout Precautions

The internal decoupling capacitors help prevent high frequency instability, however normal high frequency layout precautions are still necessary. Coupling capacitors should be physically small and be connected with short leads. It is most important that the ground connections are made with short leads to a continuous ground plane.

3. Low Frequency Response

The LF response is determined by the on chip capacitors. It can be extended by extra external decoupling on pins 5 and 1.

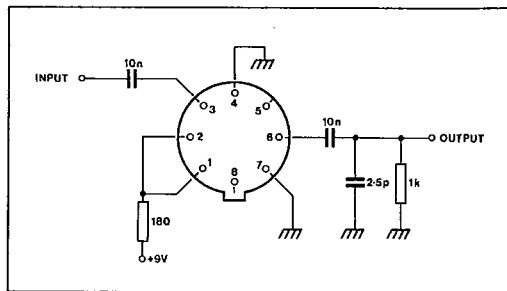


Fig. 4 Test circuit

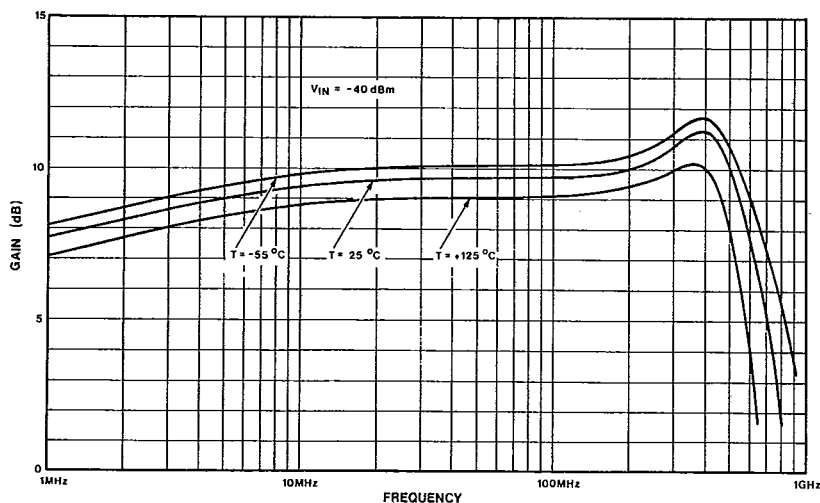


Fig. 5 Small signal frequency response