PLESSEY
Semiconductors

SL650B & C SL651B & C

MODULATOR/PHASE LOCKED LOOP CIRCUITS FOR MODEMS

The SL650/1 are versatile integrated circuits capable of performing all the common modulation functions (AM, PAM, SCAM, FM, FSK, PSK, PWM, tone-burst, delta-modulation, etc.). A wide variety of phase-locked loops can be realised using the SL650 or SL651, with all parameters accurately controllable; they can also be used to generate precise waveforms at frequencies up to 0.2MHz.

The highly accurate and stable variable frequency oscillator is programmable over a wide range of frequency by voltage, current, resistor or capacitor. In addition direct selection of one of four spot frequencies is facilitated by using the on-chip binary interface, which accepts standard logic levels at very low logic '1' input currents.

The differential input phase comparator has a wide common mode input voltage range. It has a high gain limiting amplifier at its input requiring only 1mV input to maintain lock range in a typical phase-locked loop. The current output is programmable from zero to over 2mA by an external resistor or current input, and the gain is voltage –, current –, or resistance – programmable from zero to greater than 10,000.

An auxiliary amplifier with a voltage gain of, typically, 5000 is incorpated in the SL650 for use when it is required to interface to specified levels and impedances. The auxiliary amplifier features low bias current (typically 25nA), fast recovery from overload, and a short-circuit output current of ±7.5mA.

The auxiliary amplifier is omitted from the SL651.

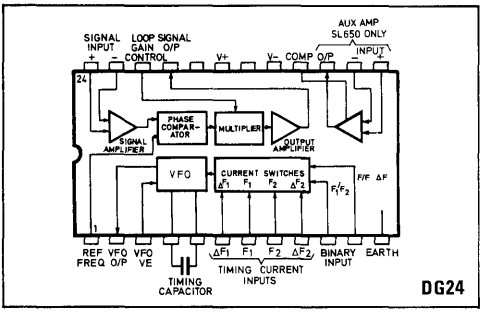

Fig.1 Pin connections (top view)

FEATURES

- VFO Frequency Variable Over 100:1 Range With Same Capacitor: Linearity 0.2%
- VFO Temperature Coefficient:
  'B' Types 20 ppm/°C Max.
  'C' Types 20 ppm/°C Typ.
- Supply sensitivity 20 ppm/% Typ.
- VFO Phase-Continuous at Transitions
- Binary Interface
- Phase Comparator O/P Can Swing to Supply Voltages
- On-Chip Auxiliary Amplifier (SL650)

APPLICATIONS

- Modems
- Modulators
- Demodulators
- Tone Decoders
- Tracking Filters
- Waveform Generators

QUICK REFERENCE DATA

Supply Voltages	±6V
Operating Temperature Range	–55°C to +125°C

ELECTRICAL CHARACTERSTICS

Test conditions (unless otherwise stated)
Supply voltage ±6V
Temperature T_A +22°C ±2°C)

Characteristics	Pins	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current I_{CC}	17,19			3	mA	
Variable frequency oscillator						
Initial frequency offset error		−3	±1	+3	%	
Normal mark/space ratio		0.98	1.00	1.02	–	
Temp. coefficient of frequency			±20		ppm/°C	See note 1
Frequency variation with supplies	17, 19		±20		ppm/%	
Voltage at timing current inputs	6, 7, 8, 9		±10		mV	See note 2
VFO output, 'low' state	2		0	0.2	V	
VFO output, 'high' state	2	+1.1	+1.3		V	$R_L \geqslant 10k\Omega$
Max. freq. of oscillation			0.5		MHz	
Binary inputs						
V_{in} to guarantee logic 'low'	10, 11			+0.6	V	See note 3
V_{in} to guarantee logic 'high'	10, 11	+2.4			V	
Input current	10, 11		0.05	0.25	mA	V_{in} = +3.0V
Phase comparator						
Differential I/P offset voltage	23, 24		±2		mV	V_{out} = 0V
Input bias current	23, 24		0.05	2.5	μA	V_{in} = 0V
Differential input resistance	23, 24		100		kΩ	
Common mode I/P voltage range	23, 24	±4			V	
Differential I/P to limit (AC)	23, 24		1.0	10	mV rms	See note 4
Output current	21, 22	±1.0	±2.0	±5.0	mA	I_{22} = 250μA
Current gain (pin 22 to pin 21)	21, 22	±4	±10		–	See note 5
Transconductance, O/P/diff.I/P	21,23,24	±100	±250		mA/V	See note 5
Output voltage, linear range	21	±5	±5.5		V	
Output current	21			±2	μA	I_{22} = 0
Phase comparator I/P 'low'	1	−4		−0.2	V	
Phase comparator I/P 'high'	1	+1.9		+5.3	V	
Auxiliary amplifier (SL650 only)						
Differential I/P offset voltage	13, 14		±2		mV	V_{out} = 0V
Input bias current	13, 14		0.025	0.5	μA	V_{in} = 0V
Differential I/P resistance	13, 14	0.2	3		MΩ	
Common mode I/P voltage range	13, 14	±4			V	
Voltage gain (13–14) to 15	13,14,15	1000	5000		–	
Output voltage range	15	±4	±4.8		V	$R_L \geqslant 2k\Omega$
Output current limit	15	±4	±6.5	±12	mA	

NOTES

1. With a timing current of 60μA and f = 1kHz (C = 0.01μF, R = 100kΩ, supply voltages = ±6V), the temperature coefficient of frequency of the SL650C is typically ±2.5ppm/°C over the range 0°C to +40°C.
2. This voltage applies for timing currents in the range 20μA to 2mA and with the relevant input selected. In the unselected state the voltage is typically +0.6V.
3. The 'low' state is maintained when the inputs are open-circuited.
4. Limiting will occur earlier if the output (pin 21) voltage-limits first.
5. For a control current input to pin 22 of 250μA The sign of the transconductance is positive when the signal input is positive and the VFO output (or phase comparator input) is 'high.'

ABSOLUTE MAXIMUM RATINGS

Supply voltages	± 7.5V
Storage temperature	−55° to +175°C
Operating temperature	−55° to +125°C
Input voltages	Not greater than supplies

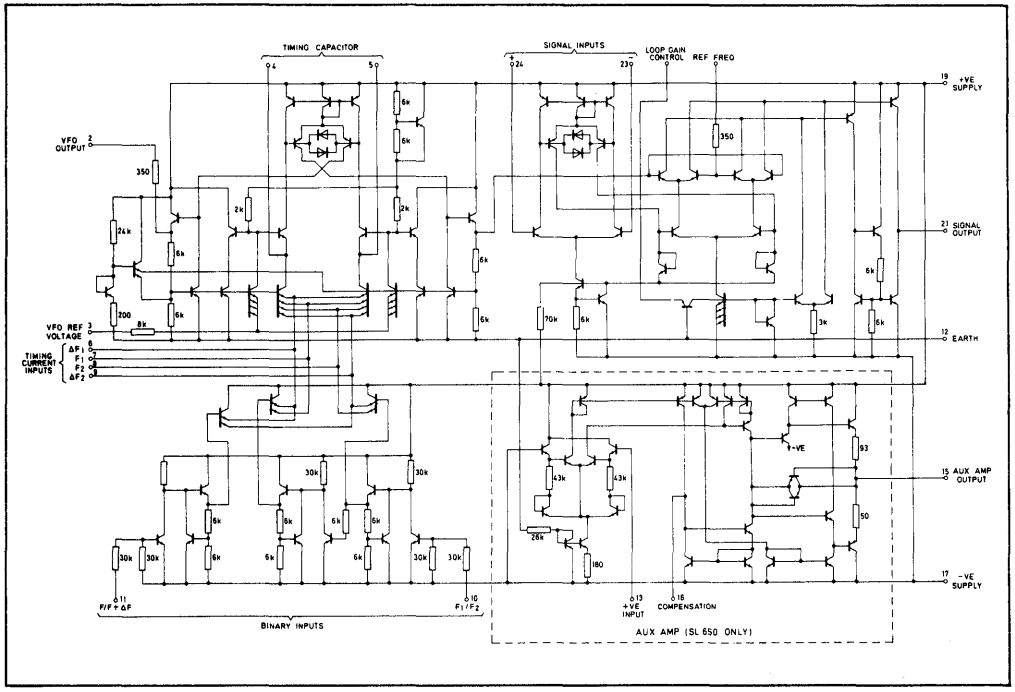

Fig. 2 Circuit diagram of SL650/SL651

OPERATING NOTES

Basic VFO Relationships

The VFO free-running frequency is inversely proportional to the value of the tuning capacitor C, connected to pins 4 and 5, and directly proportional to the VFO timing current (see Fig.3). Four current switches, controlled by TTL-compatible logic inputs on pins 10 and 11 select a combination of external resistors (connected to pins 6, 7, 8 and 9) which determine the VFO timing current. When both logic inputs are low, open-circuit, or connected to 0V however, then only the current switch associated with pin 7 is closed. the VFO timing current is then determined solely by the value of one resistor (R2 in Fig.3), and by the negative voltage connected to that resistor.

In this simplified configuration, as shown in Fig.4 the VFO frequency is determined by the relationship.

$$f = \frac{1}{CR} \cdot \frac{V_R}{V_3}$$

where f is in kHz, V in volts, C in μF and R in kΩ.

If the timing resistor R is returned to the VFO negative supply (pin 3), then

$$V_R = V_3$$

$$\text{and } f = \frac{1}{CR}$$

Pin 3 is normally connected to the chip negative supply; if, however, pin 3 is connected to a separate negative supply then the VFO can be voltage-controlled, and the VFO frequency will be:

$$f = \frac{1}{CR} \cdot \frac{V-}{V_C}$$

where V– is the chip and timing resistor negative supply and V_C is the control voltage connected to pin 3

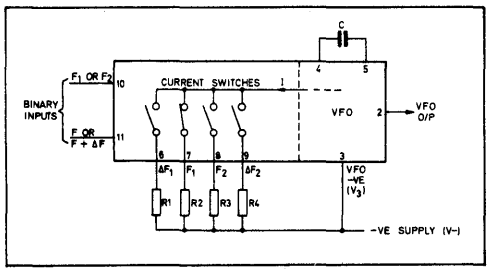

Fig. 3 VFO and binary interface

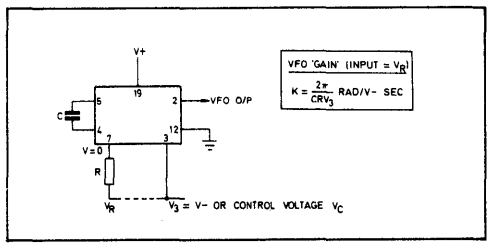

Fig. 4 VFO basic configuration

The timing current I should be between 20μA and 2mA, corresponding to a value for R between 3kΩ and 300kΩ with supplies of ±6V. For accurate timing, CR should be greater than 5μs.

When the binary interface is used as shown in Fig.3 the VFO free-running frequency is dependent on the logic input states, as shown in Table 1.

Pin 10	Pin 11	Timing Pins	VFO Frequency
LO	LO	7	$\frac{1}{CR_2}$
LO	HI	6 & 7	$\frac{1}{CR_2} + \frac{1}{CR_1}$
HI	LO	8	$\frac{1}{CR_3}$
HI	HI	8 & 9	$\frac{1}{CR_3} + \frac{1}{CR_4}$

Table 1 Binary interface relationships

Auxiliary amplifier

Internal compensation provides stability down to a closed loop gain of typically 20dB. A 30pF capacitor connected between pins 16 and 15 will give compensation down to a closed loop gain of unity. The output is short circuit protected but is not recommended for driving loads less than 2k

Phase Comparator

The phase comparator parameters are defined as follows (see Fig.5):

$$\text{Overall transconductance} = \frac{I_{21}}{V_{24} - V_{23}}$$

$$\text{Overall voltage gain} = \frac{V_{21}}{V_{24} - V_{23}}$$

The input amplifier will limit when the peak input ($V_{24} - V_{23}$) exceed ±5mV (typ.). It is recommended that R_L is kept below 5kΩ to avoid saturating the output and introducing de-saturation delays.

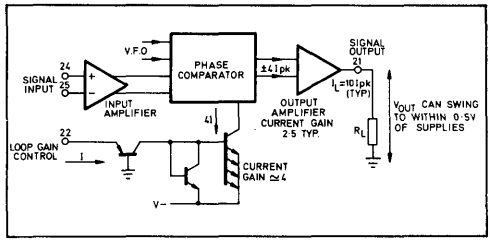

Fig. 5 Phase comparator