

SL6601C

FM IF, PLL DETECTOR (DOUBLE CONVERSION) AND RF MIXER

The SL6601 is a straight through or single conversion IF amplifier and detector for FM radio applications. Its minimal power consumption makes it ideal for hand held and remote applications where battery conservation is important. Unlike many FM integrated circuits, the SL6601 uses an advanced phase locked loop detector capable of giving superior signal to-noise ratio with excellent co-channel interference rejection, and operates with an IF of less than 1MHz. Normally the SL6601 will be fed with an input signal of up to 17MHz: there is a crystal oscillator and mixer for conversion to the IF amplifier, a PLL detector and squelch system.

FEATURES

- High Sensitivity 2 μ V Typical
- Low Power: 2.3mA Typical at 7V
- Advanced PLL Detector
- Available in Miniature 'Chip Carrier' Package
- 100% Tested for SINAD

APPLICATIONS

- Low Power NBFM Receivers
- FSK Data Equipment
- Cellular Radio Telephones

QUICK REFERENCE DATA

- Supply Voltage 7V
- 50dB S/N Ratio

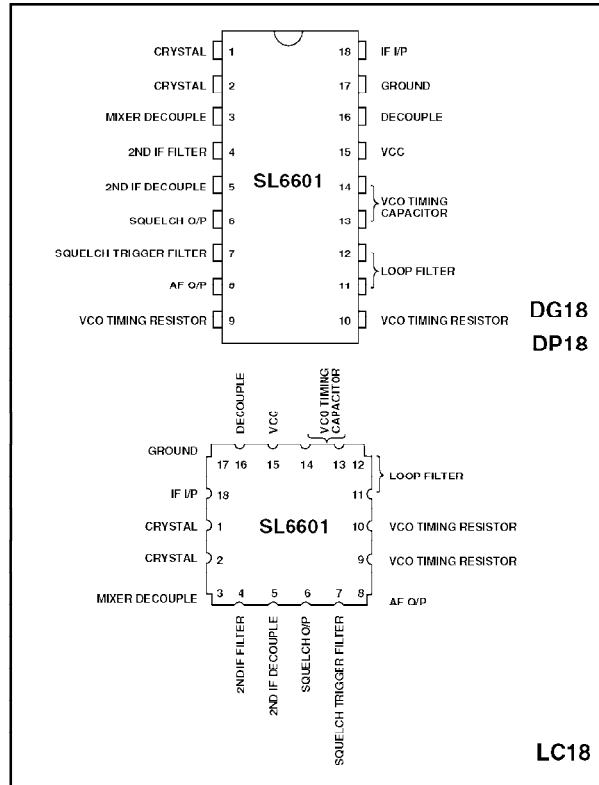


Fig. 1 Pin connections - top view

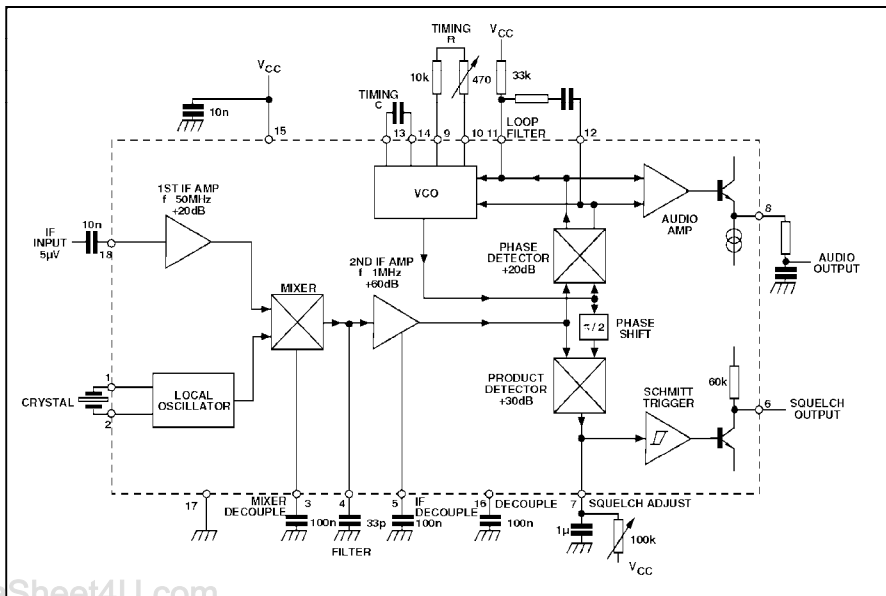


Fig. 2 SL6601 block diagram

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ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply voltage V_{CC} : 7V

Input signal frequency: 10.7MHz, frequency modulated with a 1kHz tone with a ± 2.5 kHz frequency deviation

Ambient temperature: -30°C to $+85^{\circ}\text{C}$; IF = 100kHz; AF bandwidth = 15kHz

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		2.3	2.7	mA	
Input impedance	100		300	Ω	Source impedance = 200 Ω
Input capacity	0.5	2.0	3.5	pF	
Maximum input voltage level	0.5			V rms	At pin 18
Sensitivity	5	2		$\mu\text{V rms}$	At pin 18 for S + N/N = 20dB
Audio output	35	90	140	mV rms	
Audio THD		1.3	3.0	%	1mV rms input at pin 18
S + N/N	30	50		dB	1mV rms input at pin 18
AM rejection	30	Note 1		dB	100 $\mu\text{V rms}$ input at pin 18, 30% AM
Squelch low level		0.2	0.5	V dc	20 $\mu\text{V rms}$ input at pin 18
Squelch high level	6.5	6.9		V dc	No input
Squelch hysteresis		1	6	dB	3 μV input at pin 18
Noise figure		6		dB	50 Ω source
Conversion gain		30		dB	Pin 18 to pin 4
Input gain compression		100		$\mu\text{V rms}$	Pin 18 to pin 4, 1dB compression
Squelch output load	250			k Ω	
Input voltage range	80	100		dB	At pin 8; above 20dB S + N/N
3rd order intercept point (input)		-38		dBm	Input pin 18, output pin 4
VCO frequency					
Grade 1	85		100	kHz	390pF timing capacitor } No input 390pF timing capacitor } 390pF timing capacitor }
Grade 2	95		110	kHz	
Grade 3	105		120	kHz	
Source impedance (pin 4)		25	40	k Ω	
AF output impedance		4	10	k Ω	
Lock-in dynamic range	± 8			kHz	20 μV to 1mV rms at pin 18
External LO drive level	50		250	mV rms	At pin 2
Crystal ESR			25	Ω	10.8MHz

APPLICATION NOTES

IF Amplifiers and Mixer

The SL6601 can be operated either in a 'straight through' mode with a maximum recommended input frequency of 800kHz or in a single conversion mode with an input frequency of 50MHz maximum and an IF of 100kHz or ten times the peak deviation, whichever is the larger. The crystal oscillator frequency can be equal to either the sum or difference of the two IFs; the exact frequency is not critical.

The circuit is designed to use series resonant fundamental crystals between 1 and 17MHz.

When a suitable crystal frequency is not available a fundamental crystal of one third of that frequency may be used, with some degradation in performance.

E.G. If an external oscillator is used the recommended level is 70mV rms and the unused pin should be left O/C. The input is AC coupled via a 0.01 μF capacitor.

A capacitor connected between pin 4 and ground will shunt the mixer output and limit the frequency response of the mixer output and limit the frequency response of the input signal to the second IF amplifier. A value of 33pF is advised when the second IF frequency is 100kHz; 6.8pF is advised for 455kHz.

Phase Locked Loop

The Phase Locked Loop detector features a voltage controlled oscillator with nominal frequency set by an external

capacitor equal to $(40 \pm 7)/f$ pF, where f is the VCO frequency in MHz. The nominal frequency may differ from the theoretical but there is provision for a fine frequency adjustment by means of a variable resistor between the VCO output pins: a value of 470k has negligible effect while 6.8k (recommended minimum value) increases the frequency by approximately 20%.

Care should be taken to ensure that the free running VCO frequency is correct; because the VCO and limiting IF amplifier output produce square waves, it is possible to obtain lock with the VCO frequency fractionally related to the IF, e.g. IF = 100kHz, VCO = 150kHz. This condition can produce good SINAD ratios but poor squelch performance.

The loop filter is connected between pins 11 and 12; a 33k resistor is also required between pin 11 and V_{CC} .

The values of the filter resistor R2 and capacitor C1 must be chosen so that the natural loop frequency and damping factor are suitable for the FM deviation and modulation bandwidth required. The recommended values for various conditions are tabulated below:

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Example

A frequency modulated signal has a deviation of 10kHz and a maximum modulating frequency of 5kHz. The VCO frequency is 200kHz.

Let $f_n = 6\text{kHz}$ and $D = 0.5$

Then from the graph

$$\Phi_{efn} = 0.85$$

$$\Delta f = \frac{0.85 \Delta f}{f_n} = \frac{0.85 \times 10}{6} = 1.4 \text{ rads.}$$

This is too large, so increase f_n e.g. to 10kHz.

$$\frac{f_m}{f_n} = \frac{\Phi_{efn}}{\Delta f} = 0.45$$

$$\Phi_a = \frac{0.45 \times 10}{10} = 0.45$$

- which is somewhat low

Therefore set $f_n = 7.5\text{kHz}$

$$\frac{f_m}{f_n} = 0.666$$

$$\Phi_{efn} = 0.66$$

$$\Delta f = \frac{0.66 \times 10}{7.5} = 0.88 \text{ rads.}$$

$$t_1 + t_2 = \frac{K_o K_D}{(2\pi f_n)^2}$$

$K_o K_D = 0.3f_o$ where f_o is the VCO frequency

$$t_1 + t_2 = \frac{0.3 \times 200 \times 10^3}{(2\pi \times 7.5 \times 10^3)^2} = 27\mu\text{s}$$

$$t_2 = \frac{D}{\pi f_n} - \frac{1}{K_o K_D} = \frac{0.5}{\pi \times 7.5 \times 10^3} - \frac{1}{0.3 \times 200 \times 10^3}$$

$$= 4.5\mu\text{s}$$

$$t_1 = 22.5\mu\text{s}$$

$$C = \frac{t_1}{\text{(use 1nF)}} = \frac{22.5 \times 10^{-6}}{20 \times 10^3} = 1.125\text{nF}$$

$$R = \frac{t_2}{4.5} \times 20 \times 10^3$$

$$= 22.5 \times 20 \times 10^3$$

$$= 4\text{k}\Omega \text{ (use 3.9K)}$$

Actual loop parameters can now be recalculated

$$t_1 = 20\mu\text{s} \quad t_2 = 3.9\mu\text{s}$$

$$2\pi f_n = \frac{(K_o K_D)}{7.97\text{kHz} (t_1 \times t_2)} = \frac{(2 \times 10^5 \times 0.3)}{(23.9 \times 10^{-6})} = 50.1\text{k rad/sec} =$$

$$D = \frac{f_n(t_2 + \frac{1}{K_o K_D})}{K_o K_D} = 0.515$$

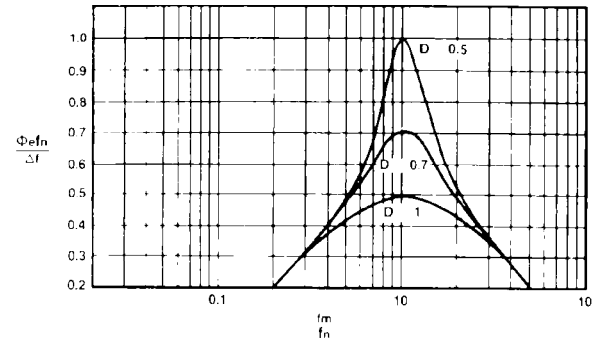


Fig. 3 Damping factor

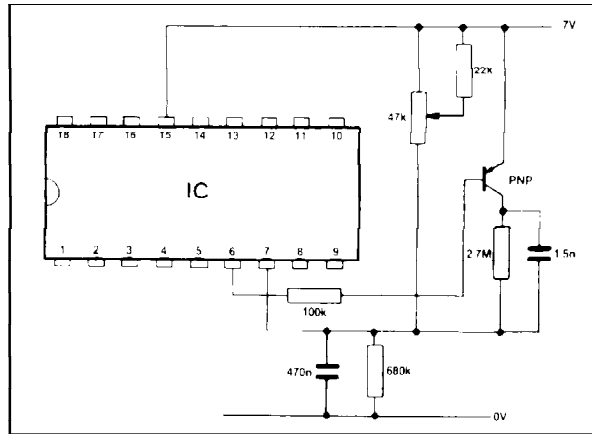


Fig. 4 Using an external PNP in squelch circuit

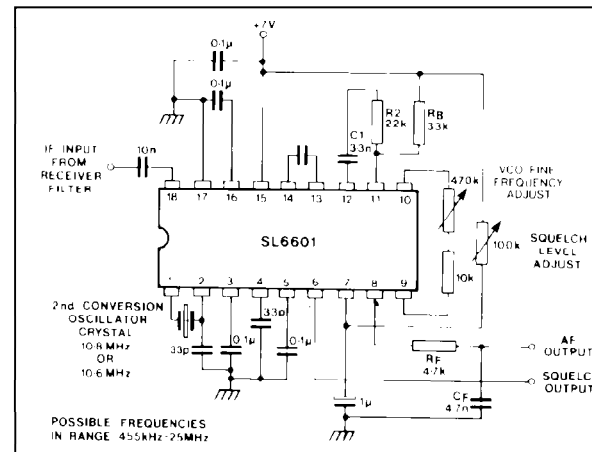


Fig. 5 SL6601 application diagram
(1st IF = 10.7MHz, 2nd IF = 100kHz)

TYPICAL CHARACTERISTICS

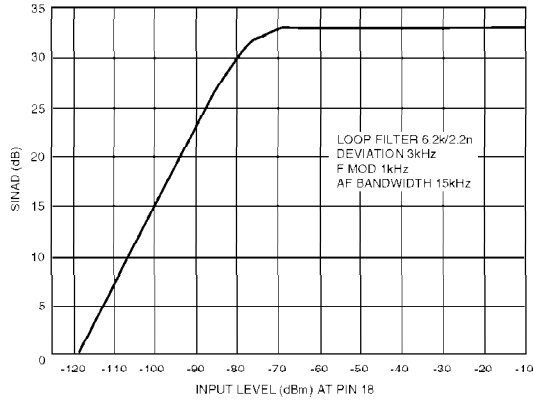


Fig. 6 Typical SINAD (signal + noise + distortion/noise + distortion)

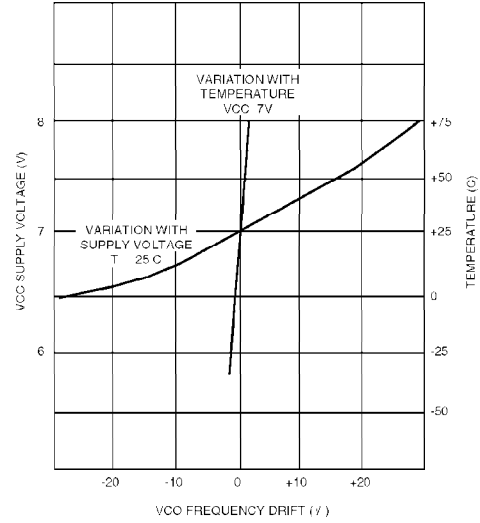


Fig. 9 Typical VCO characteristics

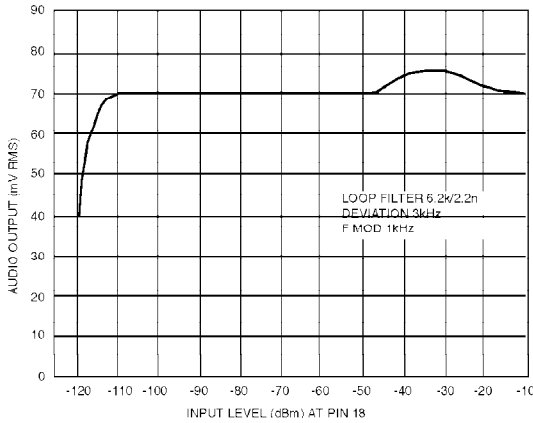


Fig. 7 Typical recovered audio v. input level (3kHz deviation)

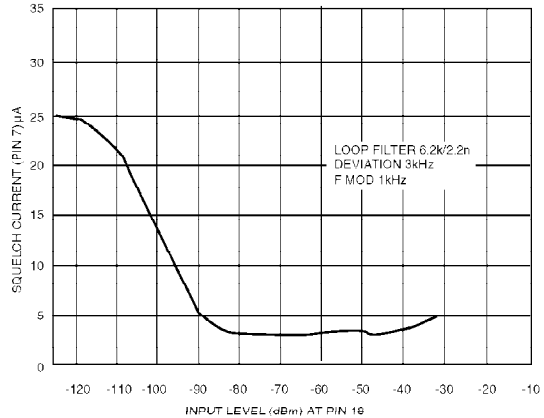


Fig. 10 Typical squelch current v. input level

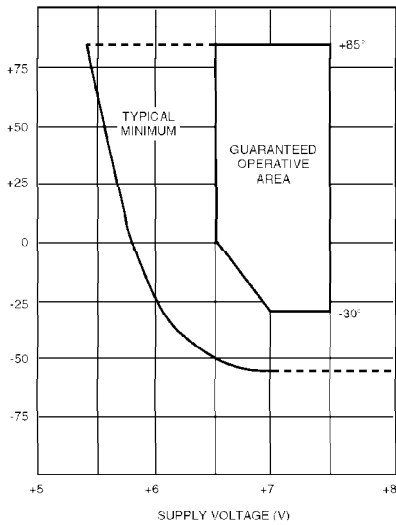


Fig. 8 Supply voltage v. temperature

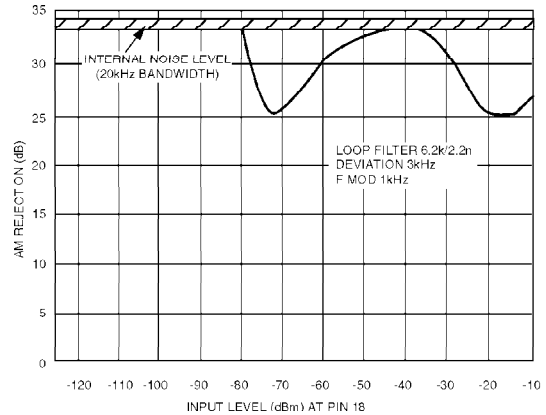


Fig. 11 Typical AM rejection

(the ratio between the audio output produced by:
 (a) a 3kHz deviation 1kHz modulation FM signal and
 (b) a 30% modulated 1kHz modulation AM signal at the same input voltage level.)

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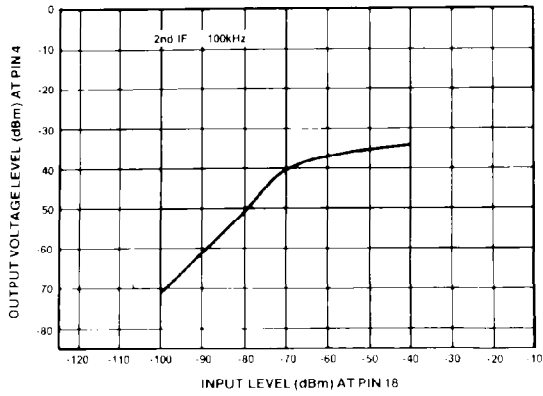


Fig. 12 Typical conversion gain (to pin 4)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	9V
Storage temperature	-55°C to +125°C (DP package)
	-55°C to +150°C (DG)
Operating temperature (see Electrical Characteristics)	-55°C to +125°C
Input voltage	1V RMS at pin 18



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