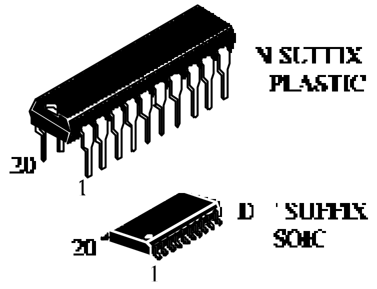
Octal 3-State Inverting Bus Transceiver

High-Performance Silicon-Gate CMOS



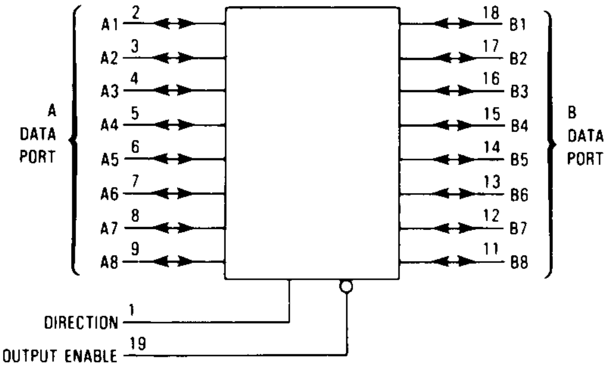
ORDERING INFORMATION
SL74HC640N Plastic
SL74HC640D SOIC
T_A = -55° to 125° C for all packages

The SL74HC640 is identical in pinout to the LS/ALS640. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

The SL74HC640 is a 3-state transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

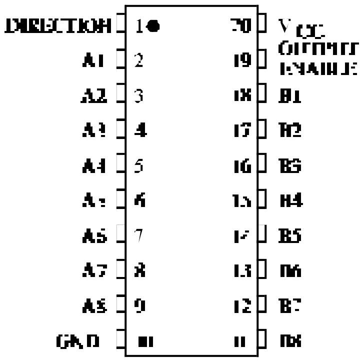
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices

LOGIC DIAGRAM



PIN 20=V_{CC}
PIN 10 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Control Inputs		Operation
Output Enable	Direction	
L	L	Data Transmitted from Bus B to Bus A (inverted)
L	H	Data Transmitted from Bus A to Bus B (inverted)
H	X	Buses Isolated (High Impedance State)

X = don’ t care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V_{CC} +1.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Current, per Pin	±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1) V_{CC} =2.0 V V_{CC} =4.5 V V_{CC} =6.0 V	0 0 0	1000 500 400	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V $\lvert I_{OUT}\rvert \leq 20$ µA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low -Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V $\lvert I_{OUT}\rvert \leq 20$ µA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20$ µA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 6.0$ mA $\lvert I_{OUT}\rvert \leq 7.8$ mA	4.5 6.0	3.98 5.48	3.84 5.34	3.7 5.2	
V_{OL}	Maximum Low-Level Output Voltage	$V_{IN}=V_{IL}$ or V_{IH} $\lvert I_{OUT}\rvert \leq 20$ µA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{IN}=V_{IL}$ or V_{IH} $\lvert I_{OUT}\rvert \leq 6.0$ mA $\lvert I_{OUT}\rvert \leq 7.8$ mA	4.5 6.0	0.26 0.26	0.33 0.33	0.4 0.4	
I_{IN}	Maximum Input Leakage Current	$V_{IN}=V_{CC}$ or GND, Pin 1 or 19	6.0	±0.1	±1.0	±1.0	µA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{IN}=V_{IL}$ or V_{IH} $V_{OUT}=V_{CC}$ or GND	6.0	±0.5	±5.0	±10	µA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{IN}=V_{CC}$ or GND I_{OUT}=0µA	6.0	4.0	40	160	µA

AC ELECTRICAL CHARACTERISTICS(C_L=50pF,Input t_r=t_f=6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to B , B to A (Figures 1 and 3)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay , Direction or Output Enable to A or B (Figures 2 and 4)	2.0 4.5 6.0	110 22 19	140 28 24	165 33 28	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay , Direction or Output Enable to A or B (Figures 2 and 4)	2.0 4.5 6.0	110 22 19	140 28 24	165 33 28	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C_{IN}	Maximum Input Capacitance (Pin 1 or Pin 19)	-	10	10	10	pF
C_{OUT}	Maximum Three-State I/O Capacitance (Output in High-Impedance State)	-	15	15	15	pF

C_{PD}	Power Dissipation Capacitance (Per Transceiver Channel)	Typical @25°C,V_{CC}=5.0 V	pF
	Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	40	

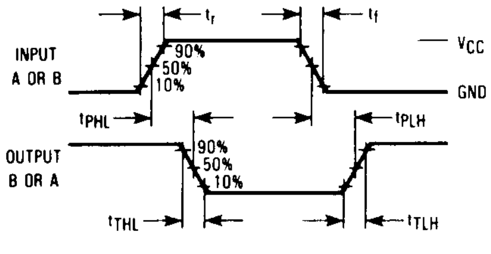


Figure 1. Switching Waveforms

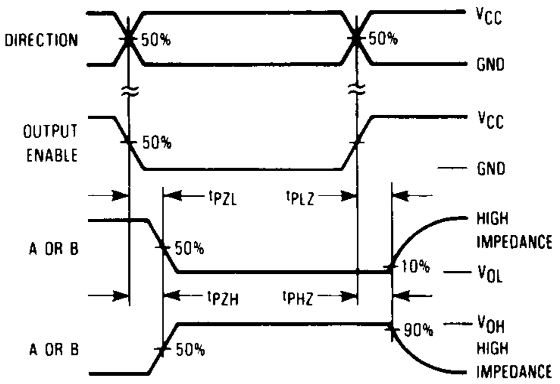
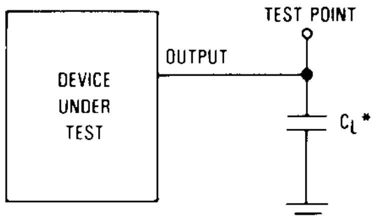
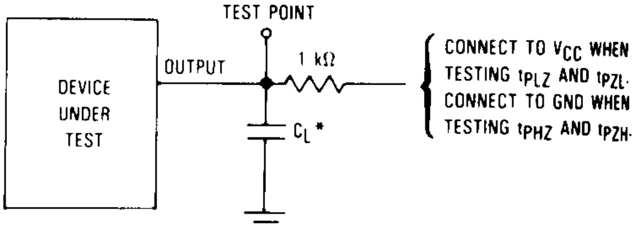


Figure 2. Switching Waveforms



*Includes all probe and jig capacitance.

Figure 3. Test Circuit



*Includes all probe and jig capacitance.

Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM