

Quad 2-Input OR Gate

High-Performance Silicon-Gate CMOS

The SL74HCT32 may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The SL74HCT32 is identical in pinout to the LS/ALS32.

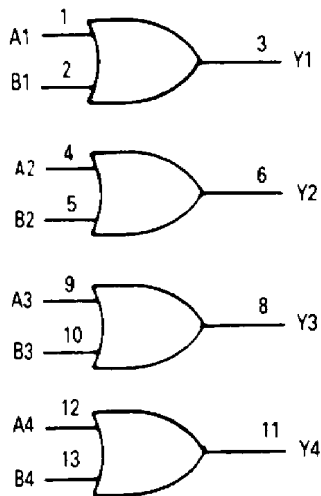
- TTL/NMOS-Compatible Input Levels.
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μ A

N SUFFIX PLASTIC

D SUFFIX SOIC

ORDERING INFORMATION
 SL74HCT32N Plastic
 SL74HCT32D SOIC
 $T_A = -55^\circ$ to 125° C for all packages

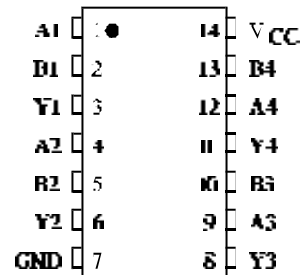
LOGIC DIAGRAM



$$Y = A + B$$

PIN 14 = V_{CC}
 PIN 7 = GND

PIN ASSIGNMENT



FUNCTION TABLE

| Inputs | | Output |
|--------|---|--------|
| A | B | Y |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | H |

SL74HCT32

MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|------------------|--|------------------------------|------|
| V _{CC} | DC Supply Voltage (Referenced to GND) | -0.5 to +7.0 | V |
| V _{IN} | DC Input Voltage (Referenced to GND) | -1.5 to V _{CC} +1.5 | V |
| V _{OUT} | DC Output Voltage (Referenced to GND) | -0.5 to V _{CC} +0.5 | V |
| I _{IN} | DC Input Current, per Pin | ±20 | mA |
| I _{OUT} | DC Output Current, per Pin | ±25 | mA |
| I _{CC} | DC Supply Current, V _{CC} and GND Pins | ±50 | mA |
| P _D | Power Dissipation in Still Air, Plastic DIP+ SOIC Package+ | 750 500 | mW |
| T _{stg} | Storage Temperature | -65 to +150 | °C |
| T _L | Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) | 260 | °C |

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|------------------------------------|--|-----|-----------------|------|
| V _{CC} | DC Supply Voltage (Referenced to GND) | 4.5 | 5.5 | V |
| V _{IN} , V _{OUT} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V _{CC} | V |
| T _A | Operating Temperature, All Package Types | -55 | +125 | °C |
| t _r , t _f | Input Rise and Fall Time (Figure 1) | 0 | 500 | ns |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | V _{CC} V | Guaranteed Limit | | | Unit |
|------------------|--|---|----------------------|----------------------|----------------|------------|------|
| | | | | 25 °C to -55°C | ≤85 °C | ≤125 °C | |
| V _{IH} | Minimum High-Level Input Voltage | V _{OUT} = V _{CC} -0.1 V I _{OUT} ≤ 20 μA | 4.5 | 2.0 | 2.0 | 2.0 | V |
| | | | 5.5 | 2.0 | 2.0 | 2.0 | |
| V _{IL} | Maximum Low-Level Input Voltage | V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 μA | 4.5 | 0.8 | 0.8 | 0.8 | V |
| | | | 5.5 | 0.8 | 0.8 | 0.8 | |
| V _{OH} | Minimum High-Level Output Voltage | V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 20 μA | 4.5 | 4.4 | 4.4 | 4.4 | V |
| | | | 5.5 | 5.4 | 5.4 | 5.4 | |
| | | V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA | 4.5 | 3.98 | 3.84 | 3.7 | |
| V _{OL} | Maximum Low-Level Output Voltage | V _{IN} = V _{IL} I _{OUT} ≤ 20 μA | 4.5 | 0.1 | 0.1 | 0.1 | V |
| | | | 5.5 | 0.1 | 0.1 | 0.1 | |
| | | V _{IN} = V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA | 4.5 | 0.26 | 0.33 | 0.4 | |
| I _{IN} | Maximum Input Leakage Current | V _{IN} =V _{CC} or GND | 5.5 | ±0.1 | ±1.0 | ±1.0 | μA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{IN} =V _{CC} or GND I _{OUT} =0μA | 5.5 | 1.0 | 10 | 40 | μA |
| ΔI _{CC} | Additional Quiescent Supply Current | V _{IN} =2.4 V, Any One Input V _{IN} =V _{CC} or GND, Other Input I _{OUT} = 0 μA | 5.5 | ≥-55° C | 25°C to 125 °C | | mA |
| | | | | 2.9 | 2.4 | | |

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AC ELECTRICAL CHARACTERISTICS ($V_{CC}=5.0\text{ V} \pm 10\%$, $C_L=50\text{ pF}$, Input $t_r=t_f=6.0\text{ ns}$)

| Symbol | Parameter | Guaranteed Limits | | | Unit |
|--------------------|---|-------------------|-------|--------|------|
| | | 25 °C to -55°C | ≤85°C | ≤125°C | |
| t_{PLH}, t_{PHL} | Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2) | 20 | 25 | 30 | ns |
| t_{TLH}, t_{THL} | Maximum Output Transition Time, Any Output (Figures 1 and 2) | 15 | 19 | 22 | ns |
| C_{IN} | Maximum Input Capacitance | 10 | 10 | 10 | pF |

| | | | | | |
|----------|--|--------------------------------------|--|--|----|
| C_{PD} | Power Dissipation Capacitance (Per Gate) | Typical @25°C, $V_{CC}=5.0\text{ V}$ | | | pF |
| | Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$ | 15 | | | |

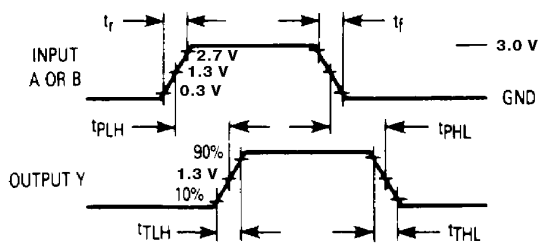
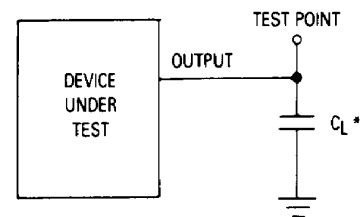


Figure 1 Switching Waveforms.



*Includes all probe and jig capacitance.

Figure 2. Test Circuit

EXPANDED LOGIC DIAGRAM (1/4 of the Device)

