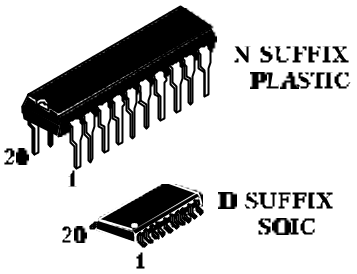
OCTAL D-TYPE TRANSPARENT LATCH (3-State)

By pinning SL74LV573 are compatible with SL74HC573 and SL74HCT573 series. Input voltage levels are compatible with stadard CMOS levels.

- Output voltage levels are compatible with input levels of CMOS, NMOS and TTL IC_S
- Voltage supply range from 1.2 to 5.5 V
- LOW input current: 1.0 µÀ; 0.1 µÀ at Ò= 25 °Ñ
- Output current 8 mÀ
- Latch current: not less than150 mÀ at Ò= 125 °Ñ
- ESD acceptable value: not less than 2000 V as per HBM and not less than 200 V as per MM



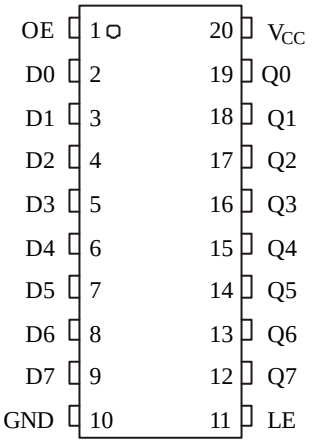
ORDERING INFORMATION
SL74LV573N Plastic DIP
SL74LV573D SOIC
T_A = -40° to 125° C
for all packages

FUNCTION TABLE

Inputs			Outputs
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	no change
H	X	X	Z

H -HIGH voltage level
L - LOW voltage level
X - don' t care
Z - High impedance state

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit	Conditions
Vcc	Supply voltage	-0.5 to +7.0	V	
Iik,	Input diode current	±20	mA	V_I<-0.5 V or V_I>Vcc>+0.5 V
Iok	Output diode current	±50	mA	V_0<-0.5 V or V_I>Vcc>+0.5 V
Io	Output current bus drivers	±35	mA	-0.5 V<Vo<Vcc+0.5 V
Icc	DC Vcc or GND current for types bus driver outputs	±70	mA	
I_{GND}	GND current	±50	mÀ	
Tstg	Storage temperature range	-65 to +150	ÎÑ	
P_D	Power dissipation per package: DIP SO	 750 500	mW	
Notes: Power dissipation value decreases for: DIP - 12 mW°C the range from 70 to 125°Ñ SO - 8 mW°C the range from 70 to 125°Ñ				

RECOMMENDED OPERATING CONDITIONS

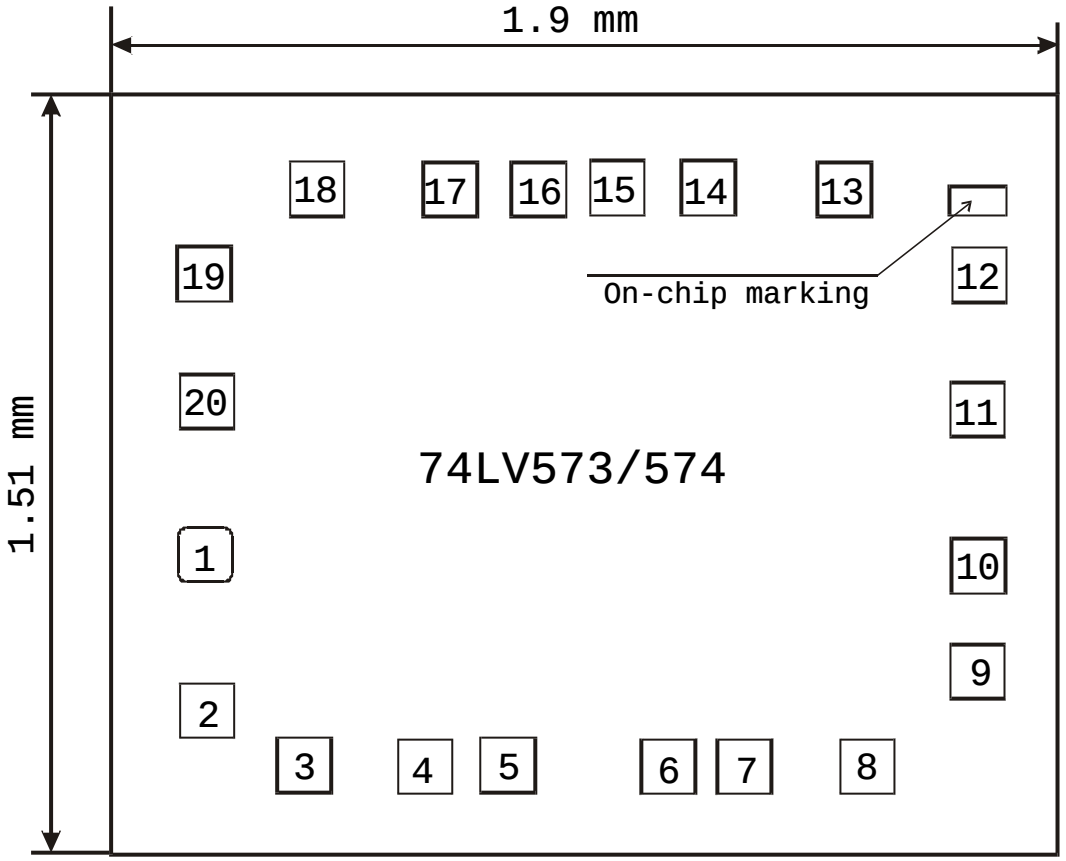
Symbol	Parameter	Min	Max	Unit	Conditions
Vcc	Supply voltage	1.0	5.5	V	
VI	Input voltage	0	Vcc	V	
Vî	Output voltage	0	Vcc	V	
T	Operating temperature range	-40	+125	°C	
t_r,t_f	Input rise and fall times		500 200 100 50	ns/V	Vcc= 1.0 ÷ 2.0 V Vcc= 2.0 ÷ 2.7 V Vcc= 2.7 ÷ 3.6 V Vcc= 3.6 ÷ 5.5 V
Note - The IC function down to Vññ = 1.0 V (input levels - V_{IL}=0 V, V_{IH}=Vcc); DC characterisics are guaranteed at Vcc=1.2 ÷ 5.5 V.					

DC CHARACTERISTICS

Symbol	Parameter	Conditions			Limits						Unit
		Vcñ	V_I		-40 to +25°C		+85îÑ		+125îÑ		
		(V)			Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH level input voltage	1.2 2.0 2.7 to 3.6 4.5 to 5.5			0.9 1.4 2.0 0.7 Vcc	- - - -	0.9 1.4 2.0 0.7 Vcc	- - - -	0.9 1.4 2.0 0.7 Vcc	- - - --	V
V_{IL}	LOW level output voltage	1.2 2.0 2.7 to 3.6 4.5 to 5.5			- - - -	0.3 0.6 0.8 0.3 Vcc	- - - -	0.3 0.6 0.8 0.3 Vcc	- - - -	0.3 0.6 0.8 0.3 Vcc	V
V_{OH}	HIGH level output voltage	1.2 2.0 2.7 3.6 5.5	V_{IH} or V_{IL}	I_O=-100 µÀ	1.05 1.85 2.55 3.45 5.35	- - - - -	1.0 1.8 2.5 3.4 5.3	- - - - -	1.0 1.8 2.5 3.4 5.3	- - - - -	V
V_{OH}	HIGH level output voltage; BUS driver outputs	3.0 4.5	V_{IH} or V_{IL}	I_O=-8 mA I_O=-16 mA	2.48 3.70	- -	2.40 3.60	- -	2.20 3.50	- -	V
V_{OL}	LOW level output voltage	1.2 2.0 2.7 3.6 5.5	V_{IH} or V_{IL}	I_O=100µÀ	- - - - -	0.15 0.15 0.15 0.15 0.15	- - - - -	0.2 0.2 0.2 0.2 0.2	- - - - -	0.2 0.2 0.2 0.2 0.2	V
V_{OL}	LOW level voltage; BUS driver outputs	3.0 4.5	V_{IH} or V_{IL}	I_O=8 mA I_O=16 mA	- -	0.33 0.40	- -	0.40 0.55	- -	0.50 0.65	V
I_I	Input leakage current	5.5	Vññ or GND		-	±1.0		±1.0	-	±1.0	µÀ
I_{OZ}	OFF-state current	5.5	V_{IH} or V_{IL}		-	±0.5		±5.0	-	±10.0	µÀ
Icc	Supply current	5.5	Vññ or GND	Io = 0		8.0		80		160	µÀ
Icc	Additional supply current per input	2.7 äî 3.6	V_I = Vcc-0.6V		-	0.2		0.5	-	0.85	mA

AC CHARACTERISICS (C_L=50 pF, R_L=1 KΩ, t_{LH} = t_{HL} = 2.5 ns)

Symbol	Parameter	Conditions		Limits						Unit
		Vcc		-40 to +25°C		+85°C		+125°C		
				Min	Max	Min	Max	Min	Max	
$t_{PHL/PLH}$	Propagation delay Dn to Qn	1.2 2.0 2.7 3.0 4.5	V_I = Vcc or GND	- - - - -	150 30 23 18 15	- - - - -	160 39 29 23 19	- - - - -	170 49 36 29 24	ns
$t_{PHL/PLH}$	Propagation delay LE to Qn	1.2 2.0 2.7 3.0 4.5	V_I = Vcc or GND	- - - - -	160 34 28 20 17	- - - - -	180 43 31 25 21	- - - - -	190 53 34 31 26	ns
$t_{PZH/PZL}$	3-state output enable time OE to Qn	1.2 2.0 2.7 3.0 4.5	V_I = Vcc or GND	- - - - -	140 28 22 17 14	- - - - -	160 37 28 22 18	- - - - -	170 48 35 28 23	ns
$t_{PHZ/PLZ}$	3-state outpiut disable time OE to Qn	1.2 2.0 2.7 3.0 4.5	V_I = Vcc or GND	- - - - -	160 31 23 20 17	- - - - -	160 39 29 24 20	- - - - -	170 48 36 29 24	ns
t_W	LE pulse width HIGH	1.2 2.0 2.7 3.0 4.5		100 29 21 17 15	- - - - -	125 34 25 20 18	- - - - -	150 41 30 24 21	- - - - -	ns
t_{su}	Setup time Dn to LE	1.2 2.0 2.7 3.0 4.5		50 15 11 8 6	- - - - -	75 17 13 10 8	- - - - -	100 20 15 12 10	- - - - -	ns
t_h	Hold time Dn to LE	1.2 2.0 2.7 3.0 4.5		40 8 8 8 8	- - - - -	40 8 8 8 8	- - - - -	40 8 8 8 8	- - - - -	ns
C_I	Input capacitance	5.0	Ò=+25 ÎÑ		7.0				-	ns
C_{PD}	Power dissipation capacitance per package	5.5	Ò=+25 ÎÑ V_I = Vcc or GND		52				-	ns



Drawing of the chip

Pads allocation Table

Pad number	coordinates (counted from lower left corner), mm		Pad size, mm
	X	Y	
01	0.128	0.545	0.108 x 0.108
02	0.128	0.229	0.108 x 0.108
03	0.330	0.120	0.108 x 0.108
04	0.576	0.120	0.108 x 0.108
05	0.738	0.120	0.108 x 0.108
06	1.054	0.120	0.108 x 0.108
07	1.216	0.120	0.108 x 0.108
08	1.466	0.120	0.108 x 0.108
09	1.682	0.314	0.108 x 0.108
10	1.682	0.533	0.108 x 0.108
11	1.682	0.839	0.108 x 0.108
12	1.682	1.108	0.108 x 0.108
13	1.422	1.274	0.108 x 0.108
14	1.149	1.274	0.108 x 0.108
15	0.971	1.274	0.108 x 0.108
16	0.811	1.274	0.108 x 0.108
17	0.633	1.274	0.108 x 0.108

18	0.360	1.274	0.108 x 0.108
19	0.128	1.108	0.108 x 0.108
20	0.128	0.854	0.108 x 0.108