SLD70R340SJ,SLU70R340SJ,SLP70R340SJ
SLF70R340SJ, SLB70R340SJ, SLI70R340SJ
700V N-Channel MOSFET

General Description

This Power MOSFET is produced using Maple semi's Advanced Super-Junction technology.

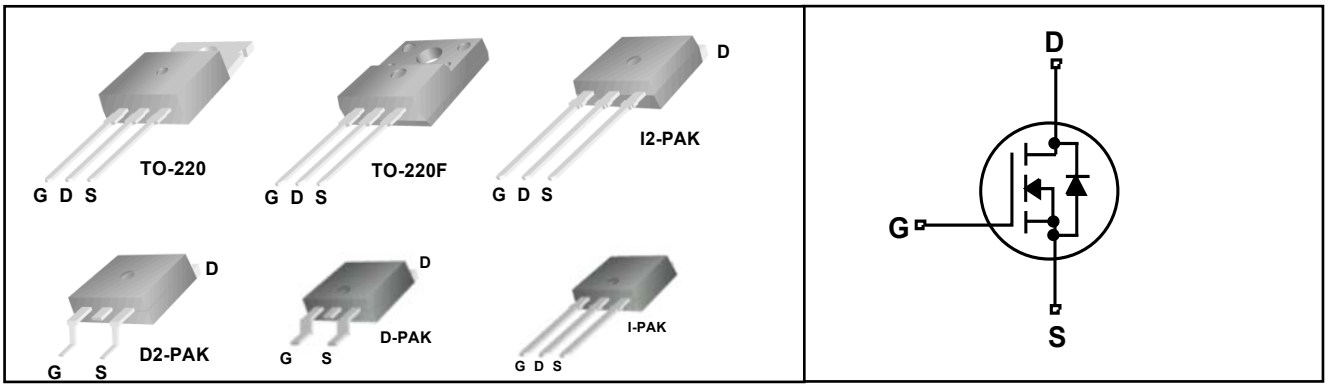
This advanced technology has been especially tailored to minimize conduction loss, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are well suited for AC/DC power conversion

Features

-15A, 700V, RDS(on) typ.= 0.3Ω@VGS = 10 V

- Low gate charge (typical 43nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



Absolute Maximum Ratings

TC = 25°C unless otherwise noted

Symbol	Parameter		D2-PAK/D-PAK I2-PAK / I-PAK/ TO-220	TO-220F	Units
VDSS	Drain-Source Voltage		700		V
ID	Drain Current	- Continuous (TC = 25℃)	15	15*	A
		- Continuous (TC = 100℃)	9.4	9.4*	A
IDM	Drain Current - Pulsed	(Note 1)	45	45*	A
VGSS	Gate-Source Voltage		±30		V
EAS	Single Pulsed Avalanche Energy	(Note 2)	284		mJ
IAR	Avalanche Current	(Note 1)	2.4		A
EAR	Repetitive Avalanche Energ	(Note 1)	0.43		mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	15		V/ns
PD	Power Dissipation (TC = 25℃)		104	32	W
		- Derate above 25℃	0.83	0.27	W/℃
TJ, TSTG	Operating and Storage Temperature Range		-55 to +150		℃
TL	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300		℃

*Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	Value						Units
		DPAK	IPAK	TO220	D2PAK	I2PAK	TO220F	
RθJC	Thermal Resistance, Junction-to-Case	1.2	1.2	1.2	1.2	1.2	3.9	℃/W
RθJS	Thermal Resistance, Case-to-Sink Typ.	-	-	0.5	0.5	0.5	-	℃/W
RθJA	Thermal Resistance, Junction-to-Ambient	62	62	62	62	62	80	℃/W

Electrical Characteristics (TC = 25 °C unless otherwise noted)

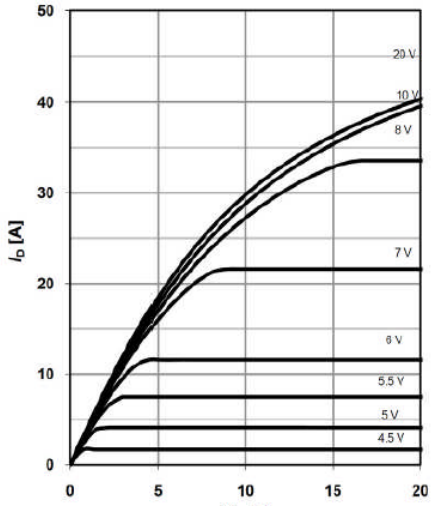
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BVDSS	Drain-Source Breakdown Voltage	VGS = 0V,ID = 250uA, TJ=25℃	700	-	-	V
		VGS = 0V,ID = 250uA, TJ=150℃	-	750	-	V
ΔBVDSS ΔTJ	Breakdown Voltage Temperature coefficient	ID = 250uA, referenced to 25°C	-	0.6	-	V/°C
IDSS	Drain-Source Leakage Current	VDS =700V, VGS = 0V	-	-	1	uA
		VDS =560V, TC = 125 °C	-	-	10	uA
IGSS	Gate-Source Leakage, Forward	VGS = 30V, VDS = 0V	-	-	100	nA
	Gate-source Leakage, Reverse	VGS = -30V, VDS = 0V	-	-	-100	nA
On Characteristics						
VGS(th)	Gate Threshold Voltage	VDS = VGS, ID = 250uA	2.5	3.5	4.5	V
RDS(ON)	Static Drain-Source On-state Resistance	VGS =10 V, ID = 7.5A	-	0.3	0.34	Ω
Dynamic Characteristics						
Ciss	Input Capacitance	VGS =0 V, VDS =25V, f = 1MHz	-	800	-	pF
Coss	Output Capacitance		-	340	-	
Crss	Reverse Transfer Capacitance		-	10	-	
Dynamic Characteristics						
td(on)	Turn-on Delay Time	VDD =350V, ID =15A, RG =25Ω	`	13	-	nS
tr	Rise Time		-	11	-	
td(off)	Turn-off Delay Time		-	100	-	
tf	Fall Time		-	12	-	
Qg	Total Gate Charge	VDS =560V, VGS =10V, ID =15A	-	43	-	nC
Qgs	Gate-Source Charge		-	5.0	-	
Qgd	Gate-Drain Charge(Miller Charge)		-	22	-	

Source-Drain Diode Ratings and Characteristics

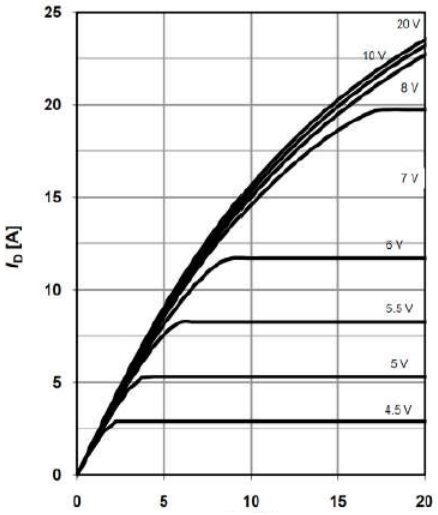
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit.
IS	Maximum Continuous Drain-Source Diode Forward Current		-	-	15	A
ISM	Maximum Pulsed Drain-Source Diode Forward Current		-	-	45	
VSD	Diode Forward Voltage	IS =7.5A, VGS =0V	-	-	1.5	V
trr	Reverse Recovery Time	IS =7.5A, VGS=0V, dIF/dt=100A/us	-	345	-	nS
Qrr	Reverse Recovery Charge		-	4.5	-	uC

NOTES

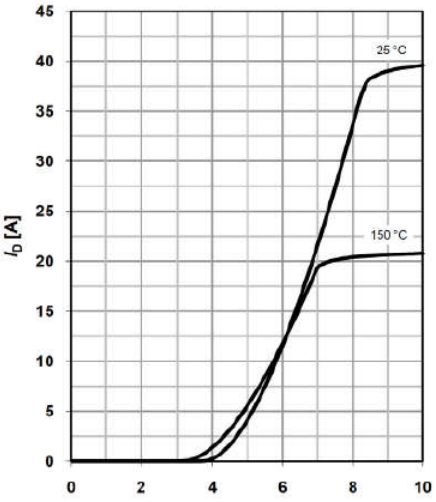
1. Repeativity rating : pulse width limited by junction temperature
2. L =100mH, IAS =2.4A, VDD = 150V, RG = 25Ω, Starting TJ = 25°C
3. ISD ≤ 7.5A, di/dt ≤ 200A/us, VDD ≤ BVDSS, Starting TJ = 25°C
4. Pulse Test : Pulse Width ≤ 300us, Duty Cycle ≤ 2%
5. Essentially independent of operating temperature.



V_{DS} (V)
Figure 1: On-Region Characteristics@25°C



V_{DS} (V)
Figure 2: On-Region Characteristics@125°C



V_{GS}(V)
Figure 3: Transfer Characteristics

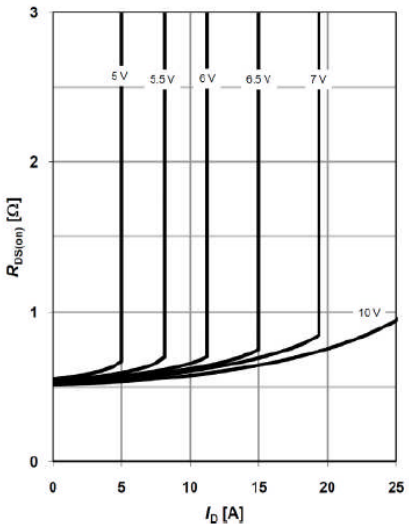


Figure 4: On-Resistance vs. Drain Current and Gate Voltage, T_j=125℃

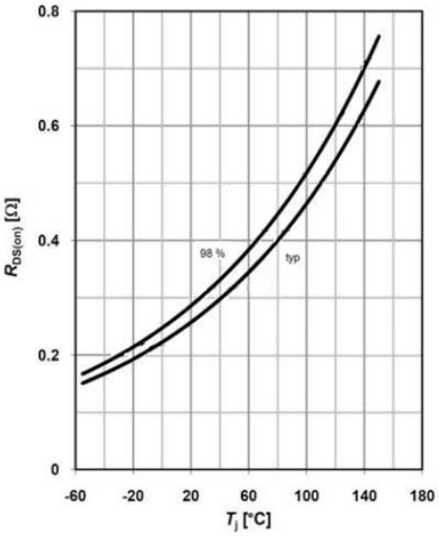
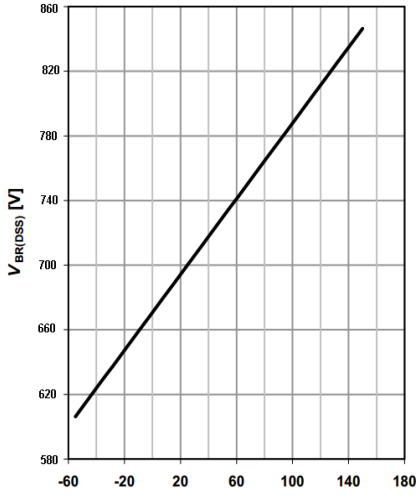


Figure 5: On-Resistance vs. Junction Temperature



TJ (°C)
Figure 6: Break Down vs. Junction Temperature

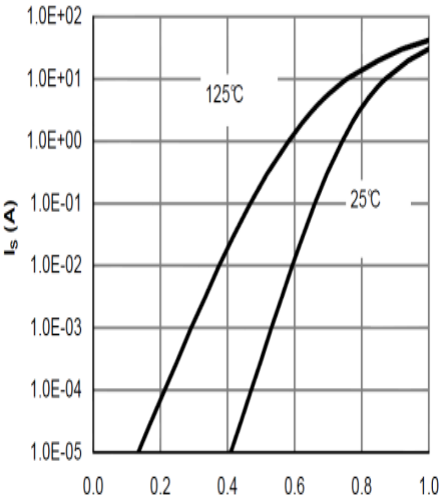


Figure 7: Body-Diode Characteristics

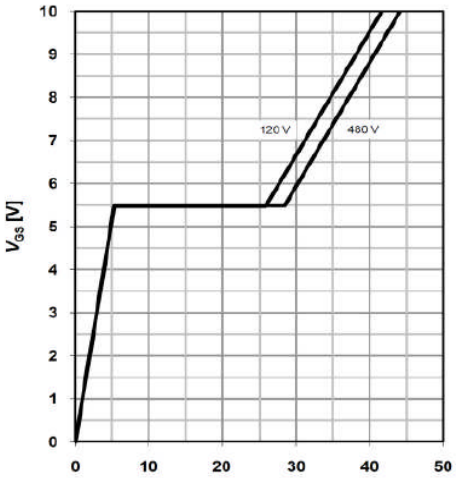


Figure 8: Gate-Charge Characteristics

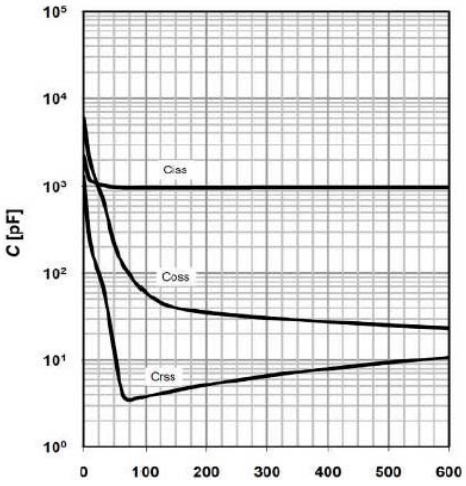


Figure 9: Capacitance Characteristics

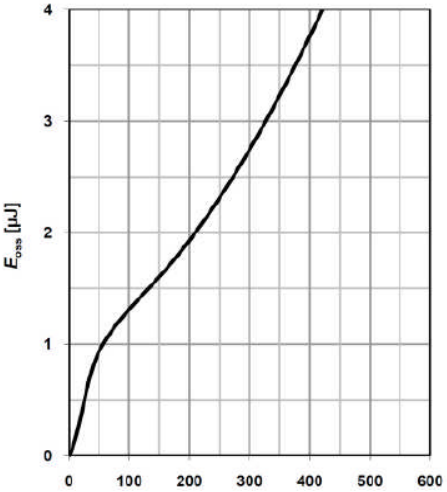


Figure 10: C_{oss} stored Energy

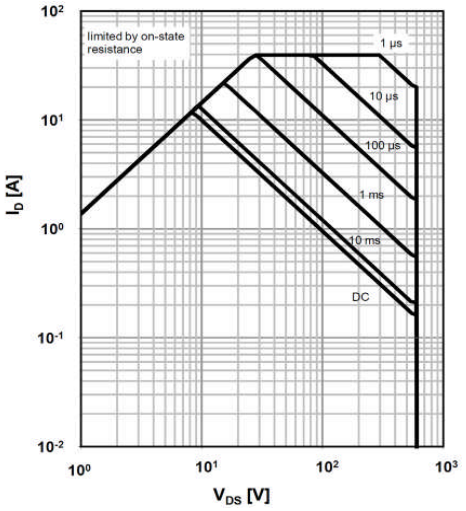


Figure 11: Maximum Forward Biased Safe Operating Area, Tc=25℃ TO-220

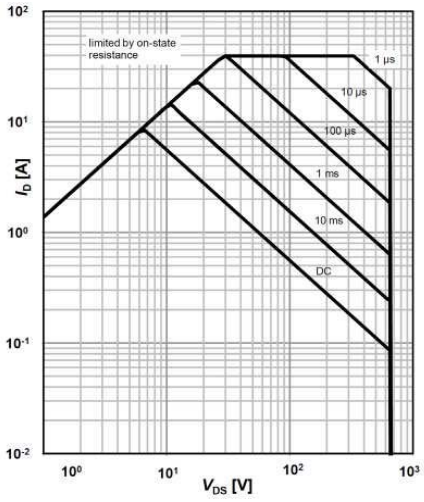


Figure 12: Maximum Forward Biased Safe Operating Area, Tc=25℃ TO-220FullPAK

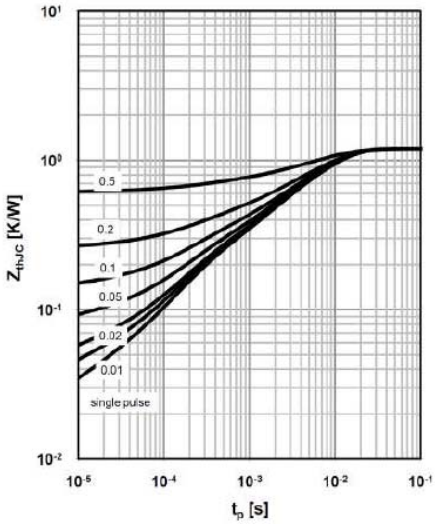


Figure 13: Max. transient thermal impedance TO-220

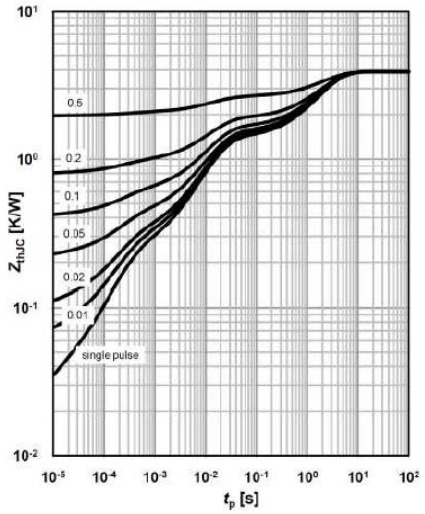


Figure 14: Max. transient thermal impedance TO-220FullPAK

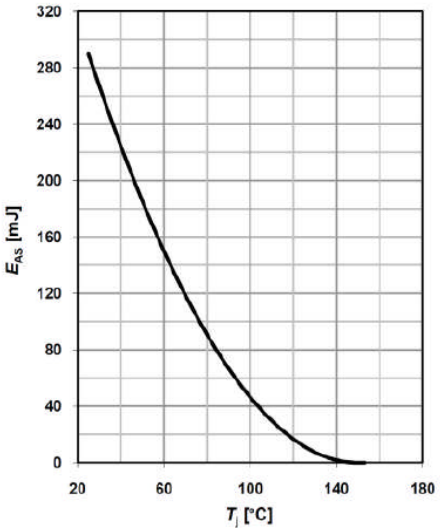
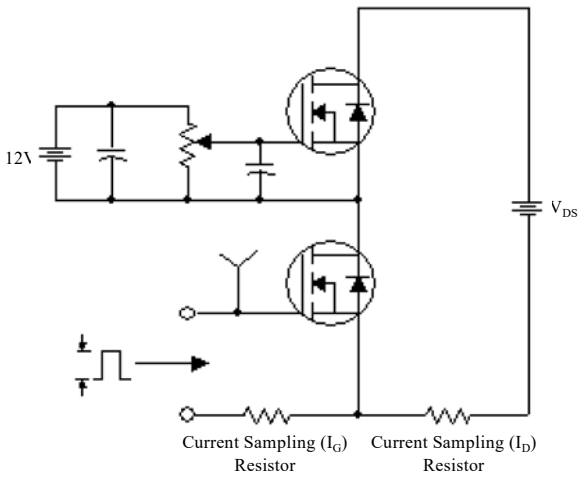
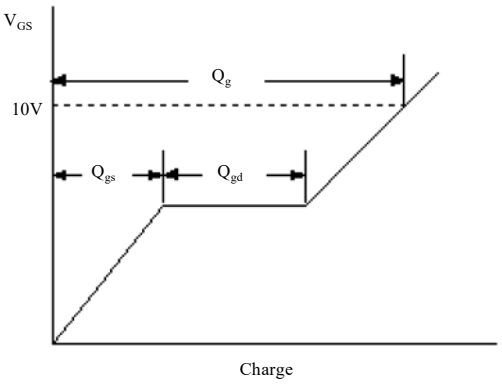


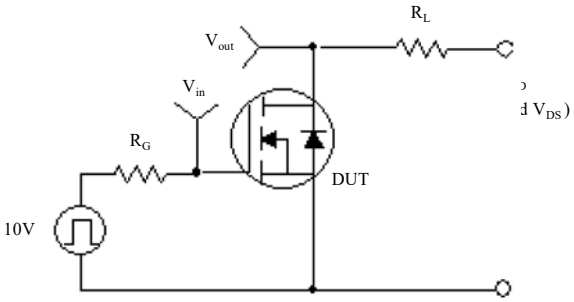
Figure 15: Avalanche energy

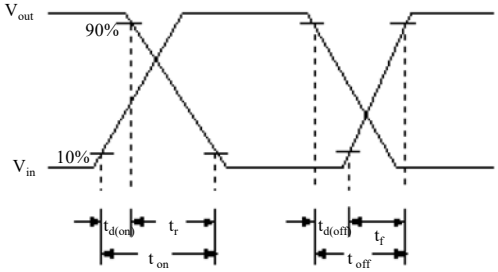
Gate Charge Test Circuit & Waveform



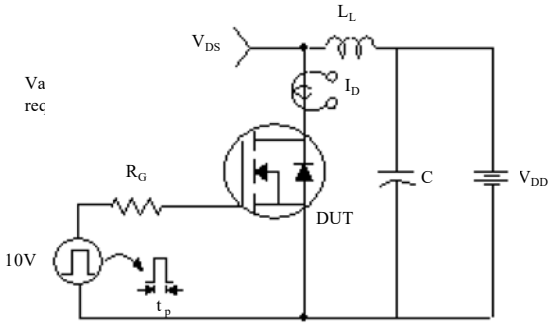


Resistive Switching Test Circuit & Waveforms

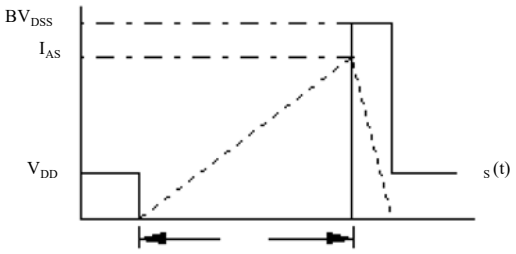




Unclamped Inductive Switching Test Circuit & Waveforms



$$E_{AS} = \frac{1}{2} L_L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



Peak Diode Recovery dv/dt Test Circuit & Waveforms