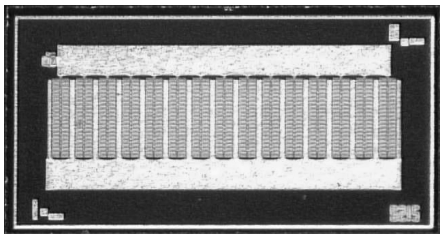
SLD-2000

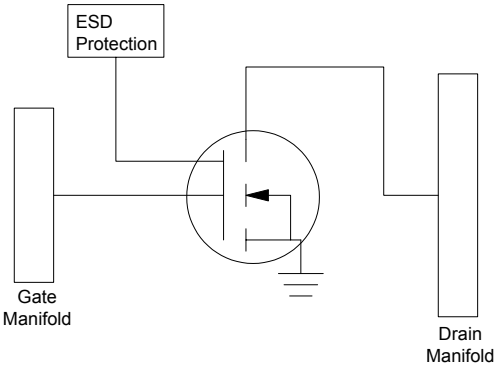
12 Watt Discrete LDMOS FET -Bare Die



Product Description

Sirenza Microdevices' **SLD2000** is a robust 12 Watt, high performance LDMOS transistor die, designed for operation from 10 to 2700MHz. It is an excellent solution for applications requiring high linearity and efficiency. The SLD2000 is typically used as a driver or output stage for power amplifier, or transmitter applications. These robust power transistors are fabricated using Sirenza's high performance XEMOS II™ process.

Functional Schematic Diagram



Source - Backside Contact

Product Features

- **12 Watt Output P_{1dB}**
- **Single Polarity Operation**
- **19dB Gain at 900 MHz**
- **XeMOS II™ LDMOS**
- **Integrated ESD Protection, Class 1B**
- **Aluminum Topside Metallization**
- **Gold Backside Metallization**

Applications

- **Base Station PA Driver**
- **Repeaters**
- **Military Communications**
- **RFID**
- **GSM, CDMA, Edge, WDCDMA**

RF Specifications

Symbol	Parameter	Unit	Min	Typ	Max
Frequency	Frequency of Operation	MHz	10	-	2700
Gain	10 Watt CW, 902 - 928MHz	dB	-	19	-
Efficiency	Drain Efficiency at 10 Watt CW, 915MHz	%	-	47	-
Linearity	3rd Order IMD at 10 Watt PEP (Two Tone), 915MHz	dBc	-	-32	-
Linearity	1dB Compression (P_{1dB})	W	-	12	-
R_{TH}	Thermal Resistance (Junction-to-Case, mounted in package)	ºC/W	-	4	-
Test Conditions: Mounted in ceramic package and tested in Sirenza Evaluation Board V_{DS} = 28.0V, I_{DQ} = 150mA, $T_{Mounting\ Surface}$ = 25ºC					

DC Specifications

Symbol	Parameter	Unit	Min	Typical	Max
g_m	Forward Transconductance @ 125mA I_{DQ}, V_{DS}=28V	mA / V		590	
V_{GS} Threshold	I_{DS}=3mA	V	3.0	3.8	5.0
V_{DS} Breakdown	1mA V_{DS} current	V	65	70	
C_{iss}	Input Capacitance (Gate to Source) V_{GS}=0V, V_{DS}=28V	pF		27.5	
C_{rss}	Reverse Capacitance (Gate to Drain) V_{GS}=0V, V_{DS}=28V	pF		0.8	
C_{oss}	Output Capacitance (Drain to Source) V_{GS}=0V, V_{DS}=28V	pF		14.7	
R_{DSON}	Drain to Source Resistance, V_{GS}=10V V_{DS}=250mV	R		0.6	0.75

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EDS-104292 Rev C

www.DataSheet4U.com

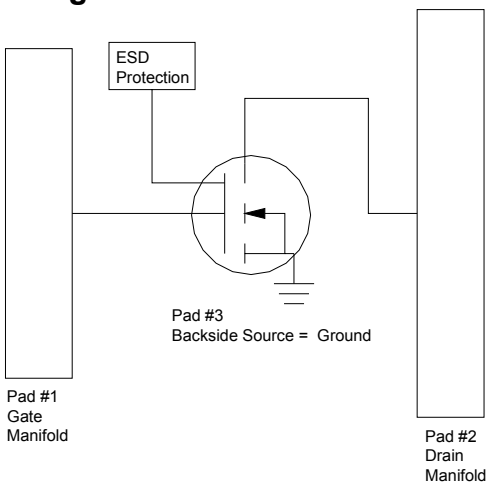
Quality Specifications

Parameter	Description	Unit	Typical
ESD Rating	Human Body Model	Volts	750
MTTF	200°C Channel	Hours	1.2×10^6

Contact Description

Pad #	Function	Description
1	Gate	Aluminum metallized manifold MOSFET Gate with ESD protection structure. (Topside contact)
2	Drain	Aluminum metallized manifold MOSFET Drain. (Topside contact)
3	Source	Chrome Gold metallized MOSFET Source contact. Appropriate electrical, mechanical and thermal connection required for proper operation. (Backside contact)

Pad Diagram



Note 1:
Gate voltage must be applied to to the device concurrently or after application of drain voltage to prevent potentially destructive oscillations. Bias voltages should never be applied to the transistor unless it is properly terminated on both input and output.

Note 2:
The required V_{GS} corresponding to a specific I_{DQ} will vary from device to device due to the normal die-to-die variation in threshold voltage with LDMOS transistors.

Note 3:
The threshold voltage (V_{GSTH}) of LDMOS transistors varies with device temperature. External temperature compensation may be required. See Sirenza application notes AN-067 LDMOS Bias Temperature Compensation.

Absolute Maximum Ratings

Parameters	Value	Unit
Drain Voltage (V_{DS})	35	Volts
Gate Voltage (V_{GS}), V_{DS} =0	20	Volts
RF Input Power	+33	dBm
Load Impedance for Continuous Operation Without Damage	10:1	VSWR
Output Device Channel Temperature	+200	ºC
Storage Temperature Range	-40 to +150	ºC

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation see typical setup values specified in the table on page one.

Caution: ESD Sensitive
Appropriate precaution in handling, packaging and testing devices must be observed.

Impedance Data

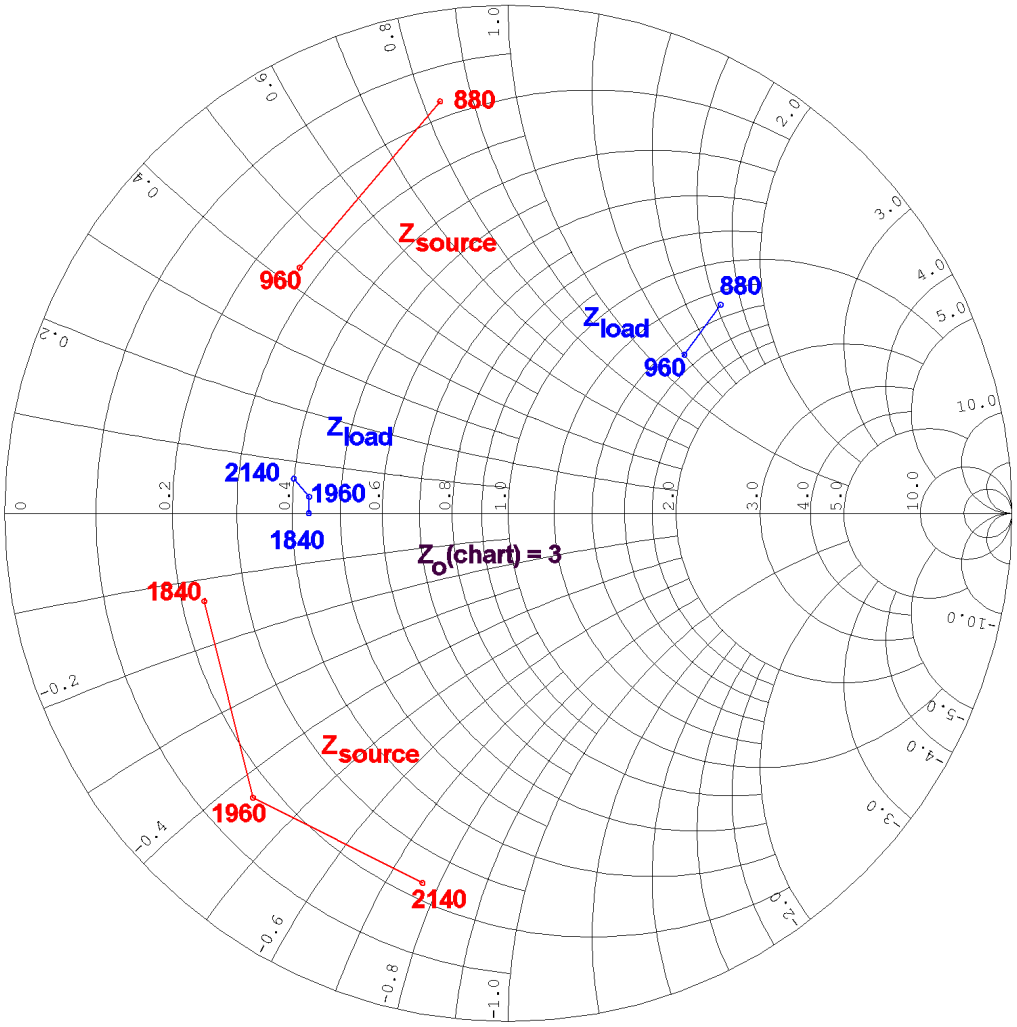
Frequency (MHz)	Z_{source}	Z_{load}
880	0.5 + j 2.5	3.9 + j 4.9
960	0.8 + j 1.3	4.5 + j 3.6
1840	0.7 - j 0.4	1.3 + j 0.0
1960	0.5 -j 1.3	1.3 + j 0.1
2140	0.7 - j 2.3	1.2 + j 0.2

Impedances Referenced to Wirebond/PCB Interface.

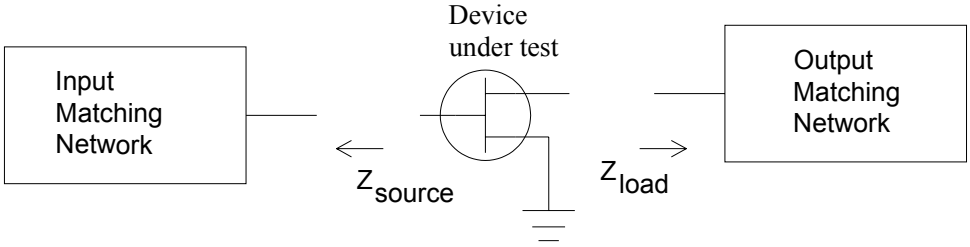
De-embedding Information

Description	Gate	Drain
Number of Bond Wires	6	9
Length of Bond Wires	0.037	0.040
Height of Bond Wires	0.006	0.007
Pitch of Bond Wires	0.012	0.008
Bond Wire Diameter	0.002	0.002

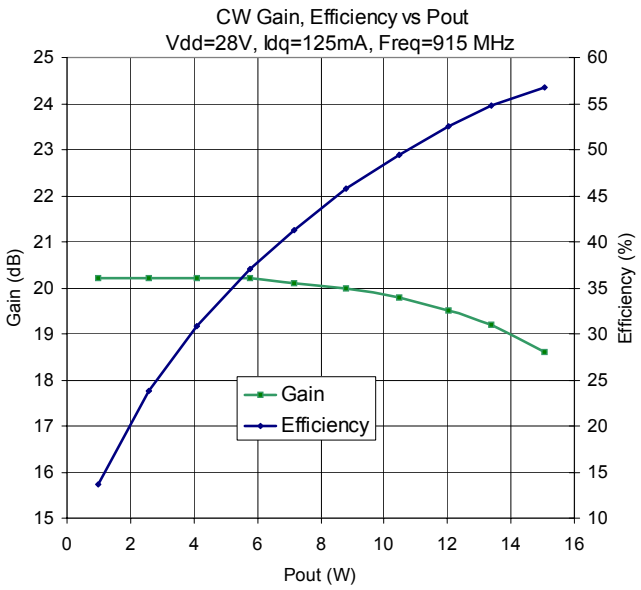
All Dimensions in Inches.
Wirebond Heights Referenced to Top Surface of Die.

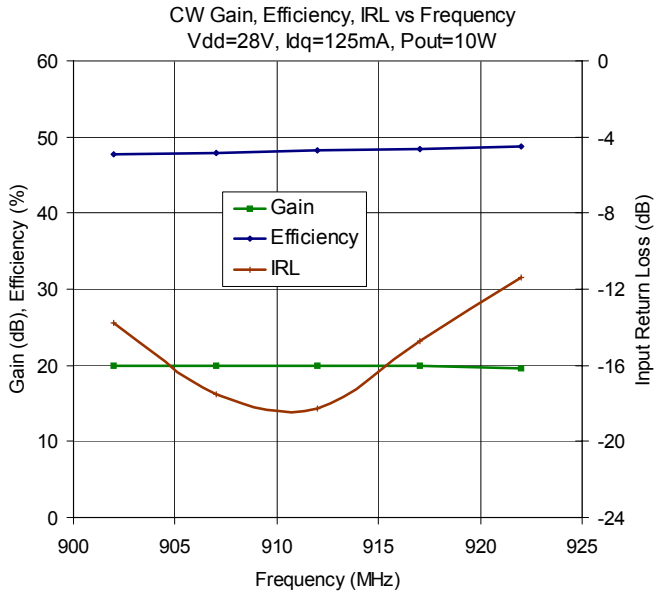


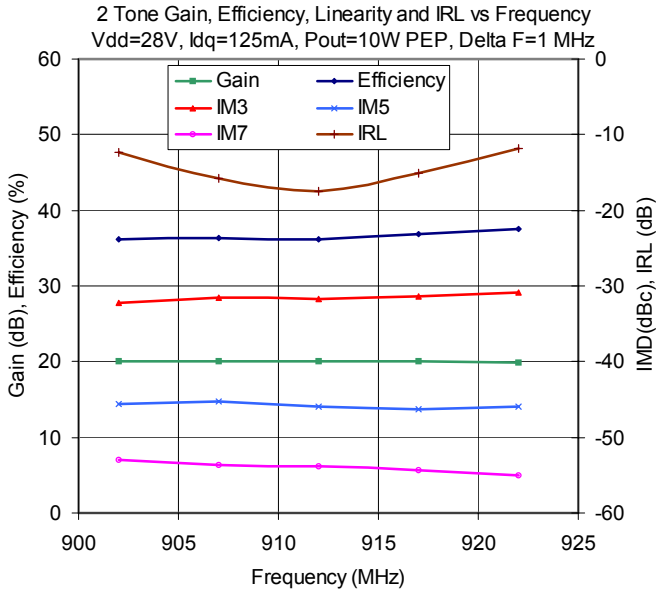
Z_{source} and Z_{load} are the optimal impedances presented to the SLD-2000 when operating at 28V, Idq=150mA, Pout=10 W PEP.

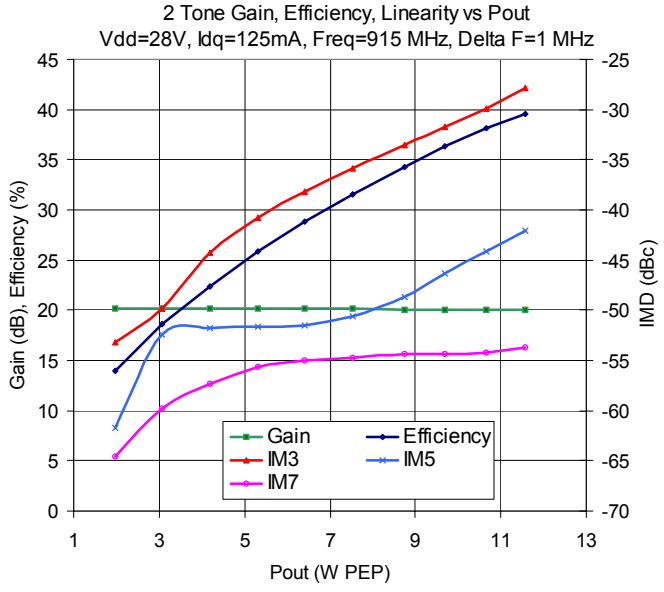


Typical Performance Curves for packaged die tested in SLD-2083CZ 900 MHz Application Circuit

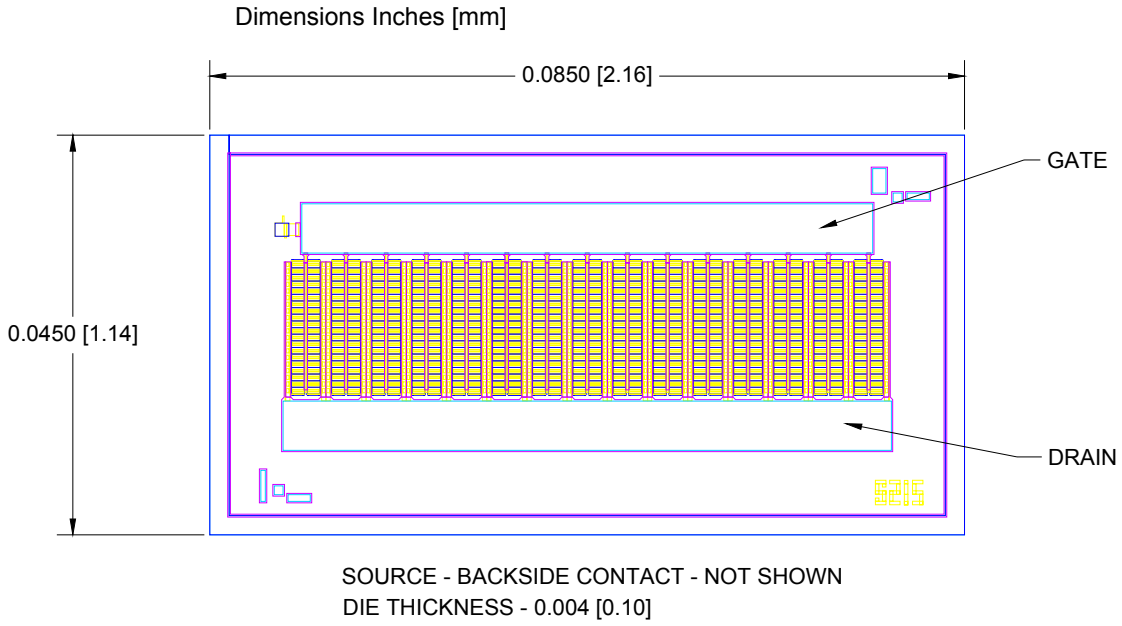








Die Map



SOURCE - BACKSIDE CONTACT - NOT SHOWN
DIE THICKNESS - 0.004 [0.10]

AuSi, AuSn, or AuGe eutectic die attach is recommended. AlSi bond wires are recommended.

Part Number Ordering Information

Part Number	Gel Pack
SLD-2000	100 pcs. per pack

Die are screened prior to dicing to DC parameters and are shipped per Sirenza application note AN-039 Visual Criteria of Unpackaged Die.