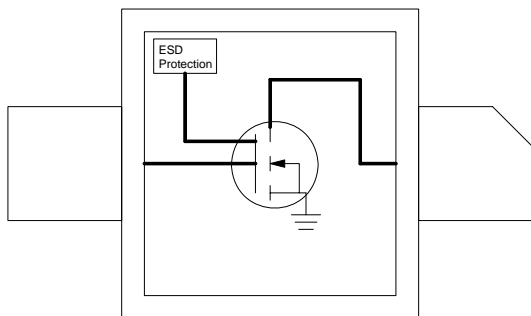




## Product Description

The **SLD2083CZ** is a 10 Watt high performance LDMOS transistor designed for operation to 2700MHz. It is an excellent solution for applications requiring high linearity and efficiency at a low cost. The SLD2083CZ is typically used in the design of driver stages for power amplifiers, repeaters, and RFID applications. The power transistor is fabricated using Sirenza's high performance XeMOS II™ process.

### Functional Schematic Diagram



Case Flange = Ground

## RF Specifications

Parameter	Description: Test Conditions in Sirenza Evaluation Board $V_{DS} = 28.0V$ , $I_{DQ} = 125mA$ , $T_{Flange} = 25^{\circ}C$	Unit	Min	Typ	Max
Frequency	Frequency of Operation	MHz	-	-	2700
Gain	10 Watt CW, 902MHz-928MHz	dB	17	18	-
Efficiency	Drain Efficiency at 10 Watt CW, 915MHz	%	40	47	-
IRL	Input Return Loss, 10 Watt Output Power, 915MHz	dB	-	-15	-10
Linearity	3 <sup>rd</sup> Order IMD at 10 Watt PEP (Two Tone), 915MHz	dBc	-	-28	-26
	1dB Compression ( $P_{1dB}$ ), 915MHz	Watt	10	11	-
	ACPR=-55dB, IS-95	Watt	1.8	1.6	-
	ACPR=-45dB, IS-95	Watt	3.2	3.6	-

The information provided herein is believed to be reliable at press time. Sirenza Microdevices assumes no responsibility for inaccuracies or omissions. Sirenza Microdevices assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. Sirenza Microdevices does not authorize or warrant any Sirenza Microdevices product for use in life-support devices and/or systems.

Copyright 2005 Sirenza Microdevices, Inc. All worldwide rights reserved.  
303 S. Technology Court, Broomfield, CO 80021

Phone: (800) SMI-MMIC

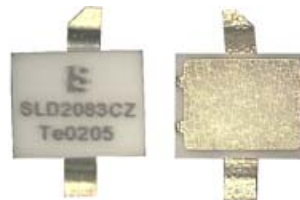
<http://www.sirenza.com>  
EDS-103754 Rev D

Preliminary

## SLD2083CZ



### 10 Watt Discrete LDMOS Device Ceramic Package



### Product Features

- 10 Watt Output  $P_{1dB}$
- Single Polarity Supply Voltage
- High Gain: 18 dB Typical
- High Efficiency
- Advanced, XeMOS II LDMOS
- Integrated ESD Protection, Class 1A

### Applications

- Base Station PA driver
- Repeater
- RFID



Preliminary

## SLD2083CZ 10 Watt LD MOS FET

## DC Specifications

Parameter		Unit	Min	Typical	Max
$g_m$	Forward Transconductance @ 125mA $I_{DQ}$	mA / V		590	
$V_{GS}$ Threshold	$I_{DS}=3mA$	Volt		3.8	
$V_{DS}$ Breakdown	1mA $I_{DS}$ current	Volt		65	
$C_{iss}$	Input Capacitance (Gate to Source) $V_{GS}=0V$ , $V_{DS}=28V$	pF		27.5	
$C_{riss}$	Reverse Capacitance (Gate to Drain) $V_{GS}=0V$ , $V_{DS}=28V$	pF		0.81	
$C_{oss}$	Output Capacitance (Drain to Source) $V_{GS}=0V$ , $V_{DS}=28V$	pF		14.65	
$R_{Dson}$	Drain to Source Resistance, $V_{GS}=10V$ , $V_{DS}=250mV$	$\Omega$		0.6	

## Quality Specifications

Parameter		Unit	Min	Typical	Max
ESD Rating	Human Body Model	Volts		500	
MTTF	85°C Leadframe, 200°C Channel	Hours		$1.2 \times 10^6$	
$R_{TH}$	Thermal Resistance (Junction to Case)	$^{\circ}C/W$		4	

## Pin Description

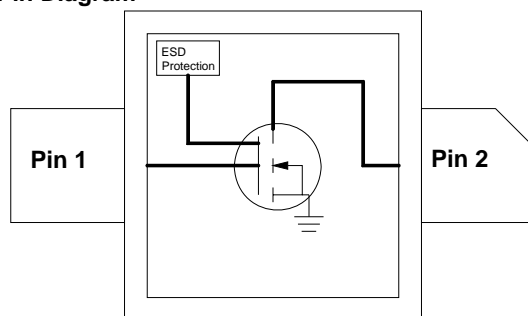
Pin #	Function	Description
1	Gate	Transistor RF input and gate bias voltage. The gate bias voltage must be temperature compensated to maintain constant bias current over the operating temperature range. Care must be taken to protect against video transients that exceed the recommended maximum input power or voltage. .
2	Drain	Transistor RF output and drain bias voltage. Typical voltage is 28V.
Flange	Source, Gnd	Exposed area on the bottom side of the package needs to be mechanically attached to the ground plane of the board for optimum thermal and RF performance. See mounting instructions for recommendation.

## Absolute Maximum Ratings

Parameters	Value	Unit
Drain Voltage ( $V_{DS}$ )	35	V
Gate Voltage ( $V_{GS}$ )	20	V
RF Input Power	+33	dBm
Load Impedance for Continuous Operation Without Damage	10:1	VSWR
Output Device Channel Temperature	+200	$^{\circ}C$
Lead Temperature During Solder Reflow	+270	$^{\circ}C$
Operating Temperature Range	-20 to +90	$^{\circ}C$
Storage Temperature Range	-40 to +100	$^{\circ}C$

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation see typical setup values specified in the table on page one.

## Pin Diagram



Case Flange = Ground

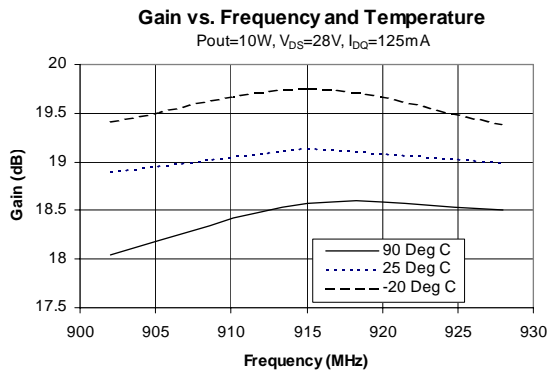
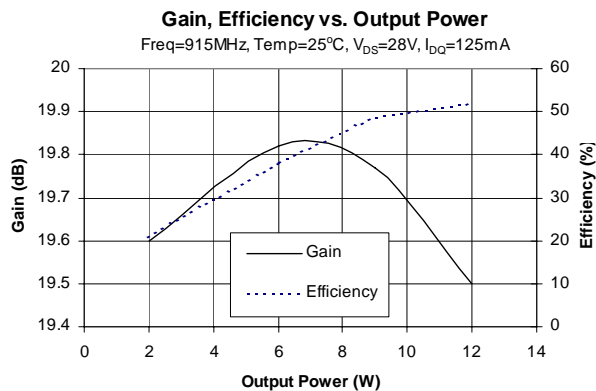
**Caution: ESD Sensitive**

Appropriate precaution in handling, packaging and testing devices must be observed.

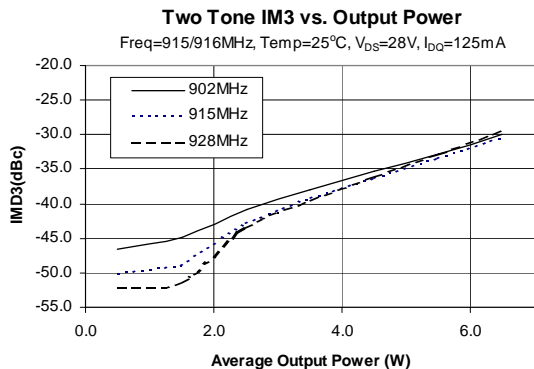


**Preliminary**  
**SLD2083CZ 10 Watt LD MOS FET**

**Typical EVB Test Data**



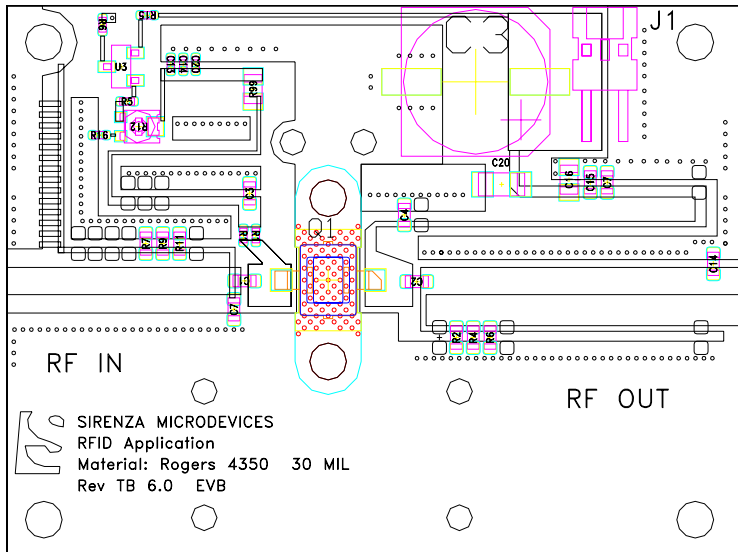
www.DataSheet4U.com





**Preliminary**  
**SLD2083CZ 10 Watt LD MOS FET**

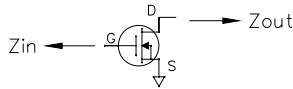
**SLD2083CZ EVB Layout and BoM**



Evaluation Board Bill of Materials	
Description	Part
Res, 10, 1/10W, 1%, 0805	R10
Polarized	J1
Inductor Coilcraft 1.6nH 0603	L1
Res, 0.0, 1/16W, 5%, 0603	R2, R4, R6, R7, R9, R11
Cap, 1000 pF, 100V, 10%, 0603	C7, C8
Cap, 0.01 uF, 100V, 5%, 0805	C10, C15
Cap, 0.5 pF, 250V, +/- .1pF, 0603	C11
Cap, 3.6 pF, 250V, +/- .1pF, 0603	C14
Cap, 12 pF, 250V, 1%, 0603	C2
Cap, 15 pF, 250V, 2%, 0603	C1
Cap, 68 pF, 250V, 5%, 0603	C3, C4, C5, C6
Res, 10 Ohm, 0402	R5, R15
CAP 0.22UF 50V CERAMIC X7R 1206	C13, C16
SLD2083CZ	Q1

Impedance Information (Typical)				
Frequency (MHz)	Input R (Ohms)	Input X (Ohms)	Output R (Ohms)	Output X (Ohms)
870	0.5	2.0	4.3	1.9
880	0.5	1.9	4.3	2.0
900	0.8	1.8	4.4	2.0
930	0.7	1.7	4.5	2.0
960	0.8	1.4	4.7	2.0

**Impedances are circuit impedances as seen from device at device lead.**

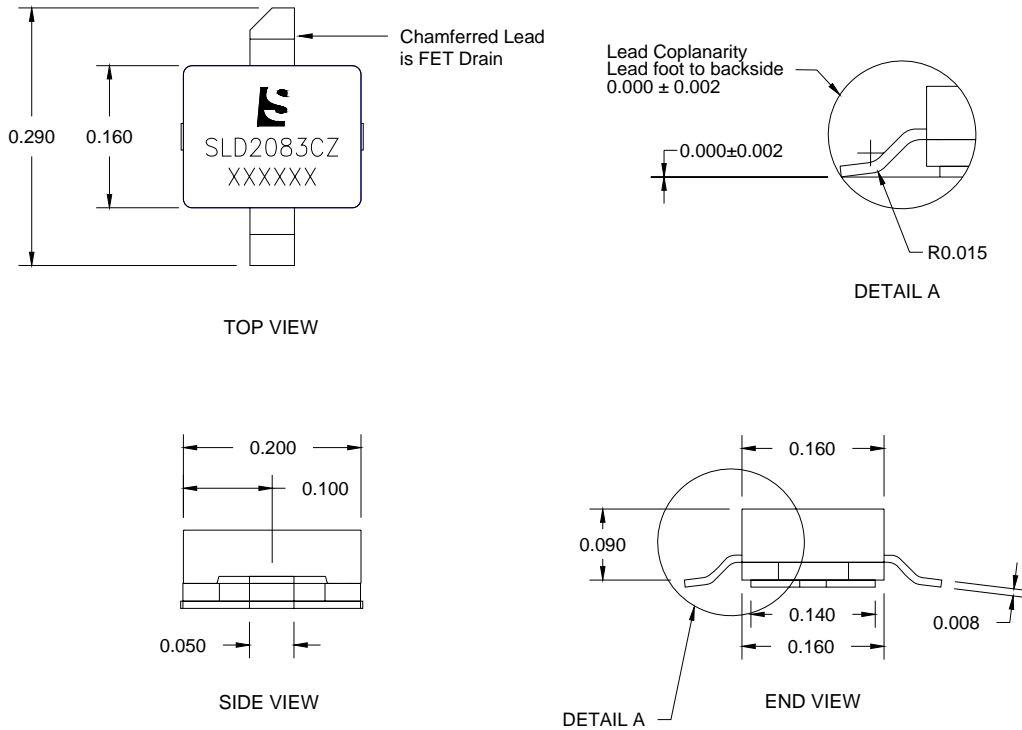


**To download Gerber files, DXF drawings, a detailed BOM, and assembly recommendations for the test board with fixture contact Sirenza applications.**

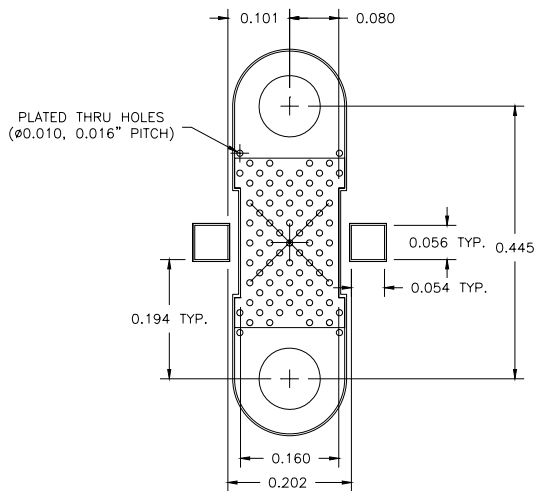


**Preliminary**  
**SLD2083CZ 10 Watt LD MOS FET**

**Package Outline Drawings**



www.DataSheet4U.com **Recommended Landing Pads for the RF083 Package**



**Part Number Ordering Information**

Part Number	Devices Per Reel	Reel Size
SLD2083CZ	500	7"

All Dimensions are in inches