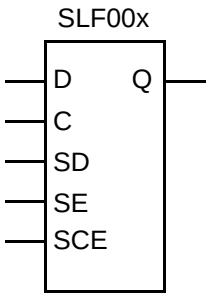
Description

SLF00x is a family of static, master-slave, multiplexed scan latch, D flip-flops. When SCE is low it is a D flip-flop with the output buffered and changes state on the rising edge of the clock. When SCE is high it is a D latch that is transparent when C is low.

Logic Symbol



Truth Table

C	D	SD	SE	SCE	Q
↑	H	X	L	L	H
↑	L	X	L	L	L
↑	X	H	H	L	H
↑	X	L	H	L	L
L	X	X	X	L	NC
L	H	X	L	H	H
L	L	X	L	H	L
L	X	H	H	H	H
L	X	L	H	H	L
H	X	X	X	H	NC

NC = No Change

HDL Syntax

Verilog ..... SLF00x *inst_name* (Q, C, D, SCE, SD, SE);

VHDL..... *inst_name*: SLF00x port map (Q, C, D, SCE, SD, SE);

Pin Loading

Pin Name	Equivalent Loads			
	SLF001	SLF002	SLF004	SLF006
C	1.0	1.0	1.0	1.0
D	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.1	2.1	2.1	2.1
SCE	2.1	2.1	2.1	2.1

AMI5HG 0.5 micron CMOS Gate Array

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
SLF001	12.0	TBD	28.7
SLF002	14.0	TBD	33.2
SLF004	16.0	TBD	37.2
SLF006	16.0	TBD	34.2

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
SLF001	From: C To: Q	t_{PLH} t_{PHL}	1.13 1.29	1.25 1.43	1.37 1.57	1.49 1.73	1.57 1.85
	From: D To: Q	t_{PLH} t_{PHL}	0.93 1.19	1.03 1.34	1.15 1.48	1.30 1.62	1.42 1.72
	From: SCE To: Q	t_{PLH} t_{PHL}	0.88 1.01	0.98 1.15	1.11 1.29	1.25 1.45	1.36 1.55
	From: SD To: Q	t_{PLH} t_{PHL}	0.95 1.17	1.05 1.32	1.17 1.46	1.32 1.61	1.43 1.71
	From: SE To: Q	t_{PLH} t_{PHL}	1.01 1.30	1.08 1.45	1.20 1.59	1.36 1.73	1.51 1.83
SLF002	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: C To: Q	t_{PLH} t_{PHL}	1.09 1.27	1.19 1.40	1.28 1.51	1.37 1.61	1.46 1.72
	From: D To: Q	t_{PLH} t_{PHL}	0.92 1.15	1.05 1.32	1.15 1.43	1.23 1.52	1.33 1.61
	From: SCE To: Q	t_{PLH} t_{PHL}	0.80 0.94	0.94 1.11	1.05 1.23	1.14 1.33	1.25 1.44
	From: SD To: Q	t_{PLH} t_{PHL}	0.92 1.11	1.03 1.26	1.13 1.38	1.23 1.49	1.34 1.61
	From: SE To: Q	t_{PLH} t_{PHL}	0.99 1.27	1.11 1.39	1.21 1.50	1.31 1.61	1.40 1.72

	Number of Equivalent Loads		1	14	28	42	56 (max)
SLF004	From: C To: Q	t_{PLH} t_{PHL}	1.15 1.30	1.25 1.46	1.35 1.61	1.46 1.73	1.57 1.83
	From: D To: Q	t_{PLH} t_{PHL}	0.96 1.20	1.09 1.40	1.19 1.52	1.27 1.62	1.35 1.69
	From: SCE To: Q	t_{PLH} t_{PHL}	0.90 1.04	1.03 1.21	1.13 1.32	1.22 1.41	1.30 1.49
	From: SD To: Q	t_{PLH} t_{PHL}	0.97 1.21	1.09 1.35	1.19 1.47	1.29 1.58	1.38 1.68
	From: SE To: Q	t_{PLH} t_{PHL}	1.03 1.37	1.15 1.52	1.26 1.63	1.36 1.73	1.45 1.81
	Number of Equivalent Loads		**1**	**21**	**42**	**62**	**83 (max)**
SLF006	From: C To: Q	t_{PLH} t_{PHL}	1.19 1.39	1.29 1.57	1.40 1.70	1.50 1.82	1.61 1.93
	From: D To: Q	t_{PLH} t_{PHL}	0.99 1.31	1.15 1.47	1.24 1.59	1.32 1.71	1.40 1.84
	From: SCE To: Q	t_{PLH} t_{PHL}	0.97 1.10	1.07 1.29	1.17 1.41	1.26 1.50	1.36 1.60
	From: SD To: Q	t_{PLH} t_{PHL}	1.04 1.21	1.13 1.45	1.23 1.58	1.34 1.66	1.45 1.73
	From: SE To: Q	t_{PLH} t_{PHL}	1.09 1.38	1.25 1.58	1.34 1.71	1.42 1.79	1.49 1.88

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			SLF001	SLF002	SLF004	SLF006
Min C Width	High	t_w	1.23	1.23	1.31	1.38
Min C Width	Low	t_w	0.83	0.87	0.87	0.87
Min D Setup		t_{su}	0.67	0.72	0.72	0.72
Min D Hold		t_h	0.14	0.14	0.14	0.14
Min SD Setup		t_{su}	0.67	0.72	0.72	0.72
Min SD Hold		t_h	0.14	0.14	0.14	0.14
Min SE Setup		t_{su}	0.81	0.85	0.85	0.85
Min SE Hold		t_h	0.14	0.14	0.14	0.14

AMI5HG 0.5 micron CMOS Gate Array

Delay (ns) From To	Parameter	Cell			
		SLF001	SLF002	SLF004	SLF006
Min SCE Setup	t_{su}	0.98	0.98	1.06	1.13
Min SCE Hold	t_h	1.03	1.05	1.09	1.13

Logic Schematic