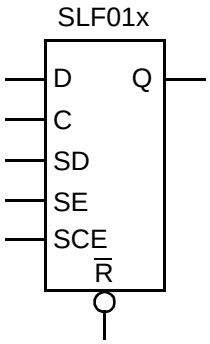
Description

SLF01x is a family of static, master-slave, multiplexed scan latch, D flip-flops. When SCE is low it is a D flip-flop with the output buffered and changes state on the rising edge of the clock. When SCE is high it is a D latch that is transparent when C is low. RESET is asynchronous and active low.

Logic Symbol



Truth Table

RN	C	D	SD	SE	SCE	Q
H	↑	H	X	L	L	H
H	↑	L	X	L	L	L
H	↑	X	H	H	L	H
H	↑	X	L	H	L	L
H	L	X	X	X	L	NC
H	L	H	X	L	H	H
H	L	L	X	L	H	L
H	L	X	H	H	H	H
H	L	X	L	H	H	L
H	H	X	X	X	H	NC
L	X	X	X	X	X	L

NC = No Change

HDL Syntax

Verilog ..... SLF01x *inst_name* (Q, C, D, RN, SCE, SD, SE);

VHDL..... *inst_name*: SLF01x port map (Q, C, D, RN, SCE, SD, SE);

Pin Loading

Pin Name	Equivalent Loads			
	SLF011	SLF012	SLF014	SLF016
C	1.0	1.0	1.0	1.0
D	1.0	1.0	1.0	1.0
RN	1.1	1.1	1.1	1.0
SD	1.0	1.0	1.0	1.0
SE	2.2	2.2	2.2	2.2
SCE	2.2	2.2	2.2	2.1

AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
SLF011	15.0	TBD	33.4
SLF012	16.0	TBD	38.3
SLF014	16.0	TBD	41.2
SLF016	17.0	TBD	43.4

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
SLF011	From: C To: Q	t_{PLH} t_{PHL}	1.17 1.33	1.26 1.47	1.38 1.62	1.54 1.77	1.66 1.88
	From: D To: Q	t_{PLH} t_{PHL}	1.06 1.21	1.17 1.34	1.29 1.49	1.43 1.66	1.54 1.79
	From: RN To: Q	t_{PLH} t_{PHL}	0.81 0.80	0.92 0.94	1.04 1.08	1.18 1.23	1.29 1.34
	From: SCE To: Q	t_{PLH} t_{PHL}	0.89 1.01	1.00 1.16	1.12 1.30	1.26 1.45	1.38 1.56
	From: SD To: Q	t_{PLH} t_{PHL}	1.09 1.19	1.19 1.33	1.32 1.48	1.46 1.64	1.57 1.77
	From: SE To: Q	t_{PLH} t_{PHL}	1.15 1.32	1.22 1.45	1.34 1.60	1.50 1.77	1.64 1.90

	Number of Equivalent Loads		1	8	15	22	30 (max)
SLF012	From: C To: Q	t_{PLH} t_{PHL}	1.17 1.26	1.27 1.41	1.35 1.54	1.44 1.65	1.54 1.77
	From: D To: Q	t_{PLH} t_{PHL}	1.12 1.14	1.23 1.32	1.32 1.44	1.41 1.53	1.49 1.63
	From: RN To: Q	t_{PLH} t_{PHL}	0.83 0.84	0.95 1.02	1.06 1.15	1.16 1.26	1.27 1.38
	From: SCE To: Q	t_{PLH} t_{PHL}	0.79 0.96	0.90 1.11	1.00 1.23	1.10 1.33	1.21 1.43
	From: SD To: Q	t_{PLH} t_{PHL}	1.11 1.13	1.24 1.30	1.34 1.41	1.42 1.52	1.51 1.62
	From: SE To: Q	t_{PLH} t_{PHL}	1.20 1.30	1.28 1.43	1.37 1.54	1.46 1.63	1.57 1.73
	Number of Equivalent Loads		**1**	**14**	**28**	**42**	**56 (max)**
SLF014	From: C To: Q	t_{PLH} t_{PHL}	1.24 1.31	1.36 1.52	1.45 1.64	1.53 1.73	1.61 1.81
	From: D To: Q	t_{PLH} t_{PHL}	1.15 1.23	1.27 1.41	1.39 1.53	1.49 1.62	1.58 1.70
	From: RN To: Q	t_{PLH} t_{PHL}	0.92 1.00	1.04 1.21	1.13 1.33	1.21 1.43	1.29 1.53
	From: SCE To: Q	t_{PLH} t_{PHL}	0.87 1.02	1.00 1.19	1.11 1.32	1.20 1.42	1.28 1.51
	From: SD To: Q	t_{PLH} t_{PHL}	1.11 1.21	1.30 1.37	1.42 1.48	1.49 1.58	1.55 1.68
	From: SE To: Q	t_{PLH} t_{PHL}	1.24 1.36	1.34 1.48	1.46 1.60	1.56 1.72	1.67 1.83

AMI5HG 0.5 micron CMOS Gate Array

	Number of Equivalent Loads		1	21	42	62	83 (max)
SLF016	From: C To: Q	t_{PLH} t_{PHL}	1.64 1.60	1.74 1.74	1.82 1.83	1.89 1.89	1.96 1.95
	From: D To: Q	t_{PLH} t_{PHL}	1.55 1.45	1.67 1.60	1.74 1.70	1.79 1.79	1.85 1.87
	From: RN To: Q	t_{PLH} t_{PHL}	1.31 0.65	1.41 0.77	1.49 0.85	1.57 0.95	1.64 1.06
	From: SCE To: Q	t_{PLH} t_{PHL}	1.38 1.32	1.49 1.45	1.57 1.54	1.63 1.61	1.69 1.68
	From: SD To: Q	t_{PLH} t_{PHL}	1.57 1.44	1.69 1.58	1.75 1.69	1.80 1.77	1.84 1.85
	From: SE To: Q	t_{PLH} t_{PHL}	1.63 1.61	1.70 1.74	1.79 1.83	1.88 1.91	1.99 1.98

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.05.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			SLF011	SLF012	SLF014	SLF016
Min C Width	High	t_w	1.27	1.27	1.35	1.27
Min C Width	Low	t_w	0.84	0.89	0.89	0.83
Min RN Width	Low	t_w	0.54	0.57	0.57	0.54
Min D Setup		t_{su}	0.66	0.72	0.72	0.66
Min D Hold		t_h	0.15	0.15	0.15	0.15
Min SD Setup		t_{su}	0.66	0.72	0.72	0.66
Min SD Hold		t_h	0.15	0.15	0.15	0.15
Min SE Setup		t_{su}	0.82	0.87	0.87	0.81
Min SE Hold		t_h	0.15	0.15	0.15	0.15
Min SCE Setup		t_{su}	1.00	1.00	1.08	1.00
Min SCE Hold		t_h	1.05	1.07	1.12	1.01
Min RN Setup		t_{su}	0.36	0.42	0.42	0.36
Min RN Hold		t_h	0.29	0.29	0.29	0.29

Logic Schematic