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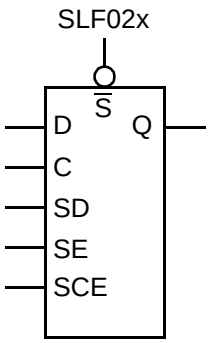
AMI5HG 0.5 micron CMOS Gate Array

Description

SLF02x is a family of static, master-slave, multiplexed scan latch, D flip-flops. When SCE is low it is a D flip-flop with the output buffered and changes state on the rising edge of the clock. When SCE is high it is a D latch that is transparent when C is low. SET is asynchronous and active low.

Logic Symbol



Truth Table

SN	C	D	SD	SE	SCE	Q
H	↑	H	X	L	L	H
H	↑	L	X	L	L	L
H	↑	X	H	H	L	H
H	↑	X	L	H	L	L
H	L	X	X	X	L	NC
H	L	H	X	L	H	H
H	L	L	X	L	H	L
H	L	X	H	H	H	H
H	L	X	L	H	H	L
H	H	X	X	X	H	NC
L	X	X	X	X	X	H

NC = No Change

HDL Syntax

Verilog ..... SLF02x *inst_name* (Q, C, D, SCE, SD, SE, SN);

VHDL..... *inst_name*:SLF02x port map (Q, C, D, SCE, SD, SE, SN);

Pin Loading

Pin Name	Equivalent Loads			
	SLF021	SLF022	SLF024	SLF026
C	1.0	1.0	1.0	1.0
D	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.2	2.2	2.2	2.2
SCE	2.1	2.2	2.2	2.1
SN	2.1	2.1	2.1	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
SLF021	13.0	TBD	29.9
SLF022	16.0	TBD	35.2
SLF024	16.0	TBD	38.1
SLF026	17.0	TBD	40.3

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
SLF021	From: C To: Q	t_{PLH} t_{PHL}	1.15 1.39	1.26 1.53	1.39 1.68	1.52 1.84	1.62 1.95
	From: D To: Q	t_{PLH} t_{PHL}	0.94 1.28	1.05 1.42	1.17 1.57	1.31 1.73	1.41 1.85
	From: SCE To: Q	t_{PLH} t_{PHL}	0.91 1.01	1.01 1.14	1.13 1.29	1.28 1.45	1.39 1.57
	From: SD To: Q	t_{PLH} t_{PHL}	0.95 1.24	1.05 1.38	1.17 1.53	1.32 1.69	1.43 1.81
	From: SE To: Q	t_{PLH} t_{PHL}	1.01 1.41	1.12 1.55	1.24 1.70	1.38 1.86	1.49 1.97
	From: SN To: Q	t_{PLH} t_{PHL}	0.55 0.74	0.65 0.94	0.77 1.19	0.92 1.50	1.04 1.74

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	Number of Equivalent Loads		1	8	15	22	30 (max)
SLF022	From: C To: Q	t_{PLH} t_{PHL}	1.06 1.41	1.18 1.55	1.28 1.65	1.38 1.75	1.47 1.85
	From: D To: Q	t_{PLH} t_{PHL}	0.93 1.27	1.04 1.46	1.14 1.57	1.24 1.66	1.35 1.75
	From: SCE To: Q	t_{PLH} t_{PHL}	0.82 0.96	0.94 1.11	1.04 1.22	1.15 1.32	1.26 1.43
	From: SD To: Q	t_{PLH} t_{PHL}	0.94 1.27	1.06 1.42	1.17 1.52	1.27 1.61	1.38 1.71
	From: SE To: Q	t_{PLH} t_{PHL}	1.05 1.42	1.15 1.55	1.24 1.66	1.31 1.76	1.40 1.87
	From: SN To: Q	t_{PLH} t_{PHL}	0.57 0.67	0.70 0.91	0.81 1.12	0.91 1.32	1.02 1.54
	Number of Equivalent Loads		**1**	**14**	**28**	**42**	**56 (max)**
SLF024	From: C To: Q	t_{PLH} t_{PHL}	1.18 1.51	1.23 1.68	1.33 1.78	1.44 1.86	1.58 1.93
	From: D To: Q	t_{PLH} t_{PHL}	0.97 1.36	1.10 1.47	1.21 1.60	1.31 1.72	1.39 1.84
	From: SCE To: Q	t_{PLH} t_{PHL}	0.92 1.00	1.01 1.21	1.11 1.33	1.22 1.42	1.32 1.49
	From: SD To: Q	t_{PLH} t_{PHL}	1.03 1.32	1.13 1.55	1.23 1.72	1.32 1.88	1.41 2.02
	From: SE To: Q	t_{PLH} t_{PHL}	1.10 1.50	1.23 1.59	1.33 1.70	1.41 1.82	1.47 1.94
	From: SN To: Q	t_{PLH} t_{PHL}	0.68 0.75	0.82 0.99	0.92 1.20	1.01 1.40	1.09 1.59

	Number of Equivalent Loads		1	21	42	62	83 (max)
SLF026	From: C To: Q	t_{PLH} t_{PHL}	1.43 1.86	1.51 1.97	1.60 2.06	1.69 2.14	1.79 2.22
	From: D To: Q	t_{PLH} t_{PHL}	1.28 1.72	1.40 1.89	1.47 1.97	1.52 2.03	1.57 2.07
	From: SCE To: Q	t_{PLH} t_{PHL}	1.19 1.41	1.30 1.55	1.39 1.65	1.45 1.73	1.52 1.81
	From: SD To: Q	t_{PLH} t_{PHL}	1.27 1.72	1.35 1.86	1.44 1.92	1.53 1.97	1.63 2.02
	From: SE To: Q	t_{PLH} t_{PHL}	1.35 1.87	1.44 2.00	1.53 2.08	1.60 2.13	1.68 2.19
	From: SN To: Q	t_{PLH} t_{PHL}	0.48 1.09	0.59 1.26	0.69 1.47	0.77 1.67	0.85 1.90

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			SLF021	SLF022	SLF024	SLF026
Min C Width	High	t_w	1.31	1.33	1.43	1.35
Min C Width	Low	t_w	0.92	0.98	0.98	0.91
Min SN Width	Low	t_w	0.37	0.44	0.44	0.38
Min D Setup		t_{su}	0.74	0.82	0.82	0.75
Min D Hold		t_h	0.15	0.15	0.15	0.15
Min SD Setup		t_{su}	0.74	0.82	0.82	0.75
Min SD Hold		t_h	0.15	0.15	0.15	0.15
Min SE Setup		t_{su}	0.90	0.97	0.97	0.90
Min SE Hold		t_h	0.15	0.15	0.15	0.15
Min SCE Setup		t_{su}	1.04	1.06	1.16	1.08
Min SCE Hold		t_h	1.04	1.07	1.12	1.01
Min SN Setup		t_{su}	0.19	0.25	0.25	0.19
Min SN Hold		t_h	0.52	0.52	0.52	0.52

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Logic Schematic