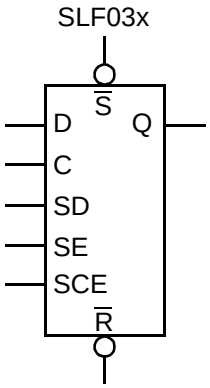
Description

SLF03x is a family of static, master-slave, multiplexed scan latch, D flip-flops. When SCE is low it is a D flip-flop with the output buffered and changes state on the rising edge of the clock. When SCE is high it is a D latch that is transparent when C is low. SET and RESET are asynchronous and active low.

Logic Symbol



Truth Table

RN	SN	C	D	SD	SE	SCE	Q
H	H	↑	H	X	L	L	H
H	H	↑	L	X	L	L	L
H	H	↑	X	H	H	L	H
H	H	↑	X	L	H	L	L
H	H	L	X	X	X	L	NC
H	H	L	H	X	L	H	H
H	H	L	L	X	L	H	L
H	H	L	X	H	H	H	H
H	H	L	X	L	H	H	L
H	H	H	X	X	X	H	NC
H	L	X	X	X	X	X	H
L	X	X	X	X	X	X	L

NC = No Change

HDL Syntax

Verilog ..... SLF03x *inst_name* (Q, C, D, RN, SCE, SD, SE, SN);

VHDL..... *inst_name*: SLF03x port map (Q, C, D, RN, SCE, SD, SE, SN);

Pin Loading

Pin Name	Equivalent Loads			
	SLF031	SLF032	SLF034	SLF036
C	1.0	1.0	1.0	1.0
D	1.0	1.0	1.0	1.0
RN	2.2	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.2	2.2	2.2	2.2
SCE	2.1	2.1	2.1	2.1
SN	2.1	2.2	2.2	2.2

AMI5HG 0.5 micron CMOS Gate Array

Size And Power Characteristics

Cell	Equivalent Gates	Size And Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
SLF031	16.0	TBD	34.7
SLF032	17.0	TBD	40.5
SLF034	18.0	TBD	43.8
SLF036	19.0	TBD	47.1

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
SLF031	From: C To: Q	t_{PLH} t_{PHL}	1.17 1.47	1.27 1.59	1.39 1.74	1.53 1.91	1.64 2.05
	From: D To: Q	t_{PLH} t_{PHL}	1.10 1.33	1.19 1.48	1.31 1.62	1.46 1.77	1.57 1.87
	From: RN To: Q	t_{PLH} t_{PHL}	0.84 0.76	0.94 0.91	1.06 1.05	1.20 1.21	1.30 1.32
	From: SCE To: Q	t_{PLH} t_{PHL}	0.96 1.02	1.06 1.15	1.18 1.30	1.32 1.46	1.44 1.59
	From: SD To: Q	t_{PLH} t_{PHL}	1.13 1.29	1.24 1.40	1.36 1.55	1.49 1.74	1.58 1.88
	From: SE To: Q	t_{PLH} t_{PHL}	1.18 1.45	1.28 1.60	1.40 1.74	1.54 1.89	1.64 1.99
	From: SN To: Q	t_{PLH} t_{PHL}	0.71 0.78	0.82 0.97	0.94 1.22	1.07 1.52	1.16 1.76

	Number of Equivalent Loads		1	8	15	22	30 (max)
SLF032	From: C To: Q	t_{PLH} t_{PHL}	1.21 1.48	1.29 1.62	1.38 1.72	1.47 1.82	1.58 1.92
	From: D To: Q	t_{PLH} t_{PHL}	1.16 1.38	1.26 1.52	1.35 1.62	1.44 1.72	1.53 1.82
	From: RN To: Q	t_{PLH} t_{PHL}	0.90 0.97	1.02 1.15	1.13 1.28	1.22 1.39	1.33 1.51
	From: SCE To: Q	t_{PLH} t_{PHL}	0.94 0.96	1.05 1.12	1.15 1.24	1.25 1.35	1.35 1.47
	From: SD To: Q	t_{PLH} t_{PHL}	1.18 1.35	1.28 1.52	1.37 1.63	1.45 1.72	1.55 1.81
	From: SE To: Q	t_{PLH} t_{PHL}	1.23 1.51	1.32 1.68	1.41 1.77	1.50 1.84	1.60 1.91
	From: SN To: Q	t_{PLH} t_{PHL}	0.62 0.76	0.75 1.00	0.86 1.21	0.96 1.41	1.08 1.63
SLF034	Number of Equivalent Loads		1	14	28	42	56 (max)
	From: C To: Q	t_{PLH} t_{PHL}	1.26 1.51	1.37 1.72	1.45 1.80	1.53 1.90	1.60 2.02
	From: D To: Q	t_{PLH} t_{PHL}	1.22 1.40	1.33 1.55	1.41 1.68	1.49 1.80	1.55 1.91
	From: RN To: Q	t_{PLH} t_{PHL}	0.95 1.12	1.06 1.32	1.16 1.44	1.26 1.55	1.36 1.64
	From: SCE To: Q	t_{PLH} t_{PHL}	0.97 1.04	1.06 1.19	1.19 1.31	1.30 1.40	1.41 1.49
	From: SD To: Q	t_{PLH} t_{PHL}	1.20 1.41	1.31 1.48	1.42 1.60	1.52 1.75	1.63 1.91
	From: SE To: Q	t_{PLH} t_{PHL}	1.29 1.57	1.41 1.75	1.51 1.84	1.60 1.92	1.68 1.98
	From: SN To: Q	t_{PLH} t_{PHL}	0.71 0.82	0.84 1.09	0.95 1.29	1.07 1.48	1.18 1.67

AMI5HG 0.5 micron CMOS Gate Array

	Number of Equivalent Loads		1	21	42	62	83 (max)
SLF036	From: C To: Q	t_{PLH} t_{PHL}	1.30 1.63	1.40 1.78	1.51 1.89	1.61 1.98	1.71 2.07
	From: D To: Q	t_{PLH} t_{PHL}	1.23 1.48	1.37 1.64	1.47 1.76	1.56 1.84	1.64 1.92
	From: RN To: Q	t_{PLH} t_{PHL}	1.03 1.28	1.09 1.49	1.20 1.62	1.31 1.74	1.43 1.84
	From: SCE To: Q	t_{PLH} t_{PHL}	1.07 1.09	1.18 1.25	1.28 1.37	1.37 1.49	1.46 1.60
	From: SD To: Q	t_{PLH} t_{PHL}	1.27 1.45	1.37 1.62	1.47 1.73	1.57 1.85	1.66 1.98
	From: SE To: Q	t_{PLH} t_{PHL}	1.34 1.62	1.43 1.76	1.53 1.88	1.62 1.99	1.72 2.11
	From: SN To: Q	t_{PLH} t_{PHL}	0.82 0.92	0.95 1.16	1.06 1.37	1.16 1.56	1.25 1.77

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell SLF031	SLF032	SLF034	SLF036
Min C Width	High	t_w	1.34	1.32	1.41	1.49
Min C Width	Low	t_w	0.94	1.02	1.02	1.02
Min RN Width	Low	t_w	0.81	0.72	0.72	0.72
Min SN Width	Low	t_w	0.53	0.45	0.45	0.45
Min D Setup		t_{su}	0.77	0.85	0.85	0.85
Min D Hold		t_h	0.14	0.15	0.15	0.15
Min RN Setup		t_{su}	0.36	0.45	0.45	0.45
Min RN Hold		t_h	0.28	0.29	0.29	0.29
Min SCE Setup		t_{su}	1.08	1.07	1.16	1.24
Min SCE Hold		t_h	1.05	1.05	1.09	1.13
Min SD Setup		t_{su}	0.77	0.85	0.85	0.85
Min SD Hold		t_h	0.14	0.15	0.15	0.15
Min SE Setup		t_{su}	0.92	1.01	1.01	1.01
Min SE Hold		t_h	0.14	0.15	0.15	0.15

Delay (ns) From / To	Parameter	Cell			
		SLF031	SLF032	SLF034	SLF036
Min SN Setup	t_{su}	0.23	0.29	0.29	0.29
Min SN Hold	t_h	0.51	0.50	0.50	0.50

Logic Schematic