美浦森半导体
M s e m i t e k

RoHS
LEAD FREE

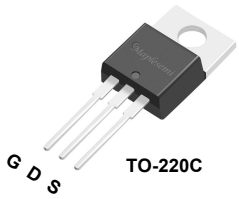
SLF12N65C/SLP12N65C
650V N-Channel MOSFET

General Description

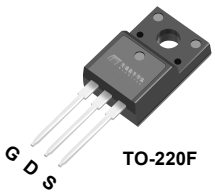
This Power MOSFET is produced using advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

Features

- 12A, 650V, $R_{DS(on)}$ = 0.75Ω@V_{GS} = 10 V
- Low gate charge (typical 52 nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



TO-220C



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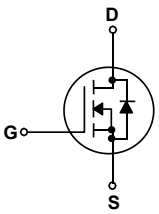


Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter		SLP12N65C	SLF12N65C	Units
V_{DSS}	Drain-Source Voltage		650		V
I_D	Drain Current - Continuous (T_C = 25℃)		12	12 *	A
	- Continuous (T_C = 100℃)		7.4	7.4 *	A
I_{DM}	Drain Current - Pulsed	(Note 1)	48	48 *	A
V_{GSS}	Gate-Source Voltage		±30		V
EAS	Single Pulsed Avalanche Energy	(Note 2)	865		mJ
I_{AR}	Avalanche Current	(Note 1)	12		A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	23		mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5		V/ns
P_D	Power Dissipation (T_C = 25℃)		230	54	W
	- Derate above 25℃		1.85	0.43	W/℃
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150		℃
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300		℃

* Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	SLP12N65C	SLF12N65C	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.54	2.33	℃/W
$R_{\theta JS}$	Thermal Resistance, Case-to-Sink Typ.	0.5	--	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	℃/W

Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 uA	650	--	--	V
$\triangle BV_{DSS}$ / $\triangle T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 uA, Referenced to 25℃	--	0.65	--	V/℃
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V	--	--	1	uA
		V_{DS} = 520 V, T_C = 125℃	--	--	10	uA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 uA	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 6 A	--	0.63	0.75	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 6 A (Note 4)	--	13	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	1850	--	pF
C_{oss}	Output Capacitance		--	180	--	pF
C_{rss}	Reverse Transfer Capacitance		--	20	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 325 V, I_D = 12 A, R_G = 25 Ω (Note 4, 5)	--	30	--	ns
t_r	Turn-On Rise Time		--	90	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	140	--	ns
t_f	Turn-Off Fall Time		--	90	--	ns
Q_g	Total Gate Charge	V_{DS} = 520 V, I_D = 12 A, V_{GS} = 10 V (Note 4, 5)	--	52	--	nC
Q_{gs}	Gate-Source Charge		--	8.5	--	nC
Q_{gd}	Gate-Drain Charge		--	20	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	12	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	48	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 12 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 12 A, dI_F / dt = 100 A/us (Note 4)	--	430	--	ns
Q_{rr}	Reverse Recovery Charge		--	5.0	--	uC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 11mH, I_{AS} = 12A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
3. $I_{SD} \leq$ 12A, di/dt ≤ 200A/us, $V_{DD} \leq BV_{DSS,}$ Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300us, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

Typical Characteristics

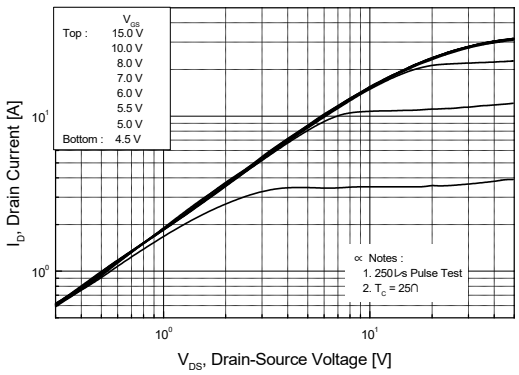


Figure 1. On-Region Characteristics

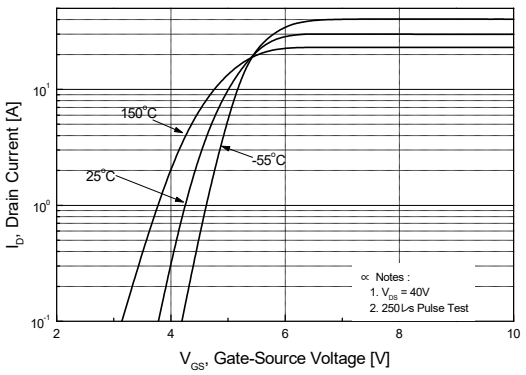


Figure 2. Transfer Characteristics

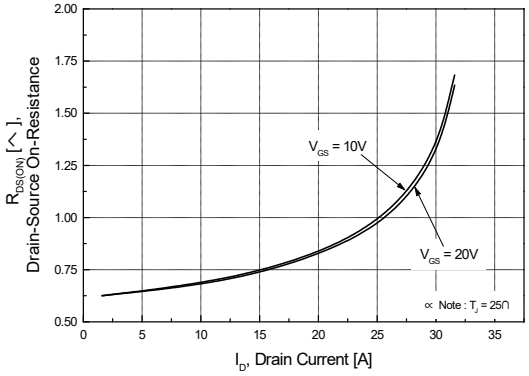


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

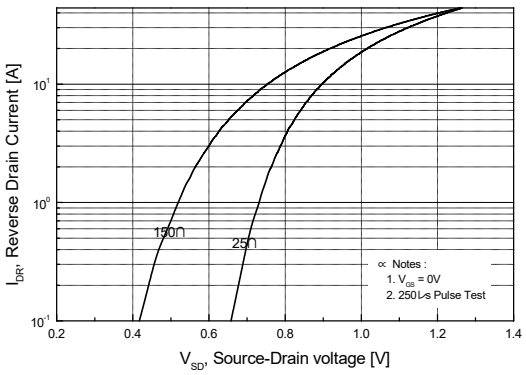


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

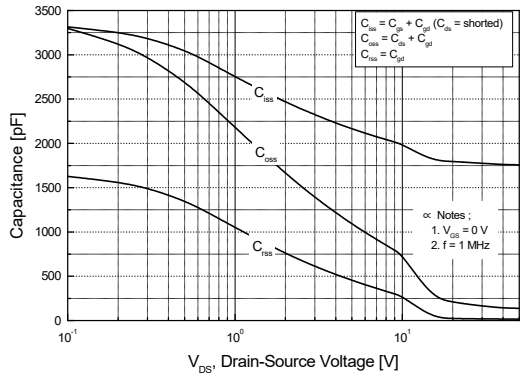


Figure 5. Capacitance Characteristics

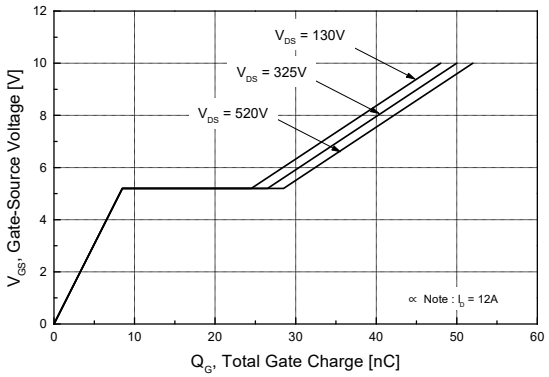


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

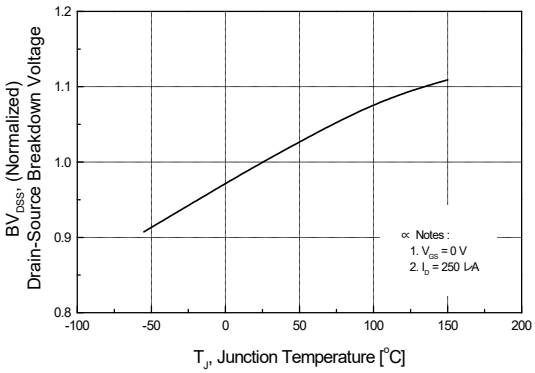


Figure 7. Breakdown Voltage Variation vs Temperature

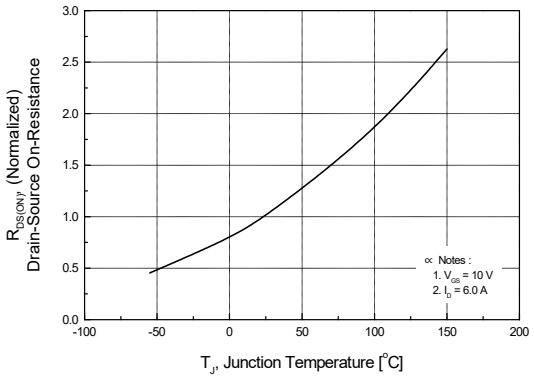


Figure 8. On-Resistance Variation vs Temperature

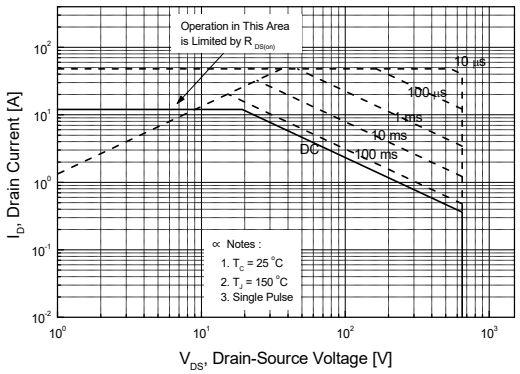


Figure 9-1. Maximum Safe Operating Area for SLP12N65C

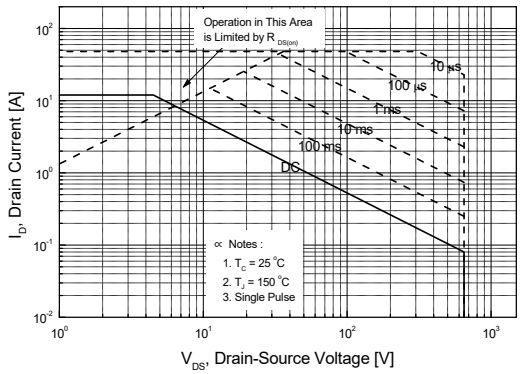


Figure 9-2. Maximum Safe Operating Area for SLF12N65C

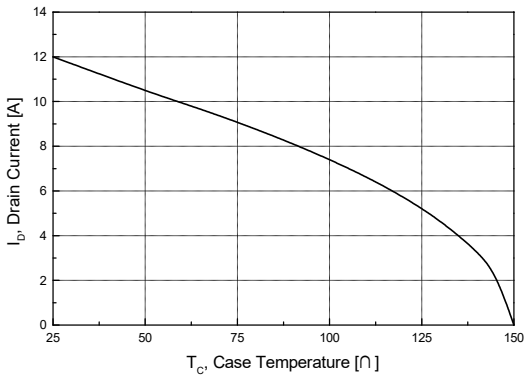


Figure 10. Maximum Drain Current vs Case Temperature

Typical Characteristics (Continued)

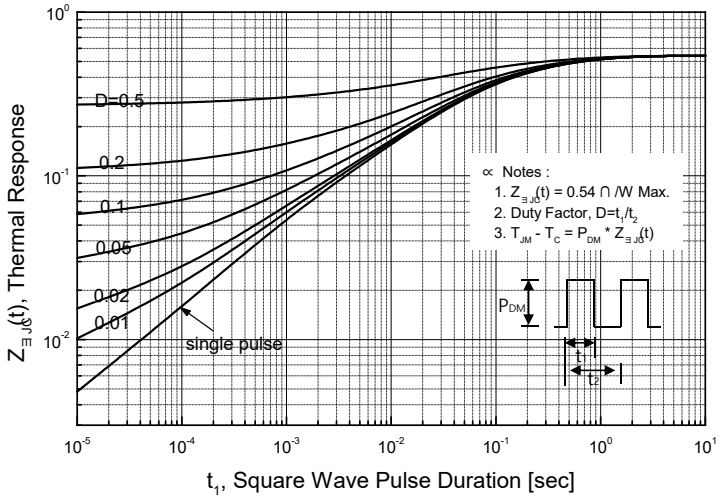


Figure 11-1. Transient Thermal Response Curve for P12N65

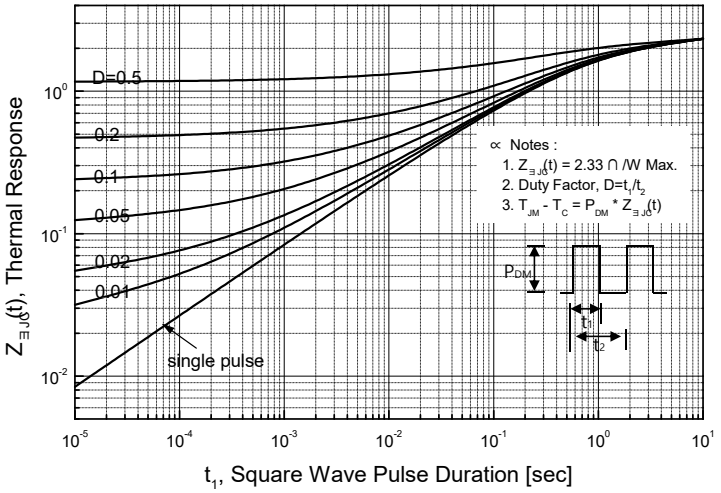
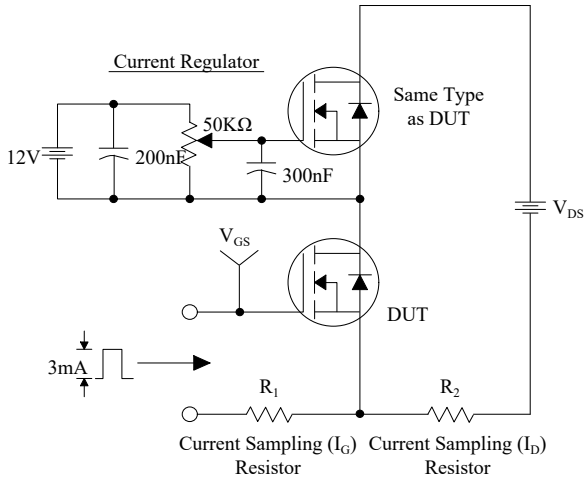
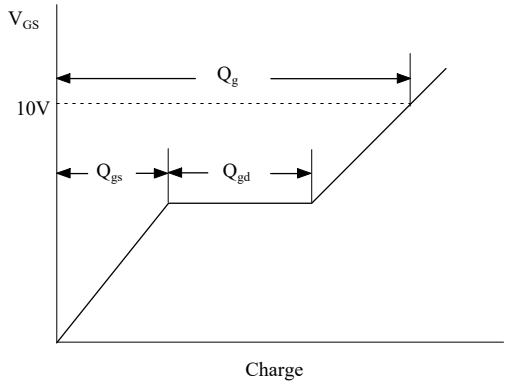


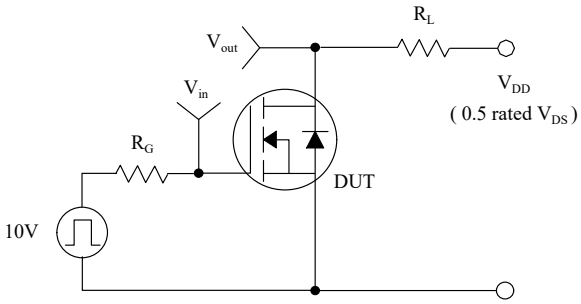
Figure 11-2. Transient Thermal Response Curve for F12N65

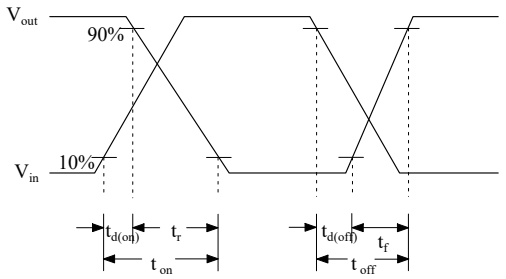
Gate Charge Test Circuit & Waveform



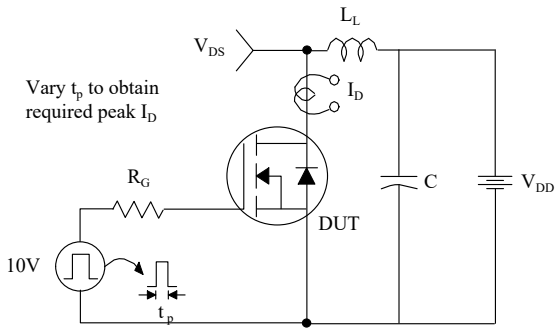


Resistive Switching Test Circuit & Waveforms

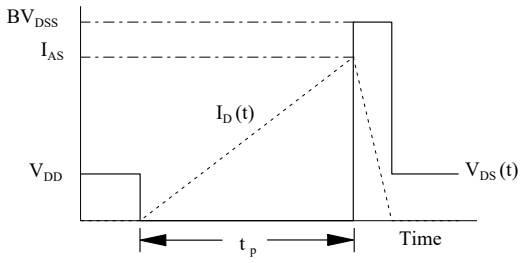




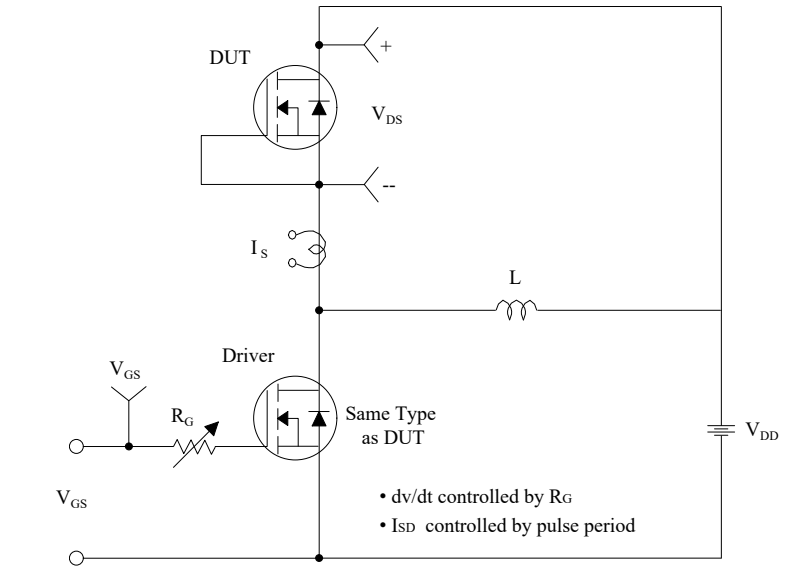
Unclamped Inductive Switching Test Circuit & Waveforms

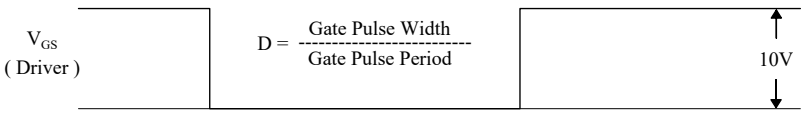


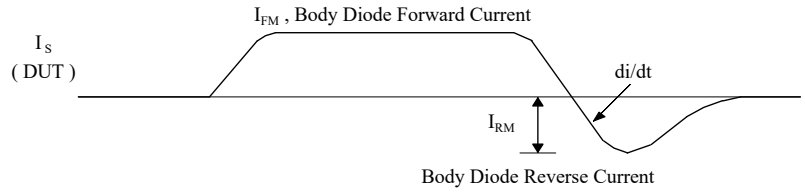
$$E_{AS} = \frac{1}{2} L_L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

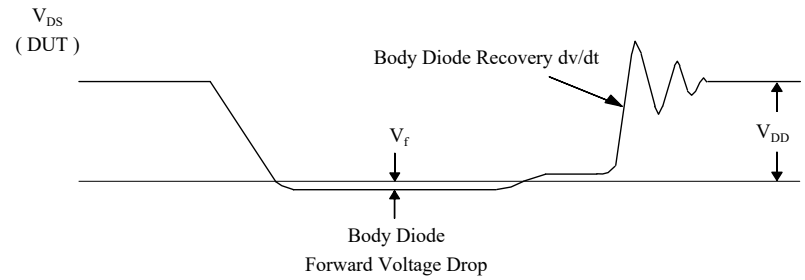


Peak Diode Recovery dv/dt Test Circuit & Waveforms

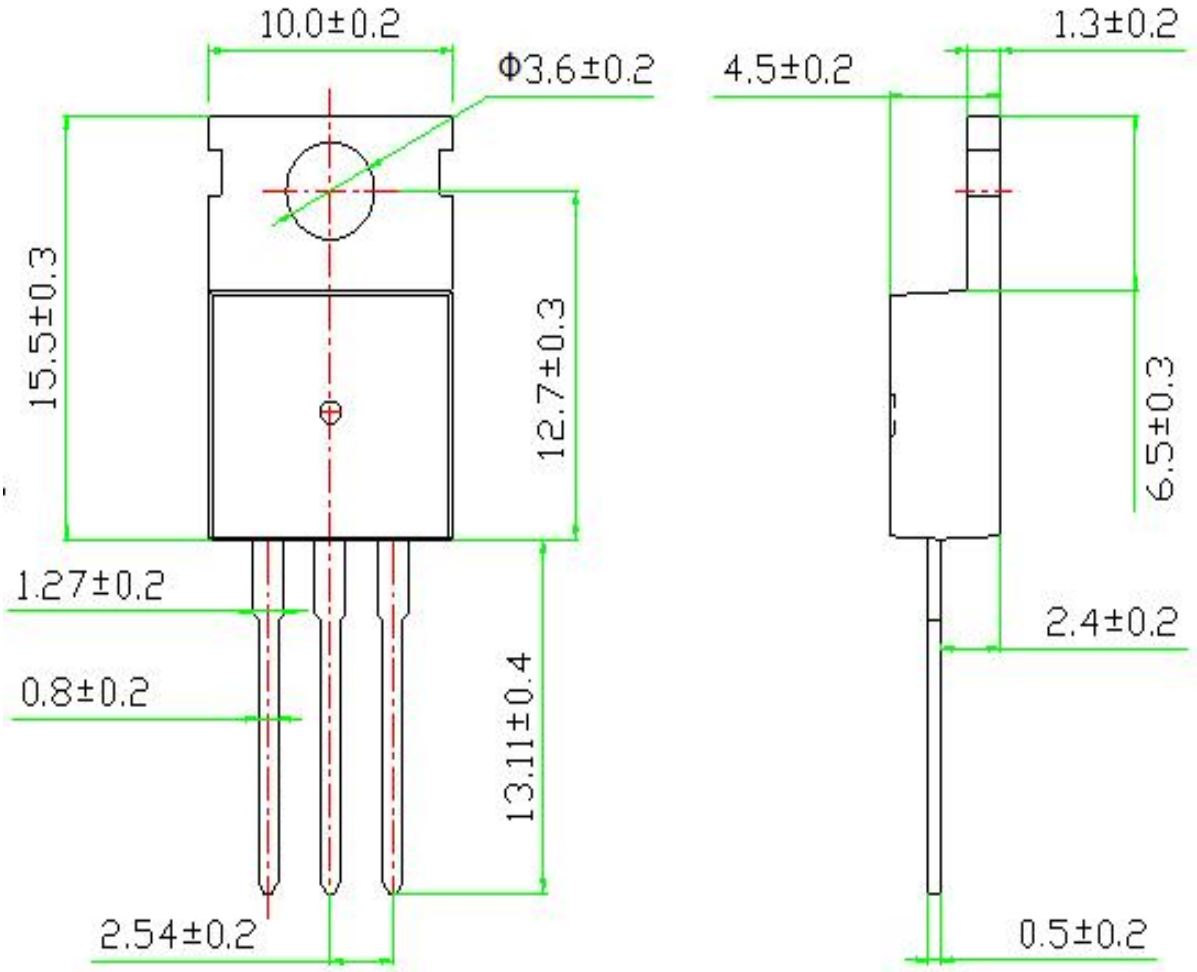




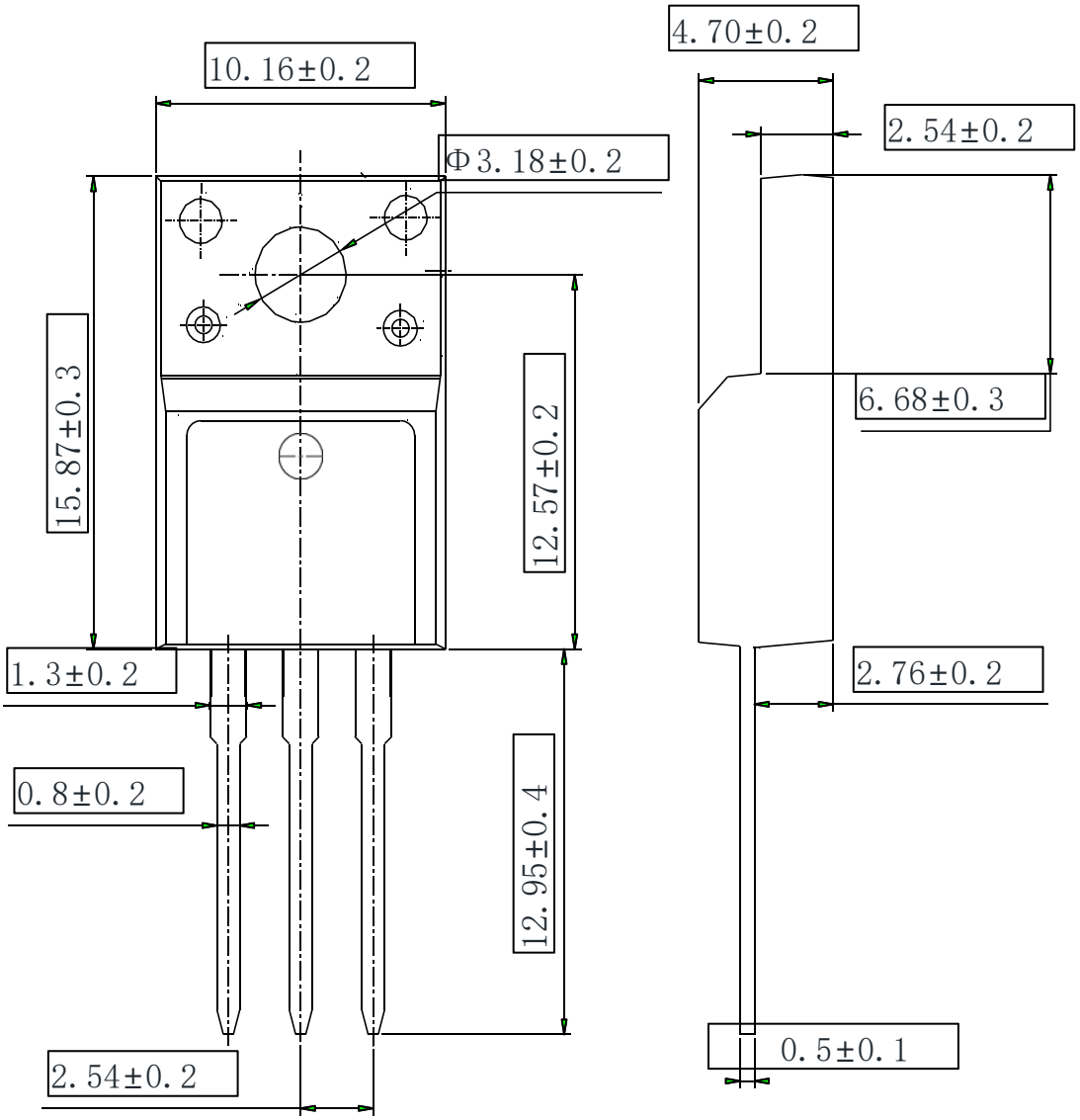




TO-220C OUTLINE



TO-220F OUTLINE



NOTE：
1The plastic package is not marked as smooth surfaceRa=0.1;Subglossy surfaceRa=0.8
2.Undeclared tolerance±0.15,Unmarked filletRmax=0.25

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