



SLP18N50C / SLF18N50C

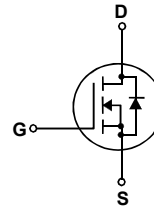
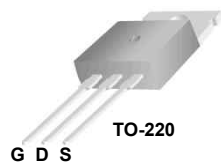
500V N-Channel MOSFET

General Description

This Power MOSFET is produced using Maple semi's advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

Features

- 18A, 500V, $R_{DS(on)typ.} = 236m\Omega @ V_{GS} = 10V$
- Low gate charge (typical 69nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



Absolute Maximum Ratings

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	SLP18N50C	SLF18N50C	Units
V_{DSS}	Drain-Source Voltage	500		V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	18.0	18.0 *	A
	- Continuous ($T_C = 100^\circ\text{C}$)	10.8	10.8 *	A
I_{DM}	Drain Current - Pulsed (Note 1)	64	64 *	A
V_{GSS}	Gate-Source Voltage	± 30		V
EAS	Single Pulsed Avalanche Energy (Note 2)	371		mJ
I_{AR}	Avalanche Current (Note 1)	18		A
E_{AR}	Repetitive Avalanche Energy (Note 1)	22.93		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5		V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	229	41	W
	- Derate above 25°C	1.83	0.33	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to $+150$		$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		$^\circ\text{C}$

* Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	SLP18N50C	SLF18N50C	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.54	3.04	$^\circ\text{C}/\text{W}$
$R_{\theta JS}$	Thermal Resistance, Case-to-Sink Typ.	0.5	--	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	$^\circ\text{C}/\text{W}$

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 uA	500	--	--	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 uA, Referenced to 25°C	--	0.5	--	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 500 V, V _{GS} = 0 V	--	--	1	uA
		V _{DS} = 400 V, T _C = 125°C	--	--	10	uA
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30 V, V _{DS} = 0 V	--	--	100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -30 V, V _{DS} = 0 V	--	--	-100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 uA	2.0	--	4.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 9 A	--	236	283	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 40 V, I _D = 9 A (Note 4)	--	12	--	S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz	--	3053	--	pF
C _{oss}	Output Capacitance		--	335	--	pF
C _{rss}	Reverse Transfer Capacitance		--	21	--	pF
Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	V _{DD} = 250 V, I _D = 18 A, R _G = 25 Ω (Note 4, 5)	--	48.5	--	ns
t _r	Turn-On Rise Time		--	43.5	--	ns
t _{d(off)}	Turn-Off Delay Time		--	261	--	ns
t _f	Turn-Off Fall Time		--	70.5	--	ns
Q _g	Total Gate Charge	V _{DS} = 400 V, I _D = 18 A, V _{GS} = 10 V (Note 4, 5)	--	69	--	nC
Q _{gs}	Gate-Source Charge		--	16.5	--	nC
Q _{gd}	Gate-Drain Charge		--	31.2	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	18	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	72	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 18 A	--	--	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 18 A,	--	452	--	ns
Q _{rr}	Reverse Recovery Charge	di _F / dt = 100 A/us (Note 4)	--	6.2	--	uC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 2.0\text{ mH}, I_{AS} = 18\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\text{ }\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 18\text{ A}, di/dt \leq 100\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

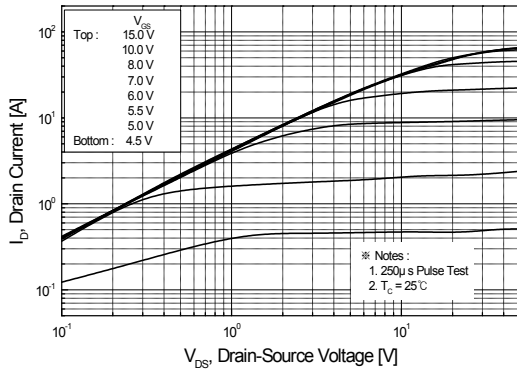


Figure 1. On-Region Characteristics

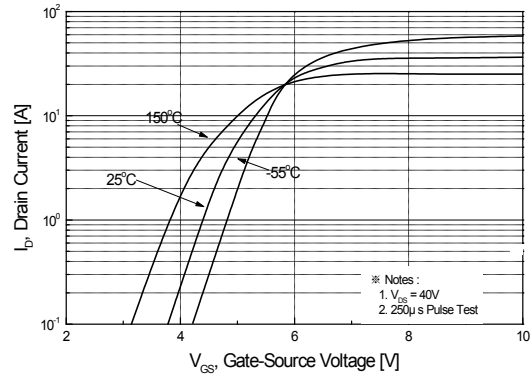


Figure 2. Transfer Characteristics

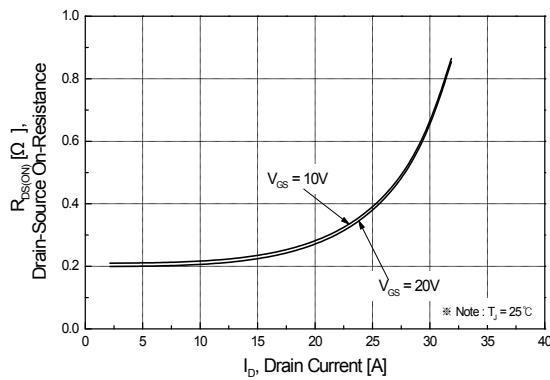


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

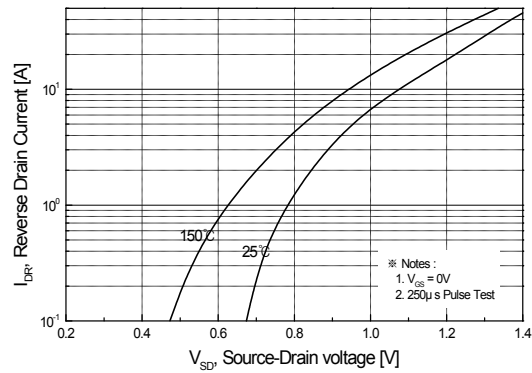


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

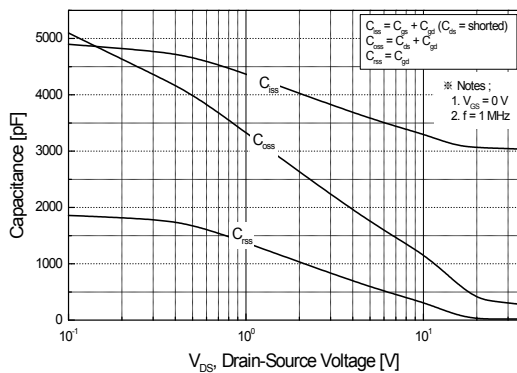


Figure 5. Capacitance Characteristics

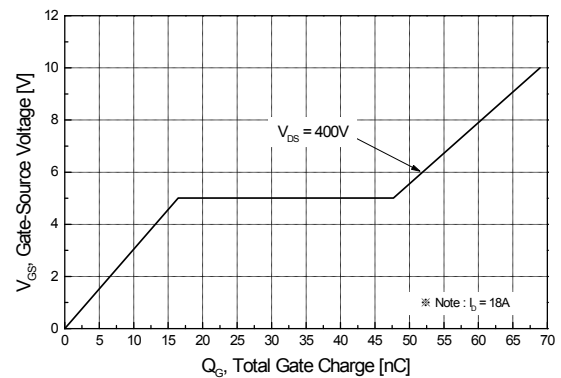


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

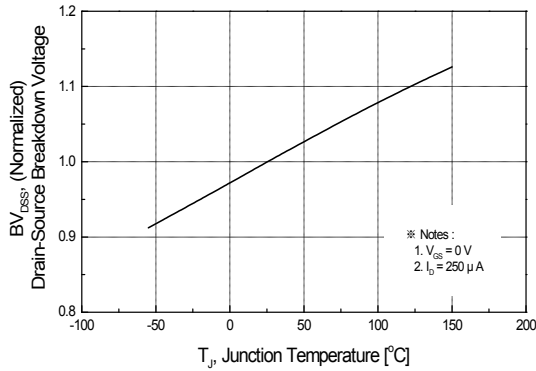


Figure 7. Breakdown Voltage Variation vs Temperature

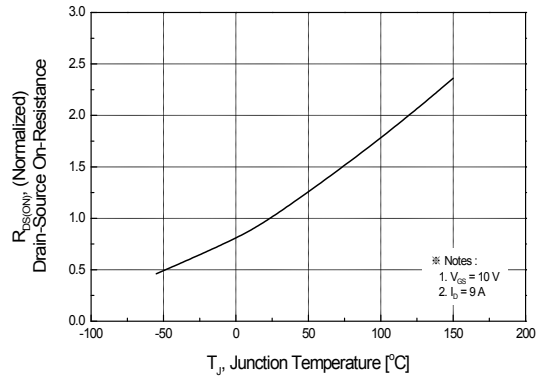


Figure 8. On-Resistance Variation vs Temperature

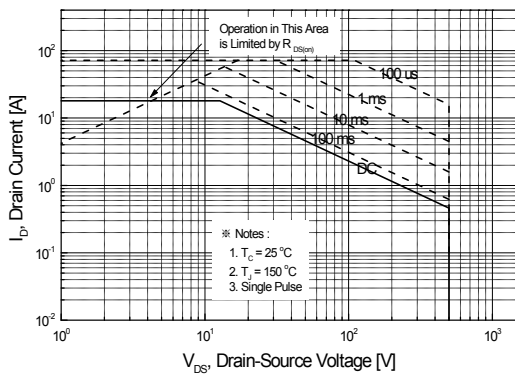


Figure 9-1. Maximum Safe Operating Area for SLP18N50C

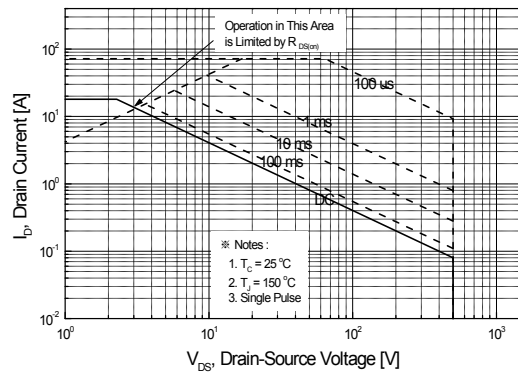


Figure 9-2. Maximum Safe Operating Area for SLF18N50C

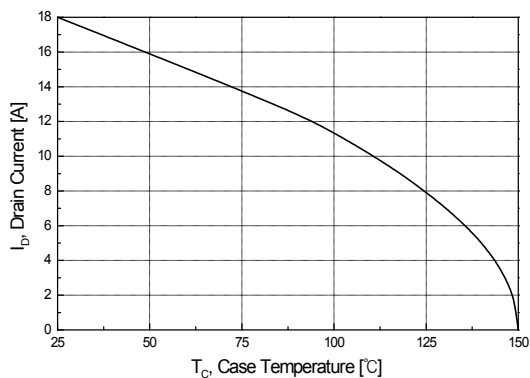


Figure 10. Maximum Drain Current vs Case Temperature

Typical Characteristics (Continued)

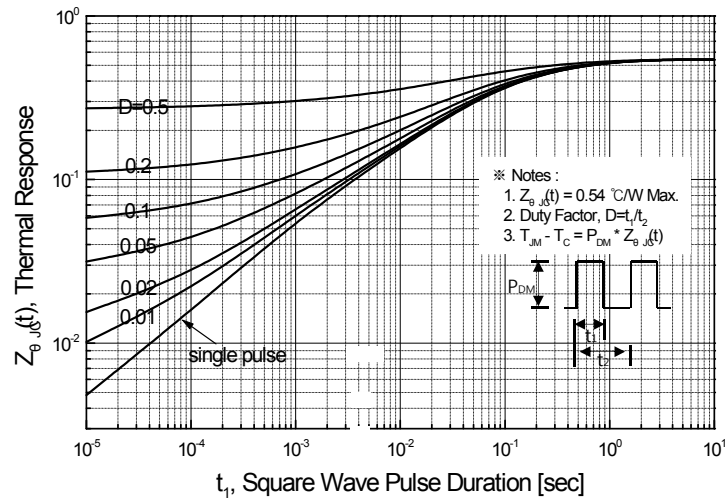


Figure 11-1. Transient Thermal Response Curve for SLP18N50C

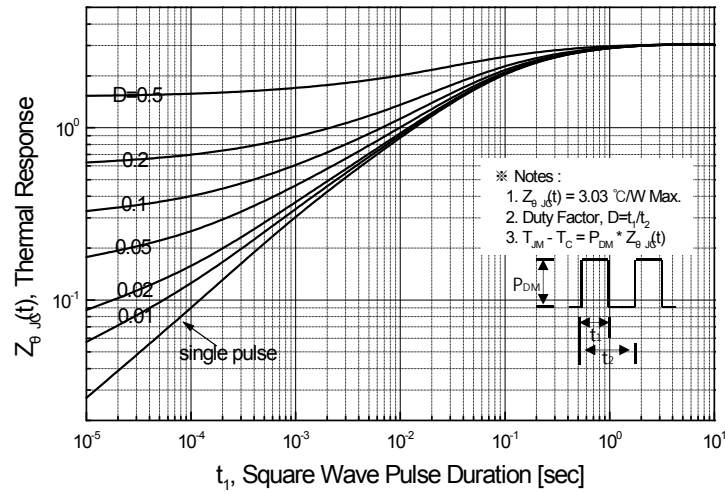
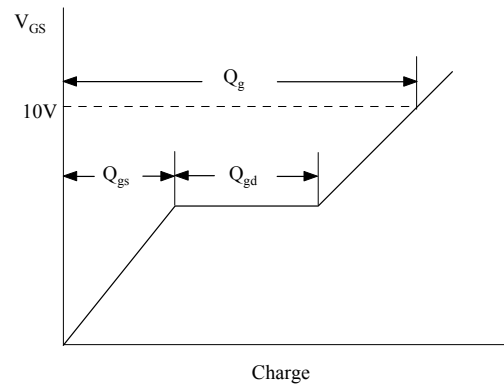
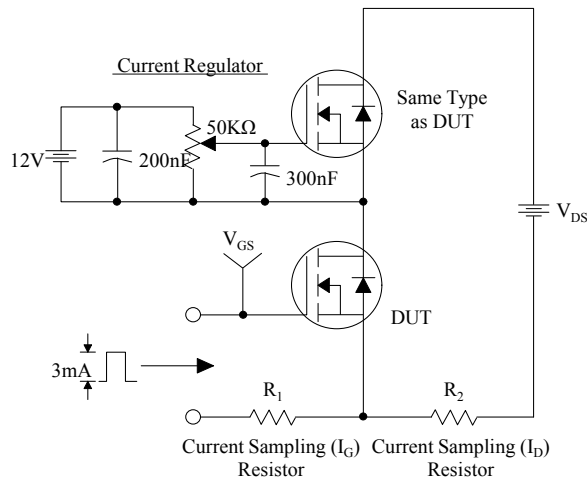
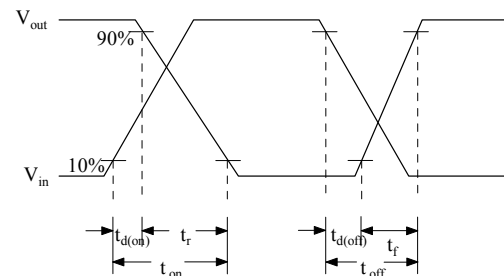
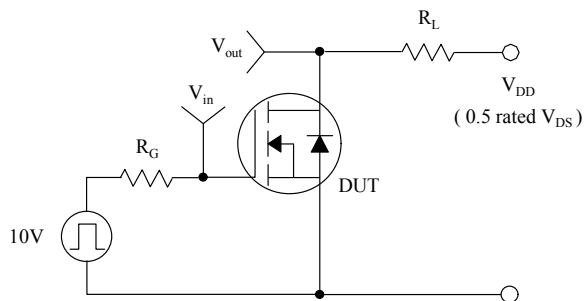


Figure 11-2. Transient Thermal Response Curve for SLF18N50C

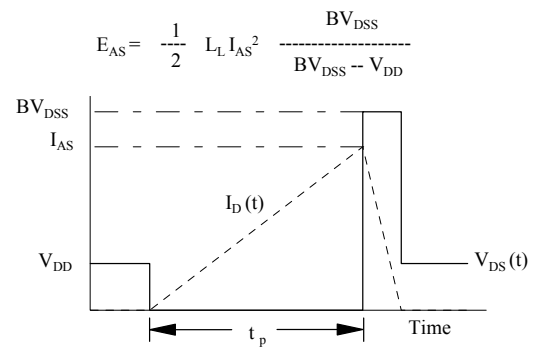
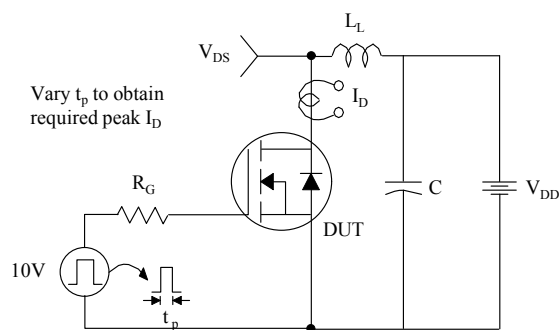
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms

