RoHS
LEAD FREE

SLF20N50C

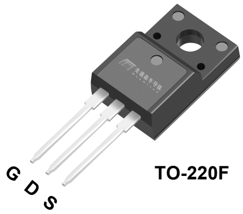
500V N-channel MOSFET

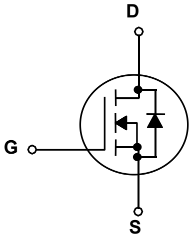
General Description

This Power MOSFET is produced using Msemitek's advanced planar stripe DMOS technology.
This advanced technology has been especially tailored to minimize conduction loss, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.
These devices are well suited for AC/DC power conversion in switching mode operation for higher efficiency.

Features

- 20A, 500V, $R_{DS(on)typ}$= 200mΩ@V_{GS} = 10 V
- Low gate charge (typical 90nC)
- LowCrss (typical 33pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability





Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter	SLF20N50C	Units
V_{DSS}	Drain-Source Voltage	500	V
I_D	Drain Current - Continuous (T_C = 25℃)	20	A
	- Continuous (T_C = 100℃)	11.7	A
I_{DM}	Drain Current - Pulsed (Note 1)	80	A
V_{GSS}	Gate-Source Voltage	±30	V
EAS	Single Pulsed Avalanche Energy (Note 2)	680	mJ
P_D	Power Dissipation (T_C = 25℃)	43	W
	- Derate above 25℃	0.34	W/℃
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	℃
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	℃

* Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	SLF20N50C	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.94	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	℃/W

Package Marking

Part Number	Top Marking	Package	Packing Method	MOQ	QTY
SLF20N50C	SLF20N50C	TO-220F	Tube	1000	5000

Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 uA	500	--	--	V
$\triangle BV_{DSS} / \triangle T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 uA, Referenced to 25℃	--	0.59	--	V/℃
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500 V, V_{GS} = 0 V	--	--	1	uA
		V_{DS} = 400 V, T_C = 125℃	--	--	10	uA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 uA	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 10A	--	200	260	mΩ

Dynamic Characteristics

C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	3290	--	pF
C_{oss}	Output Capacitance		--	356	--	pF
C_{rss}	Reverse Transfer Capacitance		--	33	--	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 250 V, I_D = 10A, R_G = 25 Ω (Note 4, 5)	--	125	--	ns
t_r	Turn-On Rise Time		--	68	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	275	--	ns
t_f	Turn-Off Fall Time		--	65	--	ns
Q_g	Total Gate Charge	V_{DS} = 250 V, I_D = 10A, V_{GS} = 10 V (Note 4, 5)	--	90	--	nC
Q_{gs}	Gate-Source Charge		--	14	--	nC
Q_{gd}	Gate-Drain Charge		--	40	--	nC
R_G	Gate Resistance	f = 1MHz	--	2	--	Ω

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	20	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	80	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 20A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 20A, dI_F / dt = 100 A/us (Note 4)	--	1250	--	ns
Q_{rr}	Reverse Recovery Charge		--	18	--	uC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 0.5 mH,V_G =10V,V_{DD} =50V, Starting T_J = 25°C
3. $I_{SD} \leq$ 20A, di/dt $\leq$ 200A/us, $V_{DD} \leq BV_{DSS}$, Starting T_J = 25°C
4. Pulse Test : Pulse width $\leq$ 300us, Duty cycle $\leq$ 2%
5. Essentially independent of operating temperature

Typical Characteristics

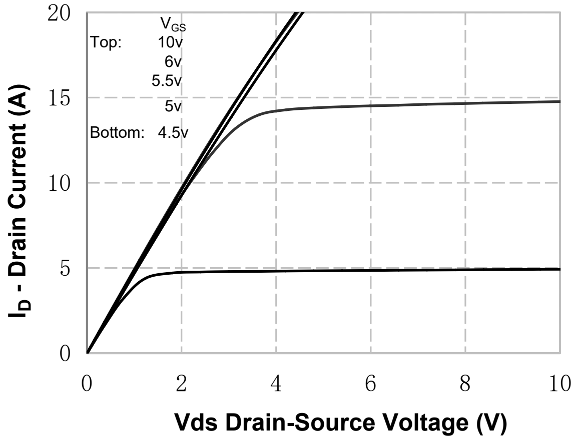


Figure 1. On-Region Characteristics

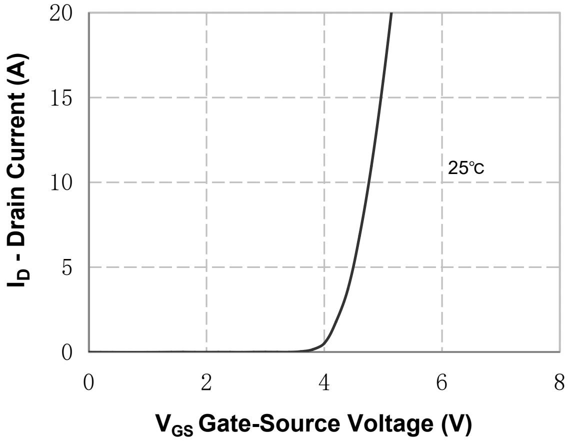


Figure 2. Transfer Characteristics

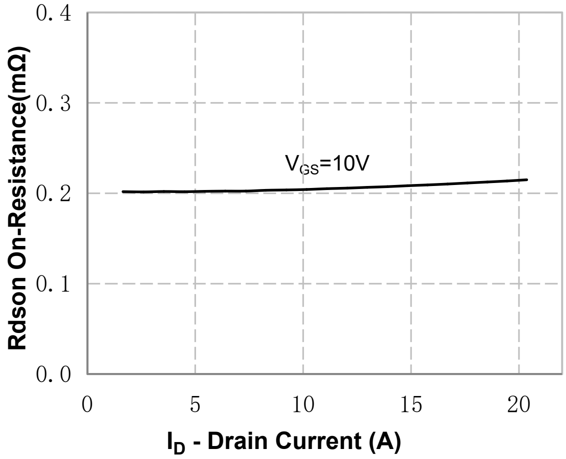


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

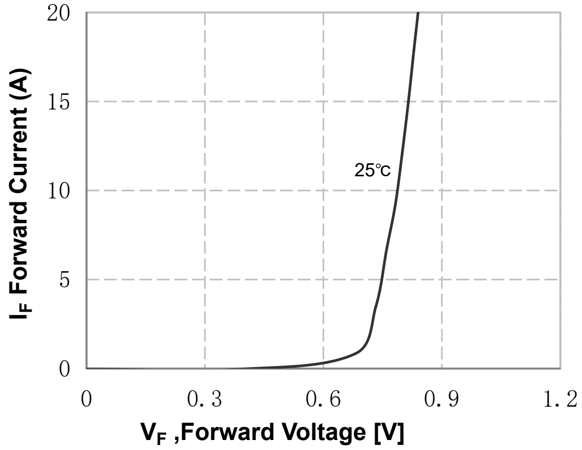


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

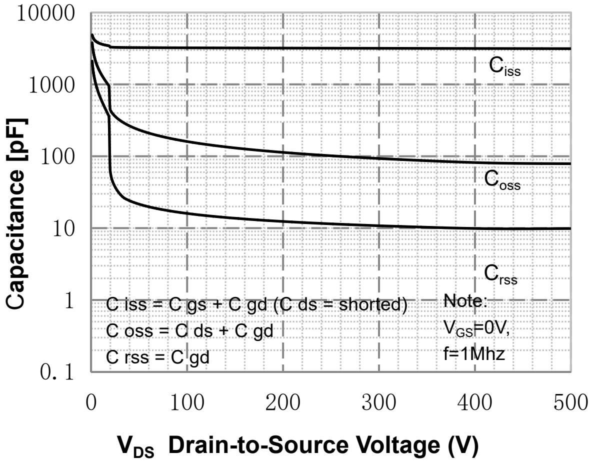


Figure 5. Capacitance Characteristics

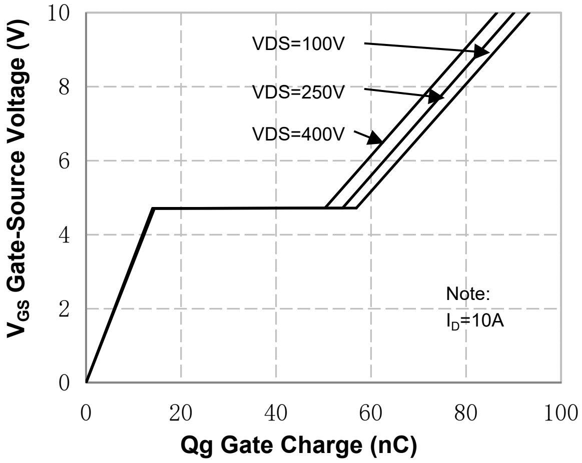


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

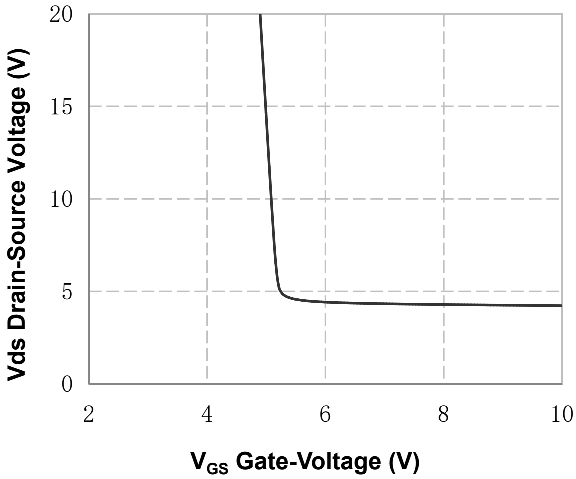


Figure 7. Vds Drain-Source Voltage vs Gate Voltage

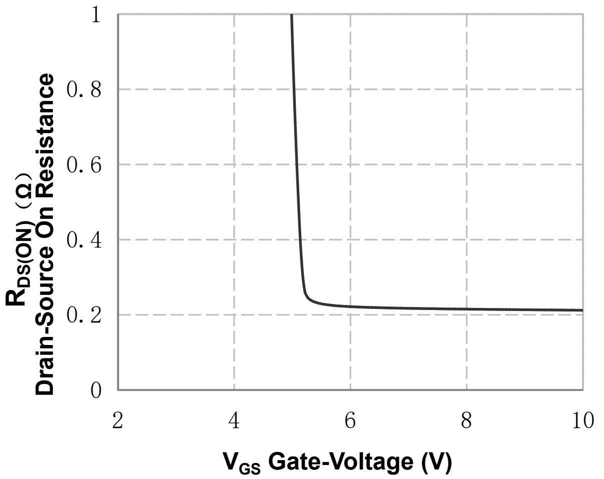


Figure 8. On-Resistance vs Gate Voltage

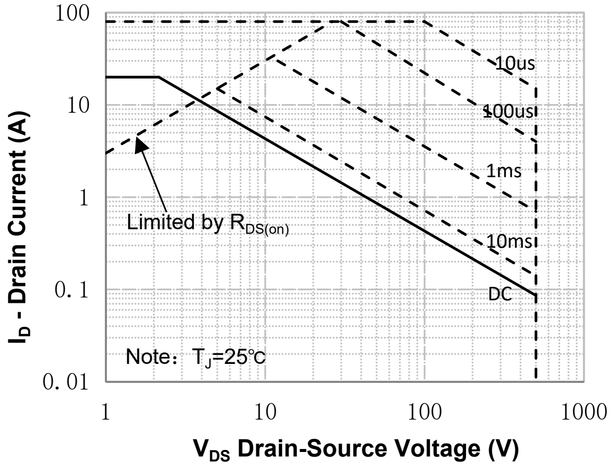


Figure 9. Maximum Safe Operating Area

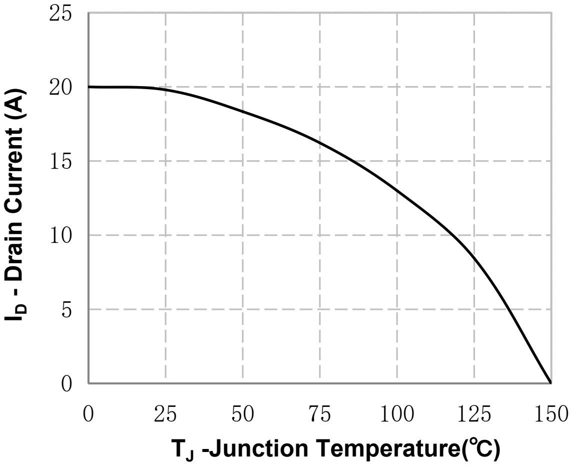


Figure 10. Maximum Drain Current vs Case Temperature

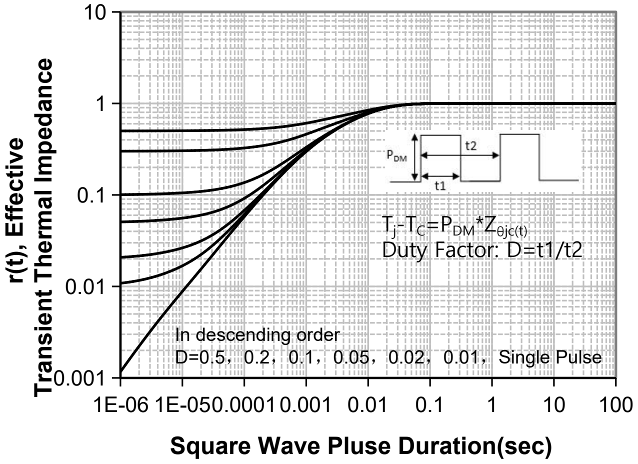
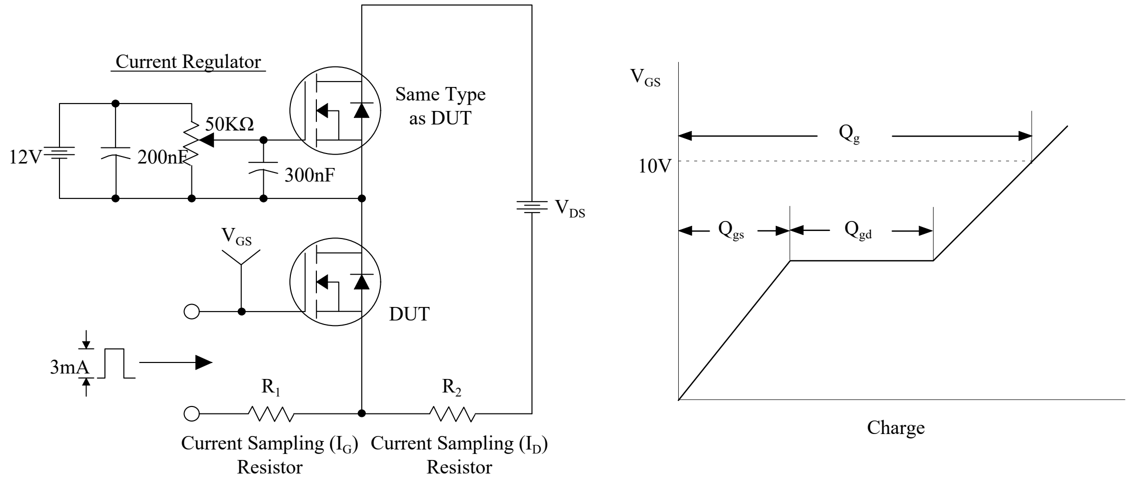
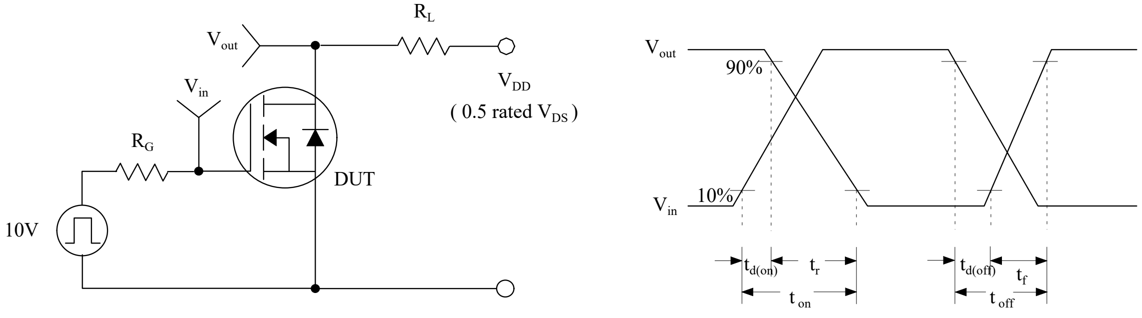


Figure 11. Transient Thermal Response Curve

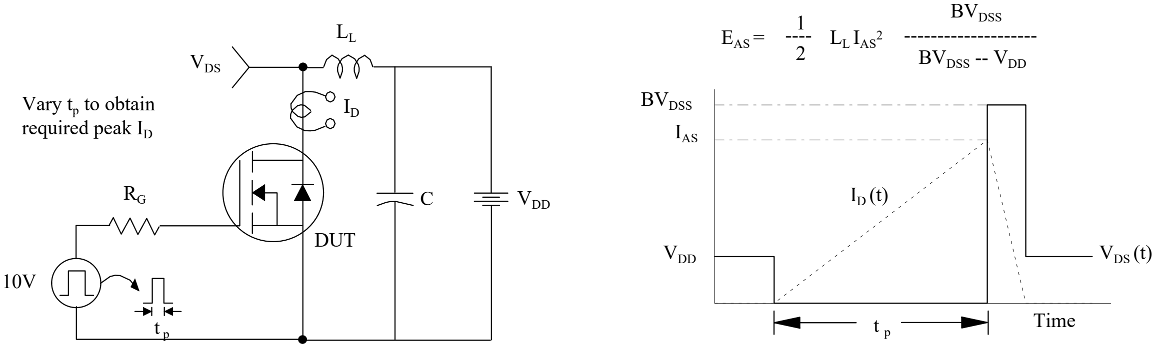
Gate Charge Test Circuit & Waveform



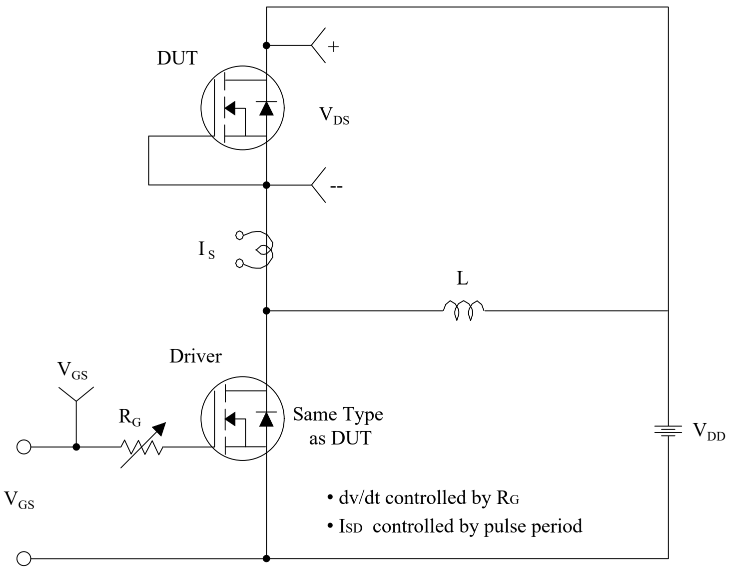
Resistive Switching Test Circuit & Waveforms

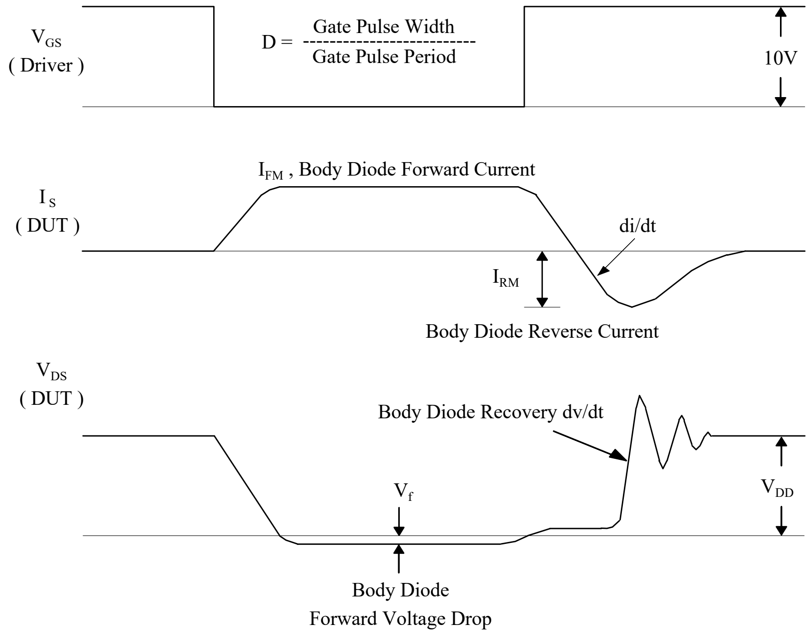


Unclamped Inductive Switching Test Circuit & Waveforms

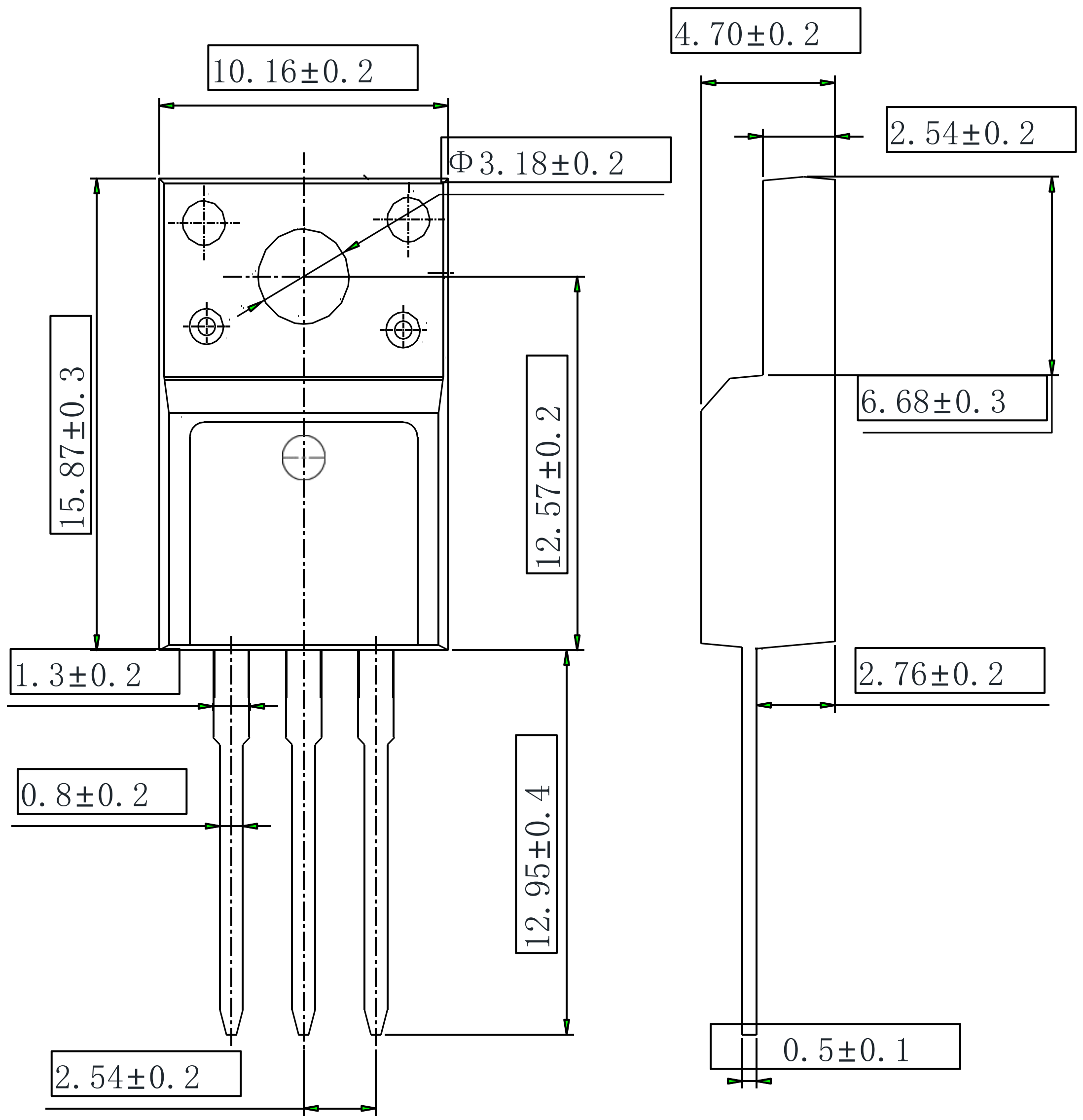


Peak Diode Recovery dv/dt Test Circuit & Waveforms





TO-220F OUTLINE



NOTE：

1The plastic package is not marked as smooth surfaceRa=0.1;Subglossy surfaceRa=0.8

2.Undeclared tolerance±0.15,Unmarked filletRmax=0.25

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