



**CB-FET**

SLP60R650SJ/SLF60R650SJ

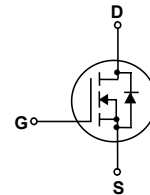
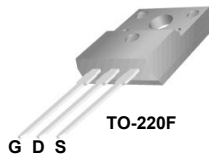
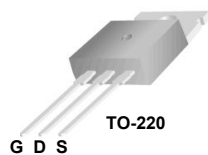
## SLP60R650SJ/SLF60R650SJ 600V N-Channel MOSFET

### General Description

This Power MOSFET is produced using Maple semi's Advanced Super-Junction technology. This advanced technology has been especially tailored to minimize conduction loss, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for AC/DC power conversion in switching mode operation for higher efficiency.

### Features

- 7A, 600V,  $R_{DS(on) typ.} = 0.58\Omega @ V_{GS} = 10V$
- Low gate charge ( typical 25nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



### Absolute Maximum Ratings

$T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	SLP60R650SJ	SLF60R650SJ	Units
$V_{DSS}$	Drain-Source Voltage	600		V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ ) - Continuous ( $T_C = 100^\circ\text{C}$ )	7	7*	A
		5	5*	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	10	10*	A
$V_{GSS}$	Gate-Source Voltage	±30		V
EAS	Single Pulsed Avalanche Energy (Note 2)	86		mJ
$I_{AR}$	Avalanche Current (Note 1)	1.7		A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	43		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5		V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	205	35	W
		1.67	0.3	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		$^\circ\text{C}$

\* Drain current limited by maximum junction temperature.

### Thermal Characteristics

Symbol	Parameter	SLP60R650SJ	SLF60R650SJ	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.6	3.5	$^\circ\text{C}/\text{W}$
$R_{\theta JS}$	Thermal Resistance, Case-to-Sink Typ.	0.5	--	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62	62	$^\circ\text{C}/\text{W}$

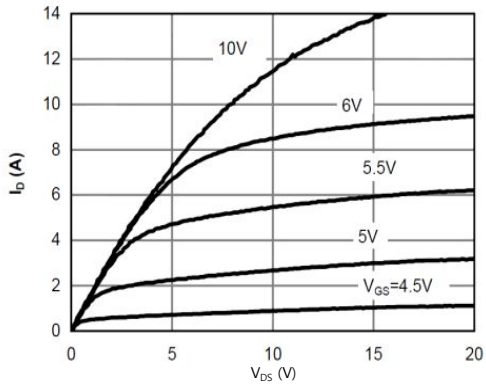
**Electrical Characteristics**T<sub>C</sub> = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA, T <sub>J</sub> =25°C	600	--	--	V
		V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA, T <sub>J</sub> =150°C	--	650	--	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	--	0.6	--	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V	--	--	1	μA
		V <sub>DS</sub> = 480 V, T <sub>C</sub> = 125°C	--	--	10	μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V	--	--	-100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.5	3.5	4.5	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3.5 A	--	0.58	0.65	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 3.5 A (Note 4)	--	16	--	S
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	--	360	--	pF
C <sub>oss</sub>	Output Capacitance		--	25	--	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	1.2	--	pF
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 400 V, I <sub>D</sub> = 3.5 A, R <sub>G</sub> = 20 Ω (Note 4, 5)	--	25	--	ns
t <sub>r</sub>	Turn-On Rise Time		--	55	--	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	70	--	ns
t <sub>f</sub>	Turn-Off Fall Time		--	40	--	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 480 V, I <sub>D</sub> = 7 A, V <sub>GS</sub> = 10 V (Note 4, 5)	--	8	--	nC
Q <sub>gs</sub>	Gate-Source Charge		--	2.0	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	2.7	--	nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	7	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	18	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 7 A	--	--	1.5	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 7 A,	--	190	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI <sub>F</sub> / dt = 100 A/μs (Note 4)	--	2.3	--	μC

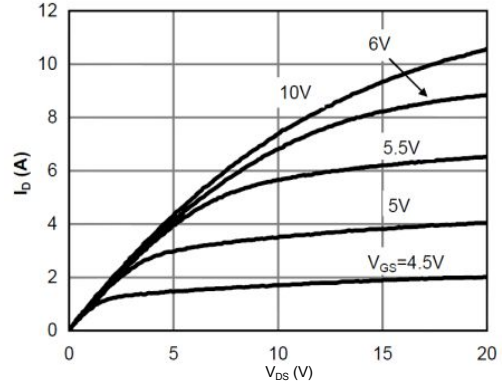
**NOTES:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L=60mH, I<sub>AS</sub>=1.7A, V<sub>DD</sub>=150V, Starting T<sub>J</sub>=25 °C
3. I<sub>SD</sub>≤7A, di/dt ≤ 200A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, Starting T<sub>J</sub> = 25 °C
4. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature Typical Characteristics

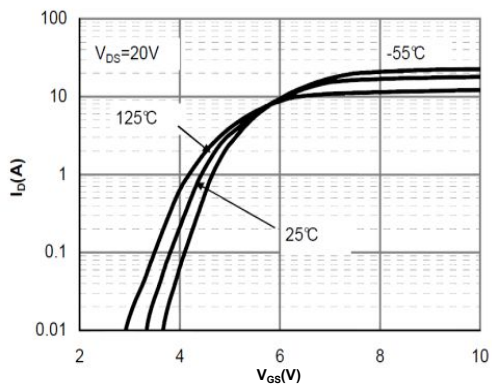
**Typical Characteristics**



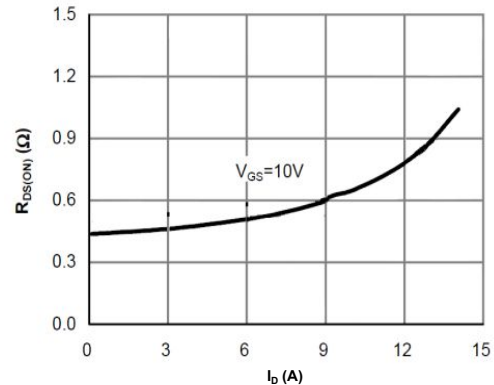
**Figure 1: On-Region Characteristics@25°C**



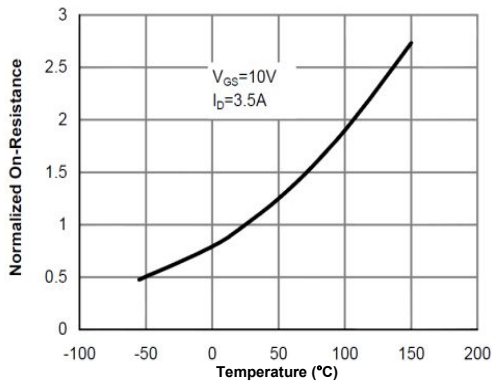
**Figure 2: On-Region Characteristics@125°C**



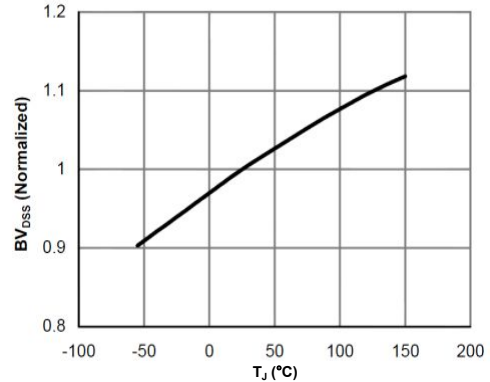
**Figure 3: Transfer Characteristics**



**Figure 4: On-Resistance vs. Drain Current and Gate Voltage**

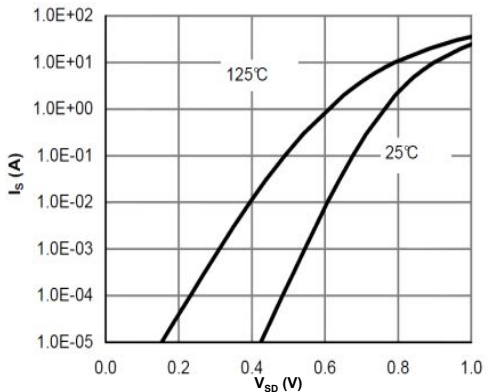


**Figure 5: On-Resistance vs. Junction Temperature**

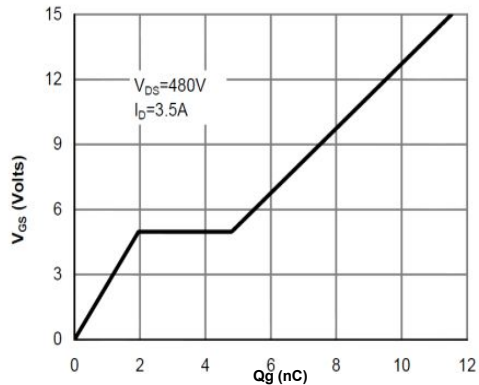


**Figure 6: Break Down vs. Junction Temperature**

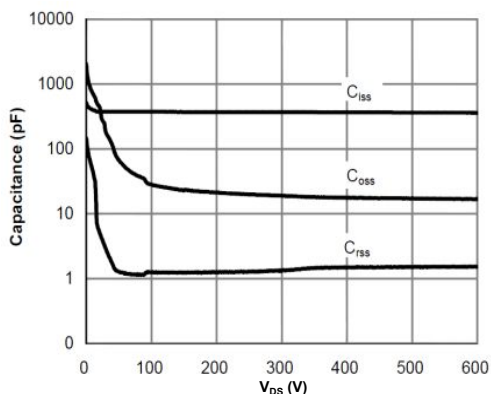
**Typical Characteristics**



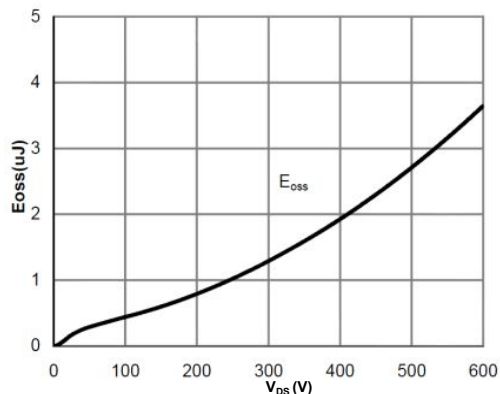
**Figure 7: Body-Diode Characteristics**



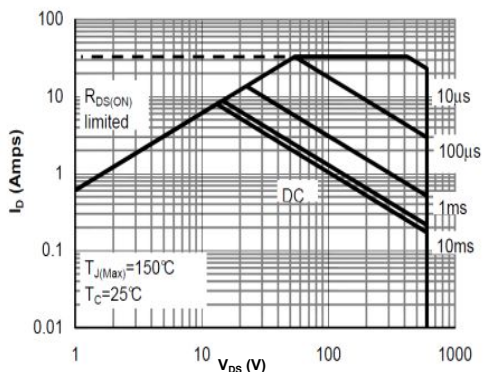
**Figure 8: Gate-Charge Characteristics**



**Figure 9: Capacitance Characteristics**



**Figure 10: C<sub>oss</sub> stored Energy**



**Figure 11: Maximum Forward Biased Safe Operating Area**

Typical Characteristics

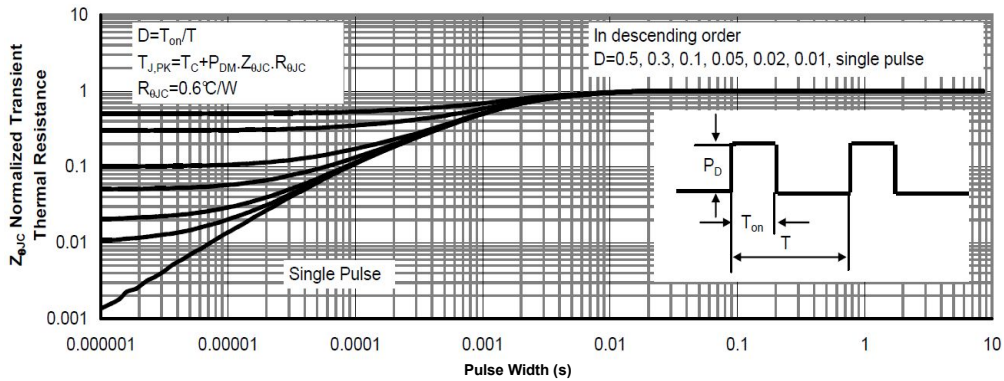


Figure 12: Normalized Maximum Transient Thermal Impedance

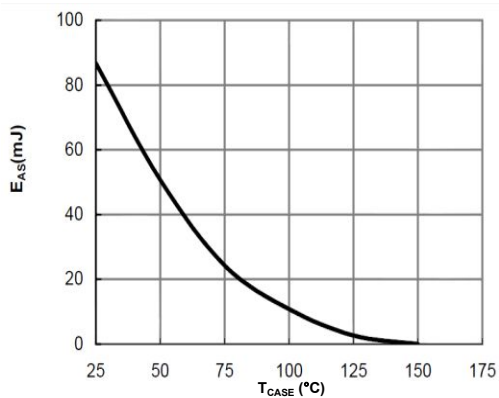


Figure 13: Avalanche energy

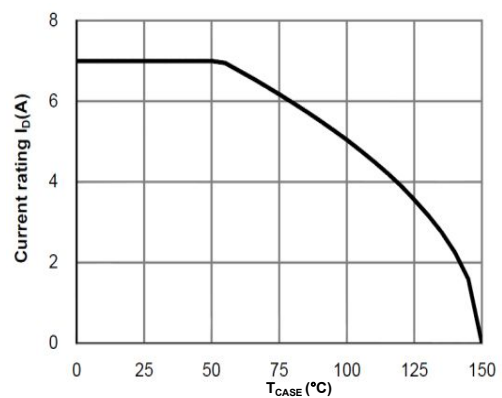


Figure 14: Current De-rating

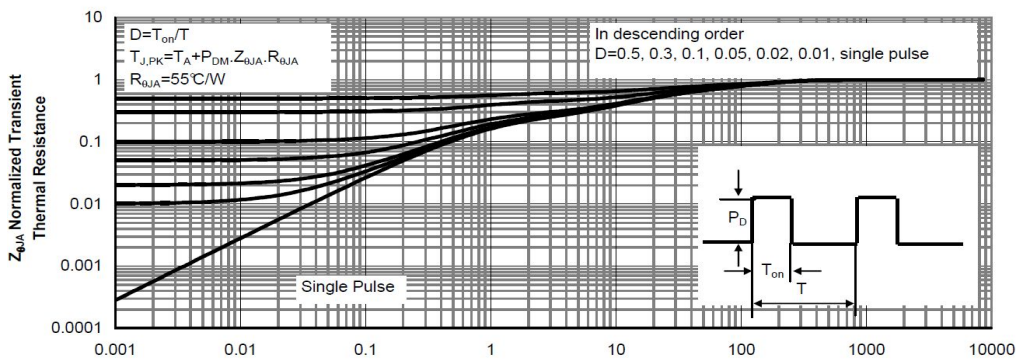
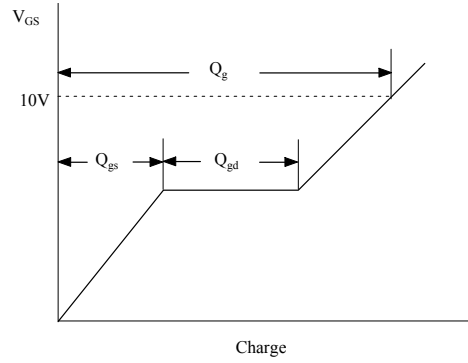
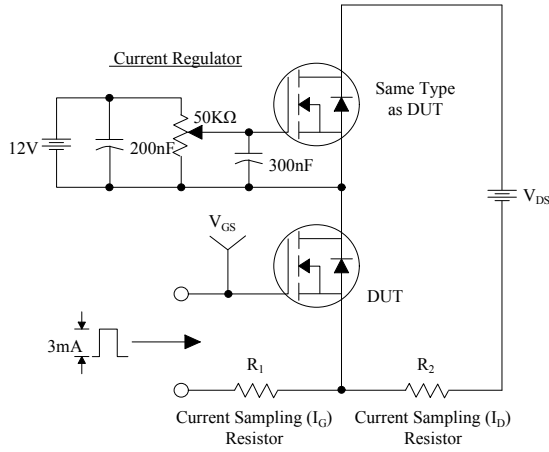
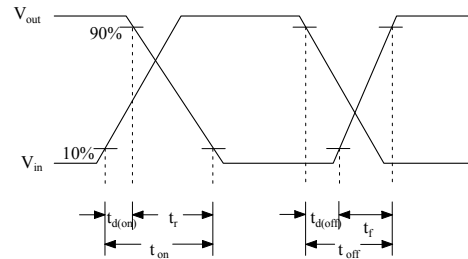
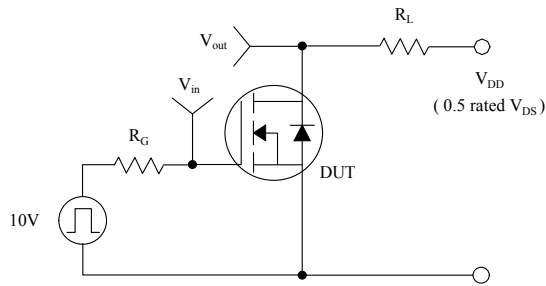


Figure 15: Normalized Maximum Transient Thermal Impedance

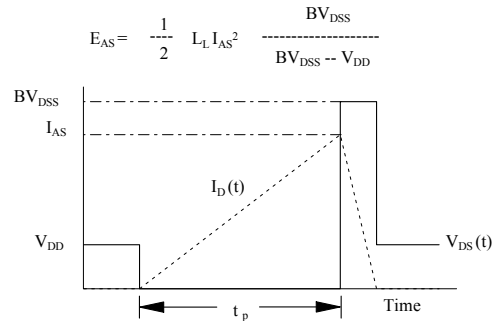
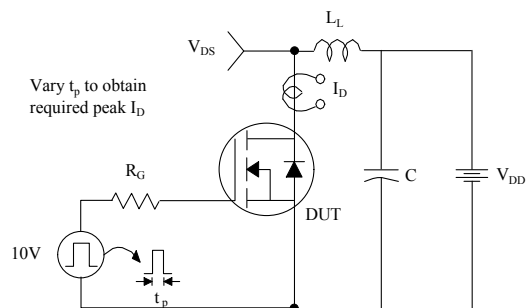
### Gate Charge Test Circuit & Waveform



### Resistive Switching Test Circuit & Waveforms



### Unclamped Inductive Switching Test Circuit & Waveforms



### Peak Diode Recovery dv/dt Test Circuit & Waveforms

