



CB-FET

SLP65R950SJ / SLF65R950SJ

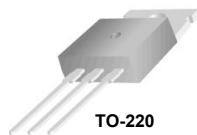
SLP65R950SJ / SLF65R950SJ 650V N-Channel MOSFET

General Description

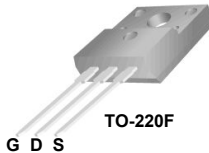
This Power MOSFET is produced using Maple semi's Advanced Super-Junction technology. This advanced technology has been especially tailored to minimize conduction loss, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for AC/DC power conversion in switching mode operation for higher efficiency.

Features

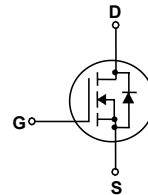
- 5A, 650V, $R_{DS(on) typ.} = 0.85\Omega @ V_{GS} = 10V$
- Low gate charge (typical 15nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



TO-220



TO-220F



Absolute Maximum Ratings

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	SLP65R950SJ	SLF65R950SJ	Units
V_{DSS}	Drain-Source Voltage	650		V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$) - Continuous ($T_C = 100^\circ\text{C}$)	5	5*	A
		4	4*	A
I_{DM}	Drain Current - Pulsed (Note 1)	16	16*	A
V_{GSS}	Gate-Source Voltage	±30		V
EAS	Single Pulsed Avalanche Energy (Note 2)	67.5		mJ
I_{AR}	Avalanche Current (Note 1)	1		A
E _{AR}	Repetitive Avalanche Energy (Note 1)	34		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5		V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$) - Derate above 25°C	205	35	W
		1.67	0.3	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		$^\circ\text{C}$

* Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	SLP65R950SJ	SLF65R950SJ	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.6	3.6	$^\circ\text{C}/\text{W}$
$R_{\theta JS}$	Thermal Resistance, Case-to-Sink Typ.	0.5	--	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62	62	$^\circ\text{C}/\text{W}$

Electrical CharacteristicsT_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 uA, T _J =25°C	650	--	--	V
		V _{GS} = 0 V, I _D = 250 uA, T _J =150°C	--	700	--	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 uA, Referenced to 25°C	--	0.6	--	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 650 V, V _{GS} = 0 V	--	--	1	uA
		V _{DS} = 480 V, T _C = 125°C	--	--	10	uA
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30 V, V _{DS} = 0 V	--	--	100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -30 V, V _{DS} = 0 V	--	--	-100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 uA	2.5	--	4.5	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 2.5 A	--	0.85	0.95	Ω
g _{FS}	Forward Transconductance	V _{DS} = 40 V, I _D = 2.5 A (Note 4)	--	8	--	S
R _g	Gate resistance	f = 1.0 MHz, Open drain	--	3.5	--	Ω
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz	--	320	--	pF
C _{oss}	Output Capacitance		--	75	--	pF
C _{rss}	Reverse Transfer Capacitance		--	4	--	pF
Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	V _{DD} = 400 V, I _D = 2.5 A, R _G = 20 Ω (Note 4, 5)	--	18	--	ns
t _r	Turn-On Rise Time		--	40	--	ns
t _{d(off)}	Turn-Off Delay Time		--	50	--	ns
t _f	Turn-Off Fall Time		--	30	--	ns
Q _g	Total Gate Charge	V _{DS} = 480 V, I _D = 5 A, V _{GS} = 10 V (Note 4, 5)	--	15	--	nC
Q _{gs}	Gate-Source Charge		--	3	--	nC
Q _{gd}	Gate-Drain Charge		--	6	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	5	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	16	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 5 A	--	--	1.5	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 5 A,	--	180	--	ns
Q _{rr}	Reverse Recovery Charge	dI _F / dt = 100 A/us (Note 4)	--	2.5	--	uC

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L=60mH, I_{AS}=1.5A, V_{DD}=150V, Starting T_J=25°C
3. I_{SD}≤4.5A, di/dt ≤ 200A/us, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test: Pulse width ≤ 300us, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

SLP65R950SJ / SLF65R950SJ

Typical Characteristics

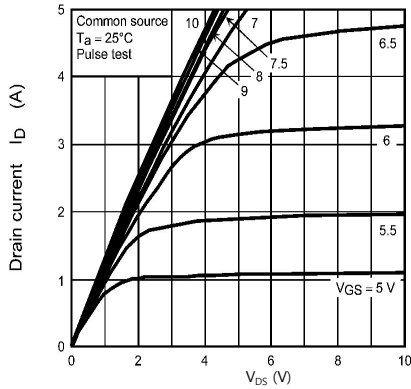


Figure 1: On-Region Characteristics@25°C

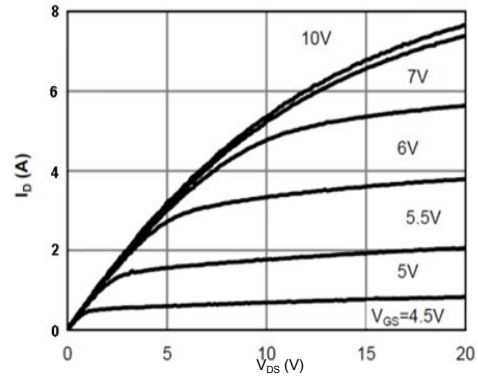


Figure 2: On-Region Characteristics@125°C

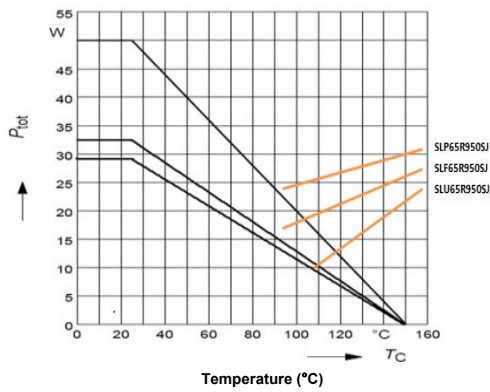


Figure 3: Power Dissipation

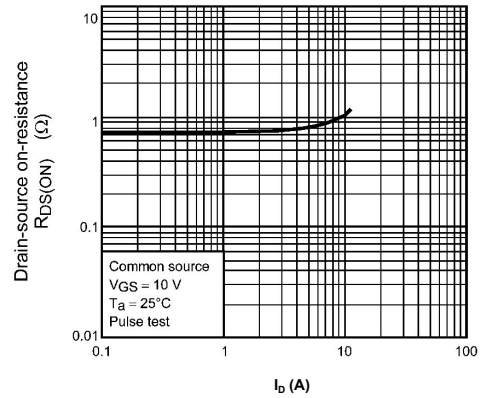


Figure 4: On-Resistance vs. Drain Current and Gate Voltage

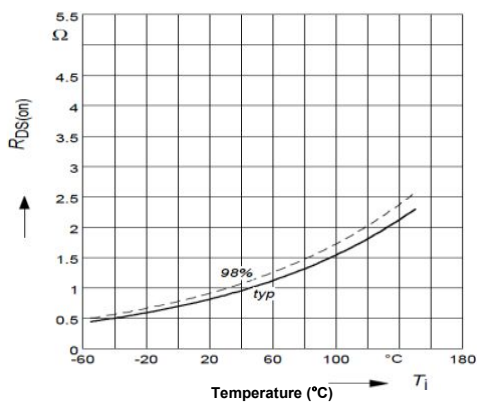


Figure 5: On-Resistance vs. Junction Temperature

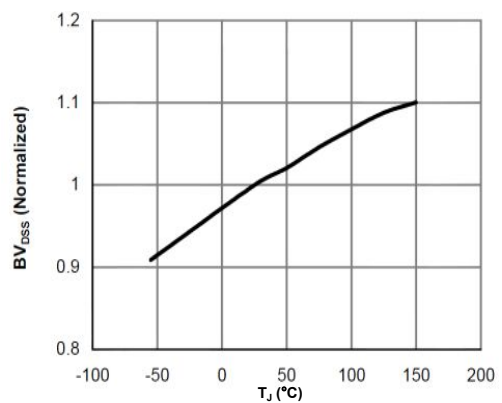


Figure 6: Break Down vs. Junction Temperature

Typical Performance Characteristics

SLP65R950SJ / SLF65R950SJ

Typical Characteristics

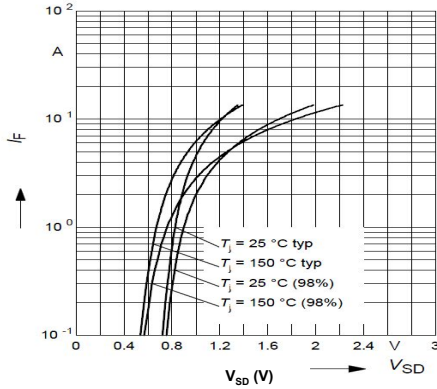


Figure 7: Body-Diode Characteristics

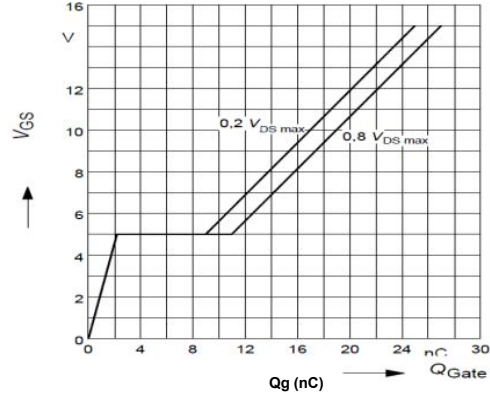


Figure 8: Gate-Charge Characteristics

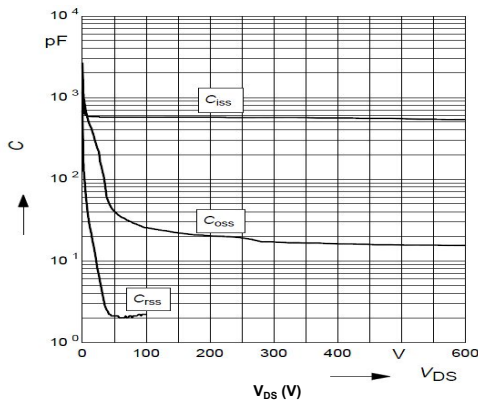


Figure 9: Capacitance Characteristics

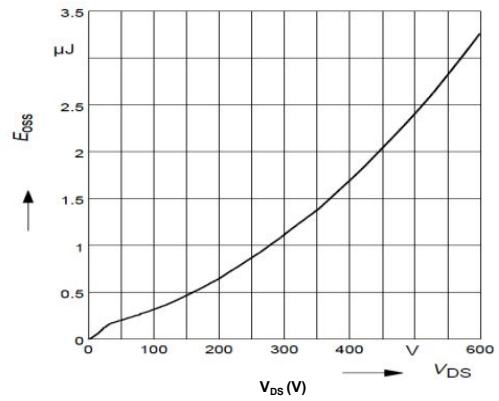


Figure 10: C_{oss} stored Energy

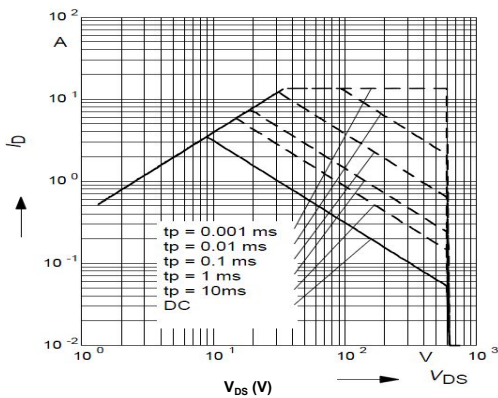


Figure 11: Maximum Forward Biased Safe Operating Area (FullPAK)

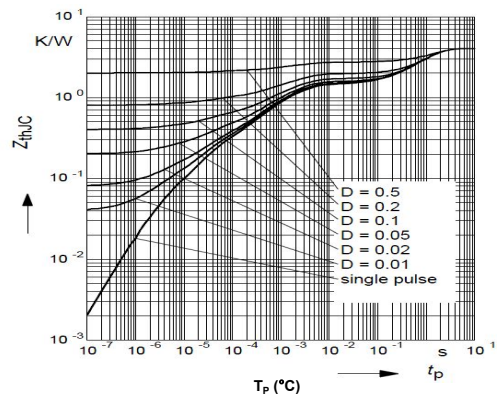


Figure 12: Sing Pulse Power Rating Junction to Case (FullPAK)

Typical Characteristics

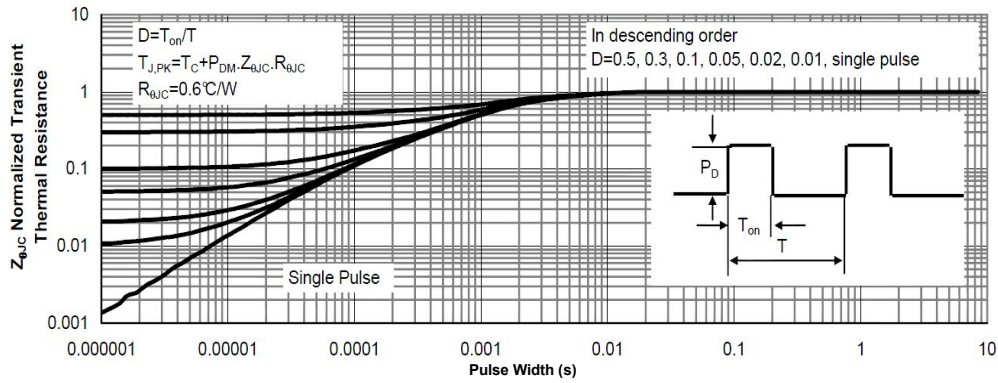


Figure 13: Normalized Maximum Transient Thermal Impedance

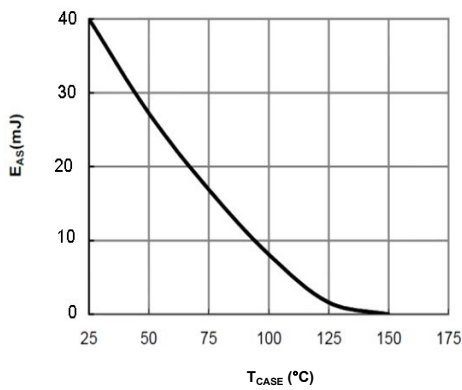


Figure 14: Avalanche energy

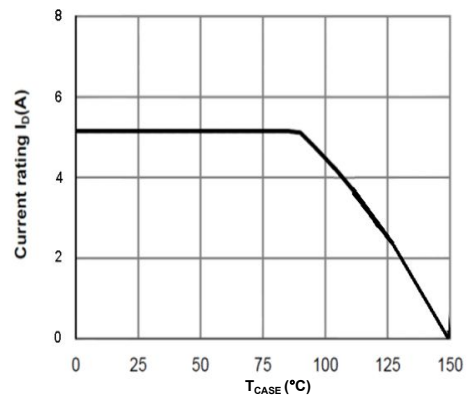


Figure 15: Current De-rating

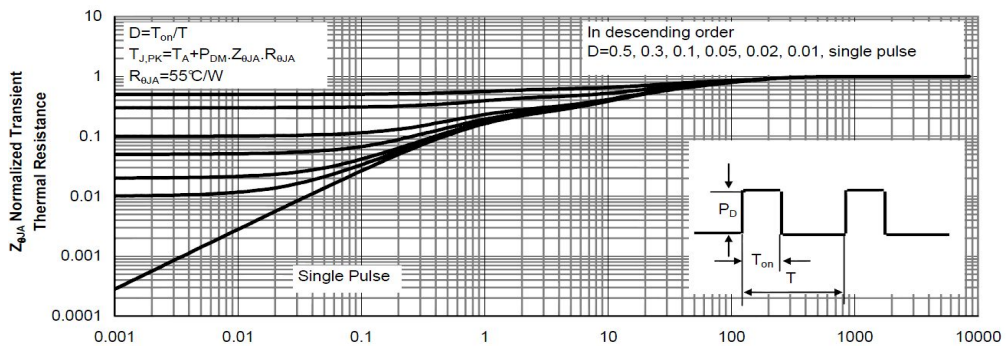
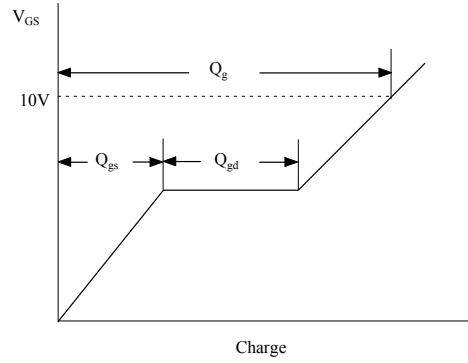
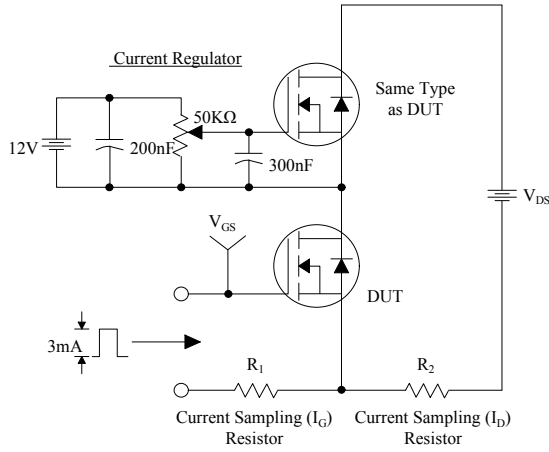
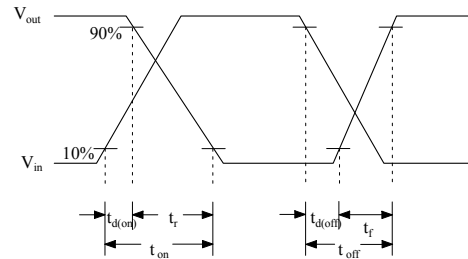
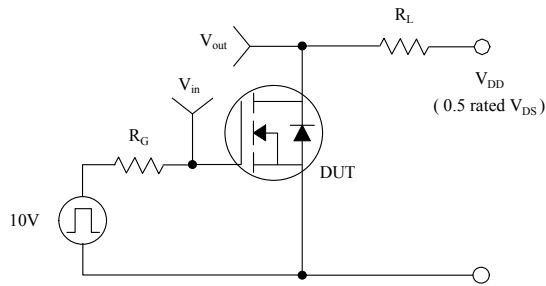


Figure 16: Normalized Maximum Transient Thermal Impedance

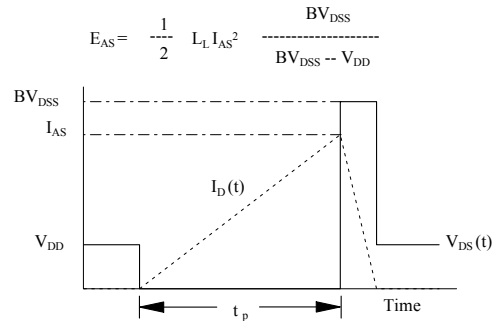
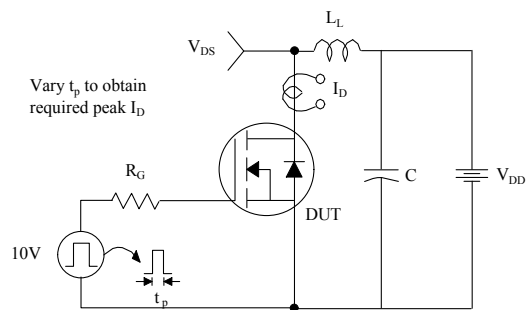
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms

