SLG3SY3952

1:3 Clock Buffer

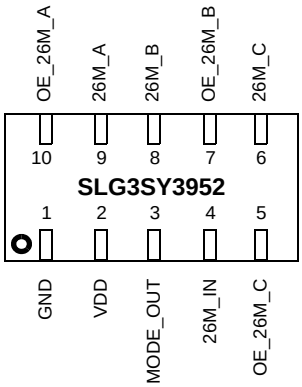
General Description

The SLG3SY3952 uses a single input 26 MHz clock source to provide three 26 MHz clock outputs.

Features

- 1.8 V VDD operation
- Current Consumption: 1.0 mA
- OE for 26M_A, 26M_B and 26M_C
- Supports Industrial temperature range
- Improved performance over temperature
- Smaller package and layout foot print
- 10-pin STDFN: 1.0 x 2.0 x 0.55 mm, 0.4 mm pitch
- Pb-Free / Halogen-Free / RoHS compliant

Pin Configuration



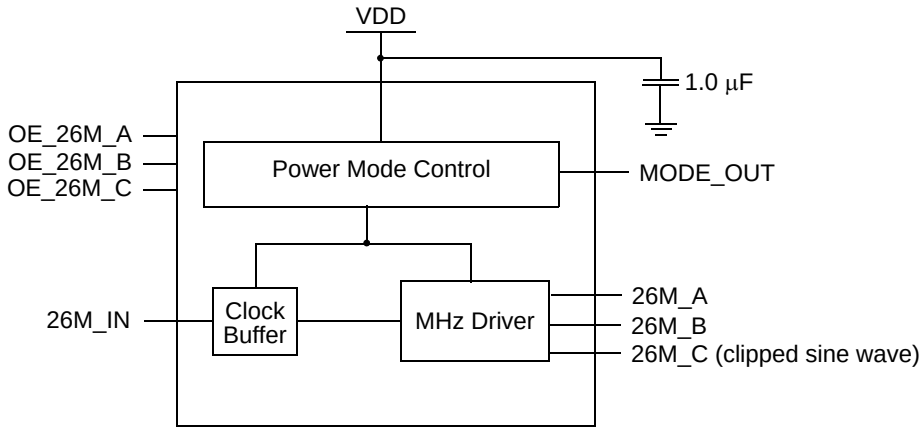
10-pin STDFN

(Top View)

Output Summary

- 3x 26 MHz clock outputs

Block Diagram



Pin Description

Pin #	Pin Name	Type[1]	Pin Description
1	GND	GND	**Ground**
2	VDD	PWR	**Power Supply:** 1.8 V as main power supply. 1.0 µF decoupling capacitor is recommended.
3	MODE_OUT	O, SE	**Mode:** 1.8 V CMOS output signal that identifies the mode SLG3SY3952 is in. May be used as clock request. PMOS Open Drain output. Requires 100 kΩ pull down resistor.
4	26M_IN	I	**Clock Input:** 26 MHz clock input.
5	OE_26M_C	I	**Output Enable:** Output enable for the 26M_C output as well as the control signal for the Power Mode switching.
6	26M_C	O, SE	**Clock Output:** 26 MHz output (Stop by OE_26M_C)
7	OE_26M_B	I	**Output Enable:** Output enable for the 26M_B output as well as the control signal for the Power Mode switching.
8	26M_B	O, SE	**Clock Output:** 26 MHz output (Stop by OE_26M_B)
9	26M_A	O, SE	**Clock Output:** 26 MHz output (Stop by OE_26M_A)
10	OE_26M_A	I	**Output Enable:** Output enable for the 26M_C output as well as the control signal for the Power Mode switching.

Notes:
1. Type Definitions
   - PWR: power
   - GND: ground
   - I: input
   - O: output
   - SE: single ended signal

CMOS Input Specifications (OE[1])

T_A = 25 °C (unless otherwise stated)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	Input Voltage HIGH		1.5	--	--	V
V_{IL}	Input Voltage LOW		--	--	0.3	V

Notes:
1. $V_{OE} < V_{DD} + 0.3$ V must be met at all times including power up, where V_{OE} is the voltage on OE pin and V_{DD} is the voltage on VDD pin.

26 MHz Clock Output Characteristics (26M)

T_A = 25 °C, V_{DD} = 1.8 V (unless otherwise stated)

Symbol	Description	Conditions	Min	Typ	Max	Unit
F_{INI}	Initial Frequency		5	--	50	MHz
DC	Duty Cycle	0.5 x V_{DD}	45	50	55	%
V_{OH}	Output Voltage HIGH	I_{OH} = 1 mA	0.8 x V_{DD}	-- [2]	--	V
V_{OL}	Output Voltage LOW	I_{OL} = -1 mA	--	-- [2]	0.2 x V_{DD}	V
t_{PU} [3,5]	Power Up Delay ($t_{PU,MHz}$)	See Note 3 & 5	--	3	5	µs
t_{OE} [4,5]	Output Enable Delay ($t_{OE,MHz}$)	See Note 4 & 5	0	1.0	2.0	µs
t_R	Rise Time	measured between $V_{OH,min}$ and $V_{OL,max}$	--	TBD	--	ns
t_F	Fall Time	measured between $V_{OH,min}$ and $V_{OL,max}$	--	TBD	--	ns
CL	Output Load Capacitance		--	8	10	pF

Notes:

1. This parameter tracks Reference Crystal characteristics.
2. V_{OH} = 1.0 x V_{DD} (typ) and V_{OL} = 0 V (typ) when driving a fully capacitive load, i.e. I_{OH} = I_{OL} = 0 mA.
3. This parameter is applicable when the device powers up into Active Mode (OE = VDD during power up) or transitions into Active Mode immediately after power up. The delay time is referenced from the point where $V_{DD} \geq V_{DD,min}$ is met to the 26 MHz output being stable and valid. If OE is left floating, t_{PU} may be longer.
4. This parameter is applicable when the device enters Active Mode from Hibernate Mode during normal operation. The delay time is referenced from the point where OE $\geq V_{IH,min}$ is met to the 26 MHz output being stable and valid.
5. Both t_{PU} and t_{OE} should be satisfied in order for the 26 MHz output to be stable and valid.

Power Supply Electrical Specifications (VDD)

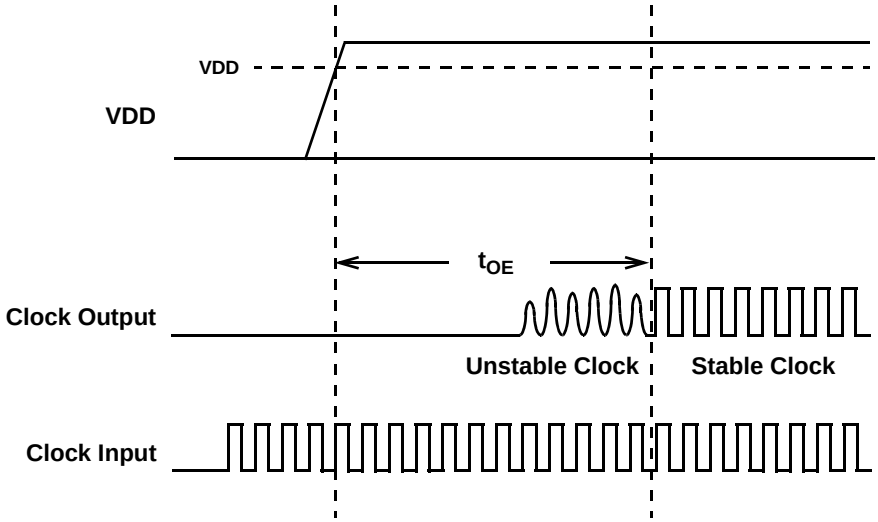
T_A = 25 °C

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DD}[1]	Operating Voltage for VDD		1.7	1.8	1.9	V
I_{VDD}[2]	V_{DD} current consumption	V_{DD} = 1.8 V	--	1.0	--	mA

Notes:
1. $V_{OE} < V_{DD} + 0.3$ V must be met at all times including power up, where V_{OE} is the voltage on OE pin and V_{DD} is the voltage on VDD pin.
2. Average current depends on application and output load. Specified values are for No Load condition.

Timing Diagrams

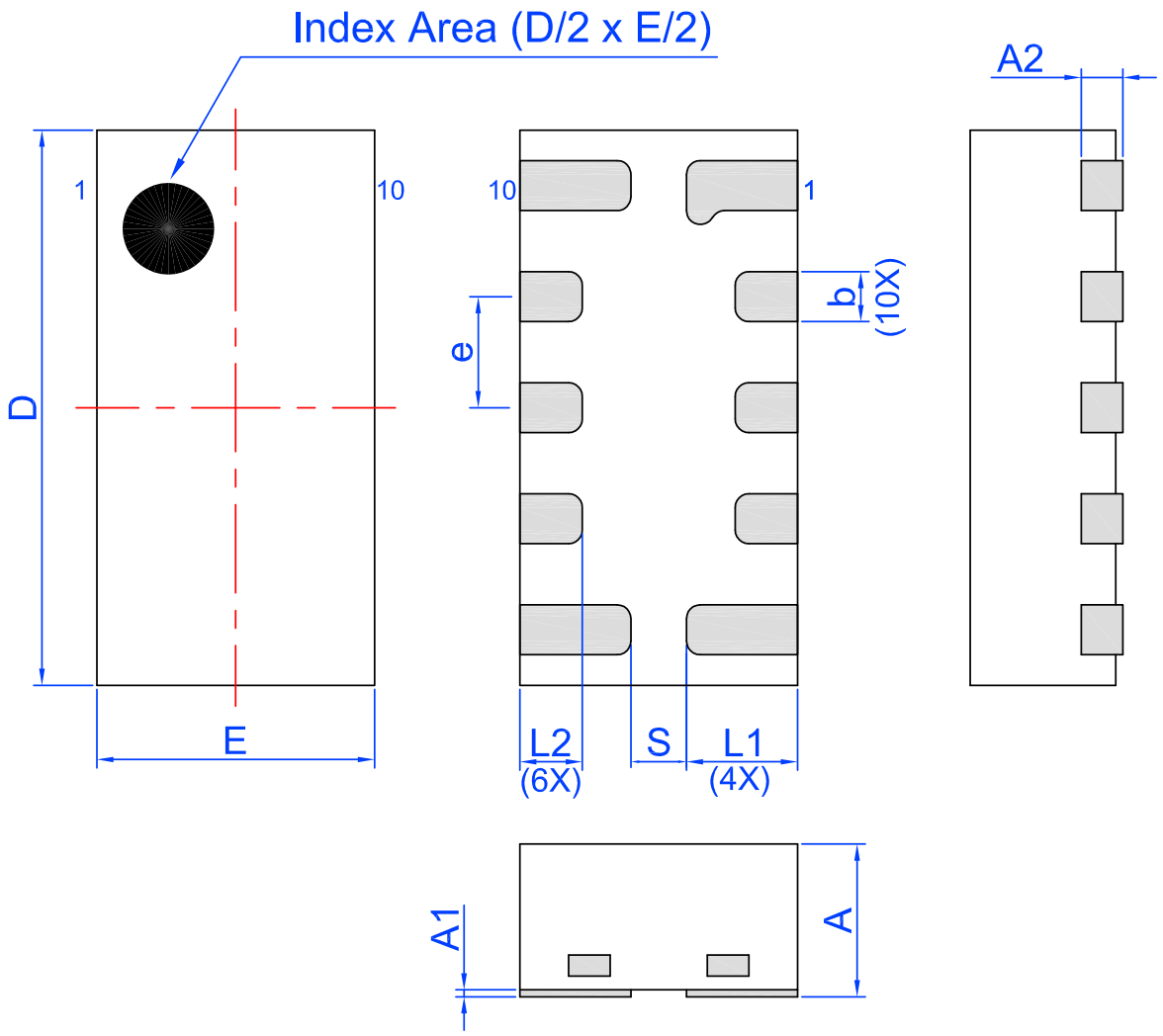
Output Enable Delay (26 MHz Output)



Package Top Marking System Definition

Package Drawing and Dimensions

10 Lead STDFN Package
JEDEC MO-252



Unit: mm

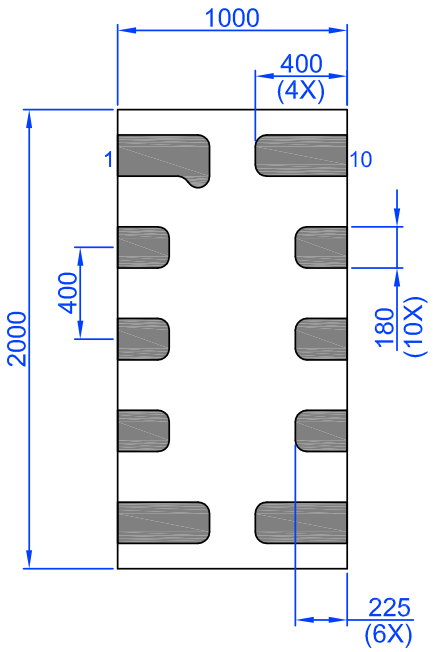
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.95	2.00	2.05
A1	0.005	-	0.060	E	0.95	1.00	1.05
A2	0.10	0.15	0.20	L1	0.35	0.40	0.45
b	0.13	0.18	0.23	L2	0.175	0.225	0.275
e	0.40 BSC			S	0.2 REF		

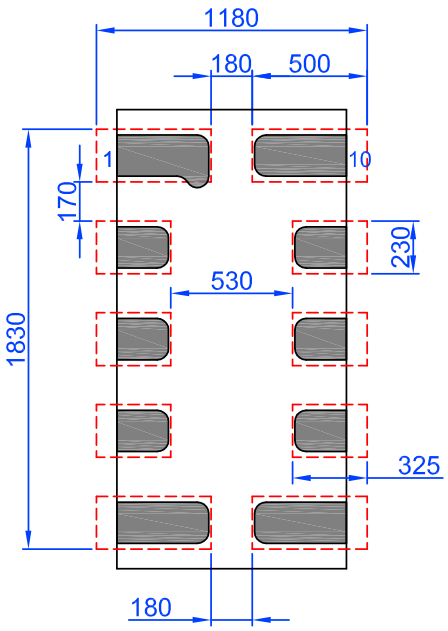
Recommended Land Pattern

Exposed Pad
(Top View)

Recommended Land Pattern
(Top View)

Units: µm





Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 1.10 mm^3 (nominal). More information can be found at www.jedec.org.

Ordering Information

Part Number	Type	Production Flow
SLG3SY3952V	10-pin STDFN	Industrial, -40 °C to 85 °C
SLG3SY3952VTR	10-pin STDFN (Tape and Reel)	Industrial, -40 °C to 85 °C

Silego Website & Support

Silego Technology Website

Silego Technology provides online support via our website at http://www.silego.com/.This website is used as a means to make files and information easily available to customers.

For more information regarding Silego Green products, please visit:

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http://greenfet.silego.com/
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Products are also available for purchase directly from Silego at the Silego Online Store at http://store.silego.com/.

Silego Technical Support

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