SLG46621

GreenPAK
Programmable Mixed-signal Matrix with Dual Supply

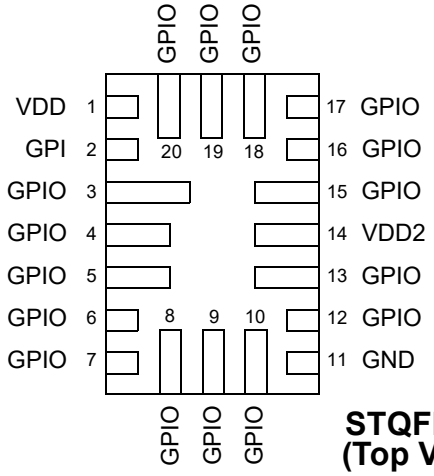
Features

- Logic & Mixed Signal Circuits
- Highly Versatile Macrocells
- Read Back Protection (Read Lock)
- 1.8 V (±5%) to 5 V (±10%) VDD
- 1.8 V (±5%) to 5 V (±10%) VDD2 (VDD2 ≤ VDD)
- Operating Temperature Range: -40°C to 85°C
- RoHS Compliant / Halogen-Free
- 20-pin STQFN: 2 x 3 x 0.55 mm, 0.4 mm pitch

Applications

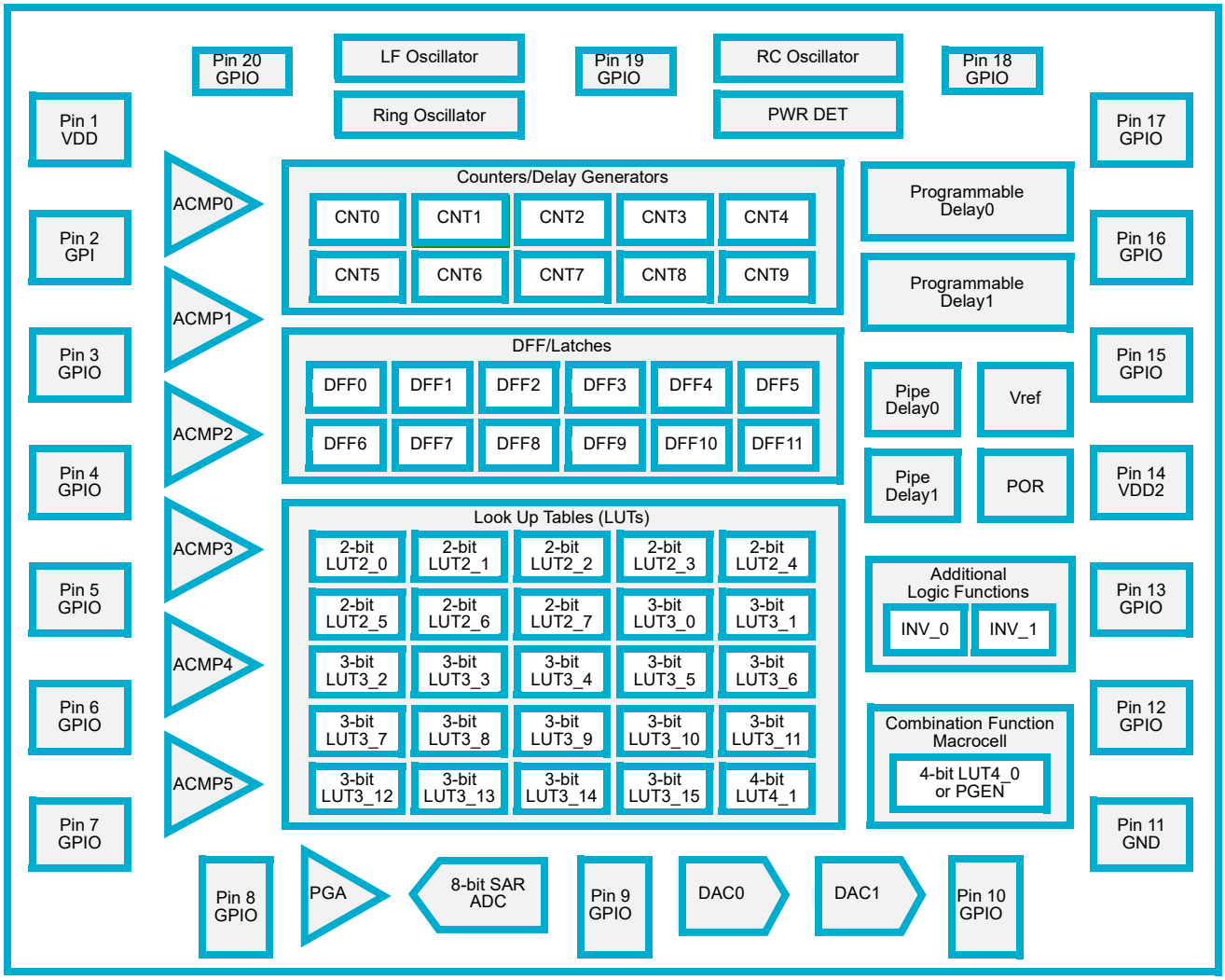
- Personal Computers and Servers
- PC Peripherals
- Consumer Electronics
- Data Communications Equipment
- Handheld and Portable Electronics

Pin Configuration



STQFN-20 (Top View)

Block Diagram



1.0 Overview

The SLG46621 provides a small, low power component for commonly used mixed-signal functions. The user creates their circuit design by programming the one time Non-Volatile Memory (NVM) to configure the interconnect logic, the I/O Pins and the macrocells of the SLG46621. This highly versatile device allows a wide variety of mixed-signal functions to be designed within a very small, low power single integrated circuit.

The additional power supply (VDD2) on the SLG46621 provides the ability to interface two independent voltage domains within the same design. Users can configure pins, dedicated to each power supply, as inputs, outputs, or both (controlled dynamically by internal logic) to both VDD and VDD2 voltage domains. Using the available macrocells designers can implement mixed-signal functions bridging both domains or simply pass through level-translation in both High to Low and Low to High directions.

The macrocells in the device include the following:

- 8-bit Successive Approximation Register Analog-to-Digital Converter (SAR ADC)
- ADC 3-bit Programmable Gain Amplifier (PGA)
- Two Digital-to-Analog Converters (DAC)
- Six Analog Comparators (ACMP)
- Two Voltage References (VREF)
- Twenty Five Combinatorial Look Up Tables (LUTs)
  - Eight 2-bit LUTs
  - Sixteen 3-bit LUTs
  - One 4-bit LUT
- One Combination Function Marcocells
  - Pattern Generator or 4-bit LUT
- Three Digital Comparators/Pulse Width Modulators (DCMPs /PWMs) w/ Selectable Deadband
- Ten Counters/Delays (CNT/DLY)
  - Two 14-bit Delay/Counter
  - One 14-bit Delay/Counter (Wake-Sleep Control)
  - One 14-bit Delay/Counter/Finite State Machine
  - Five 8-bit Delay/Counter
  - One 8-bit Delay/Counter/Finite State Machine
- Twelve D Flip-flops/Latches
- Two Pipe Delays – 16 stage/2 output
- Two Programmable Delays w/ Edge Detection
- Three Internal Oscillators
  - Low-Frequency
  - Ring
  - RC 25 kHz and 2 MHz
- Power-On-Reset (POR)
- Two Bandgaps
- Slave SPI

2.0 Pin Description

2.1 Functional Pin Description

Pin #	Pin Name	Function
1	VDD	Power Supply 1 (PIN 2, 3, 4, 5, 6, 7, 8, 9, 10 and all internal macro-cells)
2	GPI	General Purpose Input External Reset ADC CLK
3	GPIO	General Purpose I/O with OE ACMP4(+)
4	GPIO	General Purpose I/O ACMP5(+)
5	GPIO	General Purpose I/O with OE ACMP5 (-)
6	GPIO	General Purpose I/O ACMP0(+) / ACMP1(+) / ACMP2(+) / ACMP3(+) / ACMP4(+)
7	GPIO	General Purpose I/O with OE ACMP0(-) / ACMP1(-) / PGA_OUT
8	GPIO	General Purpose I/O POR_O PGA(+)
9	GPIO	General Purpose I/O with OE PGA(-)
10	GPIO	General Purpose I/O with OE ACMP0(-) / ACMP1(-) / ACMP2(-) / ACMP3(-) / ACMP4(-) Super Drive I/O
11	GND	Ground
12	GPIO	General Purpose I/O ACMP1(+) Super Drive I/O
13	GPIO	General Purpose I/O with OE ACMP2(+) / ACMP3(+)
14	VDD2	Power Supply 2 (PIN 12, 13, 15, 16, 17, 18, 19, 20)
15	GPIO	General Purpose I/O ACMP3(+) / ACMP4(+)
16	GPIO	General Purpose I/O with OE AIN MUX/CNT TESTO
17	GPIO	General Purpose I/O ADC Vref_IO
18	GPIO	General Purpose I/O with OE VrefO_2
19	GPIO	General Purpose I/O with OE VrefO_ 1
20	GPIO	General Purpose I/O

3.0 User Programmability

Non-volatile memory (NVM) is used to configure the SLG46621's connection matrix routing and macrocells. The NVM is One-Time-Programmable (OTP). However, GreenPAK development tools can be used to configure the connection matrix and macrocells, without programming the NVM, to allow on-chip emulation. This configuration will remain active on the device as long as it remains powered and can be re-written as needed to facilitate rapid design changes.

When a design is ready for in-circuit testing, the same GreenPAK development tools can be used to program the NVM and create samples for small quantity builds. Once the NVM is programmed, the device will retain this configuration for the duration of its lifetime.

Once the design is finalized, the design file can be forwarded to Renesas Electronics Corporation to integrate into the production process.

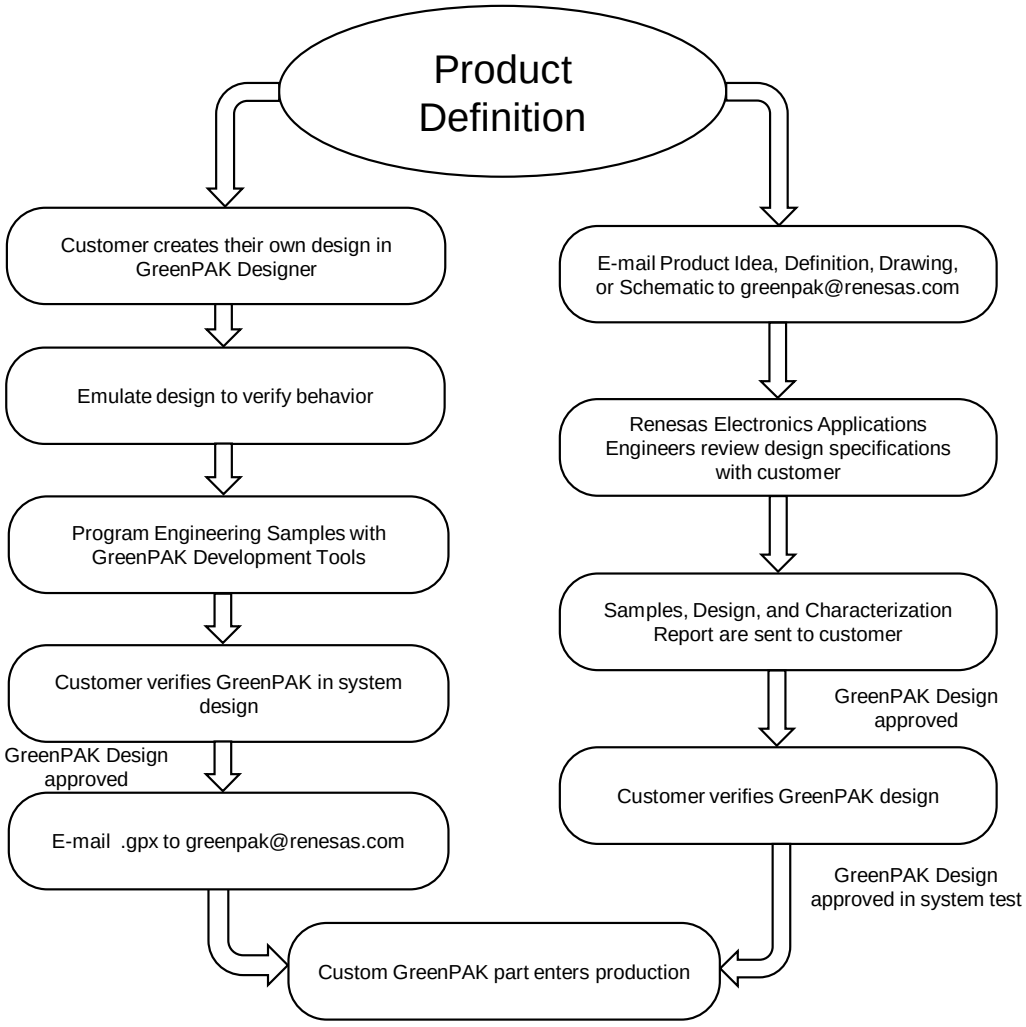


Figure 1. Steps to create a custom GreenPAK device

4.0 Ordering Information

Part Number	Type
SLG46621V	20-pin STQFN
SLG46621VTR	20-pin STQFN - Tape and Reel (3k units)

Note 1: Use SLG46621V to order. Shipments are automatically in Tape and Reel.

Note 2: "TR" suffix is no longer used. It is a legacy naming convention shown here only for informational purposes.

5.0 Electrical Specifications

5.1 Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply voltage on VDD relative to GND		-0.5	7	V
DC Input voltage		GND - 0.5	VDD + 0.5	V
PGA Input voltage*	Single-ended	--	1.98/G	V
	Differential	--	(1.98 - 0.55)/G	V
	Pseudo-differential	--	(1.98 - 0.18)/G	V
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	10	mA
	Push-Pull 2x	--	14	
	Push-Pull 4x	--	28	
	OD 1x	--	14	
	OD 2x	--	27	
	OD 4x	--	46	
Current at Input Pin		-1.0	1.0	mA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		500	--	V
Moisture Sensitivity Level		1		

*Note**: *IN+ relative to GND in Single-ended mode, IN+ and IN- relative to each other in Differential and Pseudo-differential modes..*

5.2 Electrical Characteristics (1.8V ±5% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	$V_{DD2} \leq V_{DD}$	1.71	1.80	1.89	V
I_Q	Quiescent Current	Static Inputs and Outputs, all macrocells disabled	--	0.28	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.1	V
V_{IH}	HIGH-Level Input Voltage PIN 2, 3, 4, 5, 6, 7, 8, 9, 10	Logic Input	1.087	--	V_{DD}	V
		Logic Input with Schmitt Trigger	1.296	--	V_{DD}	V
		Low-Level Logic Input	0.894	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage PIN 2, 3, 4, 5, 6, 7, 8, 9, 10	Logic Input	0	--	0.759	V
		Logic Input with Schmitt Trigger	0	--	0.562	V
		Low-Level Logic Input	0	--	0.557	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.261	0.382	0.521	V

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{LKG} (Absolute Value)	ACMP Input Leakage	Vin = 0 V	--	0.05	0.29	nA
		Vin = VDD	--	0.12	0.92	nA
	PGA Input Leakage	Vin = 0 V	--	0.03	0.13	nA
		Vin = VDD	--	0.10	0.49	nA
	Logic Input without Schmitt Trigger (Floating) Leakage	Vin = 0 V	--	0.03	0.39	nA
		Vin = VDD	--	4.02	142.92	nA
	Logic Input with Schmitt Trigger (Floating) Leakage	Vin = 0 V	--	0.03	0.24	nA
		Vin = VDD	--	4.04	143.85	nA
	Low-Level Logic Input (Floating) Leakage	Vin = 0 V	--	0.03	0.23	nA
		Vin = VDD	--	4.03	143.76	nA
V_{OH}	HIGH-Level Output Voltage PIN 2, 3, 4, 5, 6, 7, 8, 9, 10	Push-Pull 1X, Open Drain PMOS 1X, I_{OH} = 100 µA	1.680	1.788	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 100 µA	1.685	1.793	--	V
		Push-Pull 4X, Open Drain PMOS 4X, I_{OH} = 100 µA	1.697	1.799	--	V
V_{OL}	LOW-Level Output Voltage PIN 2, 3, 4, 5, 6, 7, 8, 9, 10	Push-Pull 1X, I_{OL}= 100 µA	--	0.010	0.015	V
		Push-Pull 2X, I_{OL} = 100 µA	--	0.007	0.010	V
		Push-Pull 4X, I_{OL} = 100 µA	--	0.004	0.015	V
		Open Drain NMOS 1X, I_{OL} = 100 µA	--	0.007	0.010	V
		Open Drain NMOS 2X, I_{OL} = 100 µA	--	0.003	0.010	V
		Open Drain NMOS 4X, I_{OL} = 100 µA	--	0.001	0.004	V
I_{OH}	HIGH-Level Output Pulse Current (see Note 1) PIN 2, 3, 4, 5, 6, 7, 8, 9, 10	Push-Pull 1X,Open Drain PMOS 1X, $V_{OH} = V_{DD}$ - 0.2	1.027	1.703	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, $V_{OH} = V_{DD}$ - 0.2	2.025	3.406	--	mA
		Push-Pull 4X, Open Drain PMOS 4X, $V_{OH} = V_{DD}$ - 0.2	3.916	6.759	--	mA
I_{OL}	LOW-Level Output Pulse Current (see Note 1) PIN 2, 3, 4, 5, 6, 7, 8, 9, 10	Push-Pull 1X, V_{OL} = 0.15 V	0.917	1.660	--	mA
		Push-Pull 2X, V_{OL} = 0.15 V	1.834	3.285	--	mA
		Push-Pull 4X, V_{OL} = 0.15 V	4.807	6.495	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.15 V	1.375	2.534	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.15 V	2.750	5.068	--	mA
		Open Drain NMOS 4X, V_{OL} = 0.15 V	5.500	10.136	--	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	21	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	69	mA
		T_J = 110°C	--	--	33	mA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	V_{DD}	V
T_{SU}	Startup Time (see Note 3)	from VDD rising past PON_{THR}	0.526	1.4	5.148	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	0.950	1.462	1.705	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.935	1.103	1.281	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	--	1	--	MΩ
		100 k Pull Up	--	100	--	kΩ
		10 k Pull Up	--	10	--	kΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	--	1	--	MΩ
		100 k Pull Down	--	100	--	kΩ
		10 k Pull Down	--	10	--	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7, 8, 9 and 10 are connected to one side, pins 12, 13, 15, 16, 17, 18, 19 and 20 to another.
Note 3: VDD ramp rising speed must be less than 0.6 V/µs after power on. Violating this specification may cause chip to restart.

5.3 Electrical Characteristics (3.3V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	$V_{DD2} \le V_{DD}$	3.0	3.3	3.6	V
I_Q	Quiescent Current	Static Inputs and Outputs, all macrocells disabled	--	0.37	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.2	V
V_{IH}	HIGH-Level Input Voltage PIN 2, 3, 4, 5, 6, 7, 8, 9, 10	Logic Input	1.949	--	V_{DD}	V
		Logic Input with Schmitt Trigger	2.239	--	V_{DD}	V
		Low-Level Logic Input	1.059	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage PIN 2, 3, 4, 5, 6, 7, 8, 9, 10	Logic Input	0	--	1.286	V
		Logic Input with Schmitt Trigger	0	--	1.150	V
		Low-Level Logic Input	0	--	0.686	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.326	0.469	0.599	V
I_{LKG} (Absolute Value)	ACMP Input Leakage	Vin = 0 V	--	0.063	0.34	nA
		Vin = VDD	--	0.15	1.08	nA
	PGA Input Leakage	Vin = 0 V	--	0.042	0.16	nA
		Vin = VDD	--	0.11	0.57	nA
	Logic Input without Schmitt Trigger (Floating) Leakage	Vin = 0 V	--	0.041	0.51	nA
		Vin = VDD	--	4.28	159.57	nA
	Logic Input with Schmitt Trigger (Floating) Leakage	Vin = 0 V	--	0.041	0.30	nA
		Vin = VDD	--	4.29	160.50	nA
	Low-Level Logic Input (Floating) Leakage	Vin = 0 V	--	0.041	0.29	nA
		Vin = VDD	--	4.29	160.66	nA
V_{OH}	HIGH-Level Output Voltage PIN 2, 3, 4, 5, 6, 7, 8, 9, 10	Push-Pull 1X, Open Drain PMOS 1X, I_{OH} = 3 mA	2.713	3.095	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 3 mA	2.858	3.199	--	V
		Push-Pull 4X, Open Drain PMOS 4X, I_{OH} = 3 mA	2.925	3.244	--	V
V_{OL}	LOW-Level Output Voltage PIN 2, 3, 4, 5, 6, 7, 8, 9, 10	Push-Pull 1X, I_{OL}= 3 mA	--	0.148	0.228	V
		Push-Pull 2X, I_{OL}= 3 mA	--	0.073	0.108	V
		Push-Pull 4X, I_{OL}= 3 mA	--	0.052	0.098	V
		Open Drain NMOS 1X, I_{OL}= 3 mA	--	0.080	0.147	V
		Open Drain NMOS 2X, I_{OL}= 3 mA	--	0.040	0.071	V
		Open Drain NMOS 4X, I_{OL}= 3 mA	--	0.013	0.021	V

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{OH}	HIGH-Level Output Pulse Current (see Note 1) PIN 2, 3, 4, 5, 6, 7, 8, 9, 10	Push-Pull 1X, Open Drain PMOS 1X, V_{OH} = 2.4 V	5.608	10.774	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = 2.4 V	11.015	21.100	--	mA
		Push-Pull 4X, Open Drain PMOS 4X, V_{OH} = 2.4 V	20.752	39.176	--	mA
I_{OL}	LOW-Level Output Pulse Current (see Note 1) PIN 2, 3, 4, 5, 6, 7, 8, 9, 10	Push-Pull 1X, V_{OL} = 0.4 V	4.875	7.795	--	mA
		Push-Pull 2X, V_{OL} = 0.4 V	9.750	15.243	--	mA
		Push-Pull 4X, V_{OL} = 0.4 V	20.217	29.887	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.4 V	7.313	12.370	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.4 V	14.626	24.740	--	mA
		Open Drain NMOS 4X, V_{OL} = 0.4 V	29.250	49.480	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	21	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	69	mA
		T_J = 110°C	--	--	33	mA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	V_{DD}	V
T_{SU}	Startup Time (see Note 3)	from VDD rising past PON_{THR}	0.660	1.4	3.740	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	0.953	1.462	1.707	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.935	1.103	1.281	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	--	1	--	MΩ
		100 k Pull Up	--	100	--	kΩ
		10 k Pull Up	--	10	--	kΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	--	1	--	MΩ
		100 k Pull Down	--	100	--	kΩ
		10 k Pull Down	--	10	--	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7, 8, 9 and 10 are connected to one side, pins 12, 13, 15, 16, 17, 18, 19 and 20 to another.
Note 3: VDD ramp rising speed must be less than 0.6 V/µs after power on. Violating this specification may cause chip to restart.

5.4 Electrical Characteristics (5V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	$V_{DD2} \le V_{DD}$	4.5	5.0	5.5	V
I_Q	Quiescent Current	Static Inputs and Outputs, all macrocells disabled	--	0.47	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.2	V
V_{IH}	HIGH-Level Input Voltage PIN 2, 3, 4, 5, 6, 7, 8, 9, 10	Logic Input	2.930	--	V_{DD}	V
		Logic Input with Schmitt Trigger	3.333	--	V_{DD}	V
		Low-Level Logic Input	1.157	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage PIN 2, 3, 4, 5, 6, 7, 8, 9, 10	Logic Input	0	--	1.910	V
		Logic Input with Schmitt Trigger	0	--	1.778	V
		Low-Level Logic Input	0	--	0.776	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.425	0.571	0.799	V
I_{LKG} (Absolute Value)	ACMP Input Leakage	Vin = 0 V	--	0.30	1.38	nA
		Vin = VDD	--	0.19	1.40	nA
	PGA Input Leakage	Vin = 0 V	--	0.25	0.81	nA
		Vin = VDD	--	0.15	0.75	nA
	Logic Input without Schmitt Trigger (Floating) Leakage	Vin = 0 V	--	0.27	2.11	nA
		Vin = VDD	--	4.45	172.97	nA
	Logic Input with Schmitt Trigger (Floating) Leakage	Vin = 0 V	--	0.27	1.68	nA
		Vin = VDD	--	4.42	173.37	nA
	Low-Level Logic Input (Floating) Leakage	Vin = 0 V	--	0.24	2.24	nA
		Vin = VDD	--	4.37	172.95	nA
V_{OH}	HIGH-Level Output Voltage PIN 2, 3, 4, 5, 6, 7, 8, 9, 10	Push-Pull 1X,Open Drain PMOS 1X, I_{OH} = 5 mA	4.159	4.750	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 5 mA	4.324	4.872	--	V
		Push-Pull 4X, Open Drain PMOS 4X, I_{OH} = 5 mA	4.405	4.930	--	V
V_{OL}	LOW-Level Output Voltage PIN 2, 3, 4, 5, 6, 7, 8, 9, 10	Push-Pull 1X, I_{OL}= 5 mA	--	0.189	0.270	V
		Push-Pull 2X, I_{OL}= 5 mA	--	0.098	0.131	V
		Push-Pull 4X, I_{OL}= 5 mA	--	0.068	0.131	V
		Open Drain NMOS 1X, I_{OL}= 5 mA	--	0.102	0.180	V
		Open Drain NMOS 2X, I_{OL}= 5 mA	--	0.051	0.090	V
		Open Drain NMOS 4X, I_{OL}= 5 mA	--	0.020	0.028	V

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{OH}	HIGH-Level Output Pulse Current (see Note 1) PIN 2, 3, 4, 5, 6, 7, 8, 9, 10	Push-Pull 1X, Open Drain PMOS 1X, V_{OH} = 2.4 V	20.337	30.010	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = 2.4 V	39.270	58.446	--	mA
		Push-Pull 4X, Open Drain PMOS 4X, V_{OH} = 2.4 V	74.110	109.086	--	mA
I_{OL}	LOW-Level Output Pulse Current (see Note 1) PIN 2, 3, 4, 5, 6, 7, 8, 9, 10	Push-Pull 1X, V_{OL} = 0.4 V	6.996	10.438	--	mA
		Push-Pull 2X, V_{OL} = 0.4 V	13.275	20.241	--	mA
		Push-Pull 4X, V_{OL} = 0.4 V	26.739	39.313	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.4 V	10.820	17.380	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.4 V	21.640	34.760	--	mA
		Open Drain NMOS 4X, V_{OL} = 0.4 V	43.290	69.520	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	21	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	69	mA
		T_J = 110°C	--	--	33	mA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	V_{DD}	V
T_{SU}	Startup Time (see Note 3)	from VDD rising past PON_{THR}	0.638	1.4	2.914	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	0.959	1.462	1.708	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.935	1.103	1.281	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	--	1	--	MΩ
		100 k Pull Up	--	100	--	kΩ
		10 k Pull Up	--	10	--	kΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	--	1	--	MΩ
		100 k Pull Down	--	100	--	kΩ
		10 k Pull Down	--	10	--	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7, 8, 9 and 10 are connected to one side, pins 12, 13, 15, 16, 17, 18, 19 and 20 to another.
Note 3: VDD ramp rising speed must be less than 0.6 V/µs after power on. Violating this specification may cause chip to restart.

5.5 Electrical Characteristics (1.8V ±5% V_{DD2})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD2}	Supply Voltage	$V_{DD2} \le V_{DD}$	1.71	1.80	1.89	V
V_{IH2}	HIGH-Level Input Voltage PIN 12, 13, 15, 16, 17, 18, 19, 20	Logic Input	1.087	--	V_{DD2}	V
		Logic Input with Schmitt Trigger	1.296	--	V_{DD2}	V
		Low-Level Logic Input	0.894	--	V_{DD2}	V
V_{IL2}	LOW-Level Input Voltage PIN 12, 13, 15, 16, 17, 18, 19, 20	Logic Input	0	--	0.759	V
		Logic Input with Schmitt Trigger	0	--	0.562	V
		Low-Level Logic Input	0	--	0.557	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.261	0.382	0.521	V
I_{LKG} (Absolute Value)	ACMP Input Leakage	Vin = 0 V	--	47.79	286.14	pA
		Vin = VDD	--	0.12	0.92	nA
	PGA Input Leakage	Vin = 0 V	--	34.17	128.81	pA
		Vin = VDD	--	0.10	0.49	nA
	Logic Input without Schmitt Trigger (Floating) Leakage	Vin = 0 V	--	31.45	385.30	pA
		Vin = VDD	--	4.02	142.92	nA
	Logic Input with Schmitt Trigger (Floating) Leakage	Vin = 0 V	--	31.33	239.88	pA
		Vin = VDD	--	4.04	143.85	nA
	Low-Level Logic Input (Floating) Leakage	Vin = 0 V	--	31.26	230.67	pA
		Vin = VDD	--	4.03	143.76	nA
V_{OH2}	HIGH-Level Output Voltage PIN 12, 13, 15, 16, 17, 18, 19, 20	Push-Pull 1X, Open Drain PMOS 1X, I_{OH2} = 100 µA	1.680	1.788	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH2} = 100 µA	1.685	1.793	--	V
		Push-Pull 4X, Open Drain PMOS 4X, I_{OH2} = 100 µA	1.697	1.799	--	V
V_{OL2}	LOW-Level Output Voltage PIN 12, 13, 15, 16, 17, 18, 19, 20	Push-Pull 1X, I_{OL2}= 100 µA	--	0.010	0.015	V
		Push-Pull 2X, I_{OL2} = 100 µA	--	0.007	0.010	V
		Push-Pull 4X, I_{OL2} = 100 µA	--	0.004	0.015	V
		Open Drain NMOS 1X, I_{OL2} = 100 µA	--	0.007	0.010	V
		Open Drain NMOS 2X, I_{OL2}= 100 µA	--	0.003	0.010	V
		Open Drain NMOS 4X, I_{OL2} = 100 µA	--	0.001	0.004	V
I_{OH2}	HIGH-Level Output Pulse Current (see Note 1) PIN 12, 13, 15, 16, 17, 18, 19, 20	Push-Pull 1X,Open Drain PMOS 1X, $V_{OH2} = V_{DD2} - 0.2$	1.027	1.703	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, $V_{OH2} = V_{DD2} - 0.2$	2.025	3.406	--	mA
		Push-Pull 4X, Open Drain PMOS 4X, $V_{OH2} = V_{DD2} - 0.2$	3.916	6.759	--	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{OL2}	LOW-Level Output Pulse Current (see Note 1) PIN 12, 13, 15, 16, 17, 18, 19, 20	Push-Pull 1X, V_{OL2} = 0.15 V	0.917	1.660	--	mA
		Push-Pull 2X, V_{OL2} = 0.15 V	1.834	3.285	--	mA
		Push-Pull 4X, V_{OL2} = 0.15 V	4.807	6.495	--	mA
		Open Drain NMOS 1X, V_{OL2} = 0.15 V	1.375	2.534	--	mA
		Open Drain NMOS 2X, V_{OL2} = 0.15 V	2.750	5.068	--	mA
		Open Drain NMOS 4X, V_{OL2} = 0.15 V	5.500	10.136	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	21	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	69	mA
		T_J = 110°C	--	--	33	mA

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7, 8, 9 and 10 are connected to one side, pins 12, 13, 15, 16, 17, 18, 19 and 20 to another.

5.6 Electrical Characteristics (3.3V ±10% V_{DD2})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD2}	Supply Voltage	$V_{DD2} \le V_{DD}$	3.0	3.3	3.6	V
V_{IH2}	HIGH-Level Input Voltage PIN 12, 13, 15, 16, 17, 18, 19, 20	Logic Input	1.949	--	V_{DD2}	V
		Logic Input with Schmitt Trigger	2.239	--	V_{DD2}	V
		Low-Level Logic Input	1.059	--	V_{DD2}	V
V_{IL2}	LOW-Level Input Voltage PIN 12, 13, 15, 16, 17, 18, 19, 20	Logic Input	0	--	1.286	V
		Logic Input with Schmitt Trigger	0	--	1.150	V
		Low-Level Logic Input	0	--	0.686	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.326	0.469	0.599	V
I_{LKG} (Absolute Value)	ACMP Input Leakage	Vin = 0 V	--	62.98	343.94	pA
		Vin = VDD	--	0.15	1.08	nA
	PGA Input Leakage	Vin = 0 V	--	42.50	158.19	pA
		Vin = VDD	--	0.11	0.57	nA
	Logic Input without Schmitt Trigger (Floating) Leakage	Vin = 0 V	--	41.45	509.81	pA
		Vin = VDD	--	4.28	159.57	nA
	Logic Input with Schmitt Trigger (Floating) Leakage	Vin = 0 V	--	40.62	294.96	pA
		Vin = VDD	--	4.29	160.50	nA
	Low-Level Logic Input (Floating) Leakage	Vin = 0 V	--	40.51	287.69	pA
		Vin = VDD	--	4.29	160.66	nA
V_{OH2}	HIGH-Level Output Voltage PIN 12, 13, 15, 16, 17, 18, 19, 20	Push-Pull 1X, Open Drain PMOS 1X, I_{OH2} = 3 mA	2.713	3.095	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH2} = 3 mA	2.858	3.199	--	V
		Push-Pull 4X, Open Drain PMOS 4X, I_{OH2} = 3 mA	2.925	3.244	--	V
V_{OL2}	LOW-Level Output Voltage PIN 12, 13, 15, 16, 17, 18, 19, 20	Push-Pull 1X, I_{OL2}= 3 mA	--	0.148	0.228	V
		Push-Pull 2X, I_{OL2}= 3 mA	--	0.073	0.108	V
		Push-Pull 4X, I_{OL2}= 3 mA	--	0.052	0.098	V
		Open Drain NMOS 1X, I_{OL2}= 3 mA	--	0.080	0.147	V
		Open Drain NMOS 2X, I_{OL2}= 3 mA	--	0.040	0.071	V
		Open Drain NMOS 4X, I_{OL2}= 3 mA	--	0.013	0.021	V
I_{OH2}	HIGH-Level Output Pulse Current (see Note 1) PIN 12, 13, 15, 16, 17, 18, 19, 20	Push-Pull 1X, Open Drain PMOS 1X, V_{OH2} = 2.4 V	5.608	10.774	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH2} = 2.4 V	11.015	21.100	--	mA
		Push-Pull 4X, Open Drain PMOS 4X, V_{OH2} = 2.4 V	20.752	39.176	--	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{OL2}	LOW-Level Output Pulse Current (see Note 1) PIN 12, 13, 15, 16, 17, 18, 19, 20	Push-Pull 1X, V_{OL2} = 0.4 V	4.875	7.795	--	mA
		Push-Pull 2X, V_{OL2} = 0.4 V	9.750	15.243	--	mA
		Push-Pull 4X, V_{OL2} = 0.4 V	20.217	29.887	--	mA
		Open Drain NMOS 1X, V_{OL2} = 0.4 V	7.313	12.370	--	mA
		Open Drain NMOS 2X, V_{OL2} = 0.4 V	14.626	24.740	--	mA
		Open Drain NMOS 4X, V_{OL2} = 0.4 V	29.250	49.480	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	21	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	69	mA
		T_J = 110°C	--	--	33	mA

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7, 8, 9 and 10 are connected to one side, pins 12, 13, 15, 16, 17, 18, 19 and 20 to another.

5.7 Electrical Characteristics (5V ±10% V_{DD2})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD2}	Supply Voltage	$V_{DD2} \le V_{DD}$	4.5	5.0	5.5	V
V_{IH2}	HIGH-Level Input Voltage PIN 12, 13, 15, 16, 17, 18, 19, 20	Logic Input	2.930	--	V_{DD2}	V
		Logic Input with Schmitt Trigger	3.333	--	V_{DD2}	V
		Low-Level Logic Input	1.157	--	V_{DD2}	V
V_{IL2}	LOW-Level Input Voltage PIN 12, 13, 15, 16, 17, 18, 19, 20	Logic Input	0	--	1.910	V
		Logic Input with Schmitt Trigger	0	--	1.778	V
		Low-Level Logic Input	0	--	0.776	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.425	0.571	0.799	V
I_{LKG} (Absolute Value)	ACMP Input Leakage	Vin = 0 V	--	302.45	1383.46	pA
		Vin = VDD	--	0.19	1.40	nA
	PGA Input Leakage	Vin = 0 V	--	246.01	805.84	pA
		Vin = VDD	--	0.15	0.75	nA
	Logic Input without Schmitt Trigger (Floating) Leakage	Vin = 0 V	--	272.51	2110.68	pA
		Vin = VDD	--	4.45	172.97	nA
	Logic Input with Schmitt Trigger (Floating) Leakage	Vin = 0 V	--	268.42	1683.19	pA
		Vin = VDD	--	4.42	173.37	nA
	Low-Level Logic Input (Floating) Leakage	Vin = 0 V	--	240.63	2238.70	pA
		Vin = VDD	--	4.37	172.95	nA
V_{OH2}	HIGH-Level Output Voltage PIN 12, 13, 15, 16, 17, 18, 19, 20	Push-Pull 1X,Open Drain PMOS 1X, I_{OH} = 5 mA	4.159	4.750	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 5 mA	4.324	4.872	--	V
		Push-Pull 4X, Open Drain PMOS 4X, I_{OH} = 5 mA	4.405	4.930	--	V
V_{OL2}	LOW-Level Output Voltage PIN 12, 13, 15, 16, 17, 18, 19, 20	Push-Pull 1X, I_{OL2}= 5 mA	--	0.189	0.270	V
		Push-Pull 2X, I_{OL2}= 5 mA	--	0.098	0.131	V
		Push-Pull 4X, I_{OL2}= 5 mA	--	0.068	0.131	V
		Open Drain NMOS 1X, I_{OL2}= 5 mA	--	0.102	0.180	V
		Open Drain NMOS 2X, I_{OL2}= 5 mA	--	0.051	0.090	V
		Open Drain NMOS 4X, I_{OL2}= 5 mA	--	0.020	0.028	V
I_{OH2}	HIGH-Level Output Pulse Current (see Note 1) PIN 12, 13, 15, 16, 17, 18, 19, 20	Push-Pull 1X, Open Drain PMOS 1X, V_{OH2} = 2.4 V	20.337	30.010	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH2} = 2.4 V	39.270	58.446	--	mA
		Push-Pull 4X, Open Drain PMOS 4X, V_{OH2} = 2.4 V	74.110	109.086	--	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{OL2}	LOW-Level Output Pulse Current (see Note 1) PIN 12, 13, 15, 16, 17, 18, 19, 20	Push-Pull 1X, V_{OL2} = 0.4 V	6.996	10.438	--	mA
		Push-Pull 2X, V_{OL2} = 0.4 V	13.275	20.241	--	mA
		Push-Pull 4X, V_{OL2} = 0.4 V	26.739	39.313	--	mA
		Open Drain NMOS 1X, V_{OL2} = 0.4 V	10.820	17.380	--	mA
		Open Drain NMOS 2X, V_{OL2} = 0.4 V	21.640	34.760	--	mA
		Open Drain NMOS 4X, V_{OL2} = 0.4 V	43.290	69.520	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	21	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	69	mA
		T_J = 110°C	--	--	33	mA

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7, 8, 9 and 10 are connected to one side, pins 12, 13, 15, 16, 17, 18, 19 and 20 to another.

5.8 Typical Delay Estimated for Each Macrocell

Table 1. Typical Delay Estimated for Each Macrocell

Symbol	Parameter	Note	V_{DD} = 1.8 V		V_{DD} = 3.3V		V_{DD} = 5.0V		Unit
			rising	falling	rising	falling	rising	falling	
tpd	Delay	LUT 2-bit	16.79	15.32	6.37	5.92	4.35	4.18	ns
tpd	Delay	LUT 3-bit	17.89	15.93	6.81	6.22	4.64	4.40	ns
tpd	Delay	LUT 4-bit	19.44	16.86	7.43	6.61	4.98	4.61	ns
tpd	Delay	LUT 4-bit (Shared)	23.75	22.71	9.09	8.88	6.26	6.33	ns
tpd	Delay	DFF	21.56	25.33	8.95	9.12	6.39	6.21	ns
tpd	Delay	DFF nReset	--	26.05	--	10.15	--	7.33	ns
tpd	Delay	DFF nSet	--	27.25	--	10.58	--	7.64	ns
tpd	Delay	CNT/DLY opposite to selected edge delay	46.62	41.53	19.26	17.60	13.17	12.82	ns
tpd	Delay	CNT/DLY (Shared) opposite to selected Edge Delay	47.40	40.50	18.90	17.16	12.92	12.56	ns
tpd	Delay	CNT/DLY Both Edge Detect	51.46	52.6	21.43	21.21	14.98	15	ns
tpd	Delay	CNT/DLY Rising Edge Detect	53.82	--	22.73	--	15.91	--	ns
tpd	Delay	CNT/DLY Falling Edge Detect	--	55.71	--	22.61	--	15.97	ns
tw	Width	CNT/DLY Both Edge Detect	30.16	30.19	13.75	13.75	9.77	9.76	ns
tw	Width	CNT/DLY Rising Edge Detect	30.79	--	13.91	--	9.78	--	ns
tw	Width	CNT/DLY Falling Edge Detect	--	29.32	--	13.55	--	9.55	ns
tpd	Delay	Latch	20.47	22.27	8.48	8.50	5.98	6.21	ns
tpd	Delay	Latch nReset	--	27.95	--	10.98	--	7.96	ns
tpd	Delay	Latch nSet	--	24.86	--	9.60	--	6.96	ns
tpd	Delay	Pipe Delay	32.75	33.91	13.46	12.85	9.51	9.03	ns
tpd	Delay	Pipe Delay nReset	--	35.04	--	14.76	--	11.12	ns
tpd	Delay	PGEN (Shared)	21.94	23.54	8.58	8.94	5.97	6.28	ns
tpd	Delay	PGEN (Shared) nReset to 0	--	23.46	--	8.84	--	6.24	ns
tpd	Delay	PGEN (Shared) nReset to 1	21.70	--	8.46	--	5.95	--	ns
tpd	Delay	PDLY0 1 Cells Both Edge Delay	373.01	374.69	165.49	166.405	120.49	122.21	ns
tpd	Delay	PDLY0 1 Cells Both Edge Detect	29.52	31.79	11.93	12.055	8.26	8.675	ns
tpd	Delay	PDLY0 1 Cells delayed output Both Edge Detect	189.96	192.09	75.25	76.385	48.42	48.735	ns
tpd	Delay	PDLY0 1 Cells delayed output Rising Edge Detect	190.51	--	75.49	--	48.47	--	ns
tpd	Delay	PDLY0 1 Cells delayed output Falling Edge Detect	--	192.49	--	75.955	--	48.75	ns
tpd	Delay	PDLY0 1 Cells Rising Edge Detect	30.12	--	12.27	--	8.48	--	ns
tpd	Delay	PDLY0 1 Cells Falling Edge Detect	--	32.03	--	12.195	--	8.755	ns
tpd	Delay	PDLY0 2 Cells Both Edge Delay	711.16	712.99	317.04	318.305	231.71	233.4	ns
tpd	Delay	PDLY0 2 Cells Both Edge Detect	29.44	31.79	12	12.095	8.24	8.655	ns
tpd	Delay	PDLY0 2 Cells delayed output Both Edge Detect	344.86	346.84	137.37	137.745	87.34	88.14	ns
tpd	Delay	PDLY0 2 Cells delayed output Rising Edge Detect	345.71	--	137.49	--	87.51	--	ns

Table 1. Typical Delay Estimated for Each Macrocell

Symbol	Parameter	Note	V_{DD} = 1.8 V		V_{DD} = 3.3V		V_{DD} = 5.0V		Unit
			rising	falling	rising	falling	rising	falling	
tpd	Delay	PDLY0 2 Cells delayed output Falling Edge Detect	--	347.14	--	137.505	--	88.15	ns
tpd	Delay	PDLY0 2 Cells Rising Edge Detect	30	--	12.29	--	8.51	--	ns
tpd	Delay	PDLY0 2 Cells Falling Edge Detect	--	32.05	--	12.205	--	8.75	ns
tpd	Delay	PDLY0 3 Cells Both Edge Delay	1050.51	1052.99	468.94	470.605	342.81	344.6	ns
tpd	Delay	PDLY0 3 Cells Both Edge Detect	29.46	31.77	11.97	12.095	8.24	8.655	ns
tpd	Delay	PDLY0 3 Cells delayed output Both Edge Detect	502.51	504.39	199.64	200.405	126.61	126.99	ns
tpd	Delay	PDLY0 3 Cells delayed output Rising Edge Detect	503.36	--	199.74	--	126.96	--	ns
tpd	Delay	PDLY0 3 Cells delayed output Falling Edge Detect	--	504.74	--	200.405	--	126.95	ns
tpd	Delay	PDLY0 3 Cells Rising Edge Detect	30.15	--	12.29	--	8.56	--	ns
tpd	Delay	PDLY0 3 Cells Falling Edge Detect	--	32.01	--	12.165	--	8.74	ns
tpd	Delay	PDLY0 4 Cells Both Edge Delay	1390.01	1391.99	620.74	622.155	453.91	455.35	ns
tpd	Delay	PDLY0 4 Cells Both Edge Detect	29.42	31.77	12.02	12.085	8.25	8.65	ns
tpd	Delay	PDLY0 4 Cells delayed output Both Edge Detect	656.81	658.84	261.39	261.655	165.71	166.15	ns
tpd	Delay	PDLY0 4 Cells delayed output Rising Edge Detect	657.56	--	261.74	--	166.01	--	ns
tpd	Delay	PDLY0 4 Cells delayed output Falling Edge Detect	--	659.29	--	261.855	--	166.25	ns
tpd	Delay	PDLY0 4 Cells Rising Edge Detect	30.18	--	12.27	--	8.47	--	ns
tpd	Delay	PDLY0 4 Cells Falling Edge Detect	--	32.03	--	12.215	--	8.77	ns
tw	Width	PDLY0 1 Cells Both Edge Detect Rising pulse	339.9	341.15	153.7	76.85	112.66	113.2	ns
tw	Width	PDLY0 1 Cells delayed output Both Edge Detect Rising pulse	338.35	339.55	152.45	76.225	111.48	112.14	ns
tw	Width	PDLY0 1 Cells delayed output Rising Edge Detect Rising pulse	338.2	--	152.7	--	111.6	--	ns
tw	Width	PDLY0 1 Cells delayed output Falling Edge Detect Falling pulse	--	339.60	--	76.35	--	112.34	ns
tw	Width	PDLY0 1 Cells Rising Edge Detect Rising pulse	340.2	--	153.7	--	112.66	--	ns
tw	Width	PDLY0 1Cells Falling Edge Detect Falling pulse	--	341.00	--	76.85	--	113.08	ns
tw	Width	PDLY0 2 Cells Both Edge Detect Rising pulse	678.3	679.50	305.3	152.65	223.9	224.6	ns
tw	Width	PDLY0 2 Cells delayed output Both Edge Detect Rising pulse	682.1	683.75	302.65	151.325	220.85	221.2	ns
tw	Width	PDLY0 2 Cells delayed output Rising Edge Detect Rising pulse	682.25	--	302.8	--	220.8	--	ns

Table 1. Typical Delay Estimated for Each Macrocell

Symbol	Parameter	Note	V_{DD} = 1.8 V		V_{DD} = 3.3V		V_{DD} = 5.0V		Unit
			rising	falling	rising	falling	rising	falling	
tw	Width	PDLY0 2 Cells delayed output Falling Edge Detect Falling pulse	--	683.65	--	151.4	--	221.2	ns
tw	Width	PDLY0 2 Cells Rising Edge Detect Rising pulse	678.3	--	305.35	--	224.05	--	ns
tw	Width	PDLY0 2 Cells Falling Edge Detect Falling pulse	--	679.35	--	152.675	--	224.7	ns
tw	Width	PDLY0 3 Cells Both Edge Detect Rising pulse	1017.3	1019.45	457	228.5	335.4	335.95	ns
tw	Width	PDLY0 3 Cells delayed output Both Edge Detect Rising pulse	1018.9	1021.55	452.35	226.175	332.3	333.3	ns
tw	Width	PDLY0 3 Cells delayed output Rising Edge Detect Rising pulse	1019.4	--	452.43	--	332.3	--	ns
tw	Width	PDLY0 3 Cells delayed output Falling Edge Detect Falling pulse	--	1021.30	--	226.2125	--	333.03	ns
tw	Width	PDLY0 3 Cells Rising Edge Detect Rising pulse	1017.45	--	457	--	335.45	--	ns
tw	Width	PDLY0 3 Cells Falling Edge Detect Falling pulse	--	1019.1	--	228.5	--	336	ns
tw	Width	PDLY0 4 Cells Both Edge Detect Rising pulse	1355.95	1358.5	608.75	304.375	446.5	447.1	ns
tw	Width	PDLY0 4 Cells delayed output Both Edge Detect Rising pulse	1362.55	1365.3	604.05	302.025	442.35	443.4	ns
tw	Width	PDLY0 4 Cells delayed output Rising Edge Detect Rising pulse	1362.95	--	604.1	--	442.275	--	ns
tw	Width	PDLY0 4 Cells delayed output Falling Edge Detect Falling pulse	--	1365.15	--	302.05	--	443.4	ns
tw	Width	PDLY0 4 Cells Rising Edge Detect Rising pulse	1356.15	--	609.05	--	446.6	--	ns
tw	Width	PDLY0 4 Cells Falling Edge Detect Falling pulse	--	1358.05	--	304.525	--	447.05	ns
tpd	Delay	Inverter (INV)	13.62	16.63	5.81	5.72	4.28	3.71	ns
tpd	Delay	Matrix Cross Connector	15.62	13.76	5.90	5.33	4.06	4.23	ns
tpd	Delay	Digital Input without Schmitt trigger -- NMOS	--	34.31	--	14.06	--	9.85	ns
tpd	Delay	Digital Input without Schmitt trigger -- NMOS 2x	--	32.96	--	13.43	--	9.46	ns
tpd	Delay	Digital Input without Schmitt trigger -- PMOS	45.02	--	16.15	--	10.68	--	ns
tpd	Delay	Digital Input without Schmitt trigger -- PMOS 2x	41.31	--	14.86	--	10.26	--	ns
tpd	Delay	Digital Input with Schmitt Trigger -- Push Pull	43.5	38.99	17.02	16.07	10.76	11.05	ns
tpd	Delay	Low Voltage Digital Input -- Push Pull	43.58	352.00	16.67	142.75	10.29	94.5	ns
tpd	Delay	Digital Input without Schmitt trigger -- Push Pull 1x OE	42.09	37.96	16.07	14.16	10.95	10.21	ns
tpd	Delay	Digital Input without Schmitt trigger -- Push Pull 2x OE	40.33	36.57	15.51	13.99	10.61	9.66	ns

Table 1. Typical Delay Estimated for Each Macrocell

Symbol	Parameter	Note	V_{DD} = 1.8 V		V_{DD} = 3.3V		V_{DD} = 5.0V		Unit
			rising	falling	rising	falling	rising	falling	
tpd	Delay	Digital Input without Schmitt Trigger -- Push Pull 1x	42.77	38.56	16.59	15.83	10.40	10.85	ns
tpd	Delay	Digital Input without Schmitt Trigger -- Push Pull 2x	40.19	37.08	14.91	15.07	10.21	10.55	ns

5.9 Typical Current Consumption

Table 2. Typical Current Consumption

Condition	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
Quiescent current	0.28	0.37	0.47	µA
Low frequency OSC; Clock predivider by 1	0.76	0.89	1.13	µA
Low frequency OSC; Clock predivider by 16	0.74	0.87	1.06	µA
RC OSC 25 kHz; First Clock predivider by 1	5.26	6.02	7.24	µA
RC OSC 25 kHz; First Clock predivider by 8	5.02	5.54	6.45	µA
RC OSC 2 MHz; First Clock predivider by 1	37.47	63.46	96.11	µA
RC OSC 2 MHz; First Clock predivider by 8	18.79	25.22	34.25	µA
Ring OSC; First Clock predivider by 1	90.08	118.36	165.09	µA
Ring OSC; First Clock predivider by 16	63.28	65.39	81.12	µA
ACMP with Internal Vref; Hysteresis 0 mV/25 mV; Low bandwidth Disable; Input PIN6; Buffer 1k; Gain 1x	49.72	42.35	87.13	µA
ACMP with Internal Vref; Hysteresis 0 mV; Low bandwidth Disable; Input Buffered PIN6; Buffer 1k; Gain 1x	54.85	47.85	52.36	µA
ACMP with Internal Vref; Hysteresis 0 mV; Low bandwidth Disable; Input Buffered PIN6; Buffer 5k; Gain 1x	59.91	53.3	58.06	µA
ACMP with Internal Vref; Hysteresis 0 mV; Low bandwidth Disable; Input Buffered PIN6; Buffer 20k; Gain 1x	71.31	65.54	75.34	µA
ACMP with Internal Vref; Hysteresis 0 mV; Low bandwidth Disable; Input Buffered PIN6; Buffer 50k; Gain 1x	93.00	88.94	95.01	µA
ACMP with Internal Vref; Hysteresis 0 mV; Low bandwidth Disable; Input VDD; Buffer 1k	51.41	47.49	53.34	µA
ACMP with Internal Vref; Hysteresis 0 mV/25 mV; Low bandwidth Disable; Input PIN6; Buffer 1k; Gain 1x	49.72	42.35	87.13	µA
ACMP with Internal Vref; Hysteresis 0 mV; Low bandwidth Disable; Input Buffered PIN6; Buffer 1k; Gain 1x	54.85	47.85	52.36	µA
ACMP with Internal Vref; Hysteresis 0 mV; Low bandwidth Disable; Input VDD; Buffer 1k; Gain 1x	51.53	44.23	48.39	µA
ACMP with Internal Vref; Hysteresis 0 mV/25 mV; Low bandwidth Enable; Input PIN6; Buffer 1k; Gain 1x	44.57	37.16	41.32	µA
Bandgap	38.97	31.31	35.47	µA
Bandgap + VREF0/1 output	81.93	75.28	79.42	µA
Bandgap + DAC0	50.52	43.13	47.28	µA
Bandgap + DAC1	64.92	57.86	62.01	µA
PGA; Single-end mode; Gain 0.25x; External output Disable	86.28	80.88	86.17	µA
PGA; Single-end mode; Gain 0.5x; External output Disable	86.31	80.92	86.21	µA
PGA; Single-end mode; Gain 1x	63.39	56.32	60.49	µA
PGA; Single-end mode; Gain 2x	91.84	81.25	86.55	µA
PGA; Single-end mode; Gain 4x	87.16	81.79	87.13	µA

Table 2. Typical Current Consumption

Condition	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
ADC; Single-end mode; Vref: 1.2 V; Force analog part Enable; Speed selection 100 kHz + RC OSC 25kHz; First Clock predivider by 1; Sample rate 1.56 kHz	175.97	172.4	172.78	µA
ADC; Single-end mode; Vref: 1.2 V; Force analog part Enable; Speed selection 100 kHz + RC OSC 25kHz; First Clock predivider by 16; Sample rate 97.66 Hz	176.12	172.69	177.92	µA
ADC; Single-end mode; Vref: 1.2 V; Force analog part Enable; Speed selection 100 kHz + RC OSC 2MHz; First Clock predivider by 16; Sample rate 7.81 kHz	207.59	229.92	267.06	µA
ADC; Single-end mode; Vref: 1.2 V; Force analog part Enable; Speed selection 100 kHz + RC OSC 2MHz; First Clock predivider by 1; Sample rate 125.00 kHz	214.75	247.22	297.04	µA
ADC; Single-end mode; Vref: 1.2 V; Force analog part Enable; Speed selection 100 kHz + Ring OSC; First Clock predivider by 16; Sample rate 106.45 kHz	271.72	349.02	460.02	µA
ADC; Single-end mode; Vref: 1.2 V; Force analog part Enable; Speed selection 100 kHz + Ring OSC; First Clock predivider by 1; Sample rate 1.70 MHz	306.18	431.52	868.35	µA

5.10 OSC Specifications

5.10.1 25 kHz RC Oscillator

Table 3. 25 kHz RC OSC frequency limits

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz
1.8 V ±5%	24.182	25.836	23.503	26.544	21.862	28.504
3.3 V ±10%	24.829	25.185	24.113	25.974	23.435	26.331
5 V ±10%	24.631	25.533	24.026	26.065	23.323	26.321
2.5 V - 4.5 V	24.564	25.445	24.014	26.032	23.279	26.544
1.71 V….5.5 V	22.544	27.226	21.967	27.910	20.573	29.504

Table 4. 25 kHz RC OSC frequency error (error calculated relative to nominal value)

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5%	-3.27%	3.34%	-5.99%	6.18%	-12.55%	14.01%
3.3 V ±10%	-0.68%	0.74%	-3.55%	3.90%	-6.26%	5.33%
5 V ±10%	-1.48%	2.13%	-3.90%	4.26%	-6.71%	5.29%
2.5 V - 4.5 V	-1.74%	1.78%	-3.94%	4.13%	-6.88%	6.18%
1.71 V….5.5 V	-9.82%	8.90%	-12.13%	11.64%	-17.71%	18.02%

5.10.2 2 MHz RC Oscillator

Table 5. 2 MHz RC OSC frequency limits

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz
1.8 V ±5%	1.952	2.034	1.897	2.059	1.897	2.114
3.3 V ±10%	1.963	2.034	1.878	2.060	1.878	2.106
5 V ±10%	1.966	2.121	1.872	2.132	1.872	2.157
2.5 V - 4.5 V	1.900	2.081	1.825	2.097	1.825	2.121
1.71 V….5.5 V	1.753	2.118	1.744	2.136	1.736	2.154

Table 6. 2 MHz RC OSC frequency error (error calculated relative to nominal value)

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5%	-2.40%	1.70%	-5.15%	2.95%	-5.15%	5.71%
3.3 V ±10%	-1.84%	1.69%	-6.09%	3.01%	-6.09%	5.31%
5 V ±10%	-1.68%	6.05%	-6.39%	6.58%	-6.39%	7.87%
2.5 V - 4.5 V	-4.98%	4.05%	-8.76%	4.84%	-8.76%	6.07%
1.71 V….5.5 V	-12.37%	5.89%	-12.80%	6.81%	-13.22%	7.72%

5.10.3 27 MHz Ring Oscillator

Table 7. 27 MHz Ring OSC frequency limits

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz
1.8 V ±5%	24.755	29.120	23.641	29.164	23.641	29.164
3.3 V ±10%	25.534	29.111	25.320	29.111	24.558	29.111
5 V ±10%	25.551	29.110	25.262	29.110	24.634	29.110
2.5 V - 4.5 V	25.532	29.111	25.299	29.111	24.558	29.111
1.71 V….5.5 V	24.771	29.111	23.641	29.128	23.641	29.128

Table 8. 27 MHz Ring OSC frequency error (error calculated relative to nominal value)

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5%	-8.32%	7.85%	-12.44%	8.02%	-12.44%	8.02%
3.3 V ±10%	-5.43%	7.82%	-6.22%	7.82%	-9.04%	7.82%
5 V ±10%	-5.37%	7.81%	-6.44%	7.81%	-8.76%	7.81%
2.5 V - 4.5 V	-5.44%	7.82%	-6.30%	7.82%	-9.04%	7.82%
1.71 V….5.5 V	-8.26%	7.82%	-12.44%	7.88%	-12.44%	7.88%

5.10.4 1.73 kHz LF Oscillator

Table 9. 1.73 kHz LF OSC frequency limits

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz
1.8 V ±5%	1.453	1.981	1.431	2.003	1.368	2.027
3.3 V ±10%	1.465	1.988	1.444	2.008	1.384	2.027
5 V ±10%	1.491	2.114	1.471	2.130	1.411	2.140
2.5 V - 4.5 V	1.461	2.003	1.440	2.022	1.379	2.040
1.71 V….5.5 V	1.453	2.114	1.431	2.130	1.368	2.140

Table 10. 1.73 kHz LF OSC frequency error (error calculated relative to nominal value)

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5%	-16.00%	14.53%	-17.26%	15.80%	-20.93%	17.15%
3.3 V ±10%	-15.32%	14.89%	-16.53%	16.05%	-20.03%	17.18%
5 V ±10%	-13.84%	22.19%	-14.96%	23.11%	-18.42%	23.68%
2.5 V - 4.5 V	-15.57%	15.79%	-16.76%	16.89%	-20.27%	17.95%
1.71 V….5.5 V	-16.00%	22.19%	-17.26%	23.11%	-20.93%	23.68%

5.10.5 OSC Power On delay

Table 11. Oscillators Power On delay at room temperature; RC OSC power setting: "Auto Power On", RC osc clock to matrix input: “Enable”

Power Supply Range (VDD) V	LF OSC		RC OSC 2 MHz		RC OSC 25 kHz		RING OSC	
	Typical Value, µs	Maximum Value, µs	Typical Value, ns	Maximum Value, ns	Typical Value, µs	Maximum Value, µs	Typical Value, ns	Maximum Value, ns
1.71	562.8	639.2	929.8	1100.2	41.29	43.48	179.4	238.9
1.80	561.9	638.0	898.2	1054.6	41.21	42.75	161.8	188.9
1.89	561.1	637.2	873.1	1021.5	41.09	42.33	154.0	243.5
2.50	557.1	631.1	761.4	871.5	40.58	41.32	111.5	123.3
2.70	556.0	630.8	737.7	833.7	40.50	41.18	105.0	116.0
3.00	554.6	628.4	710.1	793.9	40.39	40.94	90.0	98.6
3.30	553.0	625.7	688.7	768.5	40.33	40.92	85.0	92.6
3.60	551.4	624.1	671.9	752.6	40.30	40.87	81.3	88.4
4.20	546.6	617.4	645.9	727.3	40.25	40.90	75.9	82.3
4.50	542.5	611.8	634.8	716.3	40.20	40.86	73.9	80.2
5.00	529.2	593.7	615.4	694.8	40.12	41.07	71.2	76.9
5.50	505.4	562.8	590.5	667.4	39.90	41.43	69.1	74.3

5.11 ACMP Specifications

Table 12. ACMP Specifications

Symbol	Parameter	Description/Note	Conditions	Min.	Typ.	Max.	Unit
V_{ACMP}	ACMP Input Voltage Range	Positive Input	VDD = 1.8 V ± 5 %	0	--	V_{DD}	V
		Negative Input		0	--	1.1	V
		Positive Input	VDD = 3.3 V ± 10 %	0	--	V_{DD}	V
		Negative Input		0	--	1.2	V
		Positive Input	VDD = 5.0 V ± 10 %	0	--	V_{DD}	V
		Negative Input		0	--	1.2	V
V_{offset}	ACMP Input Offset Voltage	Low Bandwidth - Enable, Vhys = 0 mV, Gain = 1, Vref = (50..1200) mV, VDD = (1.71..5.5) V	T = 25°C	-7.4	--	6.9	mV
			T = (-40..85)°C	-11.1	--	11.7	mV
		Low Bandwidth - Disable, Vhys = 0 mV, Gain =1, Vref = (50..1200) mV, VDD = (1.71..5.5) V	T = 25°C	-6.8	--	6.1	mV
			T = (-40..85)°C	-8.0	--	6.9	mV
t_{start}	ACMP Start Time	ACMP Power On delay, Minimal required wake time for the “Wake and Sleep function”, Regulator and Charge Pump set to automatic ON/OFF	BG = 550 µs, T = 25°C VDD = (1.71..5.5) V	--	396.3	1127.0	µS
			BG = 550 µs, T = (-40..85)°C VDD = (1.71..5.5) V	--	512.4	1901.7	µS
			BG = 100 µs, T = 25°C VDD = 2.7..5.5 V	--	85.5	218.2	µS
			BG = 100 µs, T = (-40..85)°C VDD = 2.7..5.5 V	--	106.7	397.0	µS

Symbol	Parameter	Description/Note	Conditions	Min.	Typ.	Max.	Unit
V_{HYS}	Built-in Hysteresis	V_{HYS} = 25 mV $V_{IL} = V_{REF} - V_{HYS}/2$ $V_{IH} = V_{REF} + V_{HYS}/2$	LB - Enabled, T = 25°C	--	--	30.9	mV
			LB - Disabled, T = 25°C	13.2	--	32.8	mV
		V_{HYS} = 50 mV $V_{IL} = V_{REF} - V_{HYS}$ $V_{IH} = V_{REF}$	LB - Enabled, T = 25°C	43.2	--	58.3	mV
			LB - Disabled, T = 25°C	45.7	--	54.8	mV
		V_{HYS} = 200 mV $V_{IL} = V_{REF} - V_{HYS}$ V_{IH} = Vin	LB - Enabled, T = 25°C	193.6	--	209.8	mV
			LB - Disabled, T = 25°C	194.9	--	206.9	mV
		V_{HYS} = 25 mV $V_{IL} = V_{REF} - V_{HYS}/2$ $V_{IH} = V_{REF} + V_{HYS}/2$	LB - Enabled, T = (-40…+85)°C	--	--	35.5	mV
			LB - Disabled, T = (-40…+85)°C	6.2	--	33.5	mV
		V_{HYS} = 50 mV $V_{IL} = V_{REF} - V_{HYS}$ $V_{IH} = V_{REF}$	LB - Enabled, T = (-40…+85)°C	39.0	--	64.0	mV
			LB - Disabled, T = (-40…+85)°C	42.7	--	58.3	mV
		V_{HYS} = 200 mV $V_{IL} = V_{REF} - V_{HYS}$ V_{IH} = Vin	LB - Enabled, T = (-40…+85)°C	189.4	--	215.2	mV
			LB - Disabled, T = (-40…+85)°C	192.2	--	209.9	mV
R_{sin}	Series Input Resistance	Gain = 1x		--	100.0	--	MΩ
		Gain = 0.5x		--	1.0	--	MΩ
		Gain = 0.33x		--	0.8	--	MΩ
		Gain = 0.25x		--	1.0	--	MΩ
PROP	Propagation Delay, Response Time for ACMP 0 to ACMP 4	Low Bandwidth - Enable, Gain = 1, VDD = (1.71..5.5) V, Overdrive = 5 mV	Low to High, T = (-40…+85)°C	--	32.81	380.26	µS
			High to Low, T = (-40…+85)°C	--	33.81	406.54	µS
		Low Bandwidth - Disable, Gain = 1, VDD = (1.71..5.5) V, Overdrive = 5 mV	Low to High, T = (-40…+85)°C	--	1.60	4.17	µS
			High to Low, T = (-40…+85)°C	--	1.43	3.30	µS
	Propagation Delay, Response Time for ACMP 5	Low Bandwidth - Enable, Gain = 1, T = (-40…+85)°C, VDD = (1.71..5.5) V, Overdrive = 5 mV	Low to High, T = (-40…+85)°C	--	56.02	482.64	µS
			High to Low, T = (-40…+85)°C	--	56.62	510.40	µS
		Low Bandwidth - Disable, Gain = 1, VDD = (1.71..5.5) V, Overdrive = 5 mV	Low to High, T = (-40…+85)°C	--	5.85	8.66	µS
			High to Low, T = (-40…+85)°C	--	4.34	6.70	µS

Symbol	Parameter	Description/Note	Conditions	Min.	Typ.	Max.	Unit
G	Gain error (including threshold and internal Vref error), T = (-40…+85)°C	G = 1, VDD = 1.71 V	Vref = 50…1200 mV	--	1	--	
		G = 1, VDD = 3.3 V	Vref = 50…1200 mV	--	1	--	
		G = 1, VDD = 5.5 V	Vref = 50…1200 mV	--	1	--	
		G = 0.5, VDD = 1.71 V	Vref = 100 mV	-0.55%	--	1.80%	
			Vref = 600 mV	-1.00%	--	1.26%	
			Vref = 1200 mV	-1.20%	--	1.24%	
		G = 0.5, VDD = 3.3 V	Vref = 100 mV	-0.87%	--	2.82%	
			Vref = 600 mV	-0.98%	--	1.26%	
			Vref = 1200 mV	-1.09%	--	1.21%	
		G = 0.5, VDD = 5.5 V	Vref = 100 mV	-1.88%	--	4.15%	
			Vref = 600 mV	-1.05%	--	1.35%	
			Vref = 1200 mV	-1.02%	--	1.27%	
		G = 0.33, VDD = 1.71V	Vref = 100 mV	-1.28%	--	2.40%	
			Vref = 600 mV	-1.13%	--	2.00%	
			Vref = 1200 mV	-1.21%	--	2.07%	
		G = 0.33, VDD = 3.3 V	Vref = 100 mV	-1.46%	--	4.00%	
			Vref = 600 mV	-1.40%	--	1.72%	
			Vref = 1200 mV	-1.63%	--	1.53%	
		G = 0.33, VDD = 5.5 V	Vref = 100 mV	-1.28%	--	2.40%	
			Vref = 600 mV	-1.46%	--	4.00%	
			Vref = 1200 mV	-1.55%	--	4.15%	
		G = 0.25, VDD = 1.71V	Vref = 100 mV	-1.21%	--	2.56%	
			Vref = 600 mV	-1.29%	--	2.25%	
			Vref = 1200 mV	-1.37%	--	2.30%	
		G = 0.25, VDD = 3.3 V	Vref = 100 mV	-1.36%	--	3.97%	
			Vref = 600 mV	-1.45%	--	1.84%	
			Vref = 1200 mV	-1.84%	--	1.82%	
		G = 0.25, VDD = 5.5 V	Vref = 100 mV	-2.09%	--	4.63%	
			Vref = 600 mV	-1.48%	--	1.94%	
			Vref = 1200 mV	-1.47%	--	1.87%	
Vref	Internal Vref error, Vref = 1200 mV	VDD = 1.8 V ± 5 %	T = 25°C	-0.96%	--	0.95%	
			T = (-40…+85)°C	-1.30%	--	1.12%	
		VDD = 3.3 V ± 10 %	T = 25°C	-1.02%	--	1.03%	
			T = (-40…+85)°C	-1.34%	--	1.14%	
		VDD = 5.0 V ± 10 %	T = 25°C	-1.20%	--	1.15%	
			T = (-40…+85)°C	-1.58%	--	1.48%	

5.12 ADC Specifications (Including PGA)

Note: PGA input voltage should not exceed values given in Section 5.1 Absolute Maximum Conditions.

Table 13. Single-Ended ADC Operation, T = (-40 to +85)°C, VDD = (1.71 to 5.5)V, unless otherwise specified

Symbol	Parameter	Description/Note	Conditions	Min.	Max.	Unit
V_{inp}	Input Voltage Range (bit 0 to bit 255), relative to GND	G = 0.25	VDD = 5V ±10%	120	4120	mV
		G = 0.5	VDD = 2.5 to 5.5 V	60	2060	mV
		G = 1		30	1030	mV
		G = 2		20	520	mV
		G = 4		15	265	mV
		G = 8		12	137	mV
ZE	Offset Zero Error	G = 0.25	T = 25°C, VDD = 5V ±10%	--	±1.7	LSB
		G = 0.5	T = 25°C, VDD = 2.5 to 5.5 V	--	±2.6	LSB
		G = 1	T = 25°C	--	±3	LSB
		G = 2		--	±2.6	LSB
		G = 4		--	±3.3	LSB
		G = 8		--	±4.6	LSB
dZE/dT	Offset Zero Error Temperature Drift	G = 0.25	VDD = 5V ±10%	--	±0.008	%/°C
		G = 0.5	VDD = 2.5 to 5.5 V	--	±0.009	%/°C
		G = 1		--	±0.01	%/°C
		G = 2		--	±0.014	%/°C
		G = 4		--	±0.025	%/°C
		G = 8		--	±0.048	%/°C
GE	Gain Error	G = 0.25	T = 25°C, VDD = 5V ±10%	--	±1.5	LSB
		G = 0.5	T = 25°C, VDD = 2.5 to 5.5 V	--	±1.3	LSB
		G = 1	T = 25°C	--	±1.5	LSB
		G = 2		--	±1.7	LSB
		G = 4		--	±1.3	LSB
		G = 8		--	±1.2	LSB
dGE/dT	Gain Error Temperature Coefficient	G = 0.25	VDD = 5V ±10%	--	±0.007	%/°C
		G = 0.5	VDD = 2.5 to 5.5 V	--	±0.008	%/°C
		G = 1		--	±0.007	%/°C
		G = 2		--	±0.009	%/°C
		G = 4		--	±0.008	%/°C
		G = 8		--	±0.008	%/°C

Table 13. Single-Ended ADC Operation, T = (-40 to +85)°C, VDD = (1.71 to 5.5)V, unless otherwise specified

Symbol	Parameter	Description/Note	Conditions	Min.	Max.	Unit
INL	Integral Non-Linearity Error	G = 0.25	T = 25°C, VDD = 5V ±10%	--	±2.1	LSB
			VDD = 5V ±10%	--	±3.2	LSB
		G = 0.5	T = 25°C, VDD = 2.5 to 5.5 V	--	±1.9	LSB
			VDD = 2.5 to 5.5 V	--	±3.4	LSB
		G = 1	T = 25°C	--	±1.7	LSB
				--	±3.2	LSB
		G = 2	T = 25°C	--	±1.8	LSB
				--	±2.9	LSB
		G = 4	T = 25°C	--	±1.8	LSB
				--	±2.7	LSB
		G = 8	T = 25°C	--	±1.6	LSB
				--	±2.6	LSB
DNL	Differential Non-Linearity	G = 0.25, 0.5, 1, 2, 4, 8		--	±0.5	LSB
NOISE				--	±0.5	LSB

Note: To ensure linear operation, absolute input voltage on each pin should not exceed VDD-0.5

Table 14. Differential ADC Operation, T = (-40 to +85)°C, VDD = (1.71 to 5.5)V, Vcm = 500 mV, unless otherwise specified

Symbol	Parameter	Description/Note	Conditions	Min.	Max.	Unit
V_{ind}	Input Voltage Range (bit 0 to bit 255), Differential	G = 1		-500	500	mV
		G = 2		-250	250	mV
		G = 4		-125	125	mV
		G = 8		-62.5	62.5	mV
		G = 16		-31.25	31.25	mV
V_{cm}	Input Common Voltage (see Note 1)	G = 1, 2, 4, 8, 16	VDD = 1.8 V ±5%	400	550	mV
			VDD = 3.3 V ±10%	400	950	mV
			VDD = 5 V ±10%	400	950	mV
ZE	Offset Zero Error	G = 1	T = 25°C	--	±2.5	LSB
		G = 2		--	±2.7	LSB
		G = 4		--	±3.3	LSB
		G = 8		--	±4.6	LSB
		G = 16		--	±6.8	LSB
dZE/dT	Offset Zero Error Temperature Drift	G = 1		--	±0.014	%/°C
		G = 2		--	±0.015	%/°C
		G = 4		--	±0.02	%/°C
		G = 8		--	±0.032	%/°C
		G = 16		--	±0.1	%/°C

Table 14. Differential ADC Operation, T = (-40 to +85)°C, VDD = (1.71 to 5.5)V, Vcm = 500 mV, unless otherwise specified

Symbol	Parameter	Description/Note	Conditions	Min.	Max.	Unit
GE	Gain Error	G = 1	T = 25°C	--	±0.8	LSB
		G = 2		--	±0.8	LSB
		G = 4		--	±0.5	LSB
		G = 8		--	±1	LSB
		G = 16		--	±1	LSB
dGE/dT	Gain Error Temperature Drift	G = 1		--	±0.007	%/°C
		G = 2		--	±0.007	%/°C
		G = 4		--	±0.006	%/°C
		G = 8		--	±0.006	%/°C
		G = 16		--	±0.005	%/°C
INL	Integral Non-Linearity Error	G = 1	T = 25°C	--	±1.6	LSB
				--	±3.2	LSB
		G = 2	T = 25°C	--	±1.3	LSB
				--	±3	LSB
		G = 4	T = 25°C	--	±1.2	LSB
				--	±3.1	LSB
		G = 8	T = 25°C	--	±1.3	LSB
				--	±3.4	LSB
		G = 16	T = 25°C	--	±1.6	LSB
				--	±3.2	LSB
DNL	Differential Non-Linearity	G = 1, 2, 4, 8, 16		--	±0.5	LSB
NOISE				--	±0.5	LSB

Note 1: Vcm range is given for stable CMRR > 34 dB.

Note 2: To ensure linear operation, absolute input voltage on each pin should not exceed VDD-0.5.

Table 15. Pseudo-Differential ADC Operation, T = (-40 to +85)°C, VDD = (1.71 to 5.5)V, Vcm = 500 mV, unless otherwise specified

Symbol	Parameter	Description/Note	Conditions	Min.	Max.	Unit
V_{ind}	Input Voltage Range (bit 0 to bit 255), Differential	G = 1		0	980	mV
		G = 2		0	490	mV
		G = 4		0	245	mV
V_{inn}	Negative input voltage range	G = 1, 2, 4	VDD = 1.8 V ±5%	500	500	mV
			VDD = 3.3 V ±10%	500	1250	mV
			VDD = 5 V ±10%	500	1250	mV
ZE	Offset Zero Error	G = 1	T = 25°C, VDD = 2.0 to 5.5 V	--	±2.6	LSB
		G = 2	T = 25°C	--	±2.7	LSB
		G = 4		--	±3.3	LSB
dZE/dT	Offset Zero Error Temperature Drift	G = 1	T = 25°C, VDD = 2.0 to 5.5 V	--	±0.012	%/°C
		G = 2	T = 25°C	--	±0.013	%/°C
		G = 4		--	±0.018	%/°C
GE	Gain Error	G = 1	T = 25°C, VDD = 2.0 to 5.5 V	--	±1.9	LSB
		G = 2	T = 25°C	--	±2.4	LSB
		G = 4		--	±1.4	LSB
dGE/dT	Gain Error Temperature Drift	G = 1	T = 25°C, VDD = 2.0 to 5.5 V	--	±0.009	%/°C
		G = 2	T = 25°C	--	±0.013	%/°C
		G = 4		--	±0.007	%/°C
INL	Integral Non-Linearity Error	G = 1	T = 25°C, VDD = 2.0 to 5.5 V	--	±1.4	LSB
			VDD = 2.0 to 5.5 V	--	±2	LSB
		G = 2	T = 25°C	--	±1.7	LSB
				--	±2.4	LSB
		G = 4	T = 25°C	--	±1.8	LSB
				--	±2.1	LSB
DNL	Differential Non-Linearity	G = 1, 2, 4		--	±0.5	LSB
NOISE				--	±0.5	LSB

Note 1: V_{inn} is given for convenience instead of V_{cm}

Note 2: V_{inn} range is given for stable CMRR > 34 dB

Note 3: To ensure linear operation, absolute input voltage on each pin should not exceed VDD-0.5

5.13 PGA Specifications

Note: PGA input voltage should not exceed values given in Section 5.1 Absolute Maximum Conditions.

Table 16. Single-Ended PGA Operation, T = (-40 to +85)°C, VDD = (1.71 to 5.5)V, unless otherwise specified

Symbol	Parameter	Description/Note	Conditions	Min.	Typ.	Max.	Unit
V_{os}	Offset Voltage (RTI, see Note 1)	G = 0.25	T = 25°C, VDD = 5V ±10%	--	±8.5	±50.3	mV
		G = 0.5	T = 25°C, VDD = 2.5 to 5.5 V	--	±5.3	±28.3	mV
		G = 1	T = 25°C	--	±2.2	±12.1	mV
		G = 2	T = 25°C	--	±3.4	±13.7	mV
		G = 4	T = 25°C	--	±3.2	±12.0	mV
		G = 8	T = 25°C	--	±3.2	±11.6	mV
dV_{os}/dT	V_{os} (RTI) Temperature Drift	G = 0.25	VDD = 5V ±10%	--	±0.0097	±0.0584	mV/°C
		G = 0.5	VDD = 2.5 to 5.5 V	--	±0.0058	±0.0345	mV/°C
		G = 1		--	±0.0018	±0.0111	mV/°C
		G = 2		--	±0.0031	±0.0186	mV/°C
		G = 4		--	±0.0028	±0.0167	mV/°C
		G = 8		--	±0.0026	±0.0158	mV/°C
ΔG	Gain Error	G = 0.25	VDD = 5V ±10%	-0.822	0.562	1.945	%
		G = 0.5	VDD = 2.5 to 5.5 V	-0.877	0.196	1.260	%
		G = 1		-0.118	-0.012	0.093	%
		G = 2		-1.361	-0.213	0.935	%
		G = 4		-2.169	-0.554	1.060	%
		G = 8		-3.616	-1.299	1.018	%
$V_{ind}(lin)$	Linear Differential Input Voltage Range	G = 0.25	VDD = 5V ±10%	273	--	4167	mV
		G = 0.5	VDD = 2.5 to 5.5 V	126	--	2153	mV
		G = 1		59	--	1145	mV
		G = 2		39	--	572	mV
		G = 4		23	--	286	mV
		G = 8		15	--	144	mV
V_{sw}	Output Voltage Swing			--	GND to 1380	--	mV

Note 1: RTI - referred to input.

Table 17. Differential PGA Operation, T = (-40 to +85)°C, VDD = (1.71 to 5.5)V, Vcm = 500 mV, unless otherwise specified

Symbol	Parameter	Description/Note	Conditions	Min.	Typ.	Max.	Unit
V_{os}	Offset Voltage (RTO, see Note 1)	All gains	V_{id} = 0	--	550	--	mV
ΔV_{os}	Offset Voltage Error (RTO)	G = 1	T = 25°C	--	±1.4	±5.4	mV
		G = 2	T = 25°C	--	±1.1	±4.5	mV
		G = 4	T = 25°C	--	±1.1	±6.5	mV
		G = 8	T = 25°C	--	±2.2	±10.1	mV
		G = 16	T = 25°C	--	±4.0	±20.4	mV
dV_{os}/dT	V_{os} (RTO) Temperature Drift	G = 1		--	±0.0124	±0.0551	mV/°C
		G = 2		--	±0.0118	±0.0658	mV/°C
		G = 4		--	±0.0148	±0.0884	mV/°C
		G = 8		--	±0.0240	±0.1416	mV/°C
		G = 16		--	±0.0432	±0.256	mV/°C
ΔG	Gain Error	G = 1		-1.080	-0.194	0.664	%
		G = 2		-1.761	-0.568	0.629	%
		G = 4		-2.573	-0.929	0.656	%
		G = 8		-3.553	-1.620	0.225	%
		G = 16		-3.720	-1.808	0.106	%
V_{ind} (lin)	Linear Differential Input Voltage Range	G = 1		-452	--	578	mV
		G = 2		-229	--	289	mV
		G = 4		-115	--	145	mV
		G = 8		-57	--	72	mV
		G = 16		-29	--	32	mV
CMRR	Common-Mode Rejection Rate	G = 1		32	--	--	dB
		G = 2		38	--	--	dB
		G = 4		44	--	--	dB
		G = 8		50	--	--	dB
		G = 16		56	--	--	dB
ICMR	Input Common Mode Range	All gains	VDD = 1.8 V, Vind=(-500 to 500) mV/G	400	--	550	mV
			VDD = 3.3 V, Vind=(-500 to 500) mV/G	400	--	900	mV
			VDD = 5.0 V, Vind=(-500 to 500) mV/G	450	--	900	mV
V_{sw}	Output Voltage Swing			--	GND to 1380	--	mV

Note 1: RTO - referred to output.

Table 18. Pseudo-Differential PGA Operation, T = (-40 to +85)°C, VDD = (1.71 to 5.5)V, Vinn = 500 mV, unless otherwise specified

Symbol	Parameter	Description/Note	Conditions	Min.	Typ.	Max.	Unit
V_{os}	Offset Voltage (RTO, see Note 1)	All gains	V_{id} = 0	--	180	--	mV
ΔV_{os}	Offset Voltage Error (RTO)	G = 1	T = 25°C, VDD = 2.0 V to 5.5 V	--	±1.2	±3.6	mV
		G = 2	T = 25°C	--	±1.5	±5.5	mV
		G = 4	T = 25°C	--	±2.1	±6.4	mV
dV_{os}/dT	V_{os} (RTO) Temperature Drift	G = 1		--	±0.0088	±0.0493	mV/°C
		G = 2		--	±0.0098	±0.0588	mV/°C
		G = 4		--	±0.0128	±0.0772	mV/°C
ΔG	Gain Error	G = 1		-0.916	-0.455	0.549	%
		G = 2		-1.855	-0.567	0.685	%
		G = 4		-2.559	-0.918	0.735	%
V_{ind} (lin)	Linear Differential Input Voltage Range	G = 1		0	--	834	mV
		G = 2		0	--	394	mV
		G = 4		0	--	239	mV
CMRR	Common-Mode Rejection Rate	G = 1		32	--	--	dB
		G = 2		38	--	--	dB
		G = 4		44	--	--	dB
V_{inn}	Negative Input Voltage Range	All gains	VDD = 1.8 V, Vind=(0 to 1000) mV/G	500	--	500	mV
			VDD = 3.3 V, Vind=(0 to 1000) mV/G	500	--	1250	mV
			VDD = 5.0 V, Vind=(0 to 1000) mV/G	500	--	1250	mV
V_{sw}	Output Voltage Swing			--	180 to 1380	--	mV

Note 1: RTO - referred to output.

Table 19. Differential or Pseudo-Differential PGA Operation, ADC - Power Down, T = (-40 to +85)°C, VDD = (1.71 to 5.5)V, Vcm = 500 mV, unless otherwise specified

Symbol	Parameter	Description/Note	Conditions	Min.	Typ.	Max.	Unit
V_{os}	Offset Voltage (RTI, see Note 1)	All gains	T = 25°C, VDD = 3.3 V	--	±1.9	±11.2	mV
ΔG	Gain Error	G = 1		-1.080	-0.194	0.664	%
		G = 2		-1.761	-0.568	0.629	
		G = 4		-2.573	-0.929	0.656	
		G = 8		-3.553	-1.620	0.225	%
		G = 16		-3.720	-1.808	0.106	%
CMRR	Common-Mode Rejection Rate	G = 1		32	--	--	dB
		G = 2		38	--	--	dB
		G = 4		44	--	--	dB
		G = 8		50	--	--	dB
		G = 16		56	--	--	dB
V_{inn}	Negative Input Voltage Range	All gains	VDD = 1.8 V, Vind=(0 to 1000) mV/G	500	--	500	mV
			VDD = 3.3 V, Vind=(0 to 1000) mV/G	500	--	1250	mV
			VDD = 5.0 V, Vind=(0 to 1000) mV/G	500	--	1250	mV
V_{sw}	Output Voltage Swing			--	GND to 1380	--	mV

Note 1: RTI - referred to input.

Note 2: When ADC is powered down, PGA operation in Differential or Pseudo-Differential mode is not recommended. Parameters in Table 19. are for reference only.

6.0 Summary of Macrocell Function

6.1 I/O Pins

- Digital Input (low voltage or normal voltage, with or without Schmitt Trigger)
- Open Drain Outputs (1x, 2x, 4x)
- Push Pull Outputs (1x, 2x, 4x)
- Analog I/O
- 10 kΩ/100 kΩ/1 MΩ pull-up/pull-down resistors
- 40 mA 4X Drive output, Pin 10 and Pin 12 (depending on VDD)
- Pins 3, 4, 5, 6, 7, 8, 9, 10, 12, 13, 15, 16, 17, 18, 19, 20 can be configured as bidirectional IO

6.2 Connection Matrix

- Two digital connection matrices for circuit connections based on user design

6.3 Analog-to-Digital Converter

- 8-bit, 100 kHz, Successive Approximation Register ADC
- DNL < ±1LSB, INL < ±1LSB
- VIN Range: 50 mV ~ 1.05 V
- Common Mode Voltage Range: VPP/2 – 2 V
- 3-bit Programmable Gain Amplifier with gain values of (1, 2, 4, 8,16X in differential mode, 1, 2, 4X in pseudodifferential mode and 0.25, 0.5, 1, 2, 4, 8x in single-ended mode)
- SPI output format

6.4 Digital-to-Analog Converter

- Two 8-bit Digital-to-Analog Converters with the output of 0 to 1 V

6.5 Analog Comparators (6 total)

- Six general purpose ACMPs
- Selectable hysteresis 0 mV/25 mV/50 mV/200 mV
- Internal or external Vref
- Selectable gain (1x, 0.5x, 0.33x, 0.25x)
- Low bandwidth option
- Optional 100uA pullup current source on positive input node

6.6 Two Voltage References

- Used for references on Analog Comparators
- Can also be driven to external pins
- 50 mV to 1.2 V, with 50 mV resolution

6.7 Combinational Logic Look Up Tables (LUTs – 25 total)

- Eight 2-bit Lookup Tables
- Sixteen 3-bit Lookup Tables
- One 4-bit Lookup Table

6.8 Combination Function Macrocells (1 total)

- One Selectable Pattern Generator or 4-bit LUT

6.9 Delays/Counters (10 total)

- Four 14-bit delay/counters: Range 1-16384 clock cycles
- Six 8-bit delays/counters: Range 1-255 clock cycles

6.10 Digital Comparators or PWM (3 total)

- Three 8-bit 100 kHz PWMs or 10 MHz Digital Comparators

6.11 Pipe Delay (2 total)

- 16 stage delay
- Two 1-16 stage selectable outputs

6.12 Programmable Delays (2 total)

- 110 ns / 220 ns / 330 ns / 440 ns @ 3.3 V
- Includes Edge Detection function

6.13 Additional Logic Functions (2 total)

- Two Inverters

6.14 RC Oscillator

- 25 kHz and 2 MHz selectable frequency
- Pre-divider (4): OSC/1, OSC/2, OSC/4, and OSC/8
- Output to Matrix: OSC/1, OSC/2, OSC/3, OSC/4, OSC/8, OSC/12, OSC/24, OSC/64
- Output to CNT/DLY/FSM/PWM_ramp: OSC/1, OSC/4, OSC/12, OSC/24, OSC/64
- Output to ADC: OSC/1, OSC/16

6.15 Low Frequency (LF) Oscillator

- 1.73 kHz
- OSC/1, OSC/2, OSC/4, OSC/16 dividers

6.16 Ring Oscillator

- 27 MHz
- Post divider: OSC/1, OSC/4, OSC/8, OSC/16
- Output to Matrix: OSC/1, OSC/2, OSC/3, OSC/4, OSC/8, OSC/12, OSC/24, OSC/64
- Output to CNT/DLY/FSM/PWM_ramp: OSC/1, OSC/256
- Output to ADC: OSC/1, OSC/16

6.17 Digital Storage Elements (DFFs/Latches)

- User selectable initial state
- Asynchronous Set/Reset
- Output polarity selection

6.18 Slave SPI

- Serial-to-Parallel: 8 and 16-bit modes
- Parallel-to-Serial: 8 and 16-bit modes
- Can be used as ADC buffer

7.0 I/O Pins

The SLG46621 has a total of 17 multi-function I/O pins which can function as either a user defined Input or Output, as well as serving as a special function (such as outputting the voltage reference), or serving as a signal for programming of the on-chip Non Volatile Memory (NVM). Refer to Section 2.0 Pin Description for normal and programming mode pin definitions.

All of the 17 user defined I/O pins on the SLG46621, except Pin 2 can serve as both digital input and digital output. Pin 2 can only serve as a digital input pin or external reset.

The high side of the user selectable push-pull or open-drain pin output structures for each GPIO is connected to either VDD or VDD2. This allows for the appropriate voltage level output compatible with each voltage domain. The level shifters are located in lower power IO PADs (pins 12, 13, 15, 16, 17, 18, 19, 20) powered from VDD2. All configuration registers of the SLG46621 are powered from VDD, so it is possible to maintain the configuration information even after VDD2 was turned off, discharged and turned back on again.

Pins 2, 3, 4, 5, 6, 7, 8, 9 and 10 are powered from V_{DD} and, pins 12, 13, 15, 16, 17, 18, 19 and 20 are powered from $V_{DD2.}$ All internal macrocells are powered from $V_{DD.}$ Voltage on V_{DD2} Pin must be less or equal voltage on V_{DD} Pin.

In case V_{DD2} floating and any Pin powered from V_{DD2} is configured as input, ESD pin protection diodes must be considered when applying an input signal to the pin. This will cause a significant current leakage.

In case V_{DD2} floating and any Pin powered from V_{DD2} is configured as Output, the pin will behave as NMOS Open Drain.

It is not recommended to connect V_{DD2} to the GND.

7.1 Input Modes

Each I/O pin can be configured as a digital input pin with/without buffered Schmitt trigger, or can also be configured as a low voltage digital input. Pins 3, 4, 5, 6, 7, 8, 9, 10, 12, 13, 15, and 17 can also be configured to serve as analog inputs to the on-chip comparators. Pins 18 and 19 can also be configured as analog reference voltage inputs.

7.2 Output Modes

Pins 3, 4, 5, 6, 7, 8, 9, 10, 12, 13, 15, 16, 17, 18, 19, and 20 can all be configured as digital output pins.

7.3 Pull Up/Down Resistors

All I/O pins have the option for user selectable resistors connected to the input structure. The selectable values on these resistors are 10 kΩ, 100 kΩ and 1 MΩ. In the case of Pin 2, the resistors are fixed to a pull-down configuration. In the case of all other I/O pins, the internal resistors can be configured as either pull-up or pull-downs.

7.4 I/O Register Settings

7.4.1 PIN 2 Register Settings

Table 20. PIN 2 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 2 Input Mode Control	<942:941>	00: Digital in without schmitt trigger 01: Digital in with schmitt trigger 10: Low Voltage Digital in 11:Reserved
PIN 2 Pull-Up/Down Resistor Selection	<944:943>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 2 Pull-Up Resistor Enable	<945>	0: Pull-Down 1: Pull-Up

7.4.2 PIN 3 Register Settings

Table 21. PIN 3 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 3 Input Mode Control	<947:946>	00: Digital in without schmitt trigger 01: Digital in with schmitt trigger 10: Low Voltage Digital in 11: Analog IO
PIN 3 Output Mode Control	<949:948>	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-Drain 11: 2x Open-Drain
PIN 3 Pull-Up/Down Resistor Selection	<951:950>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 3 Pull-Up Resistor Enable	<952>	0: Pull Down Resistor 1: Pull Up Resistor

7.4.3 PIN 4 Register Settings

Table 22. PIN 4 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 4 Mode Control	<955:953>	000: Digital in without schmitt trigger 001: Digital in with schmitt trigger 010: Low Voltage Digital in 011: Analog IO 100: Push-Pull 101: NMOS Open-Drain 110: PMOS Open-Drain 111: Analog IO & NMOS Open-Drain
PIN 4 Pull-Up/Down Resistor Selection	<957:956>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 4 Pull-Up Resistor Enable	<958>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 4 Output Driver Current Double	<959>	0: 1X drive 1: 2X drive

7.4.4 PIN 5 Register Settings

Table 23. PIN 5 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 5 Input Mode Control	<960:961>	00: Digital in without schmitt trigger 01: Digital in with schmitt trigger 10: Low Voltage Digital in 11: Analog IO
PIN 5 Output Mode Control	<963:962>	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-Drain 11: 2x Open-Drain
PIN 5 Pull-Up/Down Resistor Selection	<965:964>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 5 Pull-Up Resistor Enable	<966>	0: Pull Down Resistor 1: Pull Up Resistor

7.4.5 PIN 6 Register Settings

Table 24. PIN 6 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 6 Mode Control	<969:967>	000: Digital in without schmitt trigger 001: Digital in with schmitt trigger 010: Low Voltage Digital in 011: Analog IO 100: Push-Pull 101: NMOS Open-Drain 110: PMOS Open-Drain 111: Analog IO & NMOS Open-Drain
PIN 6 Pull-Up/Down Resistor Selection	<971:970>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 6 Pull-Up Resistor Enable	<972>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 6 Output Driver Current Double	<973>	0: 1X drive 1: 2X drive

7.4.6 PIN 7 Register Settings

Table 25. PIN 7 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 7 Input Mode Control	<975:974>	00: Digital in without schmitt trigger 01: Digital in with schmitt trigger 10: Low Voltage Digital in 11: Analog IO
PIN 7 Output Mode Control	<977:976>	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-Drain 11: 2x Open-Drain
PIN 7 Pull-Up/Down Resistor Selection	<979:978>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 7 Pull-Up Resistor Enable	<980>	0: Pull Down Resistor 1: Pull Up Resistor

7.4.7 PIN 8 Register Settings

Table 26. PIN 8 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 8 Mode Control	<983:981>	000: Digital in without schmitt trigger 001: Digital in with schmitt trigger 010: Low Voltage Digital in 011: Analog IO 100: Push-Pull 101: NMOS Open-Drain 110: PMOS Open-Drain 111: Analog IO & NMOS Open-Drain
PIN 8 Pull-Up/Down Resistor Selection	<985:984>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 8 Pull-Up Resistor Enable	<986>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 8 Output Driver Current Double	<987>	0: 1X drive 1: 2X drive

7.4.8 PIN 9 Register Settings

Table 27. PIN 9 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 9 Input Mode Control	<989:988>	00: Digital in without schmitt trigger 01: Digital in with schmitt trigger 10: Low Voltage Digital in 11: Analog IO
PIN 9 Output Mode Control	<991:990>	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-Drain 11: 2x Open-Drain
PIN 9 Pull-Up/Down Resistor Selection	<993:992>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 9 Pull-Up Resistor Enable	<994>	0: Pull Down Resistor 1: Pull Up Resistor

7.4.9 PIN 10 Register Settings

Table 28. PIN 10 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 10 Input Mode Control	<996:995>	00: Digital in without schmitt trigger 01: Digital in with schmitt trigger 10: Low Voltage Digital in 11: Analog IO
PIN 10 Output Mode Control	<998:997>	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-Drain 11: 2x Open-Drain
PIN 10 Pull-Up/Down Resistor Selection	<1000:999>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 10 Pull-Up Resistor Enable	<1001>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 10 4x Drive Enable	<1002>	0: Disable 1: Enable

7.4.10 PIN 12 Register Settings

Table 29. PIN 12 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 12 Mode Control	<1913:1911>	000: Digital in without schmitt trigger 001: Digital in with schmitt trigger 010: Low Voltage Digital in 011: Analog IO 100: Push-Pull 101: NMOS Open-Drain 110: PMOS Open-Drain 111: Analog IO & NMOS Open-Drain
PIN 12 Pull-Up/Down Resistor Selection	<1915:1914>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 12 Pull-Up Resistor Enable	<1916>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 12 Output Driver Current Double	<1917>	0: 1X drive 1: 2X drive
PIN 12 4x Drive Enable	<1918>	0: Disable 1: Enable

7.4.11 PIN 13 Register Settings

Table 30. PIN 13 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 13 Input Mode Control	<1920:1919>	00: Digital in without schmitt trigger 01: Digital in with schmitt trigger 10: Low Voltage Digital in 11: Analog IO

Table 30. PIN 13 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 13 Output Mode Control	<1922:1921>	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-Drain 11: 2x Open-Drain
PIN 13 Pull-Up/Down Resistor Selection	<1924:1923>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 13 Pull-Up Resistor Enable	<1925>	0: Pull Down Resistor 1: Pull Up Resistor

7.4.12 PIN 15 Register Settings

Table 31. PIN 15 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 15 Mode Control	<1935:1933>	000: Digital in without schmitt trigger 001: Digital in with schmitt trigger 010: Low Voltage Digital in 011: Analog IO 100: Push-Pull 101: NMOS Open-Drain 110: PMOS Open-Drain 111: Analog IO & NMOS Open-Drain
PIN 15 Pull-Up/Down Resistor Selection	<1937:1936>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 15 Pull-Up Resistor Enable	<1938>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 15 Output Driver Current Double	<1939>	0: 1X drive 1: 2X drive

7.4.13 PIN 16 Register Settings

Table 32. PIN 16 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 16 Input Mode Control	<1941:1940>	00: Digital in without schmitt trigger 01: Digital in with schmitt trigger 10: Low Voltage Digital in 11: Analog IO
PIN 16 Output Mode Control	<1943:1942>	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-Drain 11: 2x Open-Drain
PIN 16 Pull-Up/Down Resistor Selection	<1945:1944>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 16 Pull-Up Resistor Enable	<1946>	0: Pull Down Resistor 1: Pull Up Resistor

7.4.14 PIN 17 Register Settings

Table 33. PIN 17 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 17 Mode Control	<1949:1947>	000: Digital in without schmitt trigger 001: Digital in with schmitt trigger 010: Low Voltage Digital in 011: Analog IO 100: Push-Pull 101: NMOS Open-Drain 110: PMOS Open-Drain 111: Analog IO & NMOS Open-Drain
PIN 17 Pull-Up/Down Resistor Selection	<1951:1950>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 17 Pull-Up Resistor Enable	<1952>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 17 Output Driver Current Double	<1953>	0: 1X drive 1: 2X drive

7.4.15 PIN 18 Register Settings

Table 34. PIN 18 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 18 Input Mode Control	<1955:1954>	00: Digital in without schmitt trigger 01: Digital in with schmitt trigger 10: Low Voltage Digital in 11: Analog IO
PIN 18 Output Mode Control	<1957:1956>	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-Drain 11: 2x Open-Drain
PIN 18 Pull-Up/Down Resistor Selection	<1959:1958>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 18 Pull-Up Resistor Enable	<1960>	0: Pull Down Resistor 1: Pull Up Resistor

7.4.16 PIN 19 Register Settings

Table 35. PIN 19 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 19 Input Mode Control	<1962:1961>	00: Digital in without schmitt trigger 01: Digital in with schmitt trigger 10: Low Voltage Digital in 11: Analog IO
PIN 19 Output Mode Control	<1964:1963>	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-Drain 11: 2x Open-Drain.
PIN 19 Pull-Up/Down Resistor Selection	<1966:1965>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 19 Pull-Up Resistor Enable	<1967>	0: Pull Down Resistor 1: Pull Up Resistor

7.4.17 PIN 20 Register Settings

Table 36. PIN 20 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 20 Mode Control	<1970:1968>	000: Digital in without schmitt trigger 001: Digital in with schmitt trigger 010: Low Voltage Digital in 011: Analog IO 100: Push-Pull 101: NMOS Open-Drain 110: PMOS Open-Drain 111: Analog IO & NMOS Open-Drain
PIN 20 Pull-Up/Down Resistor Selection	<1972:1971>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 20 Pull-Up Resistor Enable	<1973>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 20 Output Driver Current Double	<1974>	0: 1X drive 1: 2X drive

7.5 GPI IO Structure

7.5.1 GPI IO Structure (for Pin 2)

Input Mode [1:0]
00: Digital IN without Schmitt Trigger, WOSMT_EN = 1, OE = 0
01: Digital IN with Schmitt Trigger, SMT_EN = 1, OE = 0
10: Low Voltage Digital IN mode, LV_EN = 1, OE = 0
11: Reserved

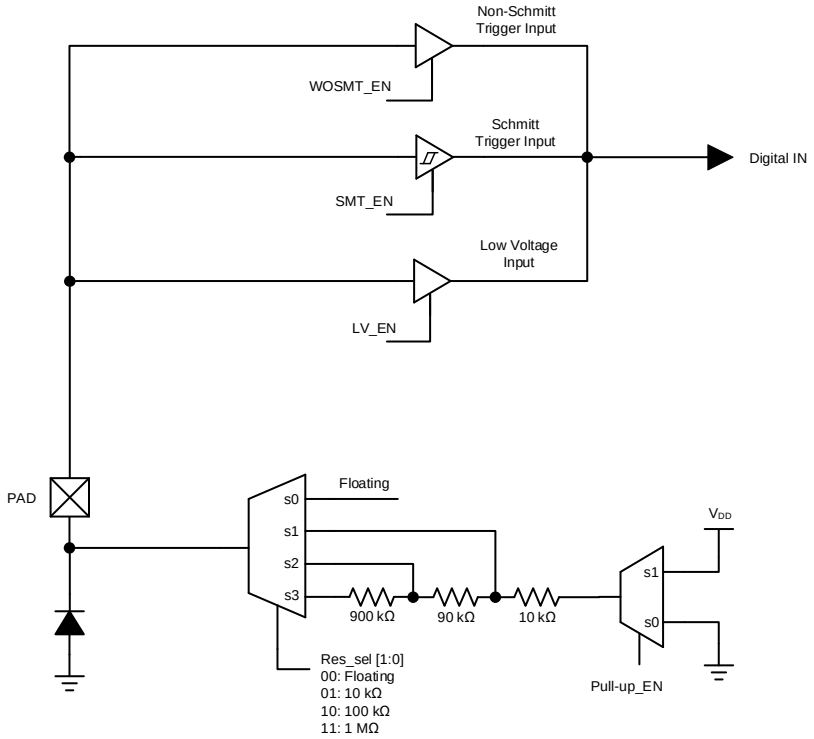


Figure 2. PIN 2 GPI IO Structure Diagram

7.6 Matrix OE IO Structure

7.6.1 Matrix OE IO Structure (for Pins 3, 5, 7, 9)

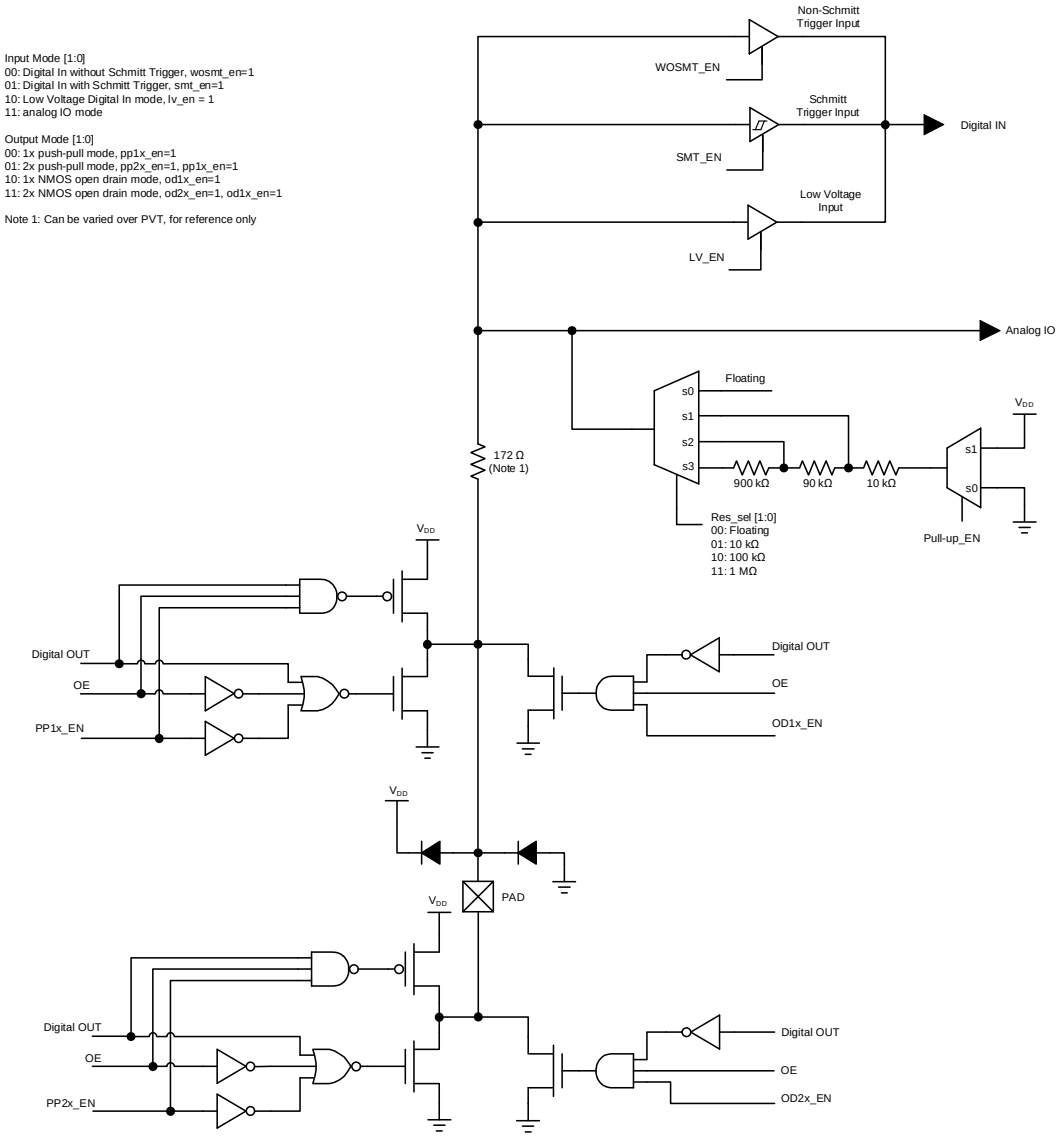


Figure 3. Matrix OE IO Structure Diagram

7.6.2 Matrix OE IO Structure (for Pins 13, 16, 18, 19)

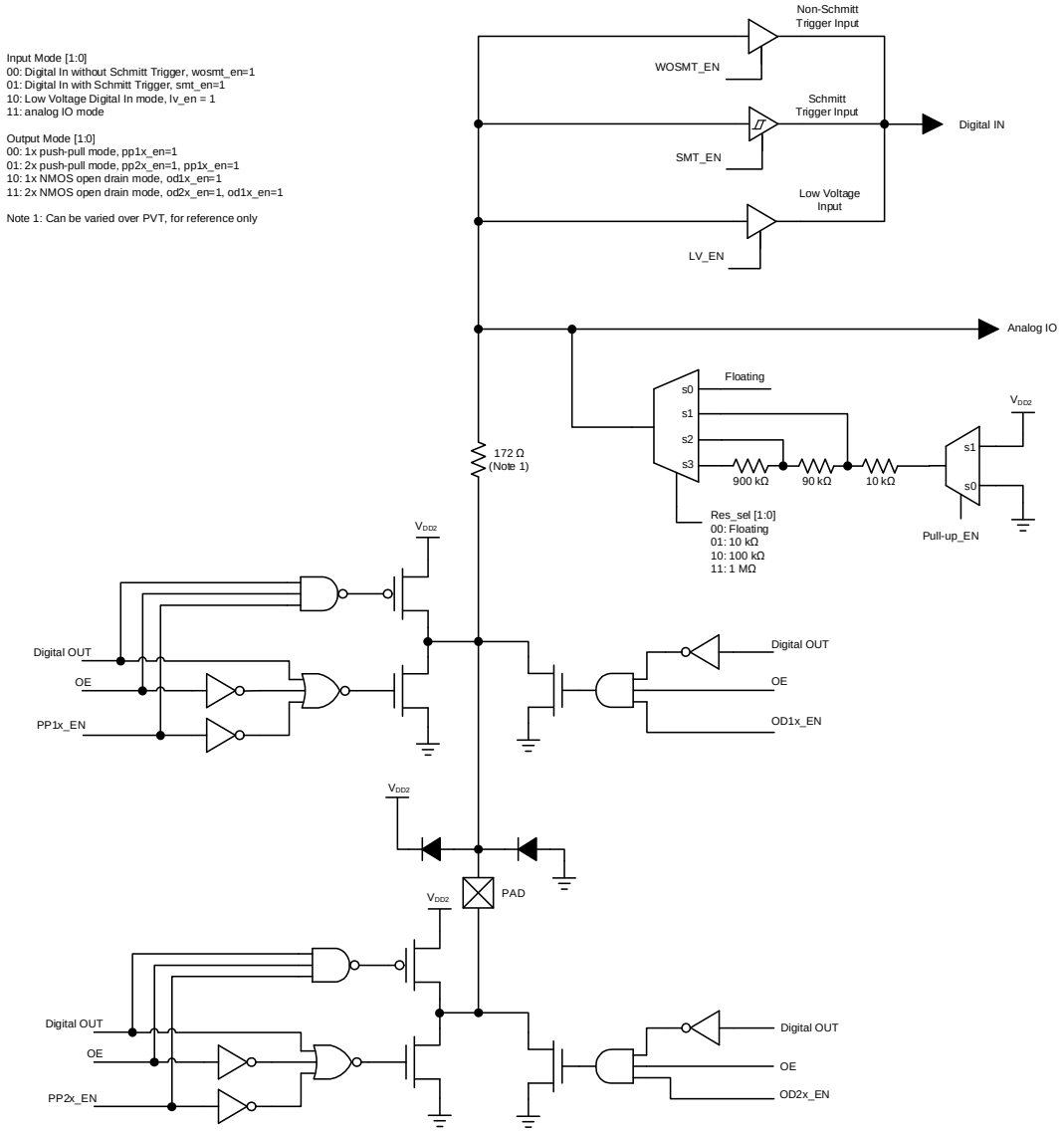


Figure 4. Matrix OE IO Structure Diagram

7.6.3 Matrix OE 4x Drive Structure (for Pin 10)

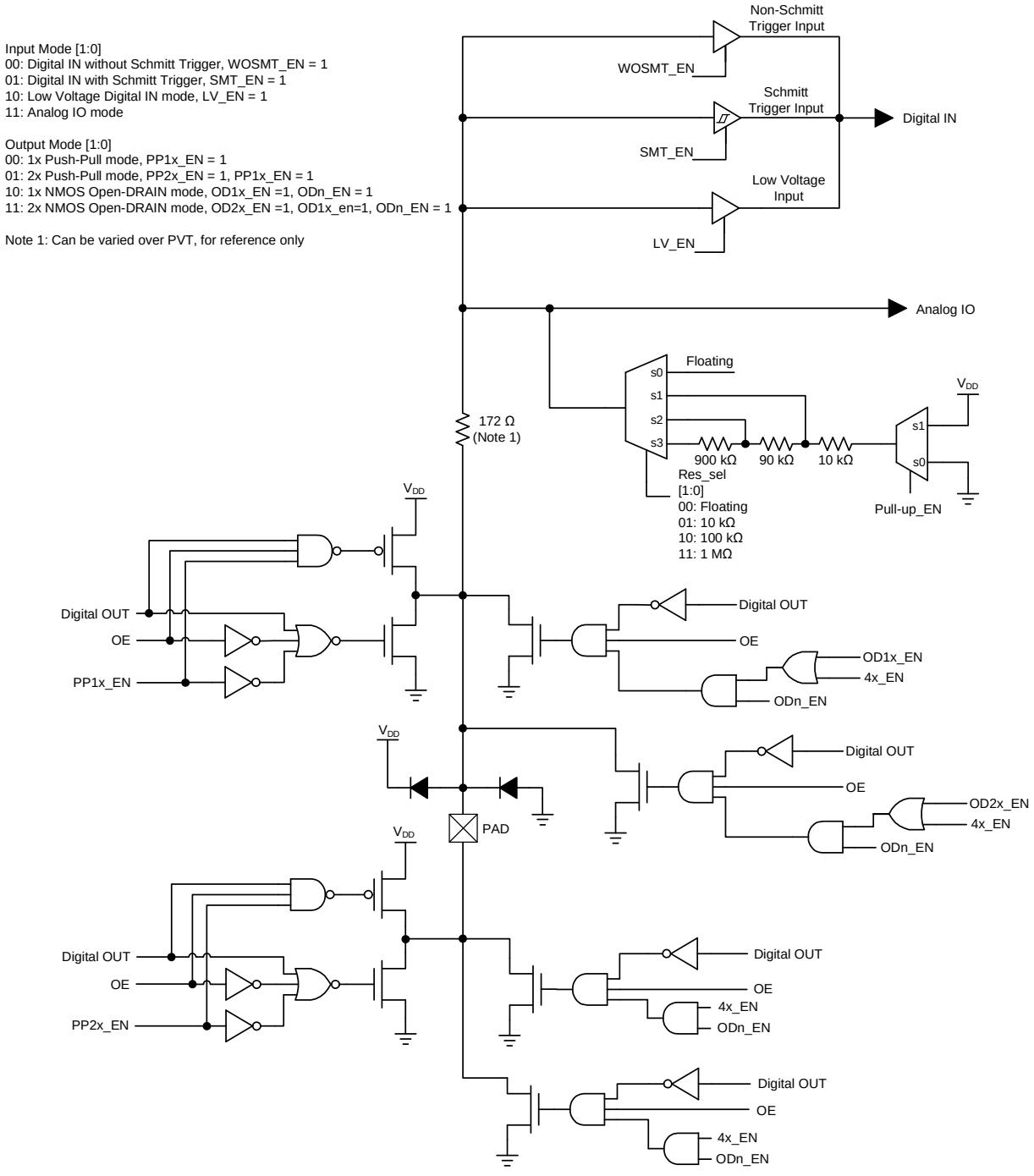


Figure 5. Matrix OE IO 4x Drive Structure Diagram

7.7 Register OE IO Structure

7.7.1 Register OE IO Structure (for Pins 4, 6, 8)

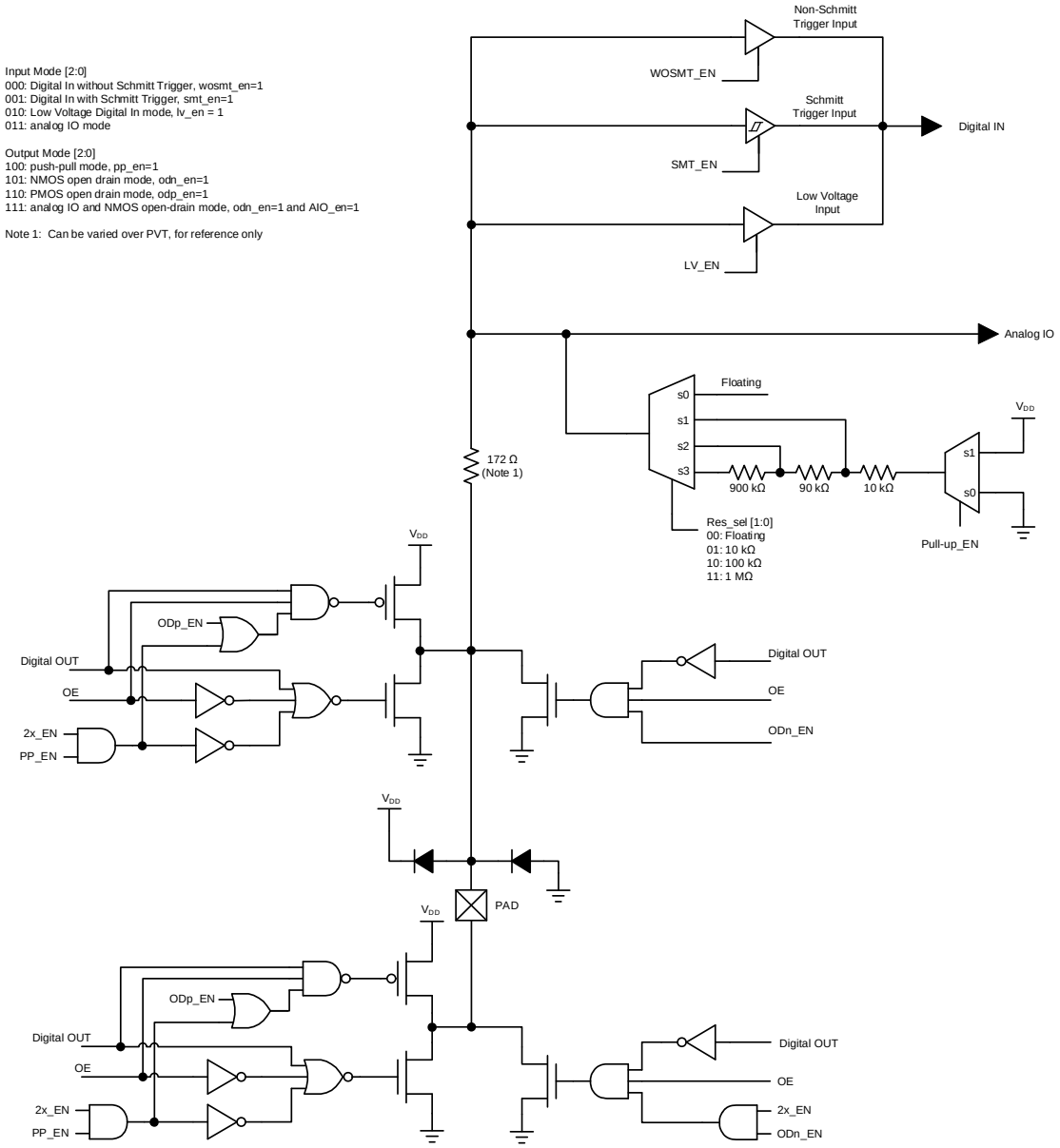


Figure 6. Register OE IO Structure Diagram

7.7.2 Register OE IO Structure (for Pins 15, 17, 20)

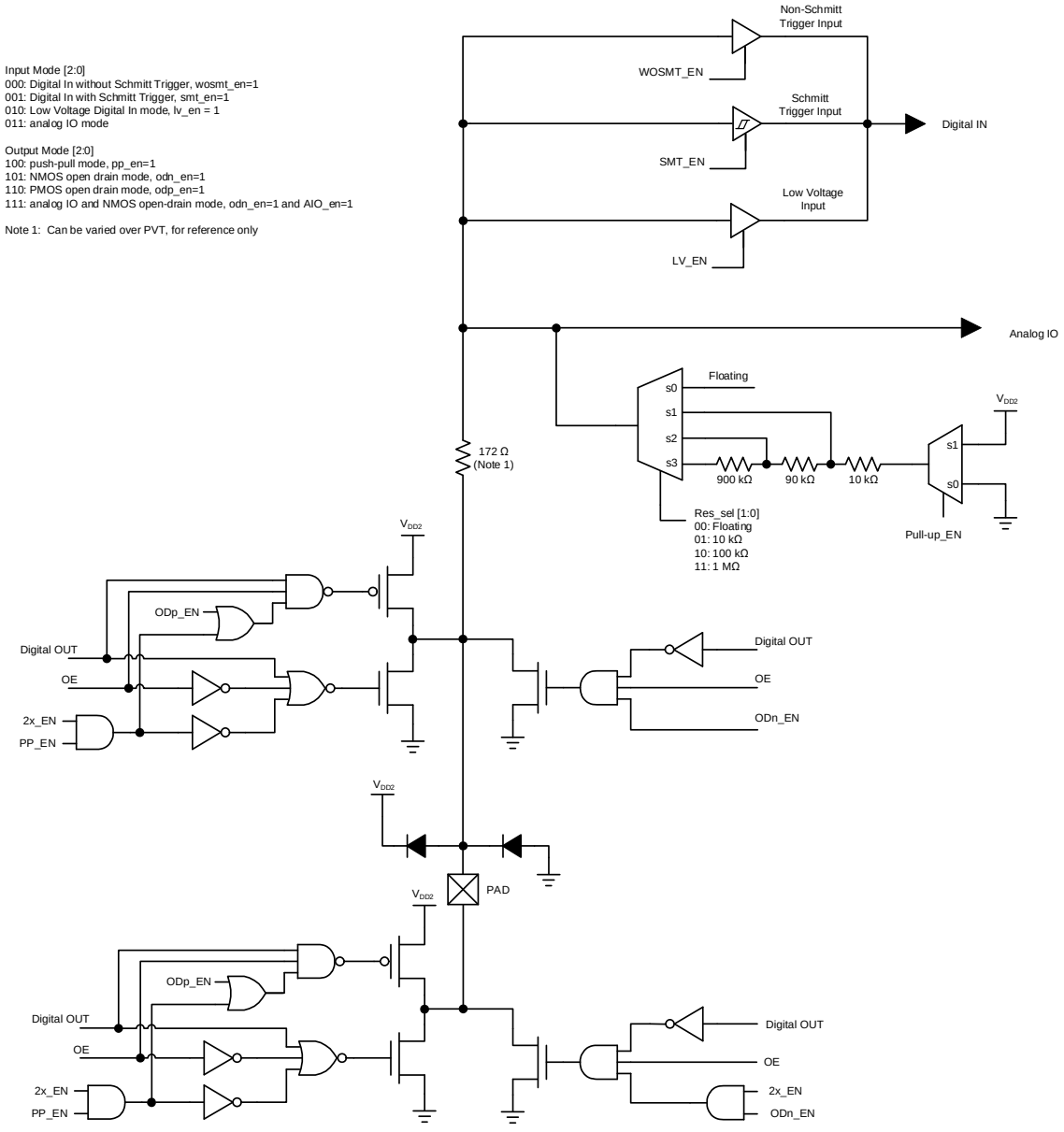


Figure 7. Register OE IO Structure Diagram

7.7.3 Register OE 4x Drive Structure (for Pin 12)

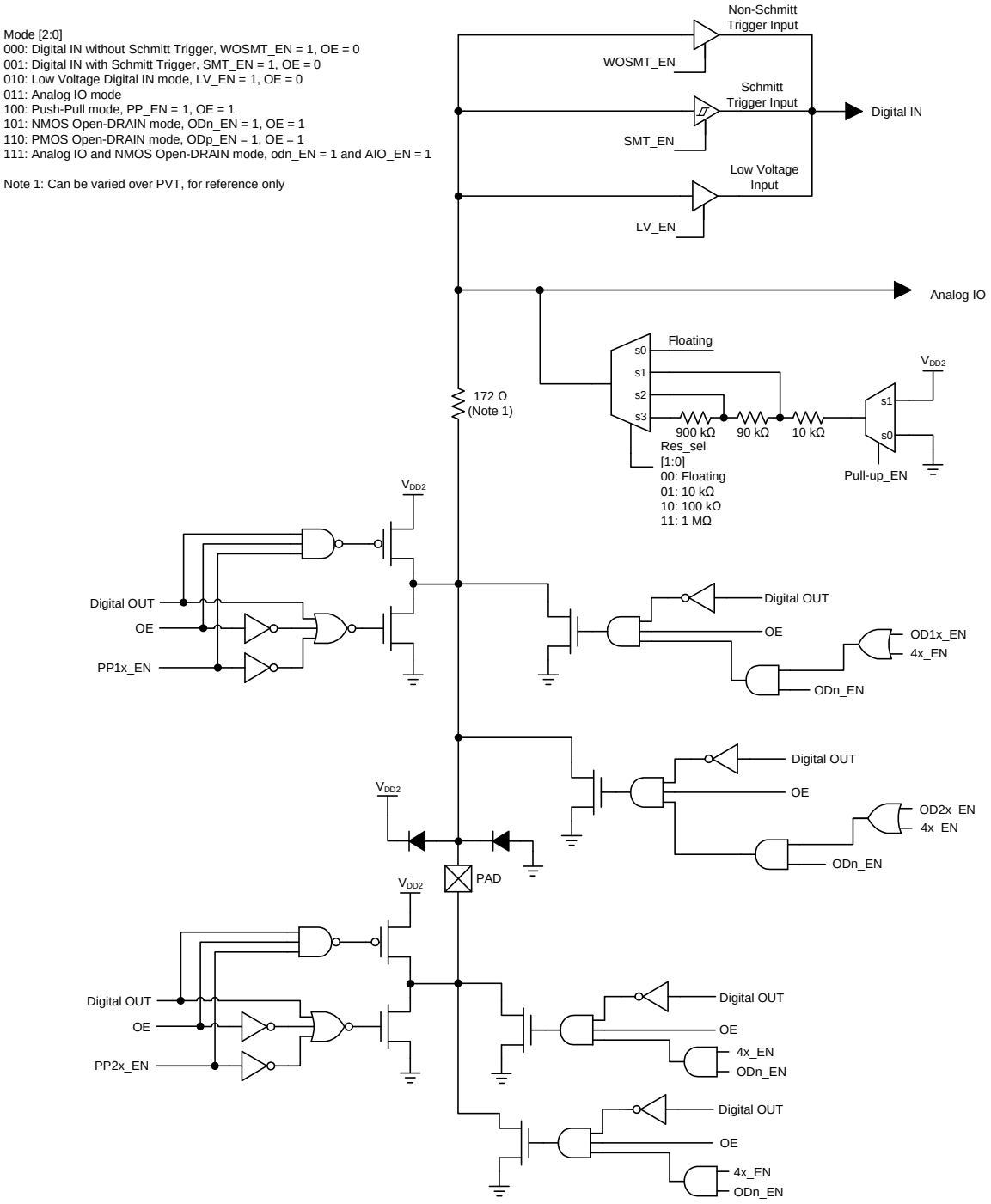


Figure 8. Matrix OE IO 4x Drive Structure Diagram

8.0 Connection Matrix

The SLG46621 has two Connection Matrices, which are used to create the internal routing for internal digital signals inside the device, once it is programmed. The registers are programmed from the one-time NVM cells during Test Mode Operation. All of the connection points for each logic cell within the SLG46621 has a specific digital bit code assigned to it that is either set to active “High” or inactive “Low” based on the design that is created. Once the 2048 register bits within the SLG46621 are programmed, a fully custom circuit will be created.

Each Connection Matrix within the device has 64 inputs and 95 outputs. Each of the 64 inputs to each Connection Matrix is hard-wired to the digital output of a particular source macrocell, including I/O pins, LUTs, ADC, analog comparators, other digital macrocells and VDD and VSS. The input to a digital macrocell uses a 6-bit register to select one of these 64 input lines. All macrocells associated with a particular matrix has both its inputs and outputs connected to that matrix. To make connections to macrocells associated with the other matrix, the user can select the Matrix Cross Connection lines (see below)

Each matrix has 10 dedicated output connections for connecting to the other matrix, known as the “Cross Connection “outputs. When using these cross connections, any macrocell can connected to any other macrocell in the device by first going through the other matrix. As there are a fixed number of the Matrix Cross Connections, it is important when making connections of the outputs of macrocells to the inputs of other macrocells that this is done within the same matrix whenever possible. This will leave the Matrix Cross Connection lines free for digital connections to resources associated with the other matrix.

For a complete list of the SLG46621’s register table, see Section *25.0 Appendix A - SLG46621 Register Definition*

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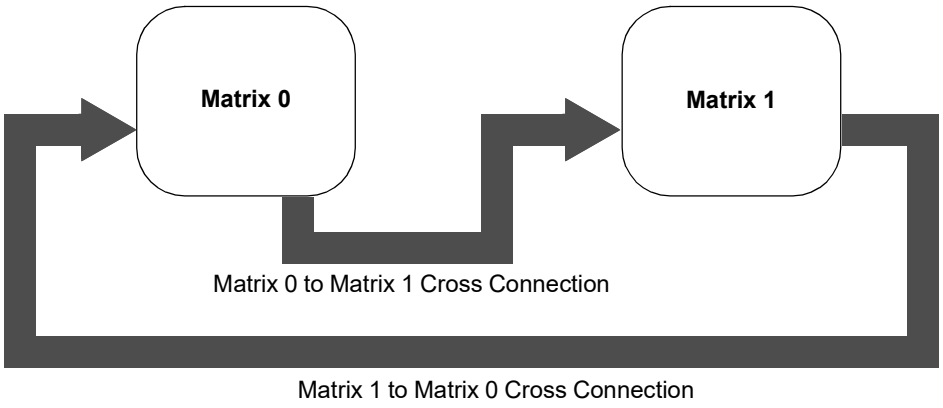
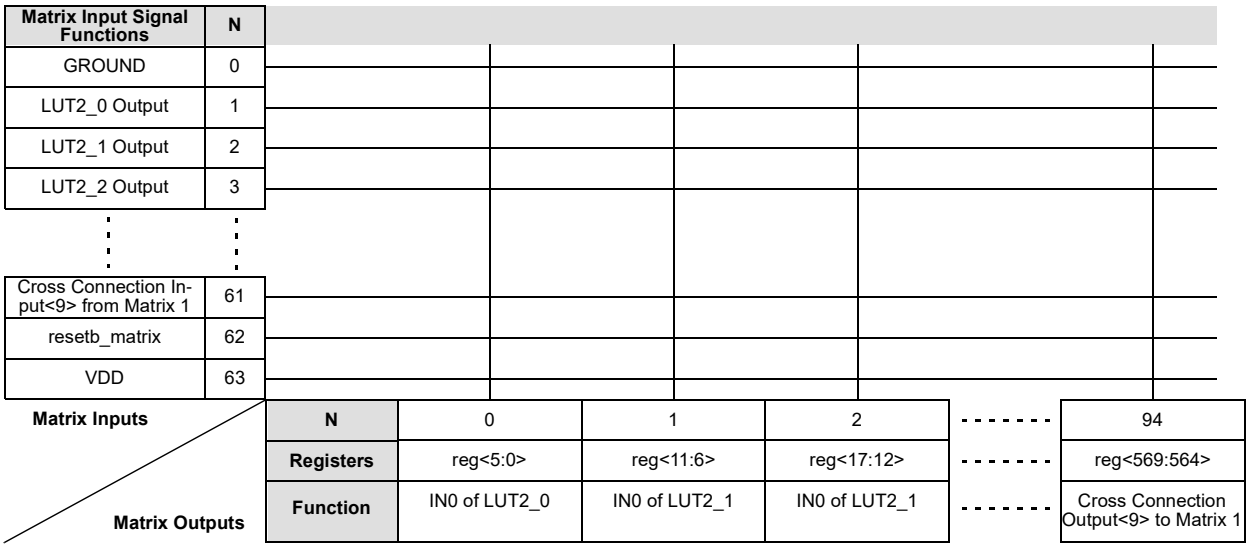


Figure 9. Matrix Cross Connection Block Diagram

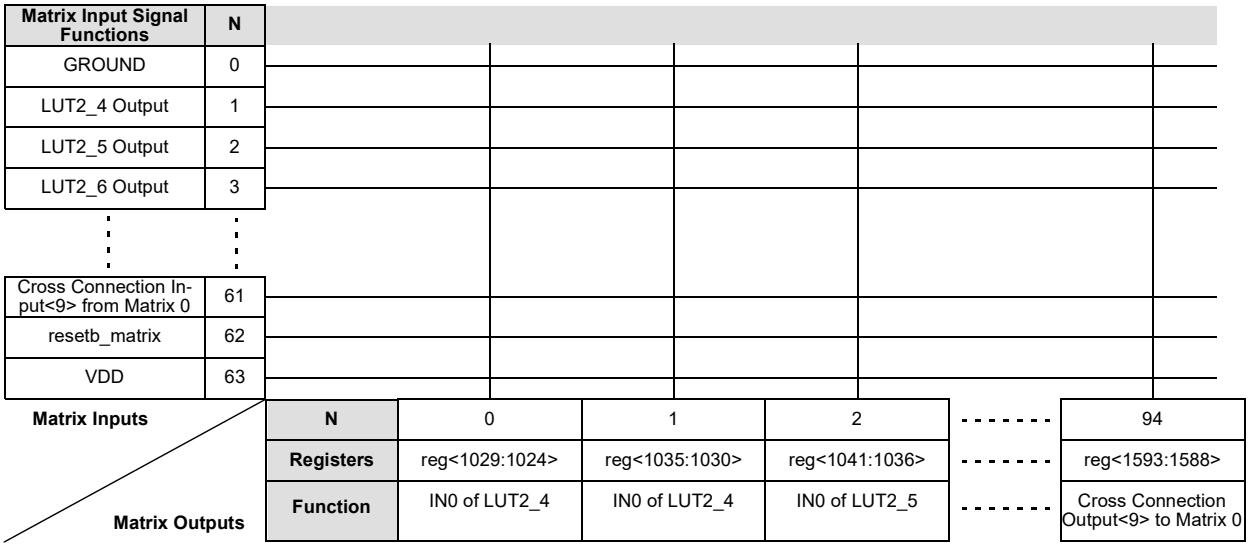


Matrix Input Signal Functions	N
GROUND	0
LUT2_0 Output	1
LUT2_1 Output	2
LUT2_2 Output	3
⋮	⋮
Cross Connection Input<9> from Matrix 1	61
resetb_matrix	62
VDD	63

Matrix Inputs / Matrix Outputs

N	0	1	2	⋯	94
Registers	reg<5:0>	reg<11:6>	reg<17:12>	⋯	reg<569:564>
Function	IN0 of LUT2_0	IN0 of LUT2_1	IN0 of LUT2_1	⋯	Cross Connection Output<9> to Matrix 1

Figure 10. Connection Matrix 0



Matrix Input Signal Functions	N
GROUND	0
LUT2_4 Output	1
LUT2_5 Output	2
LUT2_6 Output	3
⋮	⋮
Cross Connection Input<9> from Matrix 0	61
resetb_matrix	62
VDD	63

Matrix Inputs / Matrix Outputs

N	0	1	2	⋯	94
Registers	reg<1029:1024>	reg<1035:1030>	reg<1041:1036>	⋯	reg<1593:1588>
Function	IN0 of LUT2_4	IN0 of LUT2_4	IN0 of LUT2_5	⋯	Cross Connection Output<9> to Matrix 0

Figure 11. Connection Matrix 1

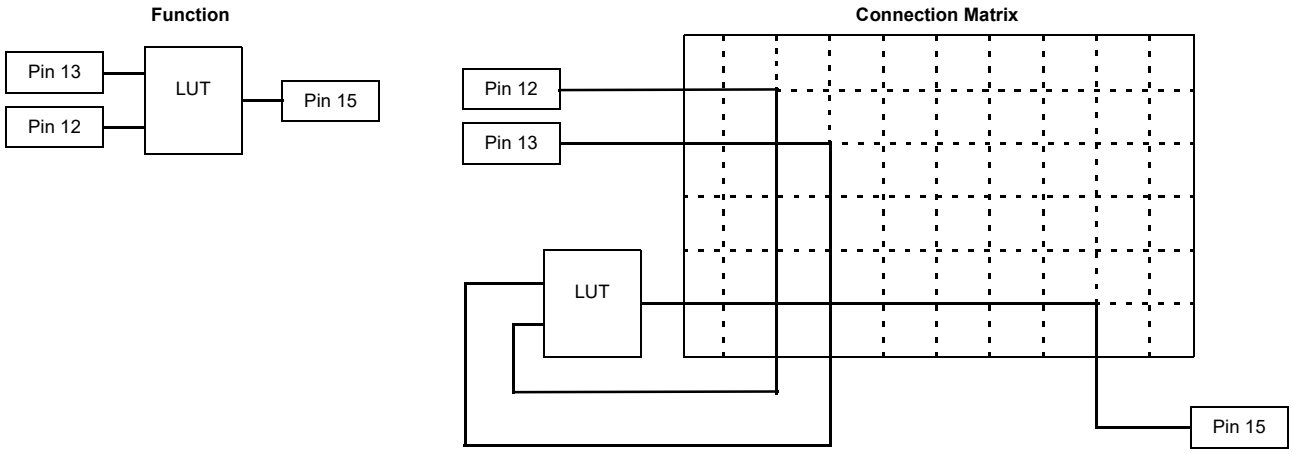


Figure 12. Connection Matrix Example

8.1 Matrix Input 0 Table

Table 37. Matrix 0 Input Table

N	Matrix 0 Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
0	GROUND	0	0	0	0	0	0
1	LUT2_0 Output	0	0	0	0	0	1
2	LUT2_1 Output	0	0	0	0	1	0
3	LUT2_2 Output	0	0	0	0	1	1
4	LUT2_3 Output	0	0	0	1	0	0
5	LUT3_0 Output	0	0	0	1	0	1
6	LUT3_1 Output	0	0	0	1	1	0
7	LUT3_2 Output	0	0	0	1	1	1
8	LUT3_3 Output	0	0	1	0	0	0
9	LUT3_4 Output	0	0	1	0	0	1
10	LUT3_5 Output	0	0	1	0	1	0
11	LUT3_6 Output	0	0	1	0	1	1
12	LUT3_7 Output	0	0	1	1	0	0
13	LUT4_0/PGEN Output	0	0	1	1	0	1
14	DFF0/LATCH0 Output	0	0	1	1	1	0
15	DFF1/LATCH1 Output	0	0	1	1	1	1
16	DFF2/LATCH2 Output	0	1	0	0	0	0
17	DFF3/LATCH3 Output	0	1	0	0	0	1
18	DFF4/LATCH4 Output	0	1	0	0	1	0
19	DFF5/LATCH5 Output	0	1	0	0	1	1
20	Pipe Delay 0 Out0	0	1	0	1	0	0
21	Pipe Delay 0 Out1	0	1	0	1	0	1
22	Edge Detect Programmable Delay 0 Output	0	1	0	1	1	0
23	Inverter 0 Output	0	1	0	1	1	1
24	Pin2 Digital Output	0	1	1	0	0	0
25	Pin3 Digital Output	0	1	1	0	0	1
26	Pin4 Digital Output	0	1	1	0	1	0
27	Pin5 Digital Output	0	1	1	0	1	1
28	Pin6 Digital Output	0	1	1	1	0	0
29	Pin7 Digital Output	0	1	1	1	0	1
30	Pin8 Digital Output	0	1	1	1	1	0
31	Pin9 Digital Output	0	1	1	1	1	1
32	Pin10 Digital Output	1	0	0	0	0	0
33	ACMP0 Output	1	0	0	0	0	1
34	ACMP4 Output	1	0	0	0	1	0
35	ACMP5 Output	1	0	0	0	1	1
36	DLY0/CNT0 Output	1	0	0	1	0	0
37	DLY2/CNT2 Output	1	0	0	1	0	1

Table 37. Matrix 0 Input Table

N	Matrix 0 Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
38	DLY5/CNT5 Output	1	0	0	1	1	0
39	DLY6/CNT6 Output	1	0	0	1	1	1
40	DLY9/CNT9 Output	1	0	1	0	0	0
41	Sig_BG_OK	1	0	1	0	0	1
42	Power Detector Output	1	0	1	0	1	0
43	ADC interrupt	1	0	1	0	1	1
44	SPI interrupt	1	0	1	1	0	0
45	GROUND	1	0	1	1	0	1
46	GROUND	1	0	1	1	1	0
47	GROUND	1	0	1	1	1	1
48	Ring Oscillator Output	1	1	0	0	0	0
49	RC Oscillator Output	1	1	0	0	0	1
50	Low Frequency Oscillator Output	1	1	0	0	1	0
51	GROUND	1	1	0	0	1	1
52	Cross Connection Input from Matrix 1 <0>	1	1	0	1	0	0
53	Cross Connection Input from Matrix 1 <1>	1	1	0	1	0	1
54	Cross Connection Input from Matrix 1 <2>	1	1	0	1	1	0
55	Cross Connection Input from Matrix 1 <3>	1	1	0	1	1	1
56	Cross Connection Input from Matrix 1 <4>	1	1	1	0	0	0
57	Cross Connection Input from Matrix 1 <5>	1	1	1	0	0	1
58	Cross Connection Input from Matrix 1 <6>	1	1	1	0	1	0
59	Cross Connection Input from Matrix 1 <7>	1	1	1	0	1	1
60	Cross Connection Input from Matrix 1 <8>	1	1	1	1	0	0
61	Cross Connection Input from Matrix 1 <9>	1	1	1	1	0	1
62	Resetb_Matrix	1	1	1	1	1	0
63	VDD	1	1	1	1	1	1

8.2 Matrix 0 Output Table

Table 38. Matrix 0 Output Table

Register Bit Address	Matrix 0 Output Signal Function	Matrix Output Number
reg<5:0>	Matrix 0 Out: In0 of LUT2_0	0
reg<11:6>	Matrix 0 Out: In1 of LUT2_0	1
reg<17:12>	Matrix 0 Out: In0 of LUT2_1	2
reg<23:18>	Matrix 0 Out: In1 of LUT2_1	3
reg<29:24>	Matrix 0 Out: In0 of LUT2_2	4
reg<35:30>	Matrix 0 Out: In1 of LUT2_2	5
reg<41:36>	Matrix 0 Out: In0 of LUT2_3	6
reg<47:42>	Matrix 0 Out: In1 of LUT2_3	7
reg<53:48>	Matrix 0 Out: In0 of LUT3_0	8
reg<59:54>	Matrix 0 Out: In1 of LUT3_0	9
reg<65:60>	Matrix 0 Out: In2 of LUT3_0	10
reg<71:66>	Matrix 0 Out: In0 of LUT3_1	11
reg<77:72>	Matrix 0 Out: In1 of LUT3_1	12
reg<83:78>	Matrix 0 Out: In2 of LUT3_1	13
reg<89:84>	Matrix 0 Out: In0 of LUT3_2	14
reg<95:90>	Matrix 0 Out: In1 of LUT3_2	15
reg<101:96>	Matrix 0 Out: In2 of LUT3_2	16
reg<107:102>	Matrix 0 Out: In0 of LUT3_3	17
reg<113:108>	Matrix 0 Out: In1 of LUT3_3	18
reg<119:114>	Matrix 0 Out: In2 of LUT3_3	19
reg<125:120>	Matrix 0 Out: In0 of LUT3_4	20
reg<131:126>	Matrix 0 Out: In1 of LUT3_4	21
reg<137:132>	Matrix 0 Out: In2 of LUT3_4	22
reg<143:138>	Matrix 0 Out: In0 of LUT3_5	23
reg<149:144>	Matrix 0 Out: In1 of LUT3_5	24
reg<155:150>	Matrix 0 Out: In2 of LUT3_5	25
reg<161:156>	Matrix 0 Out: In0 of LUT3_6	26
reg<167:162>	Matrix 0 Out: In1 of LUT3_6	27
reg<173:168>	Matrix 0 Out: In2 of LUT3_6	28
reg<179:174>	Matrix 0 Out: In0 of LUT3_7	29
reg<185:180>	Matrix 0 Out: In1 of LUT3_7	30
reg<191:186>	Matrix 0 Out: In2 of LUT3_7	31
reg<197:192>	Matrix 0 Out: In0 of LUT4_0	32
reg<203:198>	Matrix 0 Out: In1 of LUT4_0	33
reg<209:204>	Matrix 0 Out: In2 of LUT4_0 or PGEN CLK	34
reg<215:210>	Matrix 0 Out: In3 of LUT4_0 or PGEN ResetB	35
reg<221:216>	Matrix 0 Out: Set or Resetb of DFF0/Latch0	36
reg<227:222>	Matrix 0 Out: Data of DFF0/Latch0	37
reg<233:228>	Matrix 0 Out: Clock of DFF0/Latch0	38

Table 38. Matrix 0 Output Table

Register Bit Address	Matrix 0 Output Signal Function	Matrix Output Number
reg<239:234>	Matrix 0 Out: Set or Resetb of DFF1/Latch1	39
reg<245:240>	Matrix 0 Out: Data of DFF1/Latch1	40
reg<251:246>	Matrix 0 Out: Clock of DFF1/Latch1	41
reg<257:252>	Matrix 0 Out: Set or Resetb of DFF2/Latch2	42
reg<263:258>	Matrix 0 Out: Data of DFF2/Latch2	43
reg<269:264>	Matrix 0 Out: Clock of DFF2/Latch2	44
reg<275:270>	Matrix 0 Out: Data of DFF3/Latch3	45
reg<281:276>	Matrix 0 Out: Clock of DFF3/Latch3	46
reg<287:282>	Matrix 0 Out: Data of DFF4/Latch4	47
reg<293:288>	Matrix 0 Out: Clock of DFF4/Latch4	48
reg<299:294>	Matrix 0 Out: Data of DFF5/Latch5	49
reg<305:300>	Matrix 0 Out: Clock of DFF5/Latch5	50
reg<311:306>	Matrix 0 Out: Clock of Pipe Delay 0	51
reg<317:312>	Matrix 0 Out: Input Data of Pipe Delay 0	52
reg<323:318>	Matrix 0 Out: Reset of Pipe Delay 0	53
reg<329:324>	Matrix 0 Out: Input of Edge Detector and Programmable Delay 0	54
reg<335:330>	Matrix 0 Out: Input of Inverter 0	55
reg<341:336>	Matrix 0 Out: Digital Output of Pin3	56
reg<347:342>	Matrix 0 Out: OE of Pin3	57
reg<353:348>	Matrix 0 Out: Digital Output of Pin4	58
reg<359:354>	Matrix 0 Out: Digital Output of Pin5	59
reg<365:360>	Matrix 0 Out: OE of Pin5	60
reg<371:366>	Matrix 0 Out: Digital Output of Pin6	61
reg<377:372>	Matrix 0 Out: Digital Output of Pin7	62
reg<383:378>	Matrix 0 Out: OE of Pin7	63
reg<389:384>	Matrix 0 Out: Digital Output of Pin8	64
reg<395:390>	Matrix 0 Out: Digital Output of Pin9	65
reg<401:396>	Matrix 0 Out: OE of Pin9	66
reg<407:402>	Matrix 0 Out: Digital Output of Pin10	67
reg<413:408>	Matrix 0 Out: OE of Pin10	68
reg<419:414>	Matrix 0 Out: PDB(Power Down) for ACMP0	69
reg<425:420>	Matrix 0 Out: PDB(Power Down) for ACMP4	70
reg<431:426>	Matrix 0 Out: PDB(Power Down) for ACMP5	71
reg<437:432>	Matrix 0 Out: CNT0/CNT2/CNT9/ External Clock(CLK_Matrix0)	72
reg<443:438>	Matrix 0 Out: CNT5/CNT6 External Clock (CLK_Matrix1)	73
reg<449:444>	Matrix 0 Out: Input of DLY/CNT0	74
reg<455:450>	Matrix 0 Out: Input of DLY/CNT2	75
reg<461:456>	Matrix 0 Out: Keep of DLY/CNT2	76
reg<467:462>	Matrix 0 Out: Up of DLY/CNT2	77
reg<473:468>	Matrix 0 Out: Input of DLY/CNT5	78

Table 38. Matrix 0 Output Table

Register Bit Address	Matrix 0 Output Signal Function	Matrix Output Number
reg<479:474>	Matrix 0 Out: Input of DLY/CNT6	79
reg<485:480>	Matrix 0 Out: Input of DLY/CNT9	80
reg<491:486>	Matrix 0 Out: ADC Power Down	81
reg<497:492>	Matrix 0 Out: CSB of SPI	82
reg<503:498>	Matrix 0 Out: SCLK of SPI	83
reg<509:504>	Matrix 0 Out: Oscillator Power Down	84
reg<515:510>	Matrix 0 Out: Cross Connection Output to Matrix 1 <0>	85
reg<521:516>	Matrix 0 Out: Cross Connection Output to Matrix 1 <1>	86
reg<527:522>	Matrix 0 Out: Cross Connection Output to Matrix 1 <2>	87
reg<533:528>	Matrix 0 Out: Cross Connection Output to Matrix 1 <3>	88
reg<539:534>	Matrix 0 Out: Cross Connection Output to Matrix 1 <4>	89
reg<545:540>	Matrix 0 Out: Cross Connection Output to Matrix 1 <5>	90
reg<551:546>	Matrix 0 Out: Cross Connection Output to Matrix 1 <6>	91
reg<557:552>	Matrix 0 Out: Cross Connection Output to Matrix 1 <7>	92
reg<563:558>	Matrix 0 Out: Cross Connection Output to Matrix 1 <8>	93
reg<569:564>	Matrix 0 Out: Cross Connection Output to Matrix 1 <9>	94

8.3 Matrix Input 1 Table

Table 39. Matrix 1 Input Table

N	Matrix 1 Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
0	GROUND	0	0	0	0	0	0
1	LUT2_4 Output	0	0	0	0	0	1
2	LUT2_5 Output	0	0	0	0	1	0
3	LUT2_6 Output	0	0	0	0	1	1
4	LUT2_7 Output	0	0	0	1	0	0
5	LUT3_8 Output	0	0	0	1	0	1
6	LUT3_9 Output	0	0	0	1	1	0
7	LUT3_10 Output	0	0	0	1	1	1
8	LUT3_11 Output	0	0	1	0	0	0
9	LUT3_12 Output	0	0	1	0	0	1
10	LUT3_13 Output	0	0	1	0	1	0
11	LUT3_14 Output	0	0	1	0	1	1
12	LUT3_15 Output	0	0	1	1	0	0
13	LUT4_1 Output	0	0	1	1	0	1
14	DFF6/LATCH6 Output	0	0	1	1	1	0
15	DFF7/LATCH7 Output	0	0	1	1	1	1
16	DFF8/LATCH8 Output	0	1	0	0	0	0
17	DFF9/LATCH9 Output	0	1	0	0	0	1
18	DFF10/LATCH10 Output	0	1	0	0	1	0
19	DFF11/LATCH11 Output	0	1	0	0	1	1
20	Pipe Delay 1 Out0	0	1	0	1	0	0
21	Pipe Delay 1 Out1	0	1	0	1	0	1
22	Edge Detect Programmable Delay 1 Output	0	1	0	1	1	0
23	Inverter 1 Output	0	1	0	1	1	1
24	Pin12 Digital Output	0	1	1	0	0	0
25	Pin13 Digital Output	0	1	1	0	0	1
26	Reserved	0	1	1	0	1	0
27	Pin15 Digital Output	0	1	1	0	1	1
28	Pin16 Digital Output	0	1	1	1	0	0
29	Pin17 Digital Output	0	1	1	1	0	1
30	Pin18 Digital Output	0	1	1	1	1	0
31	Pin19 Digital Output	0	1	1	1	1	1
32	Pin20 Digital Output	1	0	0	0	0	0
33	ACMP1 Output	1	0	0	0	0	1
34	ACMP2 Output	1	0	0	0	1	0
35	ACMP3 Output	1	0	0	0	1	1
36	DLY1/CNT1 Output	1	0	0	1	0	0
37	DLY3/CNT3 Output	1	0	0	1	0	1

Table 39. Matrix 1 Input Table

N	Matrix 1 Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
38	DLY4/CNT4 Output	1	0	0	1	1	0
39	DLY7/CNT7 Output	1	0	0	1	1	1
40	DLY8/CNT8 Output	1	0	1	0	0	0
41	Sig_BG_OK	1	0	1	0	0	1
42	PWM0_DCMP0_Outn	1	0	1	0	1	0
43	PWM0_DCMP0_Out_positive	1	0	1	0	1	1
44	PWM1_DCMP1_Out_negative/SPI_Out<0>	1	0	1	1	0	0
45	PWM1_DCMP1_Out_positive/SPI_Out<1>	1	0	1	1	0	1
46	PWM2_DCMP2_Out_negative/SPI_Out<2>	1	0	1	1	1	0
47	PWM2_DCMP2_Out_positive/SPI_Out<3>	1	0	1	1	1	1
48	Ring Oscillator Output/SPI_Out<4>	1	1	0	0	0	0
49	RC Oscillator Output/SPI_Out<5>	1	1	0	0	0	1
50	Low Frequency Oscillator Output/SPI_Out<6>	1	1	0	0	1	0
51	GROUND/SPI_Out<7>	1	1	0	0	1	1
52	Cross Connection Input from Matrix 0 <0>	1	1	0	1	0	0
53	Cross Connection Input from Matrix 0 <1>	1	1	0	1	0	1
54	Cross Connection Input from Matrix 0 <2>	1	1	0	1	1	0
55	Cross Connection Input from Matrix 0 <3>	1	1	0	1	1	1
56	Cross Connection Input from Matrix 0 <4>	1	1	1	0	0	0
57	Cross Connection Input from Matrix 0 <5>	1	1	1	0	0	1
58	Cross Connection Input from Matrix 0 <6>	1	1	1	0	1	0
59	Cross Connection Input from Matrix 0 <7>	1	1	1	0	1	1
60	Cross Connection Input from Matrix 0 <8>	1	1	1	1	0	0
61	Cross Connection Input from Matrix 0 <9>	1	1	1	1	0	1
62	Resetb_Matrix	1	1	1	1	1	0
63	VDD	1	1	1	1	1	1

8.4 Matrix 1 Output Table

Table 40. Matrix 1 Output Table

Register Bit Address	Matrix 1 Output Signal Function	Matrix Output Number
reg<1029:1024>	Matrix 1 Out: In0 of LUT2_4	0
reg<1035:1030>	Matrix 1 Out: In1 of LUT2_4	1
reg<1041:1036>	Matrix 1 Out: In0 of LUT2_5	2
reg<1047:1042>	Matrix 1 Out: In1 of LUT2_5	3
reg<1053:1048>	Matrix 1 Out: In0 of LUT2_6	4
reg<1059:1054>	Matrix 1 Out: In1 of LUT2_6	5
reg<1065:1060>	Matrix 1 Out: In0 of LUT2_7	6
reg<1071:1066>	Matrix 1 Out: In1 of LUT2_7	7
reg<1077:1072>	Matrix 1 Out: In0 of LUT3_8	8
reg<1083:1078>	Matrix 1 Out: In1 of LUT3_8	9
reg<1089:1084>	Matrix 1 Out: In2 of LUT3_8	10
reg<1095:1090>	Matrix 1 Out: In0 of LUT3_9	11
reg<1101:1096>	Matrix 1 Out: In1 of LUT3_9	12
reg<1107:1102>	Matrix 1 Out: In2 of LUT3_9	13
reg<1113:1108>	Matrix 1 Out: In0 of LUT3_10	14
reg<1119:1114>	Matrix 1 Out: In1 of LUT3_10	15
reg<1125:1120>	Matrix 1 Out: In2 of LUT3_10	16
reg<1131:1126>	Matrix 1 Out: In0 of LUT3_11	17
reg<1137:1132>	Matrix 1 Out: In1 of LUT3_11	18
reg<1143:1138>	Matrix 1 Out: In2 of LUT3_11	19
reg<1149:1144>	Matrix 1 Out: In0 of LUT3_12	20
reg<1155:1150>	Matrix 1 Out: In1 of LUT3_12	21
reg<1161:1156>	Matrix 1 Out: In2 of LUT3_12	22
reg<1167:1162>	Matrix 1 Out: In0 of LUT3_13	23
reg<1173:1168>	Matrix 1 Out: In1 of LUT3_13	24
reg<1179:1174>	Matrix 1 Out: In2 of LUT3_13	25
reg<1185:1180>	Matrix 1 Out: In0 of LUT3_14	26
reg<1191:1186>	Matrix 1 Out: In1 of LUT3_14	27
reg<1197:1192>	Matrix 1 Out: In2 of LUT3_14	28
reg<1203:1198>	Matrix 1 Out: In0 of LUT3_15	29
reg<1209:1204>	Matrix 1 Out: In1 of LUT3_15	30
reg<1215:1210>	Matrix 1 Out: In2 of LUT3_15	31
reg<1221:1216>	Matrix 1 Out: In0 of LUT4_1	32
reg<1227:1222>	Matrix 1 Out: In1 of LUT4_1	33
reg<1233:1228>	Matrix 1 Out: In2 of LUT4_1	34
reg<1239:1234>	Matrix 1 Out: In3 of LUT4_1	35
reg<1245:1240>	Matrix 1 Out: Set or Resetb of DFF6/Latch6	36
reg<1251:1246>	Matrix 1 Out: Data of DFF6/Latch6	37
reg<1257:1252>	Matrix 1 Out: Clock of DFF6/Latch6	38

Table 40. Matrix 1 Output Table

Register Bit Address	Matrix 1 Output Signal Function	Matrix Output Number
reg<1263:1258>	Matrix 1 Out: Set or Resetb of DFF7/Latch7	39
reg<1269:1264>	Matrix 1 Out: Data of DFF7/Latch7	40
reg<1275:1270>	Matrix 1 Out: Clock of DFF7/Latch7	41
reg<1281:1276>	Matrix 1 Out: Set or Resetb of DFF8/Latch8	42
reg<1287:1282>	Matrix 1 Out: Data of DFF8/Latch8	43
reg<1293:1288>	Matrix 1 Out: Clock of DFF8/Latch8	44
reg<1299:1294>	Matrix 1 Out: Data of DFF9/Latch9	45
reg<1305:1300>	Matrix 1 Out: Clock of DFF9/Latch9	46
reg<1311:1306>	Matrix 1 Out: Data of DFF10/Latch10	47
reg<1317:1312>	Matrix 1 Out: Clock of DFF10/Latch10	48
reg<1323:1318>	Matrix 1 Out: Data of DFF11/Latch11	49
reg<1329:1324>	Matrix 1 Out: Clock of DFF11/Latch11	50
reg<1335:1330>	Matrix 1 Out: Clock of Pipe Delay 1	51
reg<1341:1336>	Matrix 1 Out: Input Data of Pipe Delay 1	52
reg<1347:1342>	Matrix 1 Out: Reset of Pipe Delay 1	53
reg<1353:1348>	Matrix 1 Out: Input of Edge Detector and Programmable Delay 1	54
reg<1359:1354>	Matrix 1 Out: Input of Inverter 1	55
reg<1365:1360>	Matrix 1 Out: Digital Output of PIN 12	56
reg<1371:1366>	Matrix 1 Out: Digital Output of PIN 13	57
reg<1377:1372>	Matrix 1 Out: OE of PIN 13	58
reg<1383:1378>	Reserved	59
reg<1389:1384>	Reserved	60
reg<1395:1390>	Matrix 1 Out: Digital Output of PIN 15	61
reg<1401:1396>	Matrix 1 Out: Digital Output of PIN 16	62
reg<1407:1402>	Matrix 1 Out: OE of PIN 16	63
reg<1413:1408>	Matrix 1 Out: Digital Output of PIN 17	64
reg<1419:1414>	Matrix 1 Out: Digital Output of PIN 18	65
reg<1425:1420>	Matrix 1 Out: OE of PIN 18	66
reg<1431:1426>	Matrix 1 Out: Digital Output of PIN 19	67
reg<1437:1432>	Matrix 1 Out: OE of PIN 19	68
reg<1443:1438>	Matrix 1 Out: Digital Output of PIN 20	69
reg<1449:1444>	Matrix 1 Out: PDB(Power Down) for ACMP1	70
reg<1455:1450>	Matrix 1 Out: PDB(Power Down) for ACMP2	71
reg<1461:1456>	Matrix 1 Out: PDB(Power Down) for ACMP3	72
reg<1467:1462>	Matrix 1 Out: CNT7/CNT8/PWM/ADC External Clock (CLK_Matrix2)	73
reg<1473:1468>	Matrix 1 Out: CNT1/CNT3/CNT4 External Clock (CLK_Matrix3)	74
reg<1479:1474>	Matrix 1 Out: Input of DLY/CNT1	75
reg<1485:1480>	Matrix 1 Out: Input of DLY/CNT3	76
reg<1491:1486>	Matrix 1 Out: Input of DLY/CNT4	77
reg<1497:1492>	Matrix 1 Out: Keep of DLY/CNT4	78

Table 40. Matrix 1 Output Table

Register Bit Address	Matrix 1 Output Signal Function	Matrix Output Number
reg<1503:1498>	Matrix 1 Out: Up of DLY/CNT4	79
reg<1509:1504>	Matrix 1 Out: Input of DLY/CNT7	80
reg<1515:1510>	Matrix 1 Out: Input of DLY/CNT8	81
reg<1521:1516>	Matrix 1 Out: PWM Power Down	82
reg<1527:1522>	Matrix 1 Out: PWM/DCMP0 Positive Input and PWM/DCMP1 Negative Input Register Selection Bit 0	83
reg<1533:1528>	Matrix 1 Out: PWM/DCMP0 Positive Input and PWM/DCMP1 Negative Input Register Selection Bit 1	84
reg<1539:1534>	Matrix 1 Out: Cross Connection Output to Matrix 0 <0>	85
reg<1545:1540>	Matrix 1 Out: Cross Connection Output to Matrix 0 <1>	86
reg<1551:1546>	Matrix 1 Out: Cross Connection Output to Matrix 0 <2>	87
reg<1557:1552>	Matrix 1 Out: Cross Connection Output to Matrix 0 <3>	88
reg<1563:1558>	Matrix 1 Out: Cross Connection Output to Matrix 0 <4>	89
reg<1569:1564>	Matrix 1 Out: Cross Connection Output to Matrix 0 <5>	90
reg<1575:1570>	Matrix 1 Out: Cross Connection Output to Matrix 0 <6>	91
reg<1581:1576>	Matrix 1 Out: Cross Connection Output to Matrix 0 <7>	92
reg<1587:1582>	Matrix 1 Out: Cross Connection Output to Matrix 0 <8>	93
reg<1593:1588>	Matrix 1 Out: Cross Connection Output to Matrix 0 <9>	94
reg<1599:1594>	Reserved	

9.0 8-bit SAR ADC Analog-to-Digital Converter (ADC)

The Analog to Digital Converter in the SLG46621 is an 8-bit Successive Approximation Register Analog to Digital Converter (SAR ADC) which operates at a sampling speed of 100 kHz. The ADC's DNL < ± 0.5 LSB and INL < ± 3.4 LSB and has a ADC V_{REF} accuracy of ± 50 mV. The ADC consists of two parts: PGA which provides signal amplification and conditioning and SAR ADC which handles analog to digital conversion. PGA can be used as amplifier when ADC is disabled. Please see section *9.3.2 PGA Output* for more details. User controlled inputs and outputs of the ADC are listed below:

Inputs:

- CH SELECTOR: Single-Ended Mode ADC Selection and Analog Input Mux Control Signal (PIN 16, VDD)
- IN+: Single-Ended Mode Input (PIN8 or PIN9) and Differential Mode Positive Input (PIN8)
- IN-: Differential Mode Negative Input (PIN 9 or DAC0)
- VREF: ADC Voltage Reference Input (ADC V_{REF}, VDD/4, none)
- CLK or CLK/16: ADC Clock Input (Ring OSC, Ext. CLK2 (matrix1_out73), RC OSC, SPI SCLK)
- Wake/Sleep

Outputs:

- PGA_Out: Output of the PGA to PIN7
- PGA_Out: Output of the PGA to ACMP1
- SER DATA: ADC serial output (SPI)
- PAR DATA: 8-bit ADC parallel data to either the SPI, PWM, or DCMP
- INT_ OUT: ADC Interrupt Output (matrix0_out43)

9.1 ADC Functional Diagram

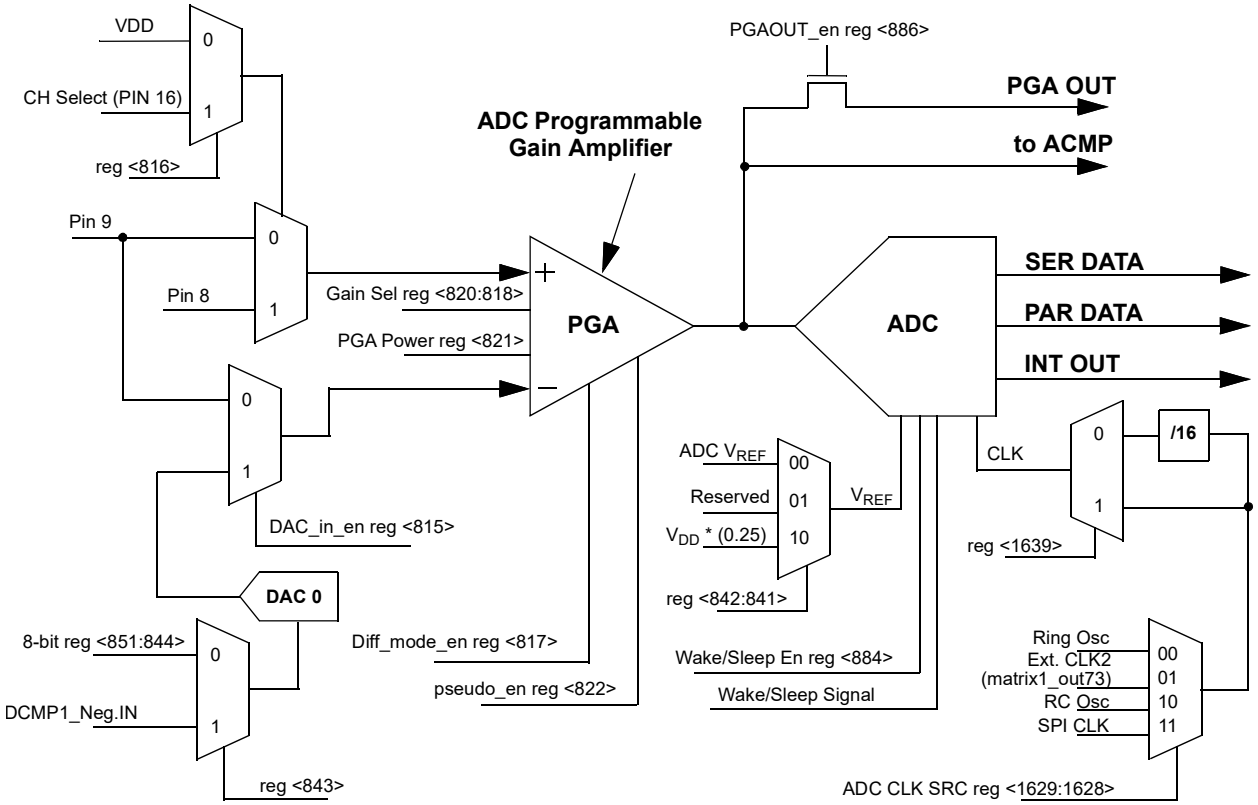


Figure 13. ADC Functional Diagram

9.2 ADC Operation Modes

The ADC has three operating modes:

- Single-Ended ADC operation using IN+ from PIN 8 or 9, when *ADC_sel* (reg <817>) is “0”
- Differential ADC operation using IN+ from PIN 8 and IN- from PIN 9, when *ADC_sel* (reg <817>) is “1”
- Pseudo-Differential ADC operation using IN+ from PIN 8 and IN- from PIN 9, when *ADC_sel* (reg <817>) and *ADC_pseudo-diff_en* (reg <822>) bits are both set to “1”.

9.3 ADC 3-bit Programmable Gain Amplifier (PGA)

The front end of the ADC is a PGA with 3 bits for setting gain. The PGA buffers the ADC in all cases. The PGA gain is set by the ADC_gain_control (reg<820:818>). See ADC Register Settings Table.

Available gain settings depending on PGA mode selected (when used as ADC front-end):

- Single-ended: 0.25x, 0.5x, 1x, 2x, 4x, 8x;
- Differential: 1x, 2x, 4x, 8x, 16x;
- Pseudo-Differential: 1x, 2x, 4x.

PGA inputs:

- CH SELECTOR: Single-Ended Mode ADC Selection and Analog Input Mux Control Signal (PIN16, VDD)
- IN+: Single-Ended Mode Input (PIN8 or PIN9) and Differential Mode Positive Input (PIN8)
- IN-: Differential Mode Negative Input (PIN9 or DAC0)

PGA output is connected directly to ADC input. Also, it is possible to connect PIN7 to PGA output (reg<886>), when ADC is not in use only. The output of PGA has an offset when used as ADC front-end. Please see section *9.3.2 PGA Output* for more details.

9.3.1 PGA 2-Channel Selection

When *ADC_channel_sel* (reg <816>) is set to “1”, the PGA of the ADC will sample either PIN 8 or PIN 9 on the IN+ input, where the selection is controlled by PIN 16.

- When PIN 16 is set to “0”, the ADC will sample PIN 9
- When PIN 16 is set to “1”, the ADC will sample PIN 8

When *ADC_channel_sel* (reg <816>) is set to “0”, the PGA of the ADC will sample PIN 8 on the IN+ input.

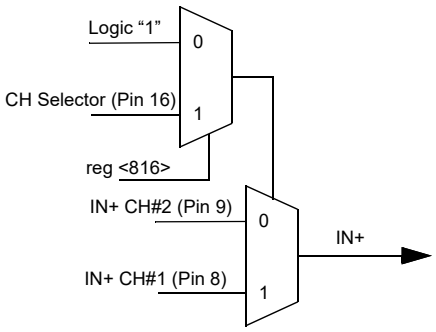


Figure 14. ADC 2-Channel Selection

9.3.2 PGA Output

PGA can be used either in standalone mode or as ADC font-end / ACMP input buffer.

In PGA standalone mode (ADC in POWER DOWN mode) PGA output is always referenced to GND. When ADC is powered on, it powers also the PGA output reference macrocell, so that the output voltage is referenced to one of predefined output offset voltages Vos(RTO) which can be found in PGA specifications. This offset is required for correct ADC operation and it does not affect output code calculation.

PGA output reference (when ADC is on):

- Single-ended mode: Vos(RTO) = GND
- Differential mode: Vos(RTO) = 550 mV
- Pseudo-Differential mode: Vos(RTO) = 180 mV

Note that the reference voltage macrocell is controlled by ADC, therefore if ADC is in POWER DOWN mode, the reference macrocell is OFF and PGA output is referenced to GND. In this case both Differential and Pseudo-Differential modes provide the same output. Typical PGA specifications in Differential/Pseudo-Differential mode with ADC in POWER DOWN state are given in specifications section for information only.

Note 1: PGA operation in Differential/Pseudo-Differential mode with ADC in POWER DOWN state is not recommended to use.

Note 2: Toggling ADC POWER DOWN mode will also toggle the PGA output reference macrocell, that will influence the ACMP input voltage.

PGA has a few output connection possibilities: to ACMP1 and/or ADC, and to external output on PIN7. Connection to external output is possible only when ADC is powered down.

PGA output connection options:

- Single-Ended mode:
  - ADC
  - ACMP
  - External output
- Differential mode:
  - ADC
  - ACMP (See Note 2)
  - External output (Operation in this mode is not recommended)
- Pseudo-Differential mode:
  - ADC
  - ACMP (See Note 2)
  - External output (Operation in this mode is not recommended)

9.3.3 PGA Power On Signal

Whenever ADC is enabled, PGA is powered on automatically. However, it is possible to use PGA separately. In this case, Power On function must be enabled, reg <821> = 1.

9.3.4 PGA Register Settings

Table 41. PGA Register Settings

Signal Function	Register Bit Address	Register Definition
PGA Native Input From Internal DAC0	<815>	0: Disable 1: Enable

Table 41. PGA Register Settings

Signal Function	Register Bit Address	Register Definition
Multichannel Input MUX Enable (Controlled By Pin16)	<816>	0: Disable (PIN16 can not control) 1: Enable
PGA Input Mode Control	<817>	0: Single ended 1: Differential input
PGA Gain Selection	<820:818>	000: 0.25x (For single-ended operation only) 001: 0.5x (For single-ended operation only) 010: 1x 011: 2x 100: 4x 101: 8x (For single-ended and differential operation) 110: 16x (For differential operation only) 111: Reserved
PGA power on signal	<821>	0: power down 1: power on *Note: in ADC wake/sleep dynamic on/off mode, must be set to 0*
PGA Pseudo-Differential Mode Enable	<822>	0: Disable 1: Enable
DAC0 Input Selection	<843>	0: From register 1: From DCMP1's input
DAC0 8 Bit Register Control	<851:844>	00: DAC0 output Is 0 FF: DAC0's output Is 1 V
Force ADC Analog Part On	<885>	0: Disable 1: Enable
PGA Output Enable	<886>	0: Disable 1: Enable

9.3.5 PGA Typical Performance

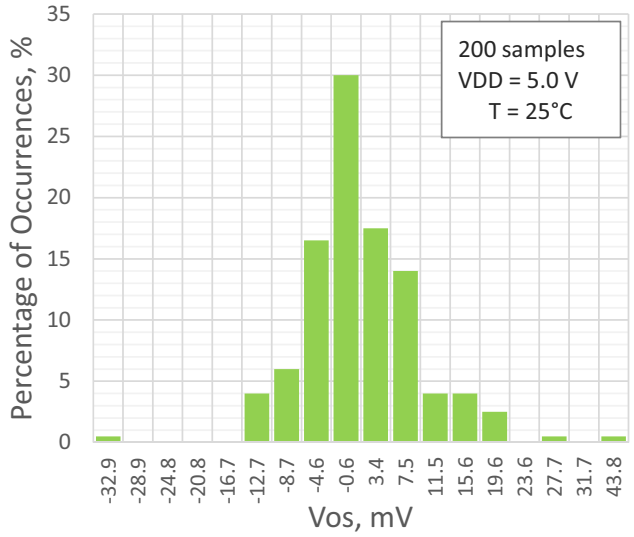


Figure 15. PGA Input Offset Distribution, Single-Ended Mode, G = 0.25

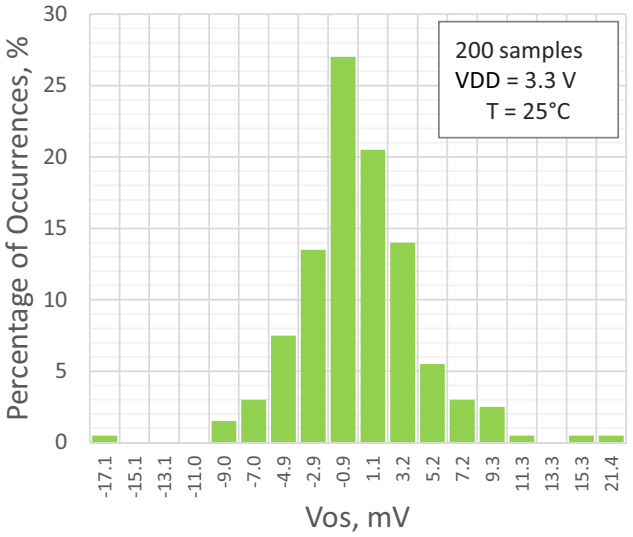


Figure 16. PGA Input Offset Distribution, Single-Ended Mode, G = 0.5

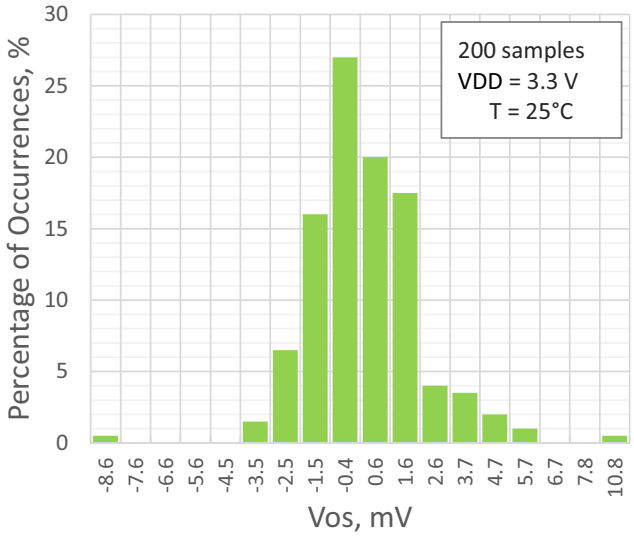


Figure 17. PGA Input Offset Distribution, Single-Ended Mode, G = 1

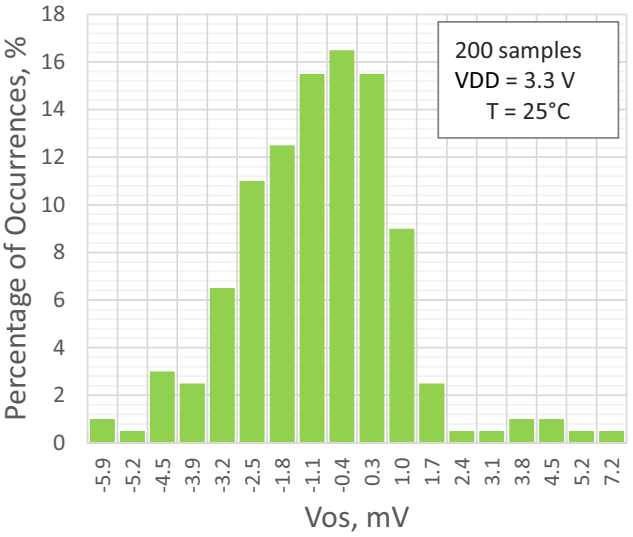


Figure 18. PGA Input Offset Distribution, Single-Ended Mode, G = 2

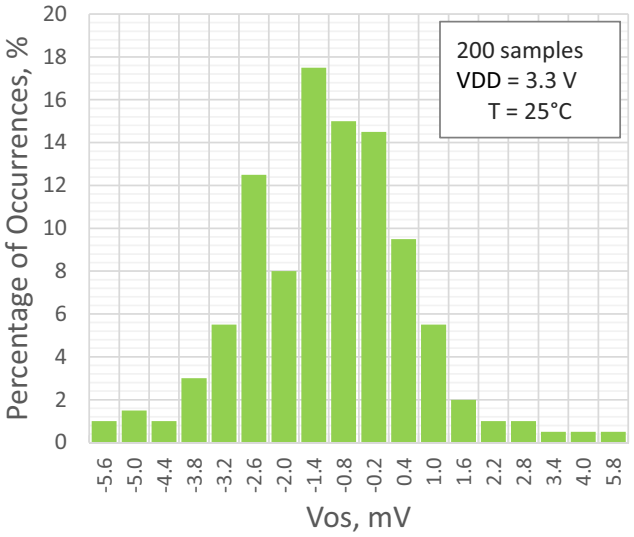


Figure 19. PGA Input Offset Distribution, Single-Ended Mode, G = 4

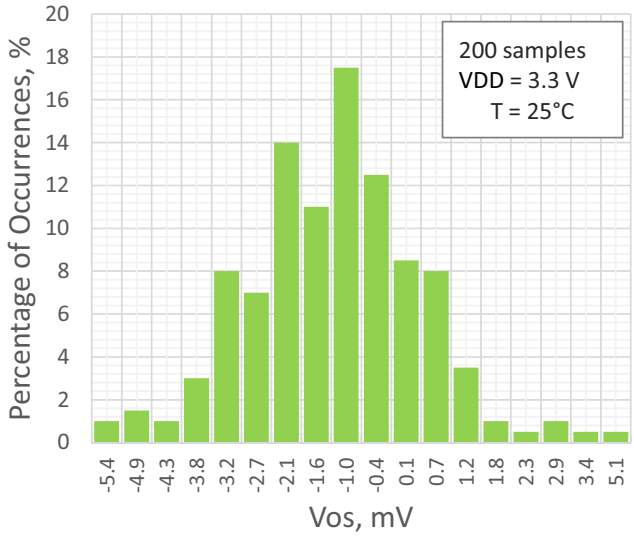


Figure 20. PGA Input Offset Distribution, Single-Ended Mode, G = 8

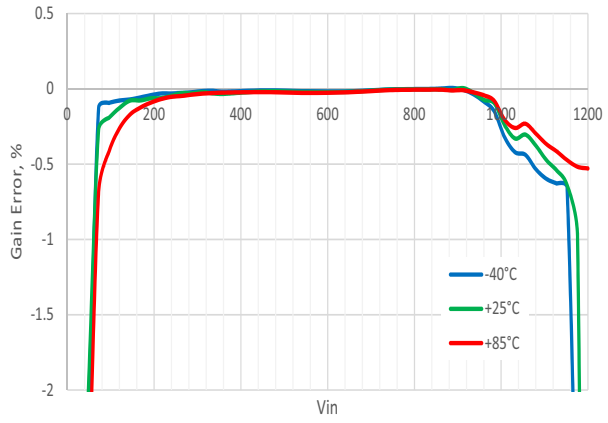


Figure 21. Typical PGA Gain Error vs. Vin, Single-Ended Mode, G = 1, VDD = 1.71 V

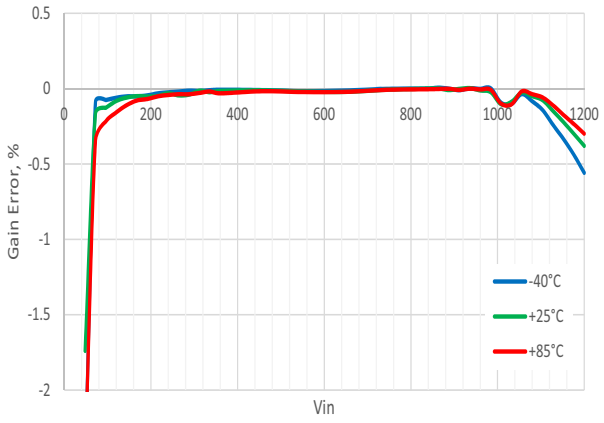


Figure 22. Typical PGA Gain Error vs. Vin, Single-Ended Mode, G = 1, VDD = 5.5 V

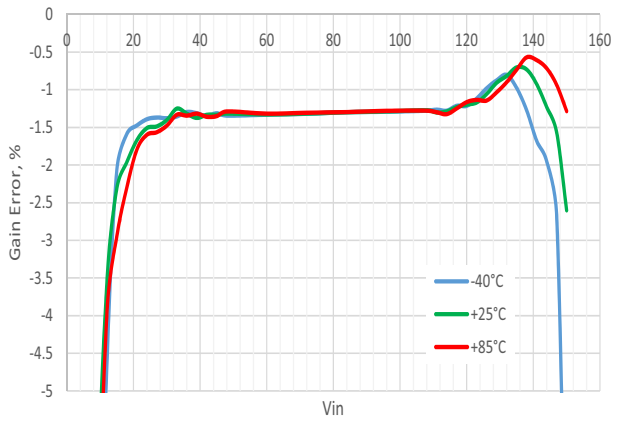


Figure 23. Typical PGA Gain Error vs. Vin, Single-Ended Mode, G = 8, VDD = 1.71 V

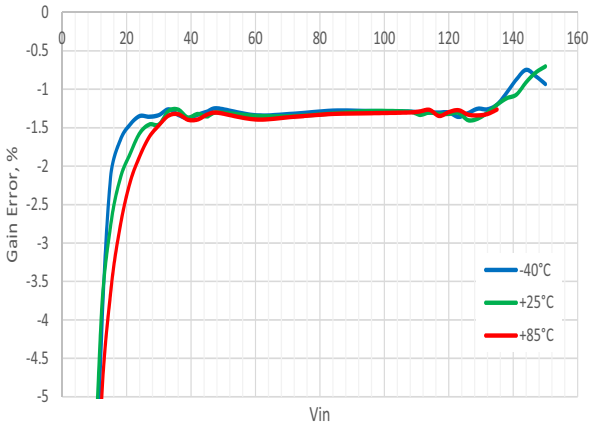


Figure 24. Typical PGA Gain Error vs. Vin, Single-Ended Mode, G = 8, VDD = 5.5 V

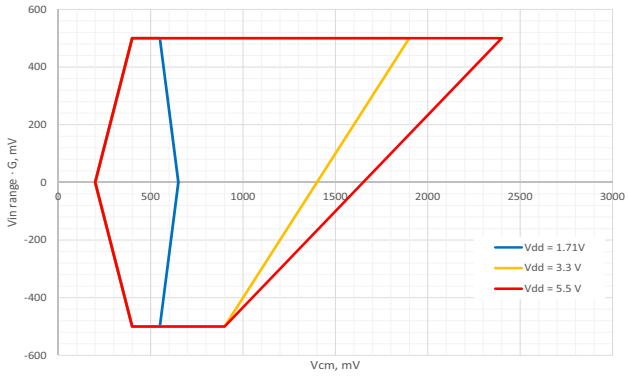


Figure 25. PGA Input Vind Range Multiplied by Gain vs. Vcm, Differential Mode

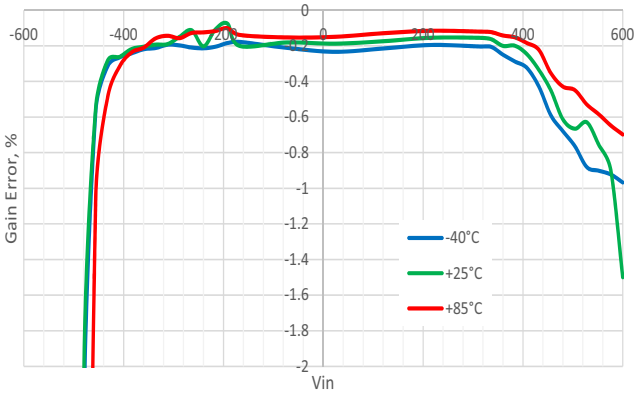


Figure 26. Typical PGA Gain Error vs. Vin, Differential Mode, G = 1, VDD = 1.71 V

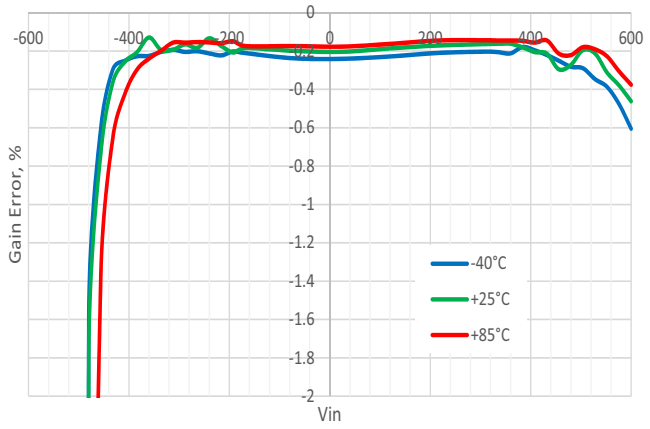


Figure 27. Typical PGA Gain Error vs. Vin, Differential Mode, G = 1, VDD = 5.5 V

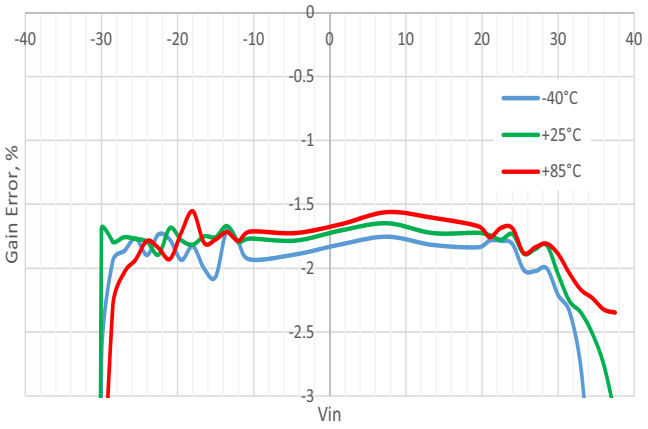


Figure 28. Typical PGA Gain Error vs. Vin, Differential Mode, G = 16, VDD = 1.71 V

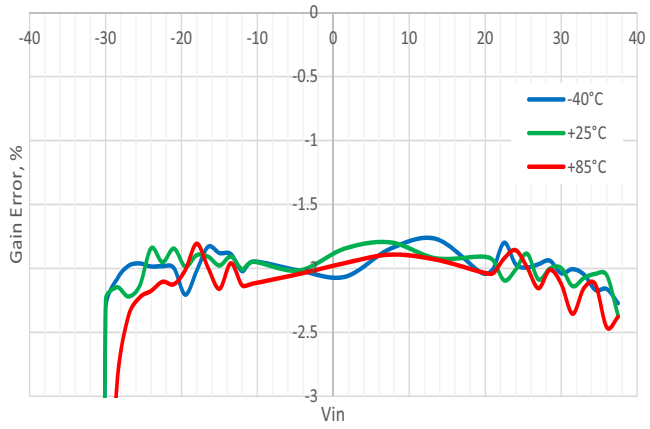


Figure 29. Typical PGA Gain Error vs. Vin, Differential Mode, G = 16, VDD = 5.5 V

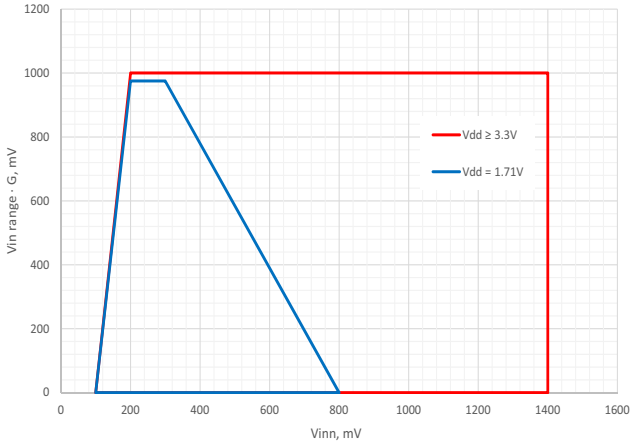


Figure 30. PGA Input Vind Range Multiplied by Gain vs. Vinn, Pseudo-Differential Mode, G = 1

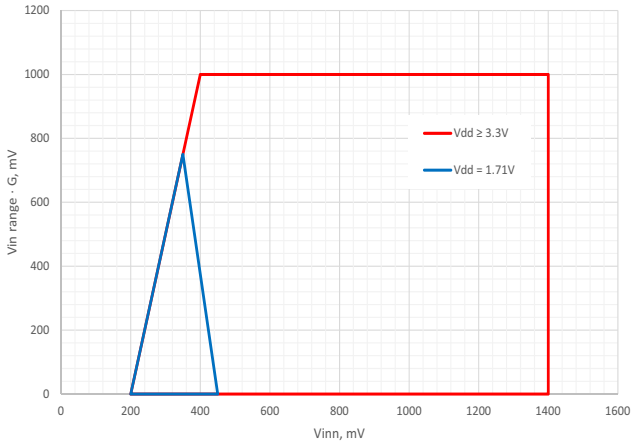


Figure 31. PGA Input Vind Range Multiplied by Gain vs. Vinn, Pseudo-Differential Mode, G = 2

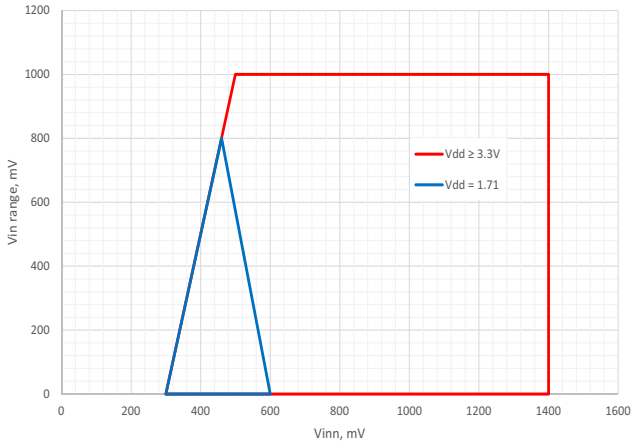


Figure 32. PGA Input Vind Range Multiplied by Gain vs. Vinn, Pseudo-Differential Mode, G = 4

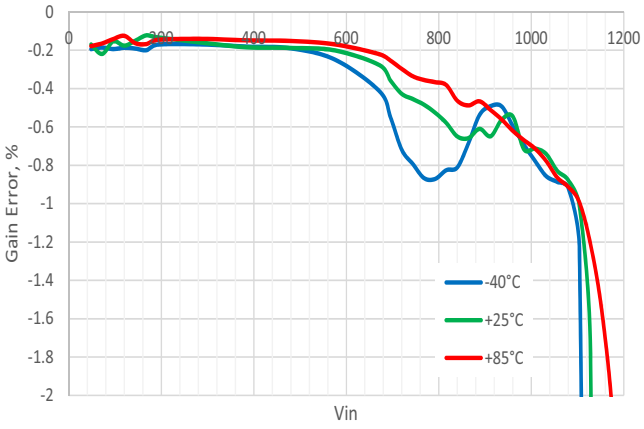


Figure 33. Typical PGA Gain Error vs. Vin, Pseudo-Differential Mode, G = 1, VDD = 2.0 V

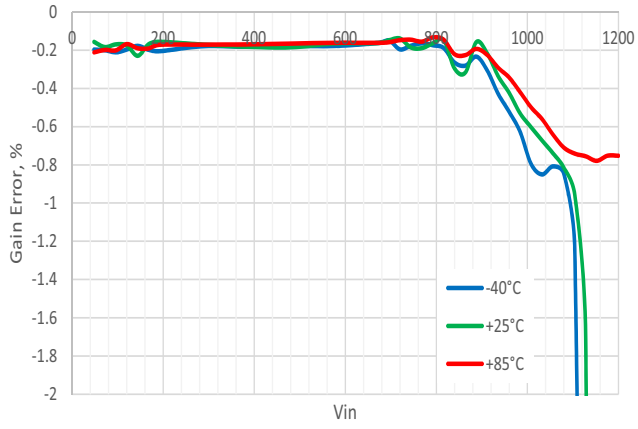


Figure 34. Typical PGA Gain Error vs. Vin, Pseudo-Differential Mode, G = 1, VDD = 5.5 V

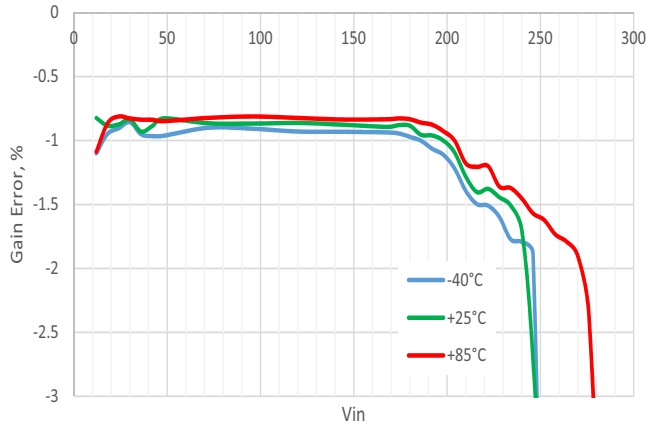


Figure 35. Typical PGA Gain Error vs. Vin, Pseudo-Differential Mode, G= 4, VDD = 1.71 V

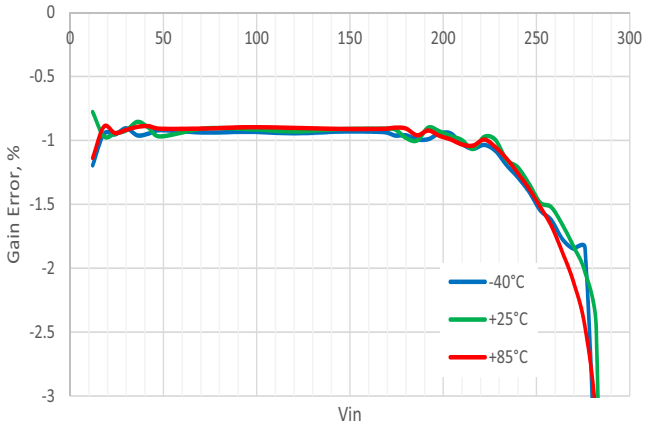


Figure 36. Typical PGA Gain Error vs. Vin, Pseudo-Differential Mode, G= 4, VDD = 5.5 V

9.4 ADC Input Voltage Definition

The ADC's input voltage (V_{IN_ADC}) is calculated based on either the single-ended or differential operation modes the logic cell is set to. In single-ended mode V_{IN_ADC} is the positive input voltage multiplied by the gain of the PGA. While in differential mode the V_{IN_ADC} is the difference between the positive and negative input voltages multiplied by the gain of the PGA plus one half of the reference voltage.

$$V_{OUT(PGA)} = V_{IN(ADC)} = G \cdot (V_{inp} + V_{os(RTI)}) \text{ - for SE mode}$$

$$V_{OUT(PGA)} = V_{IN(ADC)} = G \cdot V_{ind} + V_{os(RTO)} \text{ - for DI and PD mode}$$

V_{os} - PGA offset voltage. RTI and RTO denotes referred to input and referred to output V_{os}.

$$V_{os(RTI)} = \frac{V_{os(RTO)}}{G}$$

G - PGA nominal gain

V_{ind} - PGA input voltage (differential):

$$V_{ind} = V_{inp} - V_{inn}$$

$$V_{inp} = V_{cm} + \frac{V_{ind}}{2}$$

$$V_{inn} = V_{cm} - \frac{V_{ind}}{2}$$

V_{inn} and V_{inp} - absolute voltage at negative and positive PGA input correspondingly

V_{cm} - common mode PGA voltage:

$$V_{cm} = \frac{V_{inn} + V_{inp}}{2}$$

Note: In Pseudo-Differential mode V_{cm} is replaced by V_{inn} voltage for convenience

ADC code for PGA differential input voltage V_{ind} can be calculated as follows:

- Single-ended mode:

$$V_{ind} = V_{inp}$$

$$ADC_{code} = \frac{255}{V_{inp[max]} - V_{inp[min]}}(V_{inp} - V_{inp[min]})$$

Vinp[min] and Vinp[max] - positive input voltage for bit0 and bit255 correspondingly (can be found in ADC specifications)

- Differential and Pseudo-Differential mode:

$$ADC_{code} = \frac{255}{V_{ind[max]} - V_{ind[min]}}(Vind - Vind[min])$$

$V_{ind[min]}$ and $V_{ind[max]}$ - differential input voltage for bit0 and bit255 correspondingly (can be found in ADC specifications)

Least significant bit size (LSB) calculates as follows:

$$LSB = \frac{FS}{255}$$

where FS is full-scale range:

$$FS = V_{ind[max]} - V_{ind[min]}$$

9.5 ADC Reference Voltage

The ADC's reference voltage (V_{REF}) is controlled by ADC_Vref_sel (reg <842:841>). The two reference voltage inputs are chosen from the following:

- ADC V_{REF} from Internal Source (ADC V_{REF} = 1.2 V)
- Power Divider of (0.25) * V_{DD}

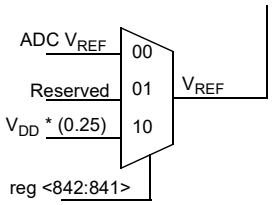


Figure 37. ADC Reference Voltage

9.6 ADC Power Down Select Mode

The ADC's power down source is selected by Matrix0_Out81 reg<491:486>. A value of "1" will drive the ADC and the PGA to power down mode. The SLG46621 also has a slow/fast power on mode feature controlled by reg<885>. When reg<885> = 0, the ADC is in slow power on mode and the entire analog macrocell is controlled by *connection matrix output0 81*. When reg<885> = 1, ADC is in fast power on mode, where only the ADC will be controlled by *connection matrix output0 81* and the analog macrocell will remain on. With this feature, the first ADC power on (with the rest of the analog macrocell) will be approximately 500 µs; the next power cycle the ADC power on (ADC only) time is <5 µs.

9.7 ADC Clock Source

The ADC clock source comes from either the internal RC Oscillator, Matrix1_Out73, Ring Oscillator, or SPI CLK. The ADC requires 16 clock cycles to sample the analog voltage and output the sampled data.

Note: sampling rate should not exceed approximately 100 kbps.

The selection is made from the *ADC_clk_sel* signal via reg <1629:1628> where:

- 00: Ring Oscillator
- 01: Matrix1_Out 73
- 10: RC Oscillator
- 11: SPI CLK

Note: It is not recommended to design in high frequency signals (input our output) on pins adjacent to the following pins: Pin7, Pin8, PIn9 as this may affect ADC performance.

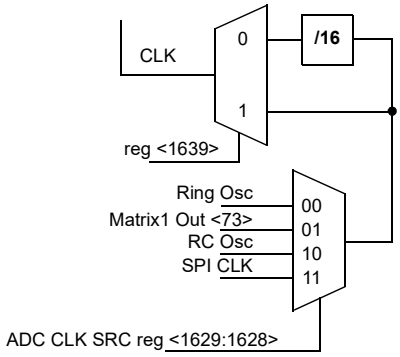


Figure 38. ADC Clock Source

9.8 ADC Outputs

The ADC's output can be shifted out through the SPI logic cell. Both SER DATA and PAR DATA produce an 8-bit data string over 16 clock cycles. See *Figure 39.*

9.8.1 ADC Serial Output

The 8-bit serial data can be output from the SLG46621 device on PIN 10. The individual 8 serial data bits can be read into an external device within the larger system design.

To initialize the *SER DATA* the ADC needs a Power Down signal, which can be configured through the connection matrix. After 6 ADC_CLK cycles the ADC will start to output the 8-Bit Serial Data. This PD signal needs to be held for at least 16 ADC_CLK cycles. The ADC_CLK is determined by either the RC Osc, Ring Osc, Matrix1_Out73, or SPI CLK.

9.8.2 ADC Parallel Output

The 16-bit parallel data can be output from the ADC logic cell to either the DCMP/PWM or FSM logic cells within the SLG46621 device.

To initialize the *PAR DATA* the ADC needs a Power Down signal, which can be configured through the connection matrix. After ten ADC_CLK cycles the ADC will start to output the 16-Bit Parallel Data. This PD signal needs to be held for at least 32 ADC_CLK cycles. The ADC_CLK is determined by either the RC Osc, Ring Osc, Matrix1_Out73, or SPI CLK.

9.9 ADC Interrupt Output Timing Diagram

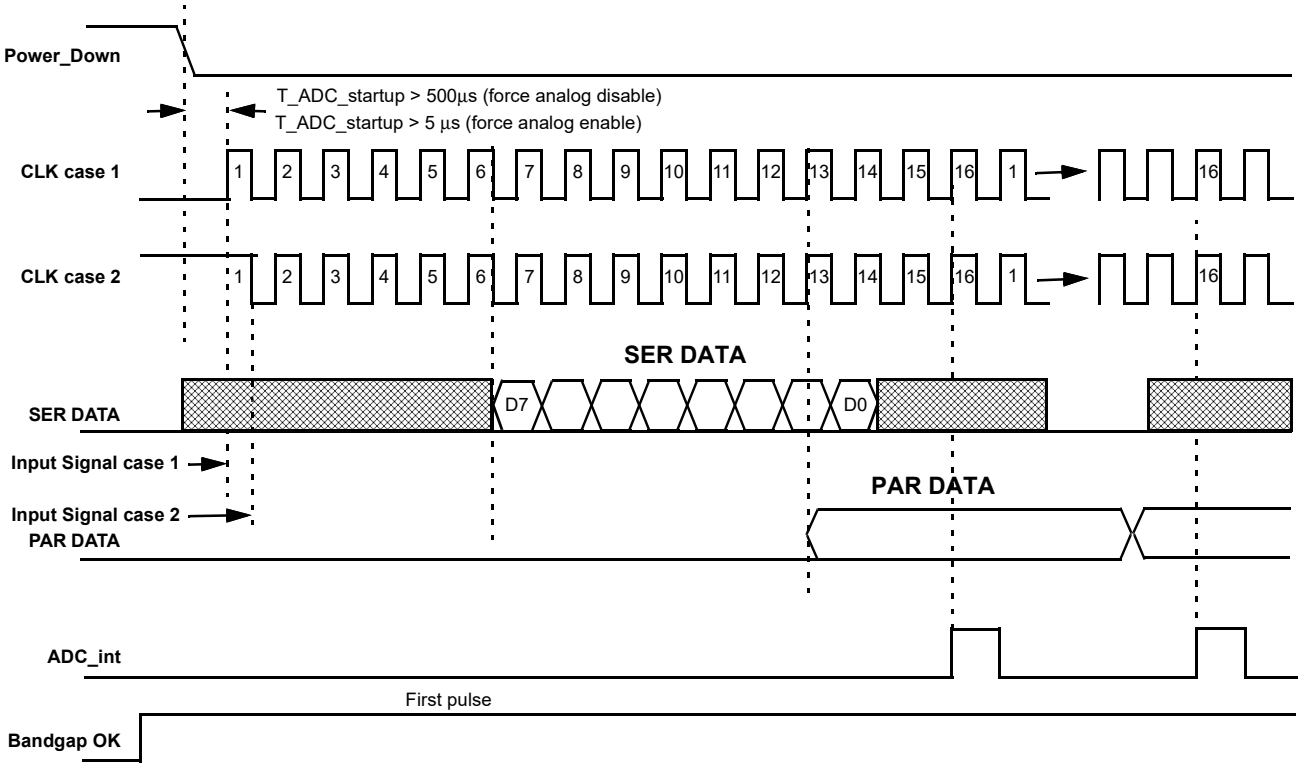


Figure 39. ADC Interrupt Output Timing Diagram

9.10 ADC Register Settings

Table 42. ADC Register Settings

Signal Function	Register Bit Address	Register Definition
ADC Speed Selection	<839:838>	00: Reserved 01: Reserved 10: 100 kHz 11: Reserved
ADC Vref Source Select	<842:841>	00: ADC V_{REF} 01: Reserved 10: 1/4 Vdd 11: None
ADC Wake Sleep Enable	<884>	0: Disable 1: Enable

Note: For PGA Register settings refer to Table 41.

10.0 8-bit Digital-to-Analog Converter (DAC)

There are two DACs in the SLG46620 (DAC0 and DAC1), they are 8-bit Digital to Analog Converters which operate at a maximum sampling speed of 100 ksps. The DAC's DNL is less than 1LSB and INL is less than 1LSB. DAC output to PIN resistance is 1 kΩ. Load resistance is recommended to be no less than 10 kΩ; load capacitance is recommended to be no more than 100 pF.

User controlled inputs and outputs of the DAC are listed below:

DAC0 Inputs:

- Registers
- CNT9_Q<7:0>
- 8LSBs SPI
- FSM0<7:0>

DAC0 Outputs:

- PIN19
- PGA negative input (00: 0 V; FF: 1 V)
- ACMP0 negative input
- ACMP1 negative input
- ACMP2 negative input
- ACMP3 negative input
- ACMP4 negative input
- ACMP5 negative input

DAC1 Inputs:

- Registers
- CNT9_Q<7:0>
- 8LSBs SPI
- FSM0<7:0>

DAC1 Outputs:

- PIN18
- ACMP0 negative input
- ACMP1 negative input
- ACMP2 negative input
- ACMP3 negative input
- ACMP4 negative input
- ACMP5 negative input

If a DAC output is connected to one of SLG46620's external pins (Pin19 for DAC0 and Pin18 for DAC1), it is necessary to enable those external pins as analog input/output. Reg <840>: 0 - DAC0 power off, 1 - DAC0 power on. Reg <834>: 0 - DAC1 power off, 1 - DAC1 power on.

DAC0 output range: 0 V…1 V

DAC1 output range: 50 mV…1.05 V

Please note that DAC1 is shared with ADC macrocell. Therefore it is impossible to use DAC1, when ADC is used. Also to activate DAC1, DAC0 must be enabled (reg <840> = 1 and reg <834> = 1). In addition, DAC0 is used as a part of pseudo-differential mode of PGA macrocell. Therefore DAC0 is not available when PGA is in pseudo-differential mode.

10.1 DAC0 Functional Diagram

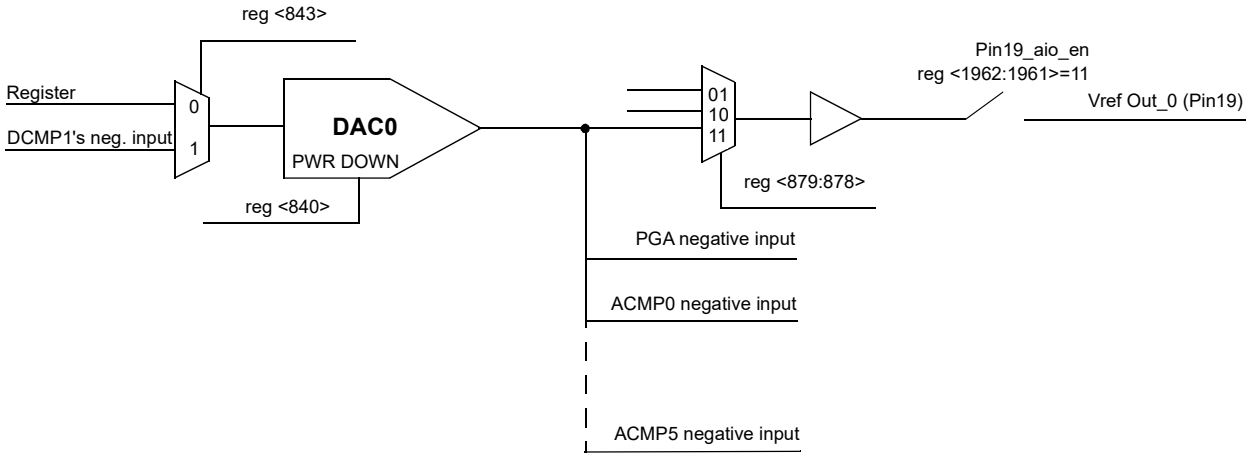


Figure 40. DAC0 Functional Diagram

10.2 DAC1 Functional Diagram

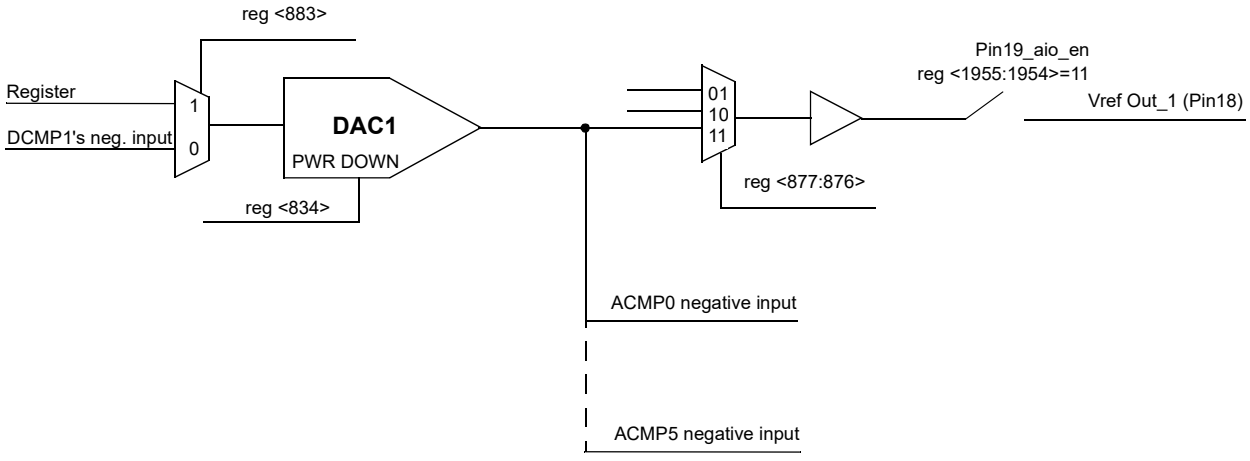


Figure 41. DAC1 Functional Diagram

10.3 DAC Register Settings

Table 43. DAC Register Settings

Register Bit Address	Signal Function	Register Definition
reg<830:823>	DAC1 8 bit register control	00: DAC1 output is ADC Vref bottom voltage FF: DAC1's output is ADC Vref top voltage
reg<834>	DAC1 power on signal	0: power down 1: power on
reg<840>	DAC0 power on signal	0: power down 1: power on When DAC0 used only, need set this bit
reg<843>	DAC0 input selection	0: from register 1: from DCMP1's input
reg<851:844>	DAC0 8 bit register control	00: DAC0 output is 0 FF: DAC0's output is 1 V
reg<883>	DAC1 input selection	0: from DCMP1's Negative input 1: from register
reg<885>	Force ADC analog part on	0: disable 1: enable

11.0 Combinatorial Logic

Combinatorial logic is supported via twenty five Lookup Tables (LUTs) within the SLG46621. There are eight 2-bit LUTs, sixteen 3-bit LUTs, and one 4-bit LUT. The device also includes one Combination Function Macrocell that can be used as a 4-bit LUT. For more details, please see Section *12.0 Combination Function Macrocells*.

Inputs/Outputs for the twenty five LUTs are configured from one of the connection matrices with specific logic functions being defined by the state of NVM bits. The outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

11.1 2-Bit LUT

The eight 2-bit LUTs each take in two input signals from one of the two connection matrices and produce a single output, which goes back into the same connection matrix that the inputs came from. The output state of each 2-bit LUT is defined by four register bits, the output state is based on the appropriate bit selected by the value of the two inputs to the LUT. .

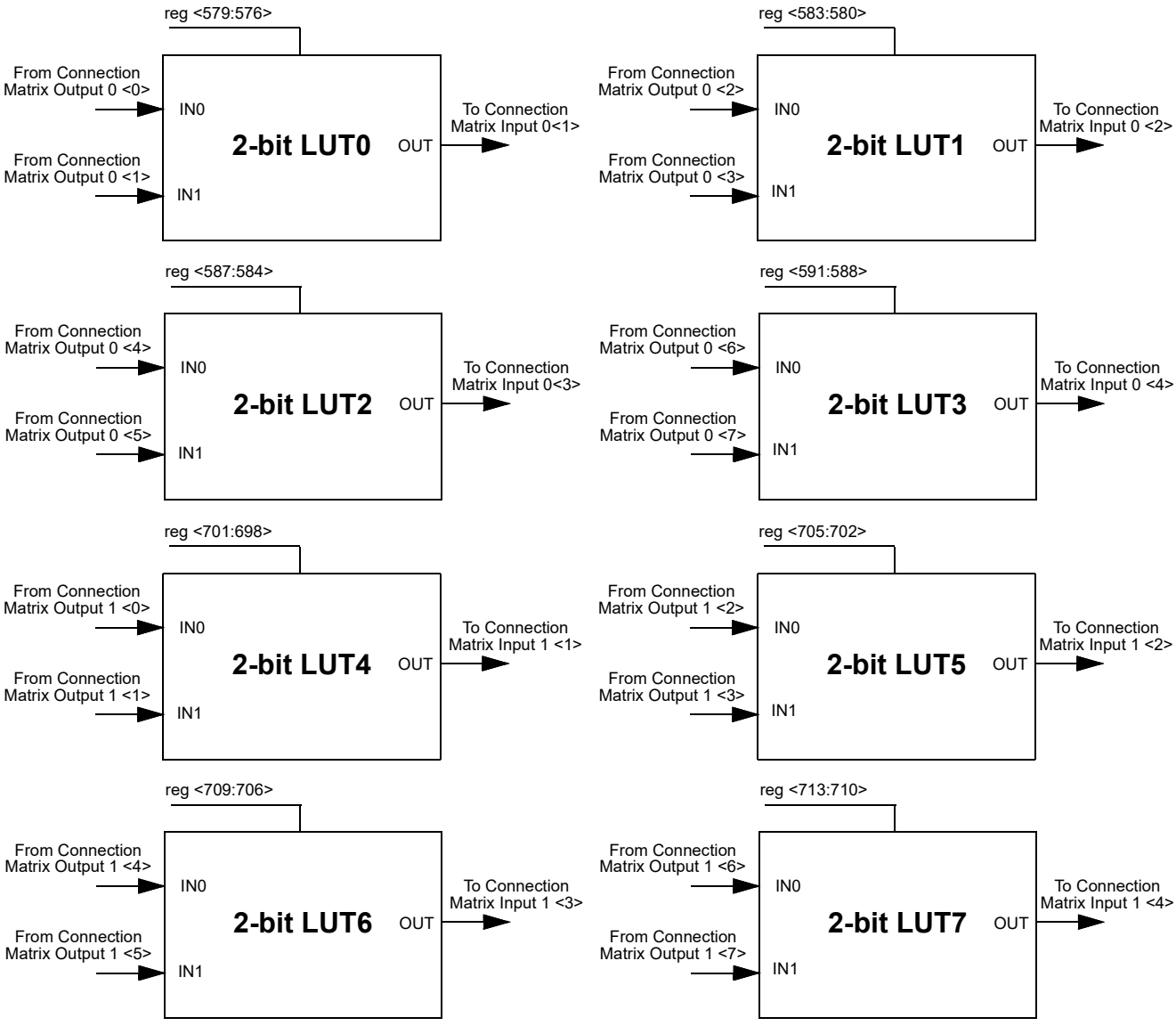


Figure 42. 2-bit LUTs

Table 44. 2-bit LUT0 Truth Table

IN1	IN0	OUT
0	0	reg <576>
0	1	reg <577>
1	0	reg <578>
1	1	reg <579>

Table 45. 2-bit LUT1 Truth Table

IN1	IN0	OUT
0	0	reg <580>
0	1	reg <581>
1	0	reg <582>
1	1	reg <583>

Table 46. 2-bit LUT2 Truth Table

IN1	IN0	OUT
0	0	reg <584>
0	1	reg <585>
1	0	reg <586>
1	1	reg <587>

Table 47. 2-bit LUT3 Truth Table

IN1	IN0	OUT
0	0	reg <588>
0	1	reg <589>
1	0	reg <590>
1	1	reg <591>

Table 48. 2-bit LUT4 Truth Table

IN1	IN0	OUT
0	0	reg <698>
0	1	reg <699>
1	0	reg <700>
1	1	reg <701>

Table 49. 2-bit LUT5 Truth Table

IN1	IN0	OUT
0	0	reg <702>
0	1	reg <703>
1	0	reg <704>
1	1	reg <705>

Table 50. 2-bit LUT6 Truth Table

IN1	IN0	OUT
0	0	reg <706>
0	1	reg <707>
1	0	reg <708>
1	1	reg <709>

Table 51. 2-bit LUT7 Truth Table

IN1	IN0	OUT
0	0	reg <710>
0	1	reg <711>
1	0	reg <712>
1	1	reg <713>

Each Macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function;

2-Bit LUT0 is defined by reg<579:576>

2-Bit LUT1 is defined by reg<583:580>

2-Bit LUT2 is defined by reg<587:584>

2-Bit LUT3 is defined by reg<591:588>

2-Bit LUT4 is defined by reg<701:698>

2-Bit LUT5 is defined by reg<705:702>

2-Bit LUT6 is defined by reg<709:706>

2-Bit LUT7 is defined by reg<713:710>

The table below shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 2-bit LUT logic cells.

Table 52. 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

11.2 3-Bit LUT

The sixteen 3-bit LUTs each take in three input signals from one of the two connection matrices and produce a single output, which goes back into the same connection matrix that the inputs came from. The output state of each 3-Bit LUT is defined by eight register bits, the output state is based on the appropriate bit selected by the value of the three inputs to the LUT.

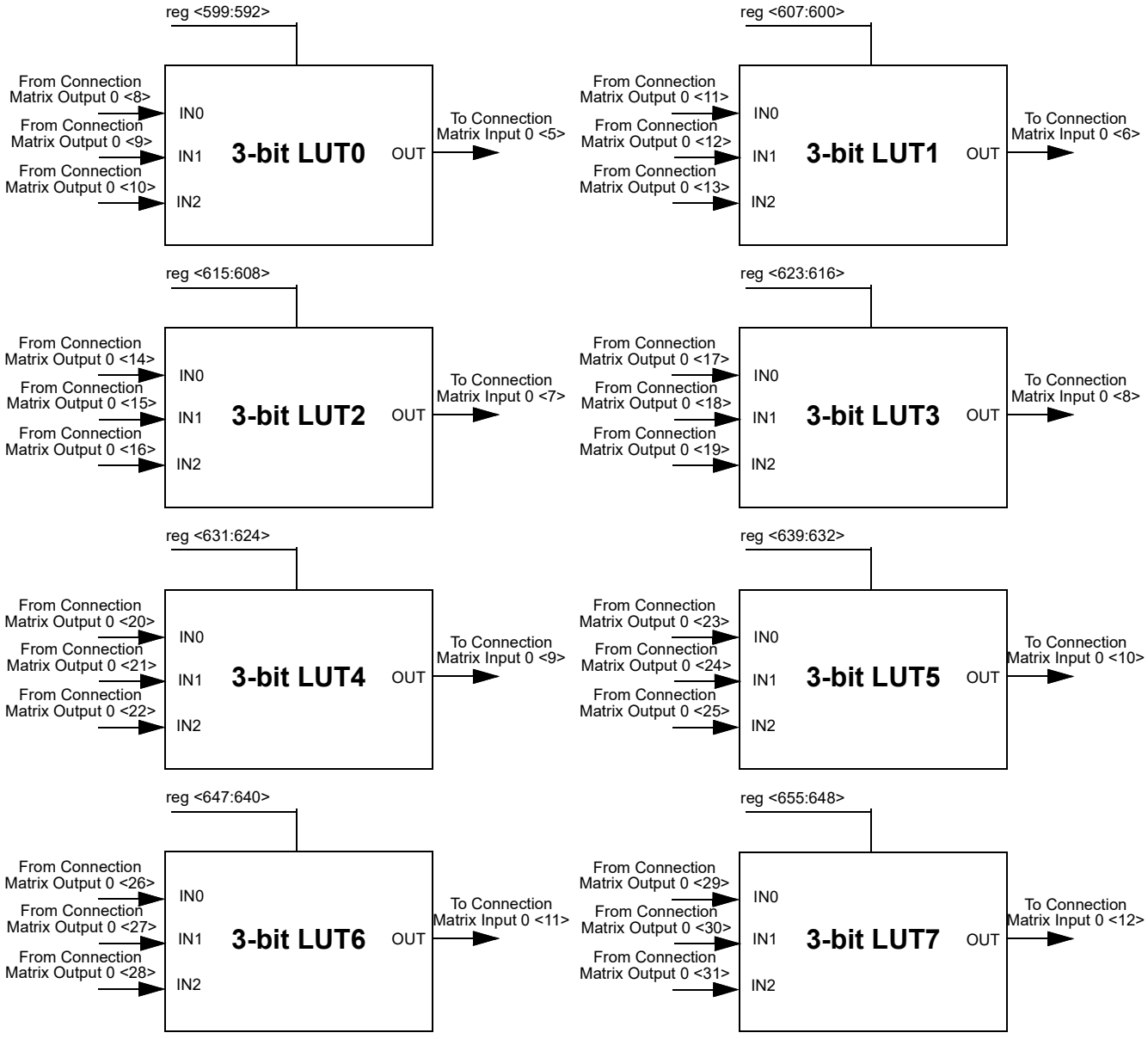


Figure 43. 3-bit LUTs

Figure 44. 3-bit LUTs

Table 53. 3-bit LUT0 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <592>
0	0	1	reg <593>
0	1	0	reg <594>
0	1	1	reg <595>
1	0	0	reg <596>
1	0	1	reg <597>
1	1	0	reg <598>
1	1	1	reg <599>

Table 54. 3-bit LUT1 Truth Table

IN2	IN1	IN0	OUT
0	0	0	reg <600>
0	0	1	reg <601>
0	1	0	reg <602>
0	1	1	reg <603>
1	0	0	reg <604>
1	0	1	reg <605>
1	1	0	reg <606>
1	1	1	reg <607>

Table 55. 3-bit LUT2 Truth Table

IN2	IN1	IN0	OUT
0	0	0	reg <608>
0	0	1	reg <609>
0	1	0	reg <610>
0	1	1	reg <611>
1	0	0	reg <612>
1	0	1	reg <613>
1	1	0	reg <614>
1	1	1	reg <615>

Table 56. 3-bit LUT3 Truth Table

IN2	IN1	IN0	OUT
0	0	0	reg <616>
0	0	1	reg <617>
0	1	0	reg <618>
0	1	1	reg <619>
1	0	0	reg <620>
1	0	1	reg <621>
1	1	0	reg <622>
1	1	1	reg <623>

Table 57. 3-bit LUT4 Truth Table

IN2	IN1	IN0	OUT
0	0	0	reg <624>
0	0	1	reg <625>
0	1	0	reg <626>
0	1	1	reg <627>
1	0	0	reg <628>
1	0	1	reg <629>
1	1	0	reg <630>
1	1	1	reg <631>

Table 58. 3-bit LUT5 Truth Table

IN2	IN1	IN0	OUT
0	0	0	reg <632>
0	0	1	reg <633>
0	1	0	reg <634>
0	1	1	reg <635>
1	0	0	reg <636>
1	0	1	reg <637>
1	1	0	reg <638>
1	1	1	reg <639>

Table 59. 3-bit LUT6 Truth Table

IN2	IN1	IN0	OUT
0	0	0	reg <640>
0	0	1	reg <641>
0	1	0	reg <642>
0	1	1	reg <643>
1	0	0	reg <644>
1	0	1	reg <645>
1	1	0	reg <646>
1	1	1	reg <647>

Table 60. 3-bit LUT7 Truth Table

IN2	IN1	IN0	OUT
0	0	0	reg <648>
0	0	1	reg <649>
0	1	0	reg <650>
0	1	1	reg <651>
1	0	0	reg <652>
1	0	1	reg <653>
1	1	0	reg <654>
1	1	1	reg <655>

Table 61. 3-bit LUT8 Truth Table

IN2	IN1	IN0	OUT
0	0	0	reg <714>
0	0	1	reg <715>
0	1	0	reg <716>
0	1	1	reg <717>
1	0	0	reg <718>
1	0	1	reg <719>
1	1	0	reg <720>
1	1	1	reg <721>

Table 62. 3-bit LUT9 Truth Table

IN2	IN1	IN0	OUT
0	0	0	reg <722>
0	0	1	reg <723>
0	1	0	reg <724>
0	1	1	reg <725>
1	0	0	reg <726>
1	0	1	reg <727>
1	1	0	reg <728>
1	1	1	reg <729>

Table 63. 3-bit LUT10 Truth Table

IN2	IN1	IN0	OUT
0	0	0	reg <730>
0	0	1	reg <731>
0	1	0	reg <732>
0	1	1	reg <733>
1	0	0	reg <734>
1	0	1	reg <735>
1	1	0	reg <736>
1	1	1	reg <737>

Table 64. 3-bit LUT11 Truth Table

IN2	IN1	IN0	OUT
0	0	0	reg <738>
0	0	1	reg <739>
0	1	0	reg <740>
0	1	1	reg <741>
1	0	0	reg <742>
1	0	1	reg <743>
1	1	0	reg <744>
1	1	1	reg <745>

Table 65. 3-bit LUT12 Truth Table

IN2	IN1	IN0	OUT
0	0	0	reg <746>
0	0	1	reg <747>
0	1	0	reg <748>
0	1	1	reg <749>
1	0	0	reg <750>
1	0	1	reg <751>
1	1	0	reg <752>
1	1	1	reg <753>

Table 66. 3-bit LUT13 Truth Table

IN2	IN1	IN0	OUT
0	0	0	reg <754>
0	0	1	reg <755>
0	1	0	reg <756>
0	1	1	reg <757>
1	0	0	reg <758>
1	0	1	reg <759>
1	1	0	reg <760>
1	1	1	reg <761>

Table 67. 3-bit LUT14 Truth Table

IN2	IN1	IN0	OUT
0	0	0	reg <762>
0	0	1	reg <763>
0	1	0	reg <764>
0	1	1	reg <765>
1	0	0	reg <766>
1	0	1	reg <767>
1	1	0	reg <768>
1	1	1	reg <769>

Table 68. 3-bit LUT15 Truth Table

IN2	IN1	IN0	OUT
0	0	0	reg <770>
0	0	1	reg <771>
0	1	0	reg <772>
0	1	1	reg <773>
1	0	0	reg <774>
1	0	1	reg <775>
1	1	0	reg <776>
1	1	1	reg <777>

Each 3-bit LUT uses an 8-bit register signal to define their output functions;

3-Bit LUT0 is defined by reg<599:592>

3-Bit LUT1 is defined by reg<607:600>

3-Bit LUT2 is defined by reg<615:608>

3-Bit LUT3 is defined by reg<623:616>

3-Bit LUT4 is defined by reg<631:624>

3-Bit LUT5 is defined by reg<639:632>

3-Bit LUT6 is defined by reg<647:640>

3-Bit LUT7 is defined by reg<655 648>

3-Bit LUT8 is defined by reg<721:714>

3-Bit LUT9 is defined by reg<729:722>

3-Bit LUT10 is defined by reg<737:730>

3-Bit LUT11 is defined by reg<745:738>

3-Bit LUT12 is defined by reg<753:746>

3-Bit LUT13 is defined by reg<761:754>

3-Bit LUT14 is defined by reg<769:762>

3-Bit LUT15 is defined by reg<777:770>

The table below shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 3-bit LUT logic cells.

Table 69. 3-bit LUT Standard Digital Functions

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

11.3 4-Bit LUT

The one 4-bit LUT (LUT4_1) takes in four input signals from connection matrix 1 and produces a single output, which goes back into connection matrix 1. The output state of the 4-bit LUT is defined by sixteen register bits, the output state is based on the appropriate bit selected by the value of the four inputs to the LUT.

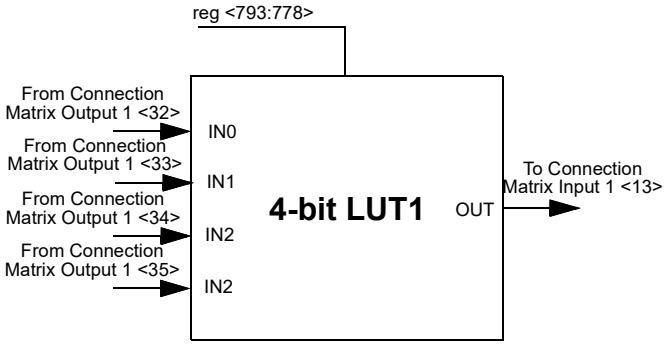


Figure 45. 4-bit LUT_1

11.3.1 The device also includes one Combination Function Macrocell that can be used as a 4-bit LUT. For more details, please see Section *12.0 Combination Function Macrocells*.

Table 70. 4-bit LUT1 Truth Table

IN3	IN2	IN1	IN0	OUT
0	0	0	0	reg <778>
0	0	0	1	reg <779>
0	0	1	0	reg <780>
0	0	1	1	reg <781>
0	1	0	0	reg <782>
0	1	0	1	reg <783>
0	1	1	0	reg <784>
0	1	1	1	reg <785>
1	0	0	0	reg <786>
1	0	0	1	reg <787>
1	0	1	0	reg <788>
1	0	1	1	reg <789>
1	1	0	0	reg <790>
1	1	0	1	reg <791>
1	1	1	0	reg <792>
1	1	1	1	reg <793>

Each 4-bit LUT uses an 16-bit register signal to define their output functions;

4-Bit LUT1 is defined by reg<793:778>

The table below shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within the 4-bit LUT logic cell.

Table 71. 4-bit LUT Standard Digital Functions

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1

12.0 Combination Function Macrocells

The SLG46621 has one combination function macrocell that can serve as a logic or timing function. This macrocell can serve as a Look Up Table (LUT), or Programmable Function Generator (PGEN).

When used to implement LUT functions, the 4-bit LUT takes in four input signals from the connection matrix 0 and produce a single output, which goes back into the connection matrix 0. When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR). The user can also define the combinatorial relationship between inputs and outputs to be any selectable function.

When operating as a Programmable Function Generator, the output of the macrocell with clock out a sequence of two to sixteen bits that are user selectable in their bit values, and user selectable in the number of bits (up to sixteen) that are output before the pattern repeats.See *Figure 47.*

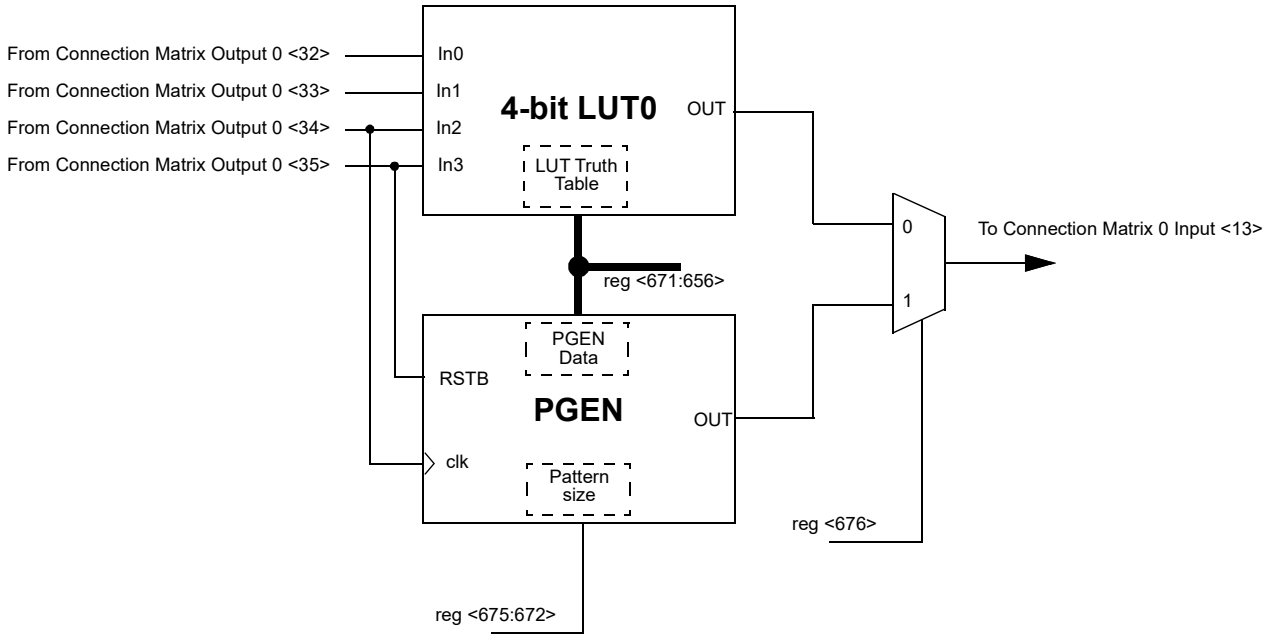


Figure 46. 4-bit LUT0 or PGEN

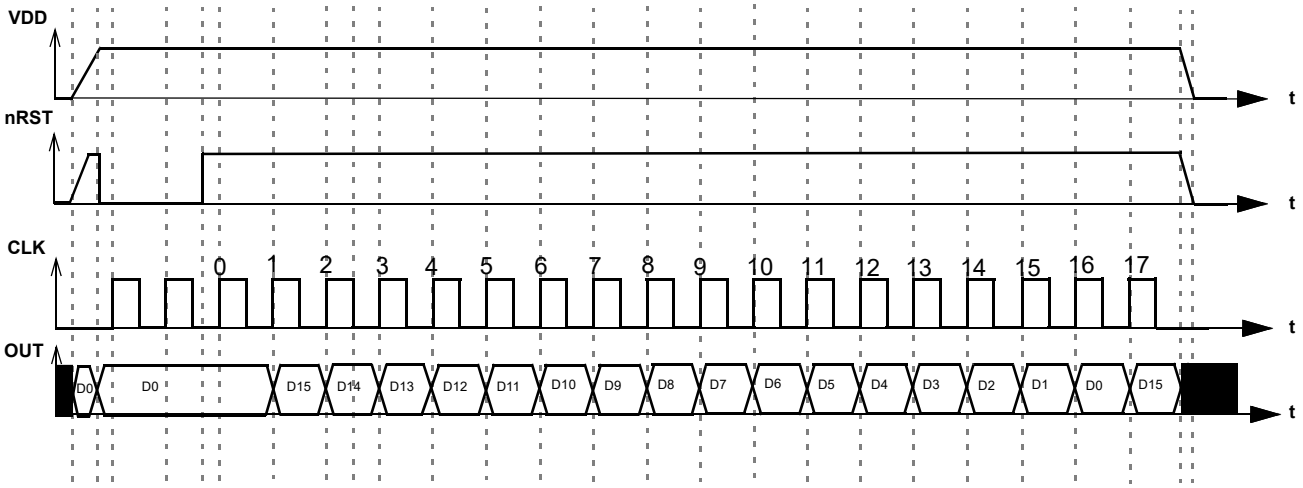


Figure 47. PGEN Timing Diagram

When this macrocell is used to implement LUT function, the 4-bit LUT uses a 16-bit register signal to define its output function;

4-Bit LUT0 is defined by reg<671:656>.

Table 72. 4-bit LUT0 Truth Table.

IN3	IN2	IN1	IN0	OUT
0	0	0	0	reg <656>
0	0	0	1	reg <657>
0	0	1	0	reg <658>
0	0	1	1	reg <659>
0	1	0	0	reg <660>
0	1	0	1	reg <661>
0	1	1	0	reg <662>
0	1	1	1	reg <663>
1	0	0	0	reg <664>
1	0	0	1	reg <665>
1	0	1	0	reg <666>
1	0	1	1	reg <667>
1	1	0	0	reg <668>
1	1	0	1	reg <669>
1	1	1	0	reg <670>
1	1	1	1	reg <671>

12.1 4-Bit LUT0 or Programmable Function Generator Register Settings

Table 73. 4-Bit LUT0 or Programmable Function Generator Register Settings

Signal Function	Register Bit Address	Register Definition
LUT4_1 & PGEN data	<671:656>	Data
4-bit counter data in PGEN	<675:672>	Data
PGEN Enable Signal	<676>	0: LUT4 Function 1: PGEN Function

13.0 Analog Comparators (ACMP)

There are six Analog Comparator (ACMP) macrocells in the SLG46621. In order for the ACMP cells to be used in a GreenPAK design, the power up signals (ACMPx_pdb) need to be active. By connecting to signals coming from the Connection Matrix, it is possible to have each ACMP be always on, always off, or power cycled based on a digital signal coming from the Connection Matrix. When ACMP is powered down, output is low.

PWR UP = 1 => ACMP is powered up

PWR UP = 0 => ACMP is powered down

During ACMP power up, its output will remain low, and then becomes valid 2.08 ms (max) after ACMP power up signal goes high, see *Figure 48.* . If VDD is greater or equal to 2.7 V, it is possible to decrease turn-on time by setting the BG ok delay to 100 µs, see *Figure 49.* . The ACMP cells have an input "Low bandwith" signal selection, which can be used to save power and reduce noise impact when lower bandwidth signals are being compared. To ensure proper chip startup operation, it is recommended to enable the ACMPs with the POR signal, and not the VDD signal..

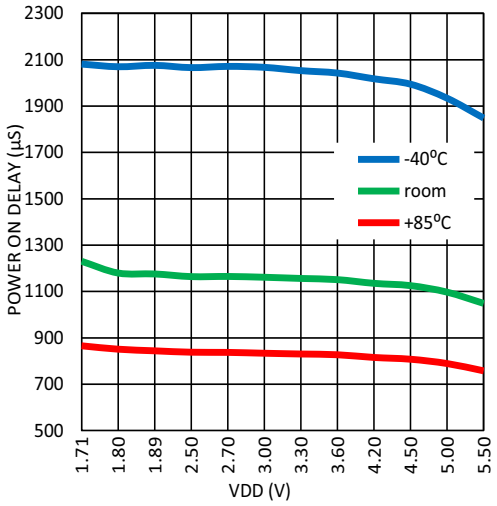


Figure 48. Maximum Power On Delay vs. VDD, BG=550 µs, Regulator and Charge Pump set to automatic ON/OFF

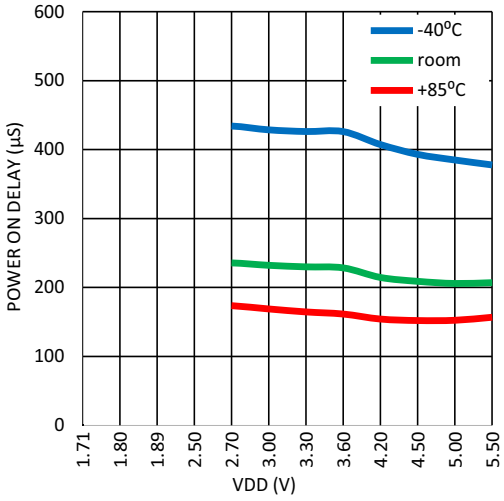


Figure 49. Maximum Power On Delay vs. VDD, BG=100 µs, Regulator and Charge Pump set to automatic ON/OFF

Each of the ACMP cells has a positive input signal that can be provided by a variety of external sources. There is also a selectable gain stage (1X, 0.5X, 0.33X, 0.25X) before connection to the analog comparator. The Gain divider is unbuffered and consists of 250 KΩ (typ.) resistors, see *Table 74*. For gain divider accuracy refer to *Table 75*. IN- voltage range: 0 - 1.2 V. Can use Vref selection VDD/4 and VDD/3 to maintain this input range.

Input bias current < 1 nA (typ).

Table 74. Gain Divider Input Resistance (typical)

Gain	x1	x0.5	x0.33	x0.25
Input Resistance	100 GΩ	1 MΩ	0.75 MΩ	1 MΩ

Table 75. Gain Divider typical Accuracy at T = (-40..+85°C), VDD = 3.3 V

Gain	x0.5	x0.33	x0.25
Accuracy	±0.50%	±0.33%	±0.25%

Each cell also has a hysteresis selection, to offer hysteresis of 0 mV, 25 mV, 50 mV or 200 mV. The 50 mV and 200 mV hysteresis options can be used with internal voltage reference only, while 25 mV hysteresis option can be used with both internal and external voltage reference. The 50 mV and 200 mV hysteresis options are one way hysteresis. It means that the actual thresholds will be Vref (high threshold) and Vref - hysteresis (low threshold). The ACMP output will retain its previous value, if the input voltage is within threshold window (between Vref and Vref - hysteresis). Please note: for the 25 mV hysteresis option threshold levels will be Vref + hysteresis/2 (high threshold) and Vref – hysteresis/2 (low threshold).

Note: Any ACMP powered on enables the BandGap internal circuit as well. An analog voltage will appear on Vref even when the Force BandGap option is set as Disabled.

For high input impedance when using the gain divider (x0.25, x0.33, x0.5), it is possible to use the input buffer (except ACMP5). However, this will add an offset, see *Figure 50.* to *Figure 53.* .

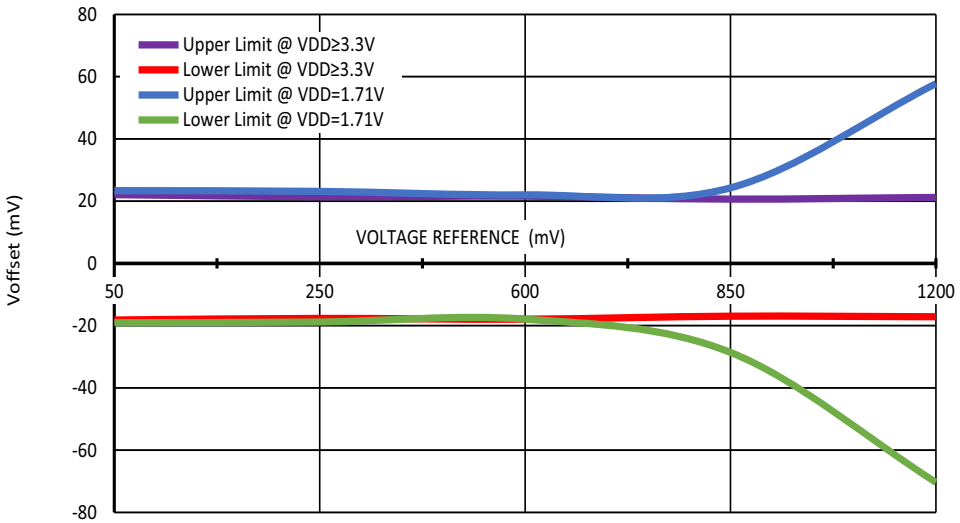


Figure 50. Buffer Input Voltage Offset vs. Voltage Reference at T = (-40.... +85)°C, Buffer Bandwidth = 1 kHz, Vhys = 0 mV, Gain = 1.

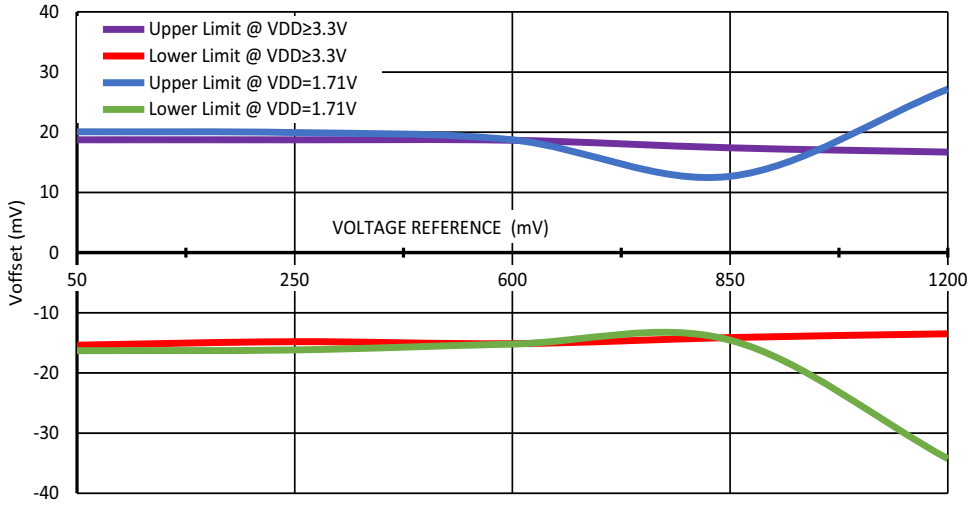


Figure 51. Buffer Input Voltage Offset vs. Voltage Reference at T = (-40.... +85)°C, Buffer Bandwidth = 5 kHz, Vhys = 0 mV, Gain = 1.

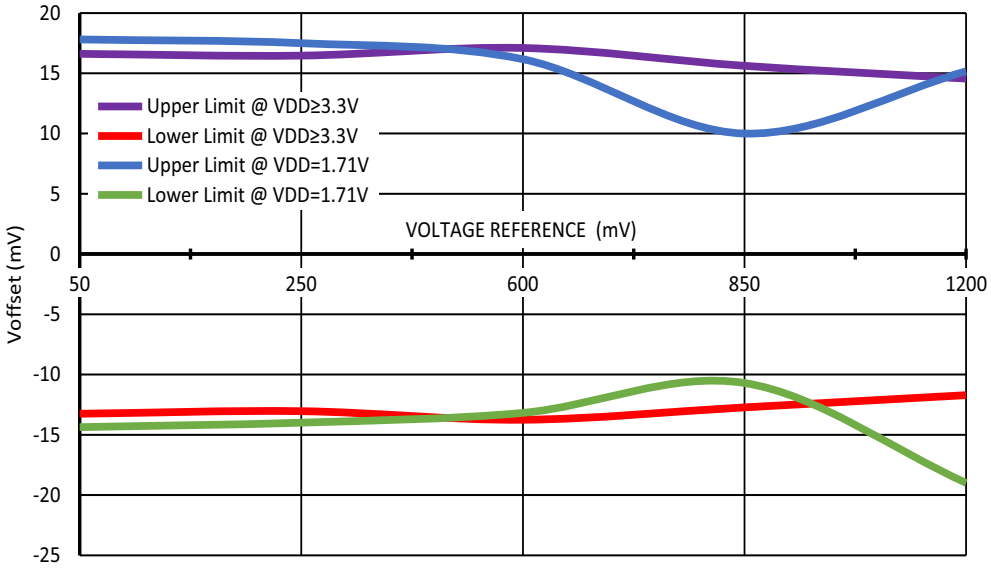


Figure 52. Buffer Input Voltage Offset vs. Voltage Reference at T = (-40.... +85)°C, Buffer Bandwidth = 20 kHz, Vhys = 0 mV, Gain = 1.

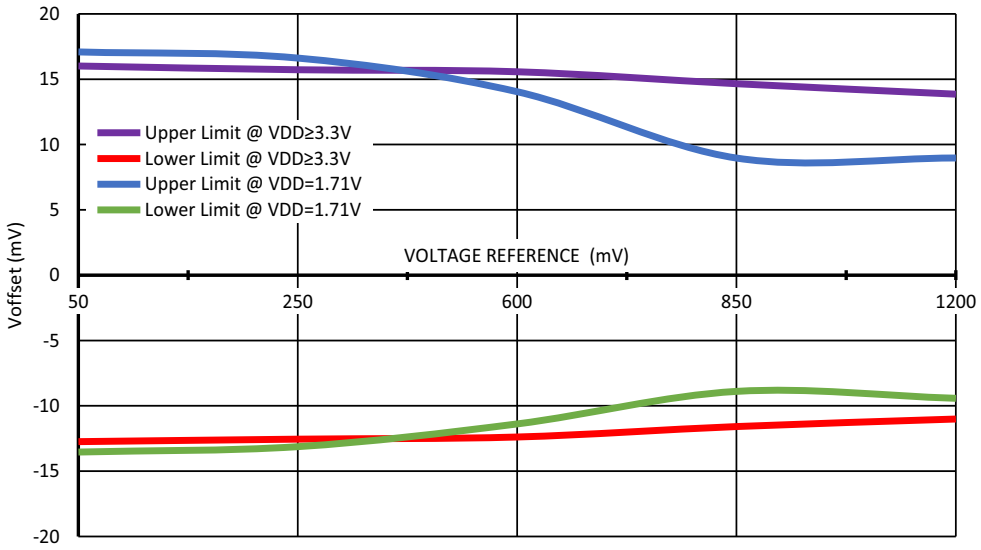


Figure 53. Buffer Input Voltage Offset vs. Voltage Reference at T = (-40.... +85)°C, Buffer Bandwidth = 50 kHz, Vhys = 0 mV, Gain = 1.

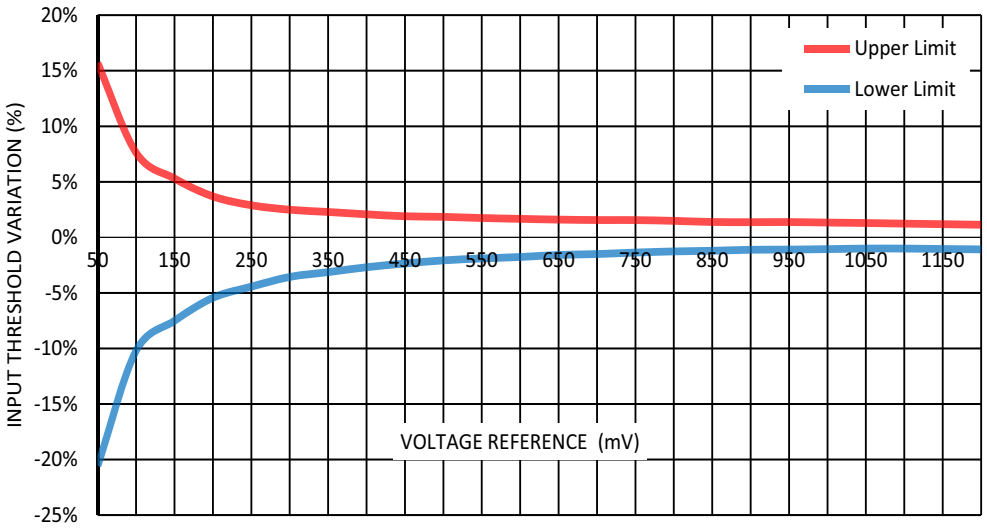


Figure 54. Input Threshold Vatiation (including Vref variation, ACMP offset) vs. Voltage Reference at T = (-40.... +85)°C, LMB Mode - Disable, Vhys = 0 mV.

Note 1: When VDD < 1.8 V voltage reference should not exceed 1100 mV.

Note 2: For electrical specification refer to section 5.11 ACMP Specifications.

13.1 ACMP Master Architecture

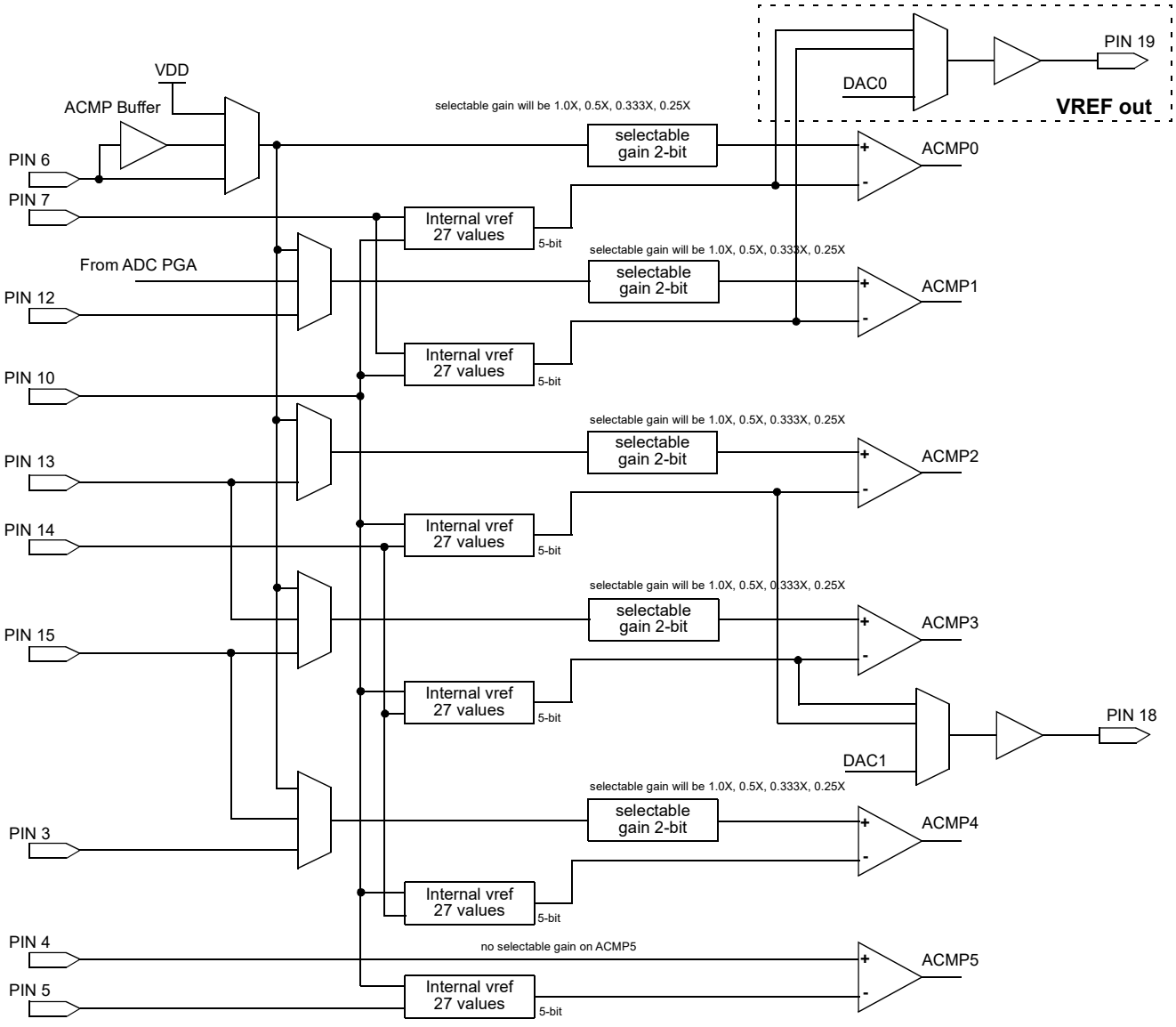


Figure 55. ACMP Master Architecture Diagram

13.2 ACMP0 Block Diagram

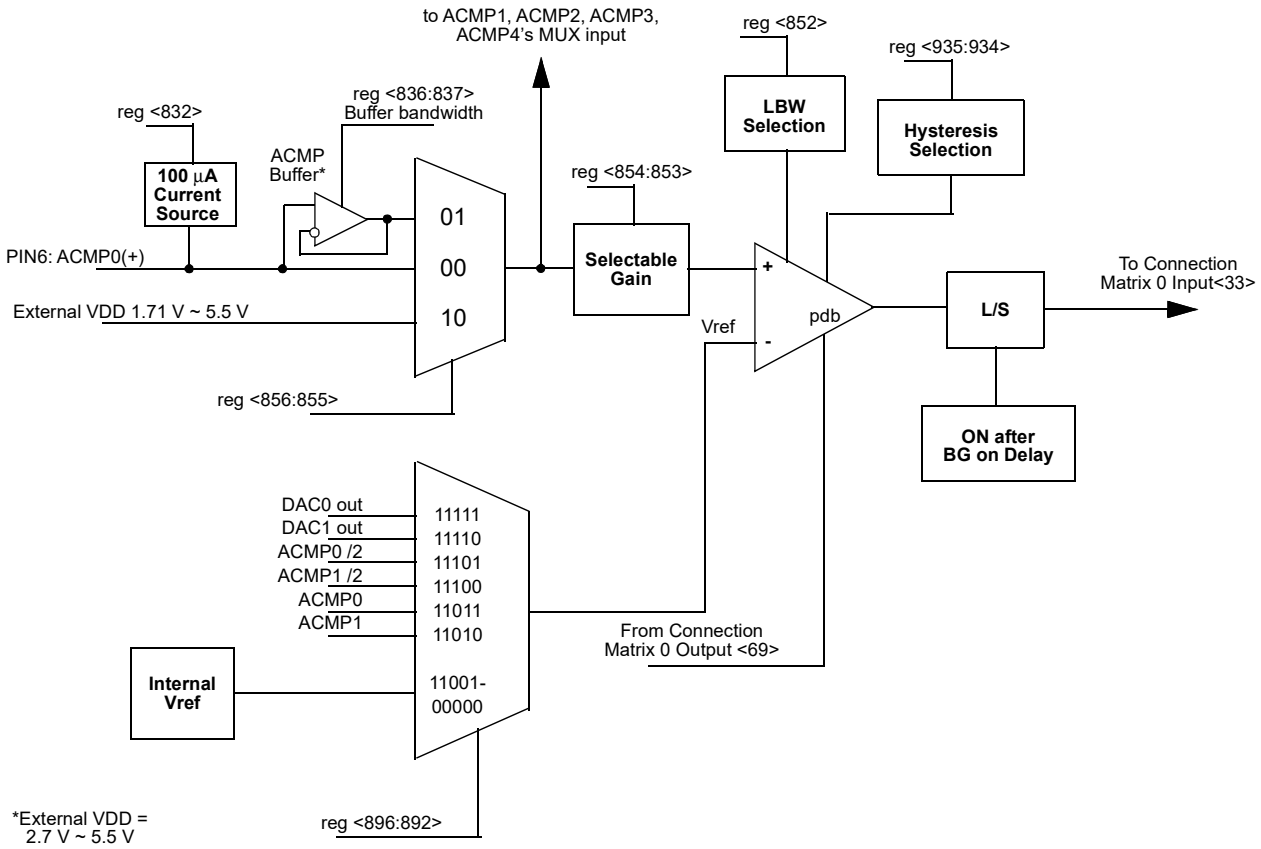


Figure 56. ACMP0 Block Diagram

13.3 ACMP0 Register Settings

Table 76. ACMP0 Register Settings

Signal Function	Register Bit Address	Register Definition
ACMP0 Hysteresis Enable	reg<935:934>	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV)
ACMP0 In Voltage Select	reg<896:892>	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: Vdd/3 11001: Vdd/4 11010: Vref_Ext_ACMP1 11011: Vref_Ext_ACMP0 11100: Vref_Ext_ACMP1 / 2 11101: Vref_Ext_ACMP0 / 2 11110: DAC1_out 11111: DAC0_out
ACMP0 Input Selection	<856:855>	00: PIN 6 Input 01: With Buffer 10: Vdd 11: None
ACMP0 Positive Input Gain Control	reg<854:853>	00: 1.00X 01: 0.50X 10: 0.33X 11: 0.25X
ACMP0 Low Bandwidth (Max: 1 MHz) Enable	reg<852>	1: On 0: Off
ACMP0 Input 100u Current Source Enable	reg<832>	1: Disable 0: Enable

13.4 ACMP1 Block Diagram

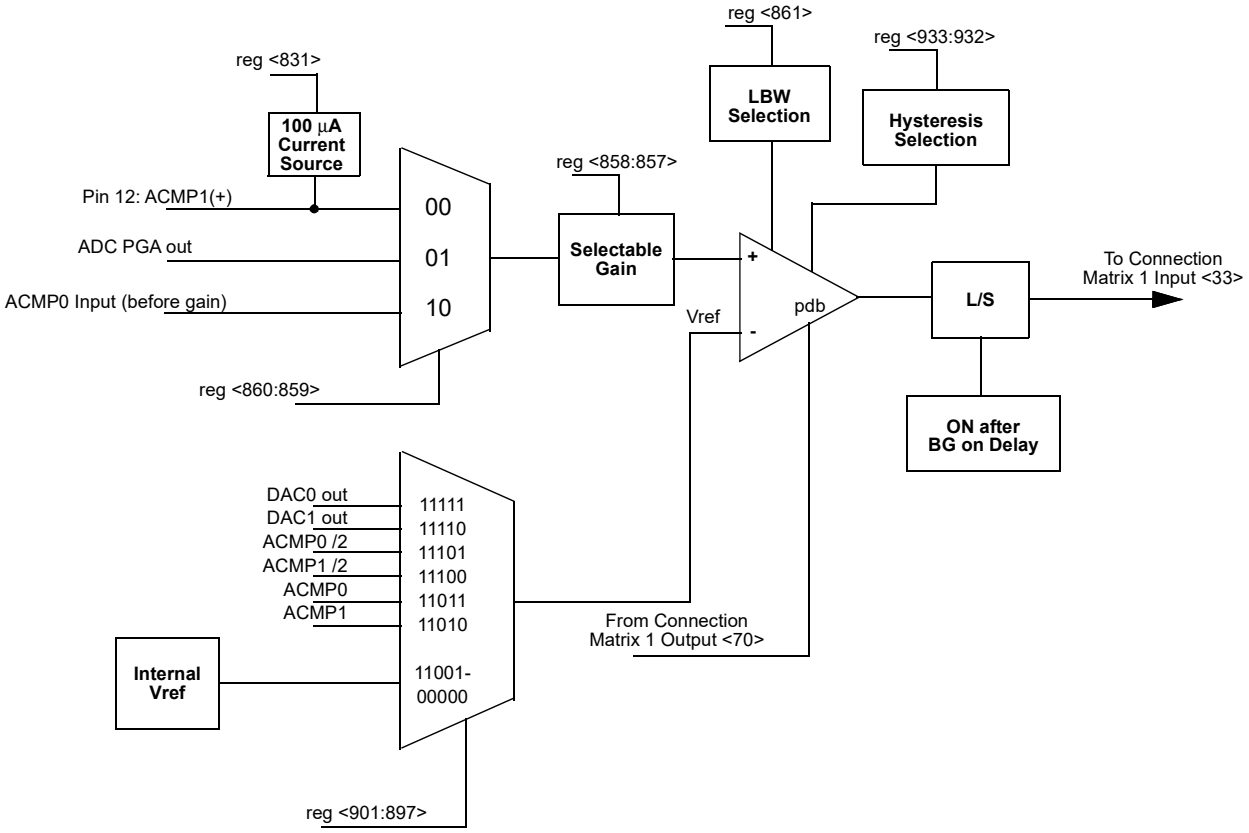


Figure 57. ACMP1 Block Diagram

13.5 ACMP1 Register Settings

Table 77. ACMP1 Register Settings

Signal Function	Register Bit Address	Register Definition
ACMP1 Hysteresis Enable	reg<933:932>	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV)
ACMP1 In Voltage Select	reg<901:897>	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: Vdd/3 11001: Vdd/4 11010: Vref_Ext_ACMP1 11011: Vref_Ext_ACMP0 11100: Vref_Ext_ACMP1 / 2 11101: Vref_Ext_ACMP0 / 2 11110: DAC1_out 11111: DAC0_out
ACMP1 Input Selection	<860:859>	00: PIN 12 Input 01: ADC PGA out 10: ACMP 0 Input (before Gain) 11: None
ACMP1 Positive Input Gain Control	reg<858:857>	00: 1.00X 01: 0.50X 10: 0.33X 11: 0.25X
ACMP1 Low Bandwidth (Max: 1 MHz) Enable	reg<861>	1: On 0: Off
ACMP1 Input 100u Current Source Enable	reg<831>	1: Disable 0: Enable

13.6 ACMP2 Block Diagram

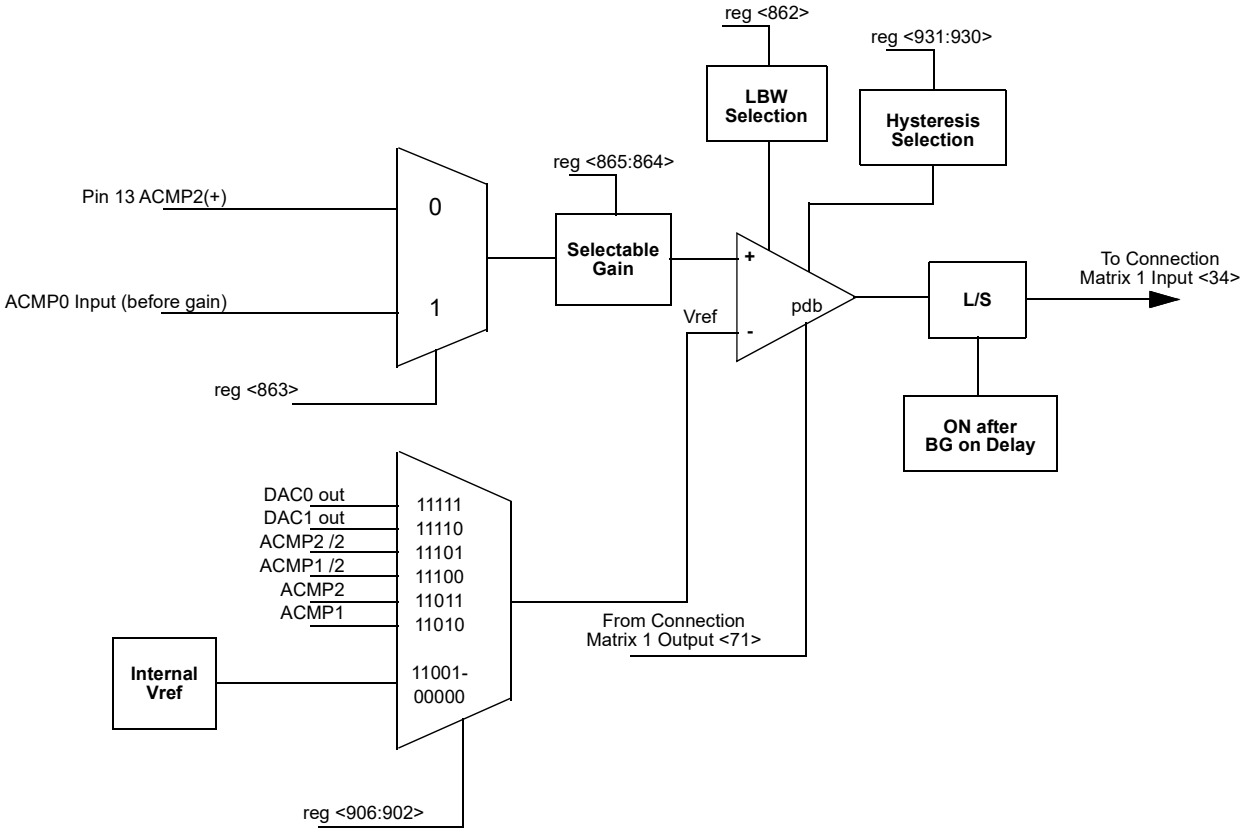


Figure 58. ACMP2 Block Diagram

13.7 ACMP2 Register Settings

Table 78. ACMP2 Register Settings

Signal Function	Register Bit Address	Register Definition
ACMP2 Hysteresis Enable	reg<931:930>	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV)
ACMP2 In Voltage Select	reg<906:902>	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: Vdd/3 11001: Vdd/4 11010: Vref_Ext_ACMP1 11011: Vref_Ext_ACMP2 11100: Vref_Ext_ACMP1 / 2 11101: Vref_Ext_ACMP2 / 2 11110: DAC1_out 11111: DAC0_out
ACMP2 Input Selection	reg<863>	0: PIN 13 Input 1: ACMP 0 Input (before Gain)
ACMP2 Positive Input Gain Control	reg<865:864>	00: 1.00X 01: 0.50X 10: 0.33X 11: 0.25X
ACMP2 Low Bandwidth (Max: 1 MHz) Enable	reg<862>	1: On 0: Off

13.8 ACMP3 Block Diagram

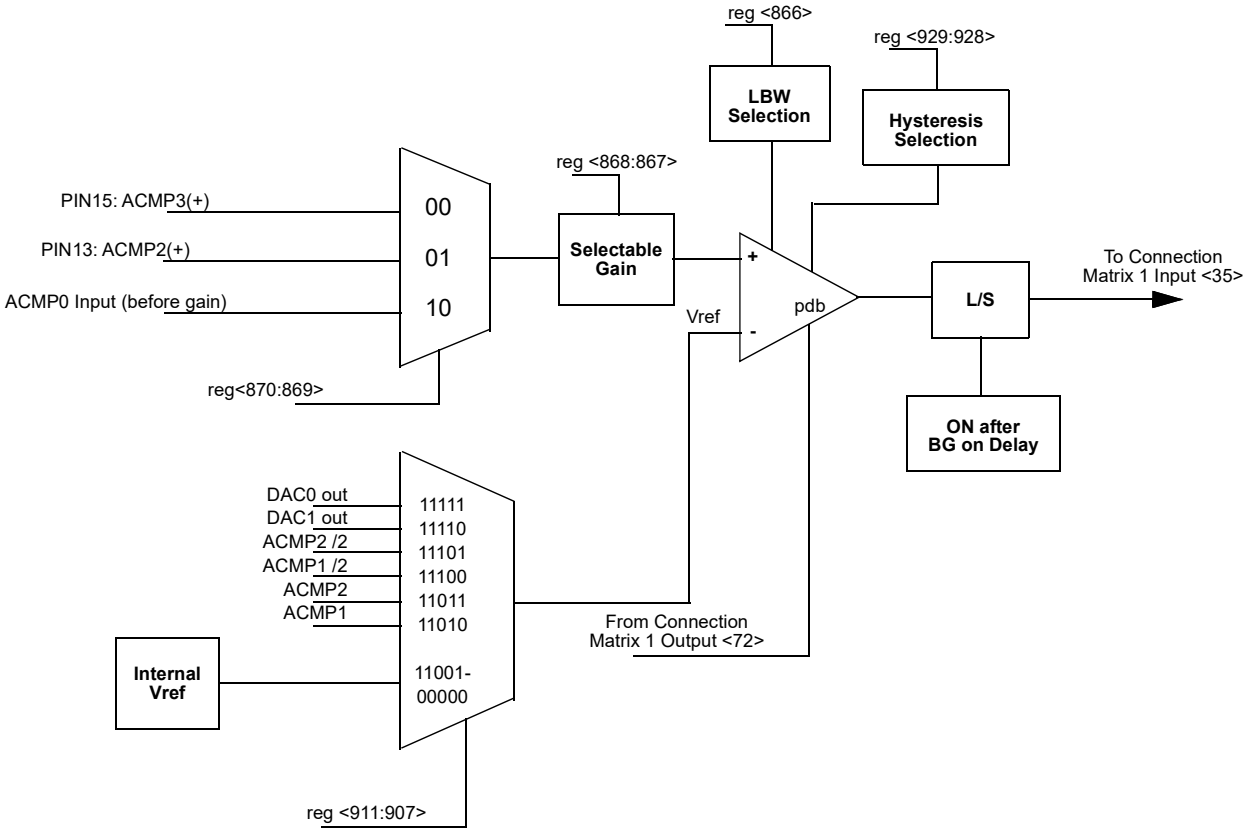


Figure 59. ACMP3 Block Diagram

13.9 ACMP3 Register Settings

Table 79. ACMP3 Register Settings

Signal Function	Register Bit Address	Register Definition
ACMP3 Hysteresis Enable	reg<929:928>	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV)
ACMP3 In Voltage Select	reg<911:907>	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: Vdd/3 11001: Vdd/4 11010: Vref_Ext_ACMP1 11011: Vref_Ext_ACMP2 11100: Vref_Ext_ACMP1 / 2 11101: Vref_Ext_ACMP2 / 2 11110: DAC1_out 11111: DAC0_out
ACMP3 Input Selection	reg<870:869>	00: PIN 15 Input 01: PIN 13 Input 10: ACMP 0 Input (before Gain) 11: None
ACMP3 Positive Input Gain Control	reg<868:867>	00: 1.00X 01: 0.50X 10: 0.33X 11: 0.25X
ACMP3 Low Bandwidth (Max: 1 MHz) Enable	reg<866>	1: On 0: Off

13.10 ACMP4 Block Diagram

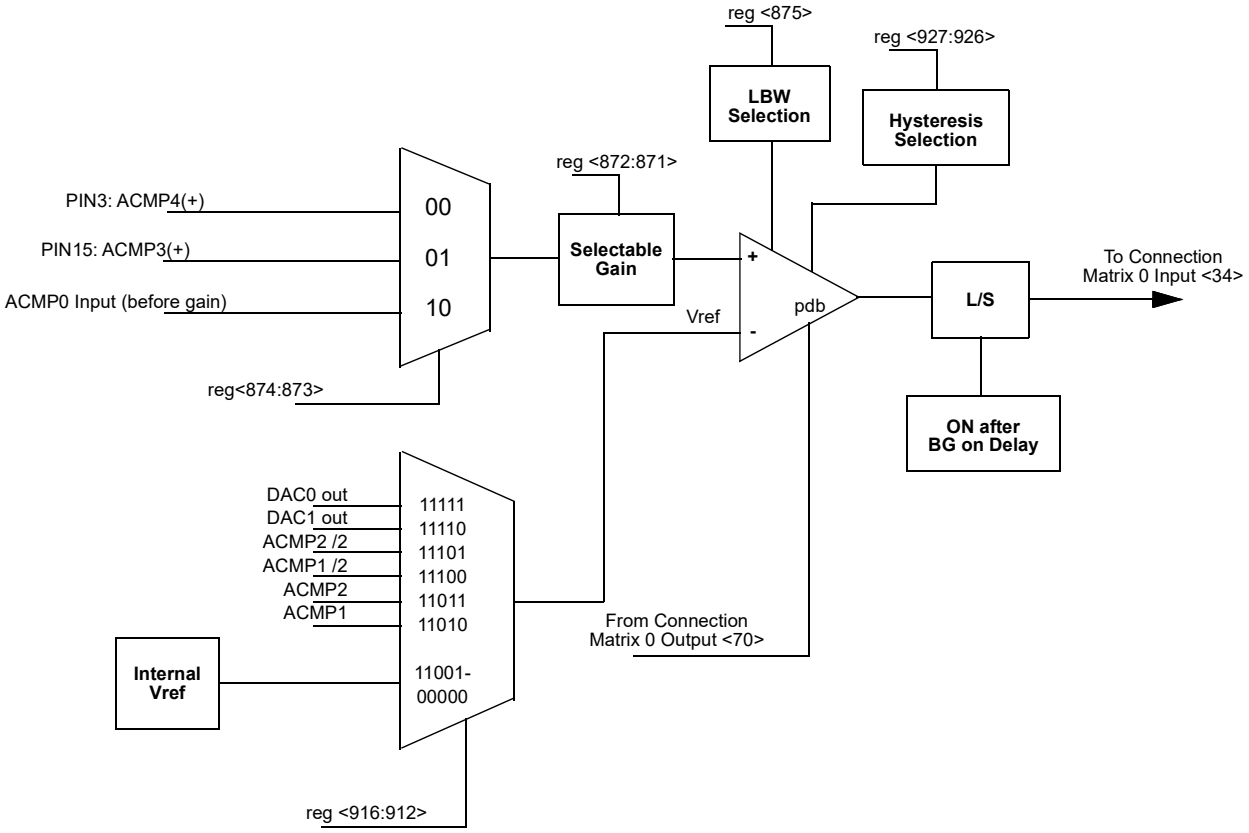


Figure 60. ACMP4 Block Diagram

13.11 ACMP4 Register Settings

Table 80. ACMP4 Register Settings

Signal Function	Register Bit Address	Register Definition
ACMP4 Hysteresis Enable	reg<927:926>	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV)
ACMP4 In Voltage Select	reg<916:912>	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: Vdd/3 11001: Vdd/4 11010: Vref_Ext_ACMP1 11011: Vref_Ext_ACMP2 11100: Vref_Ext_ACMP1 / 2 11101: Vref_Ext_ACMP2 / 2 11110: DAC1_out 11111: DAC0_out
ACMP4 Input Selection	reg<874:873>	00: PIN 3 Input 01: PIN 15 Input 10: ACMP 0 Input (before Gain) 11: None
ACMP4 Positive Input Gain Control	reg<872:871>	00: 1.00X 01: 0.50X 10: 0.33X 11: 0.25X
ACMP4 Low Bandwidth (Max: 1 MHz) Enable	reg<875>	1: On 0: Off

13.12 ACMP5 Block Diagram

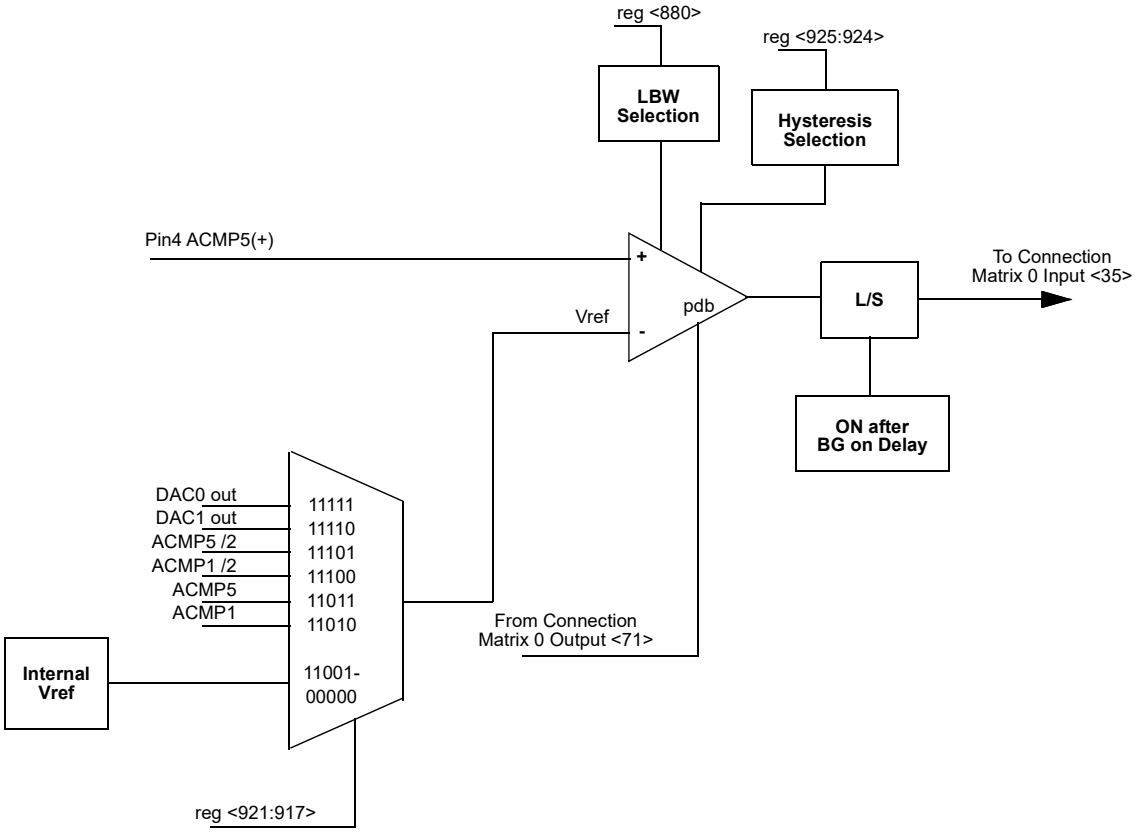


Figure 61. ACMP5 Block Diagram

13.13 ACMP5 Register Settings

Table 81. ACMP5 Register Settings

Signal Function	Register Bit Address	Register Definition
ACMP5 Hysteresis Enable	reg<925:924>	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV)
ACMP5 In Voltage Select	reg<921:917>	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: Vdd/3 11001: Vdd/4 11010: Vref_Ext_ACMP1 11011: Vref_Ext_ACMP5 11100: Vref_Ext_ACMP1 / 2 11101: Vref_Ext_ACMP5 / 2 11110: DAC1_out 11111: DAC0_out
ACMP5 Low Bandwidth (Max: 1 MHz) Enable	reg<880>	1: On 0: Off

14.0 Digital Storage Elements (DFFs/Latches)

There are twelve D Flip Flop / Latches (DFF/Latch) logic cells within the SLG46621 available for design. The source and destination of the inputs and outputs for the DFF/Latches are configured from the connection matrix. All DFF/Latch macrocells have user selection for initial state. The macrocells DFF0, DFF1, DFF2, DFF6, DFF7, and DFF8 have an additional input from the matrix that can serve as a nSet or nReset function to the macrocell.

The operation of the D Flip-Flop and Latch will follow the functional descriptions below:

DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change.

Latch: when CLK is Low, then Q = D; otherwise Q remains its previous value (input D has no effect on the output, when CLK is High).

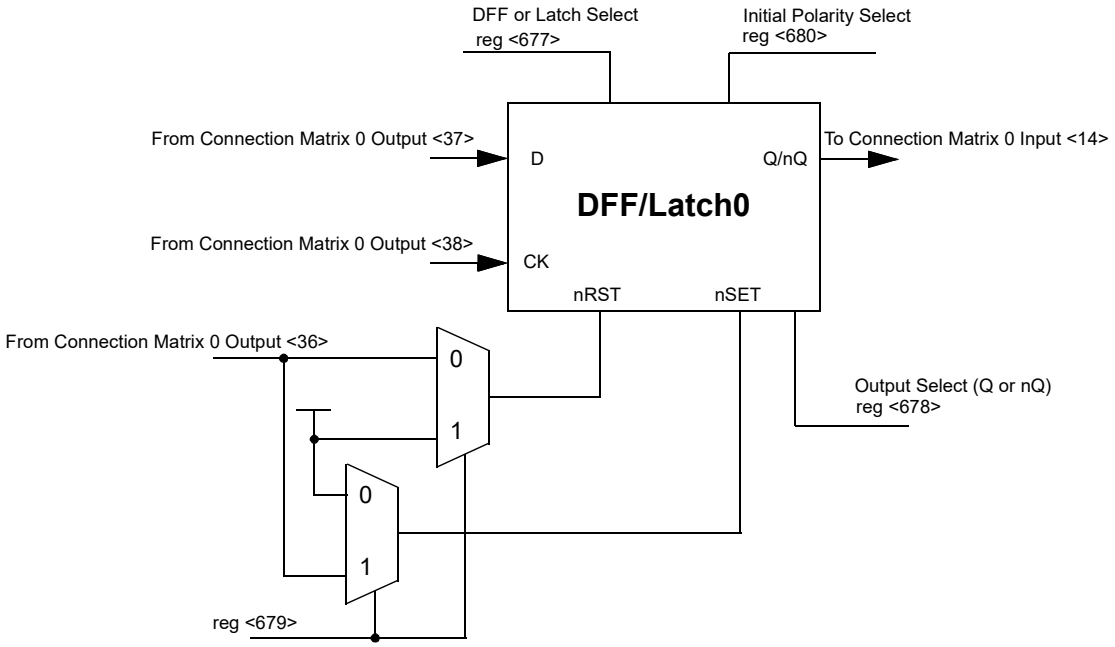


Figure 62. DFF/Latch0

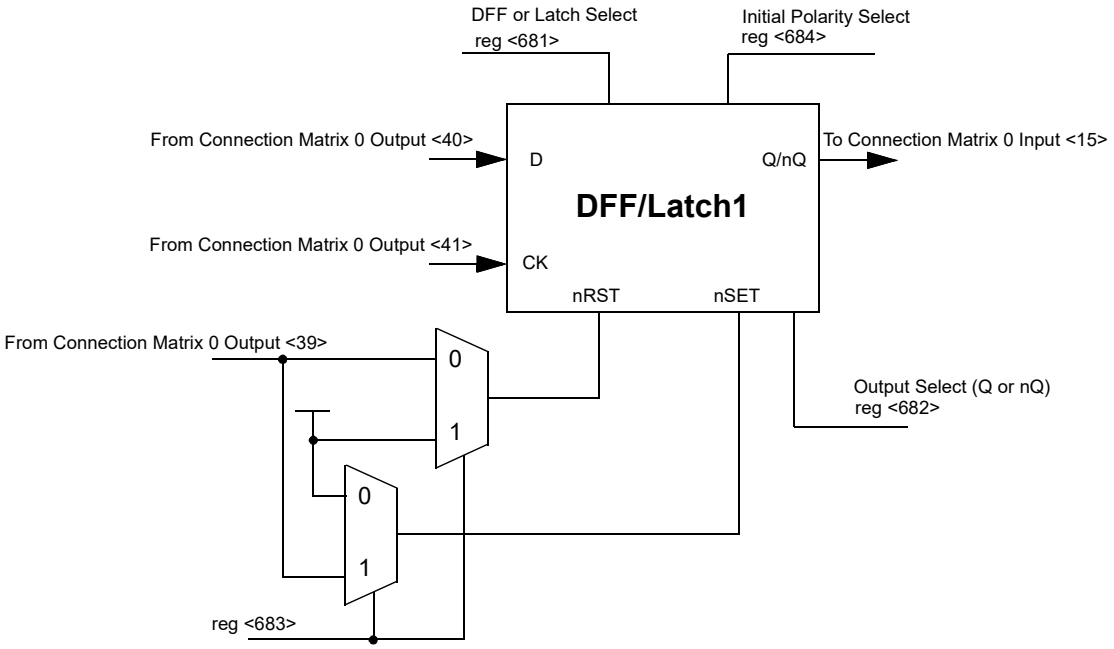


Figure 63. DFF/Latch1

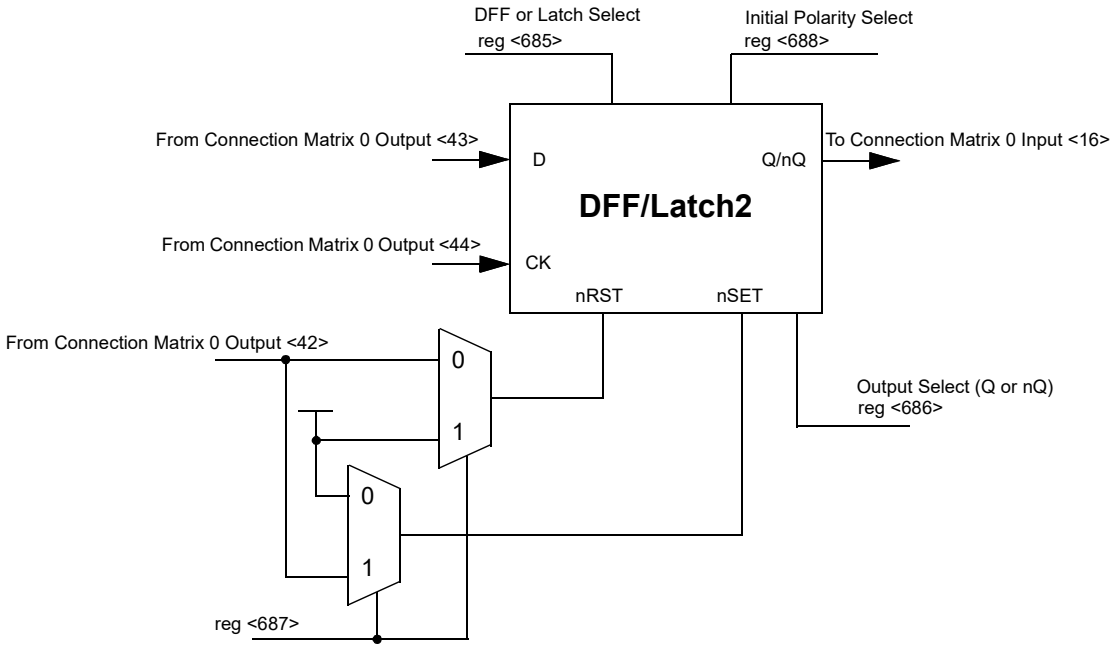


Figure 64. DFF/Latch2

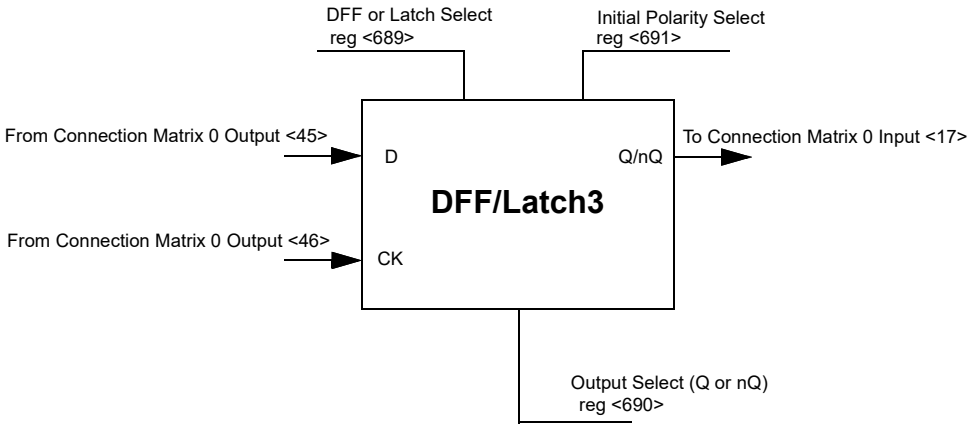


Figure 65. DFF/Latch3

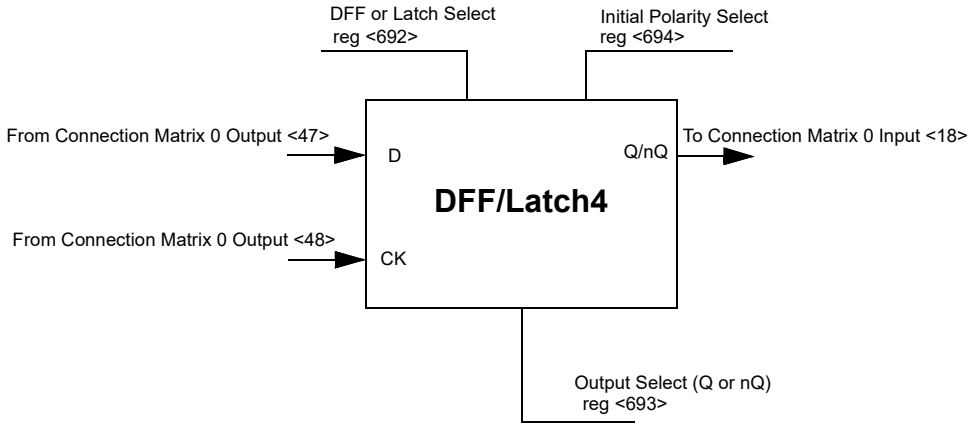


Figure 66. DFF/Latch4

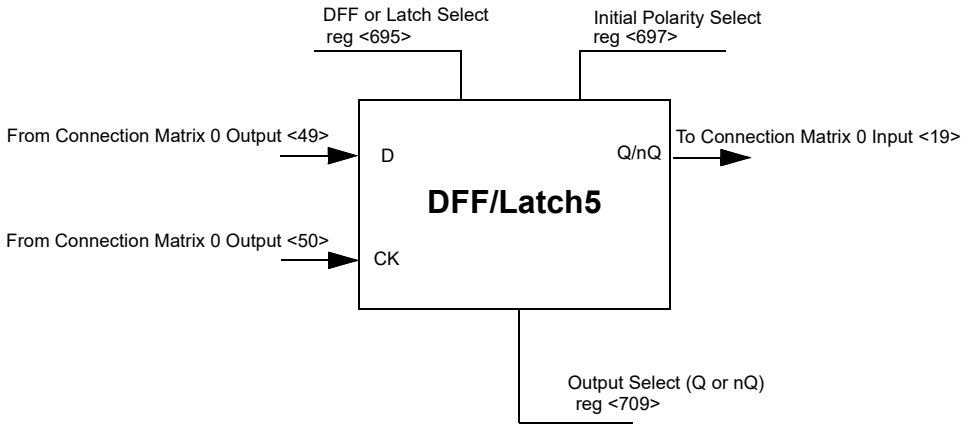


Figure 67. DFF/Latch5

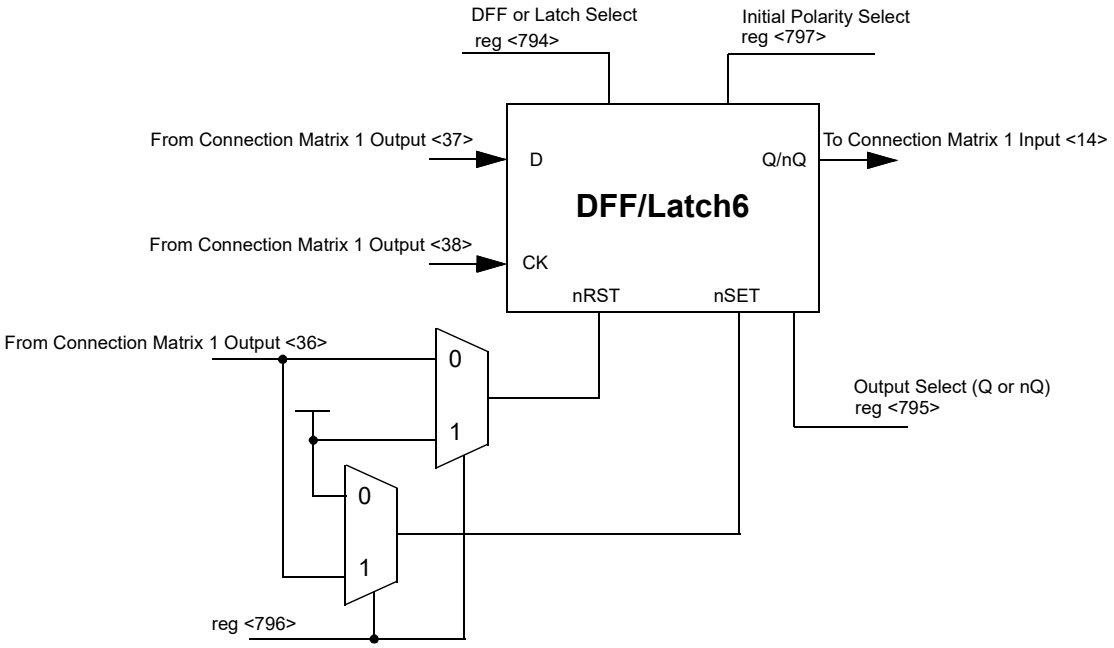


Figure 68. DFF/Latch6

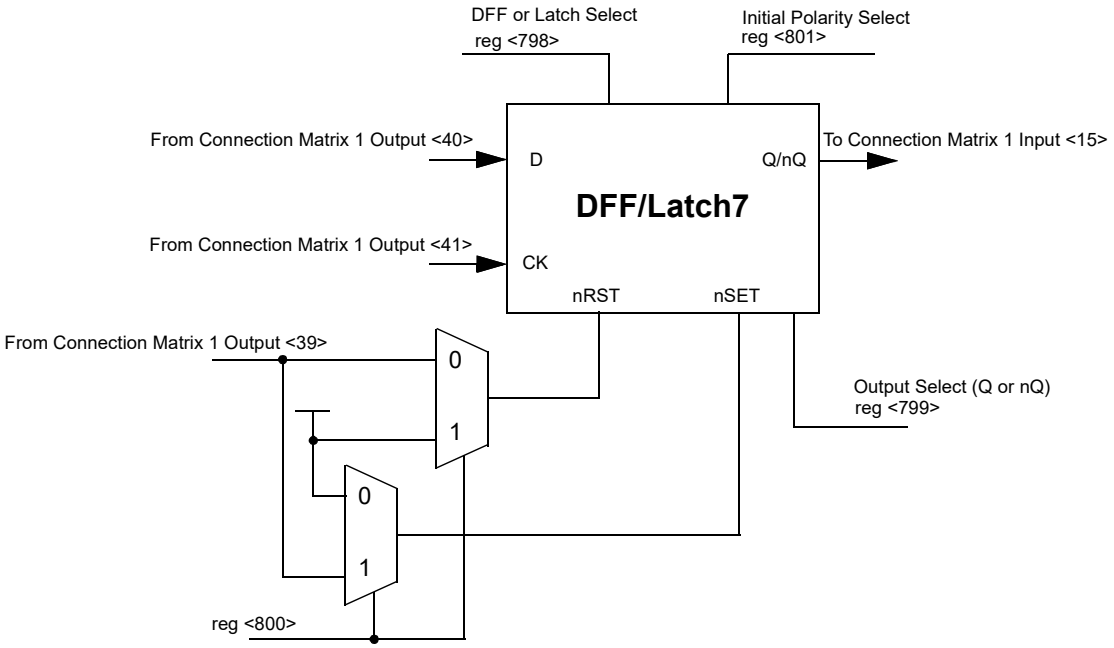


Figure 69. DFF/Latch7

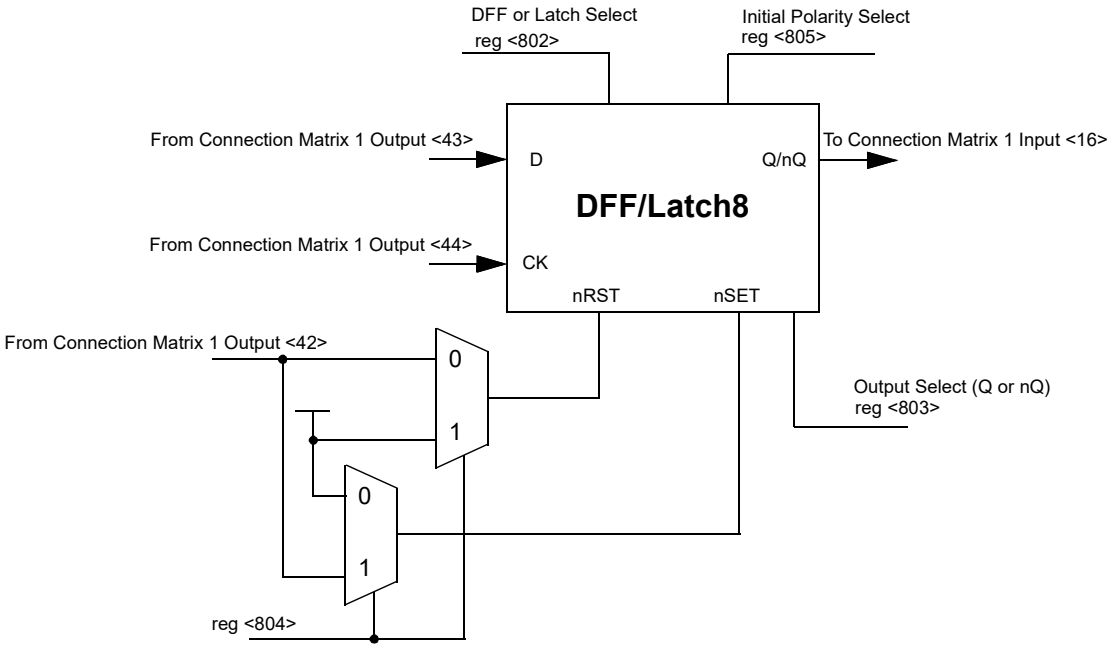


Figure 70. DFF/Latch8

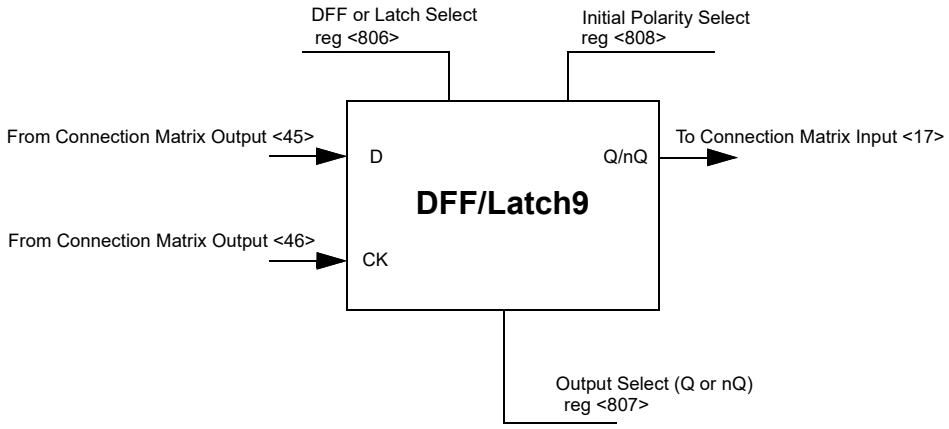


Figure 71. DFF/Latch9

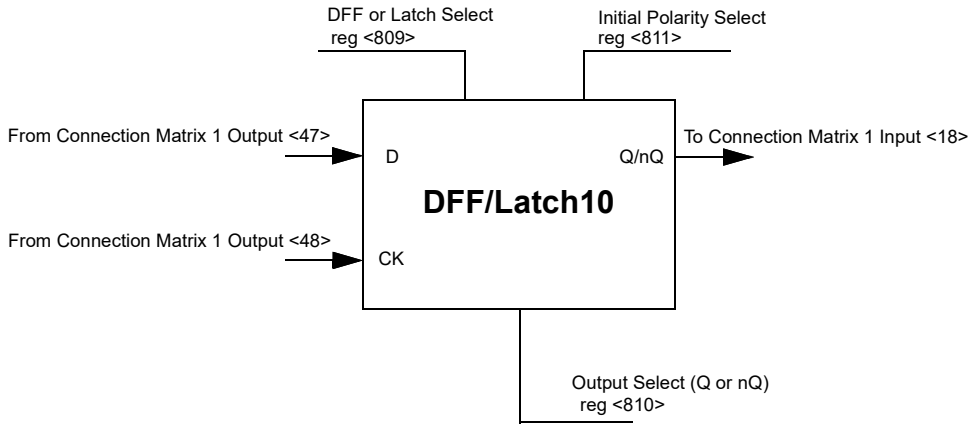


Figure 72. DFF/Latch10

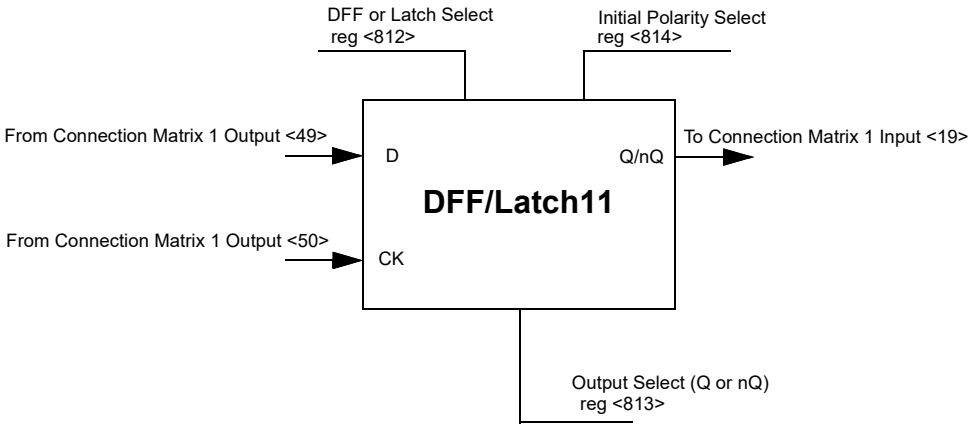


Figure 73. DFF/Latch11

14.1 Initial Polarity Operations

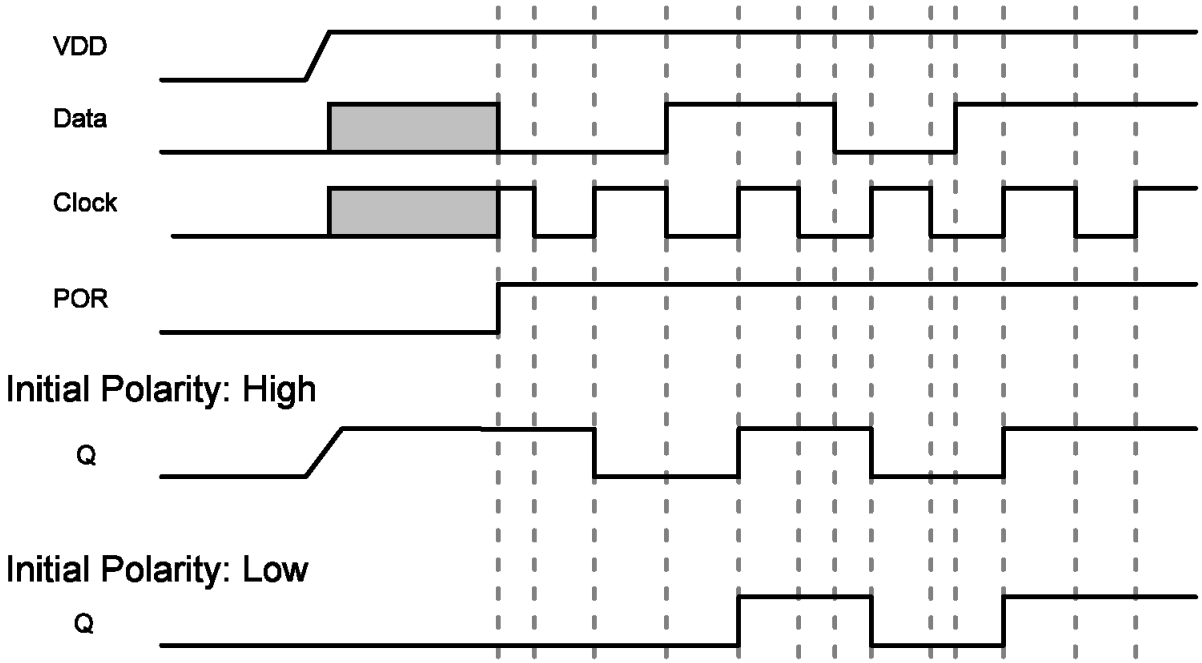


Figure 74. DFF Polarity Operations

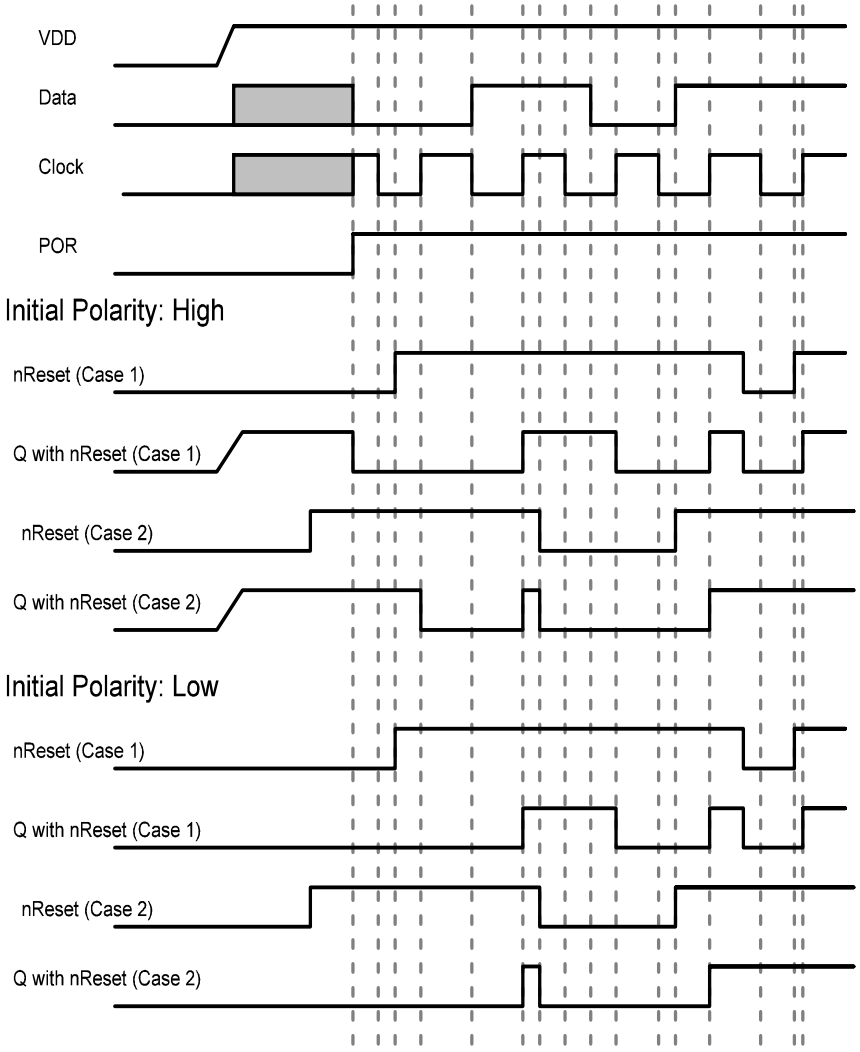


Figure 75. DFF Polarity Operations with nReset

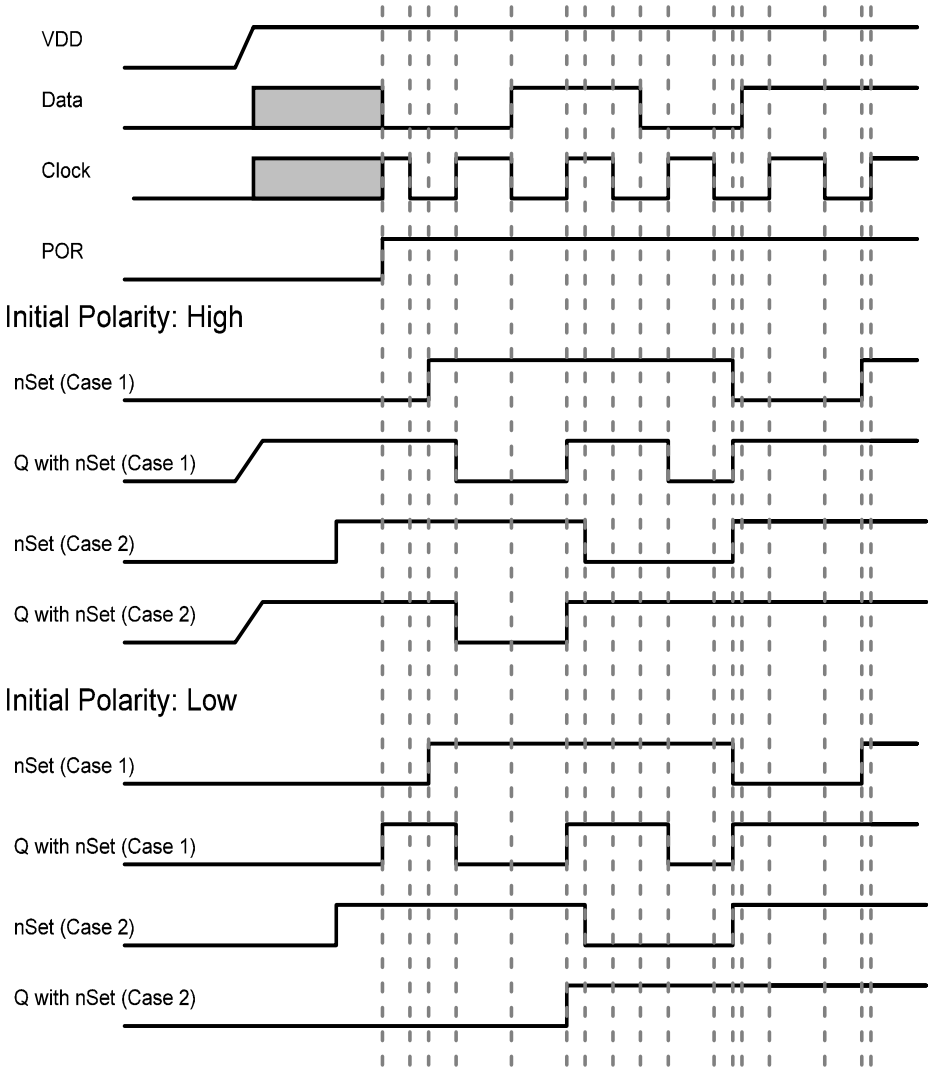


Figure 76. DFF Polarity Operations with nSet

15.0 Counters/Delay Generators (CNT/DLY)

There are ten configurable counters/delay generators in the SLG46621. Four of these counters/delay generators (CNT/DLY 0, 1, 2 and 3) are 14-bit, and six of the counters/delay generators (CNT/DLY 4, 5, 6, 7, 8 and 9) are 8-bit. Each macrocell has a dedicated matrix input connection, some of the macrocells have additional matrix connections to support optional functions, as listed below. For flexibility, each of these macrocells has a large selection of internal and external clock sources, as well as the option to chain from the output of the previous (N-1) CNT/DLY macrocell, to implement longer count / delay circuits.

The delay time and counter output equation is as follows:

Delay time = ((counter data + 1) + variable) / Clock
*Variable = (0 or 1) * period*
Counter period = (counter data + 1) / Clock

Note: Variable can be negative, since OSC can operate while Delay input changes. In this case it might be possible that we will not see first period, if OSC rising edge appears immediately after input change.

Counter/delay macrocells (0,2,5,6,9) are connected to Matrix 0 with both inputs and outputs , counter/delay macrocells (1,3,4,7,8) are connected to Matrix 1 with both inputs and outputs.

Four of the counter/delay generator macrocells (CNT/DLY 0,1,2,3) have an optional Edge Detector function

Two of the counter/delay generator macrocells (CNT/DLY 2,4) have an optional Finite State Machine (FSM) function. These two macrocells each have two additional matrix inputs for Up and Keep to support FSM functionality

Two of the counter/delay generator macrocells (CNT/DLY 8,9) have an optional PWM Ramp function.

One of the counter/delay generator macrocells (CNT/DLY 0) can optionally serve as a Wake/Sleep Counter.

Please see table below for a summary of all optional functions:

Table 82. Counter/Delay Macrocell Functions Summary

Macrocell	Bit-Width	Counter	Delay	Finite State Machine (FSM)	PWM Ramp	Edge Detector	Wake/Sleep Counter
CNT/DLY0	14-bit	X	X			X	X
CNT/DLY1	14-bit	X	X			X	
CNT/DLY2	14-bit	X	X	X		X	
CNT/DLY3	14-bit	X	X			X	
CNT/DLY4	8-bit	X	X	X			
CNT/DLY5	8-bit	X	X				
CNT/DLY6	8-bit	X	X				
CNT/DLY7	8-bit	X	X				
CNT/DLY8	8-bit	X	X		X		
CNT/DLY9	8-bit	X	X		X		

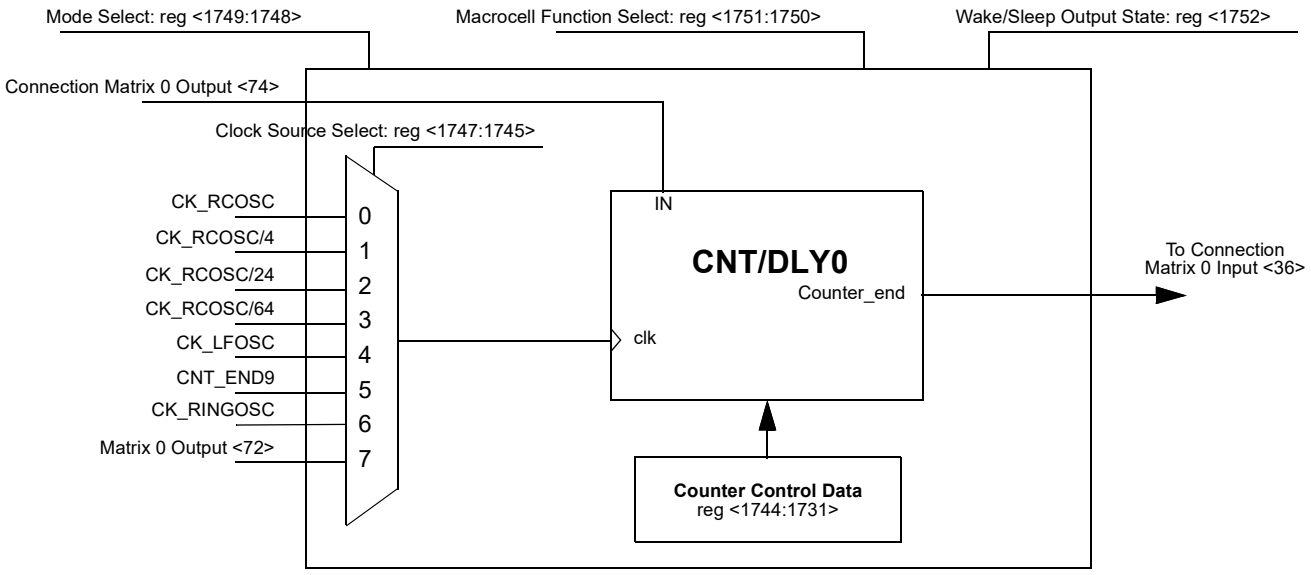


Figure 77. CNT/DLY0

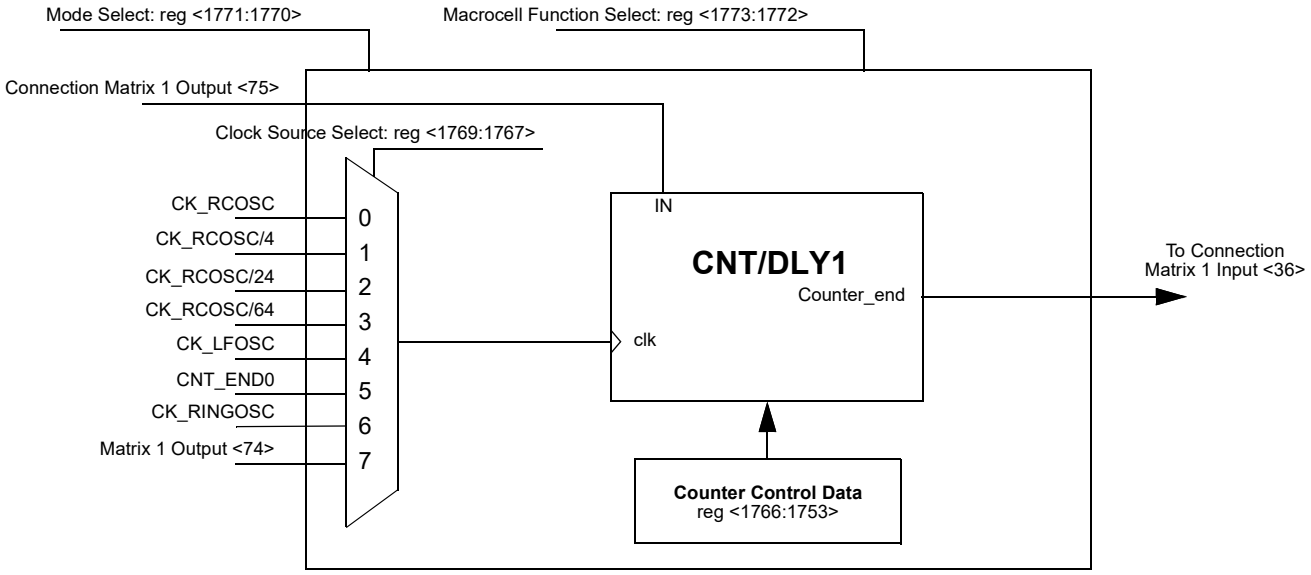


Figure 78. CNT/DLY1

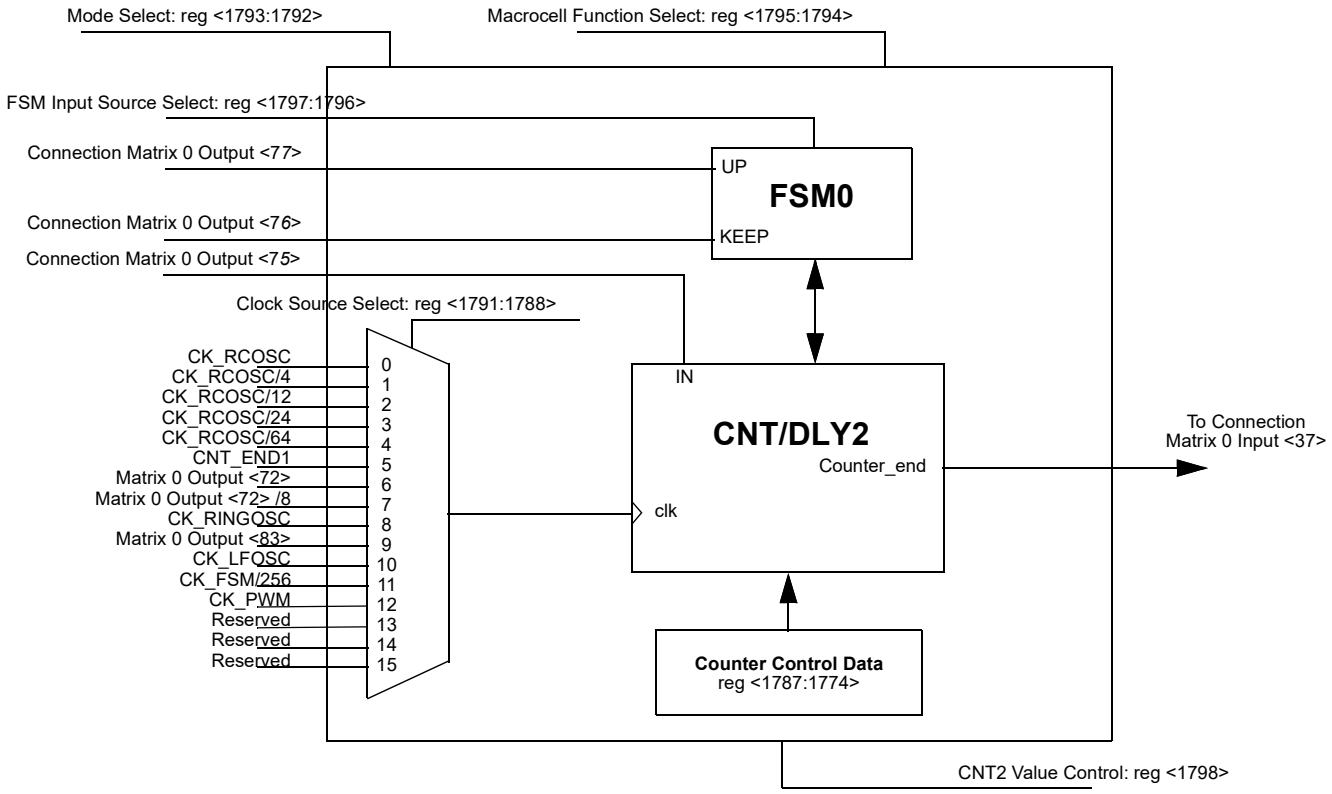


Figure 79. CNT/DLY2/FSM0

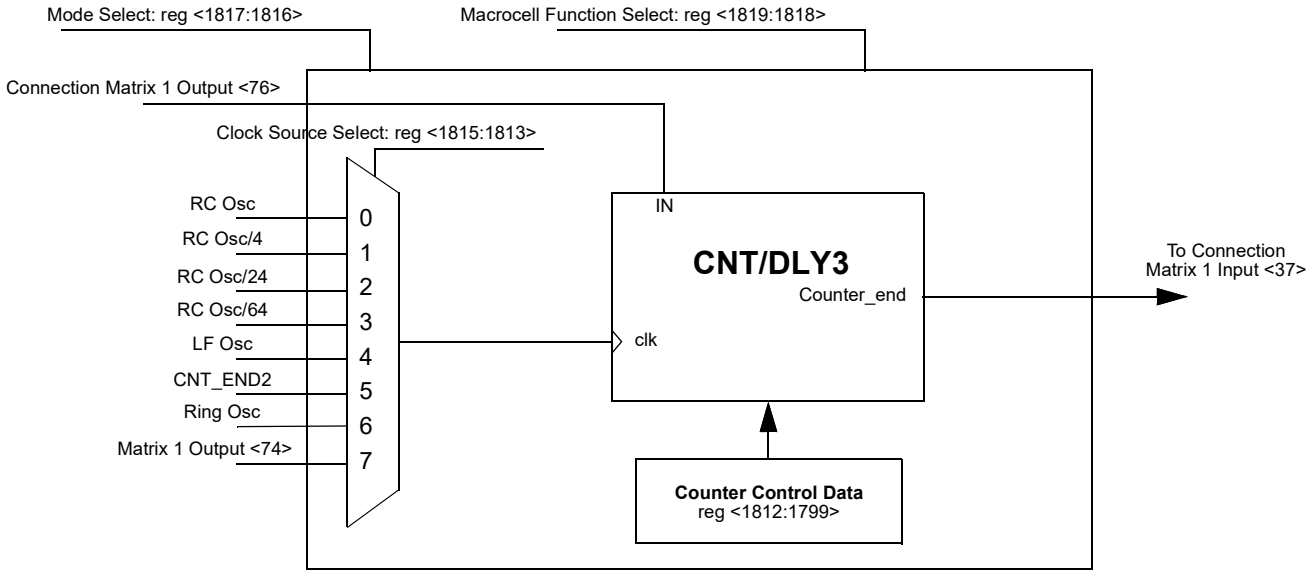


Figure 80. CNT/DLY3

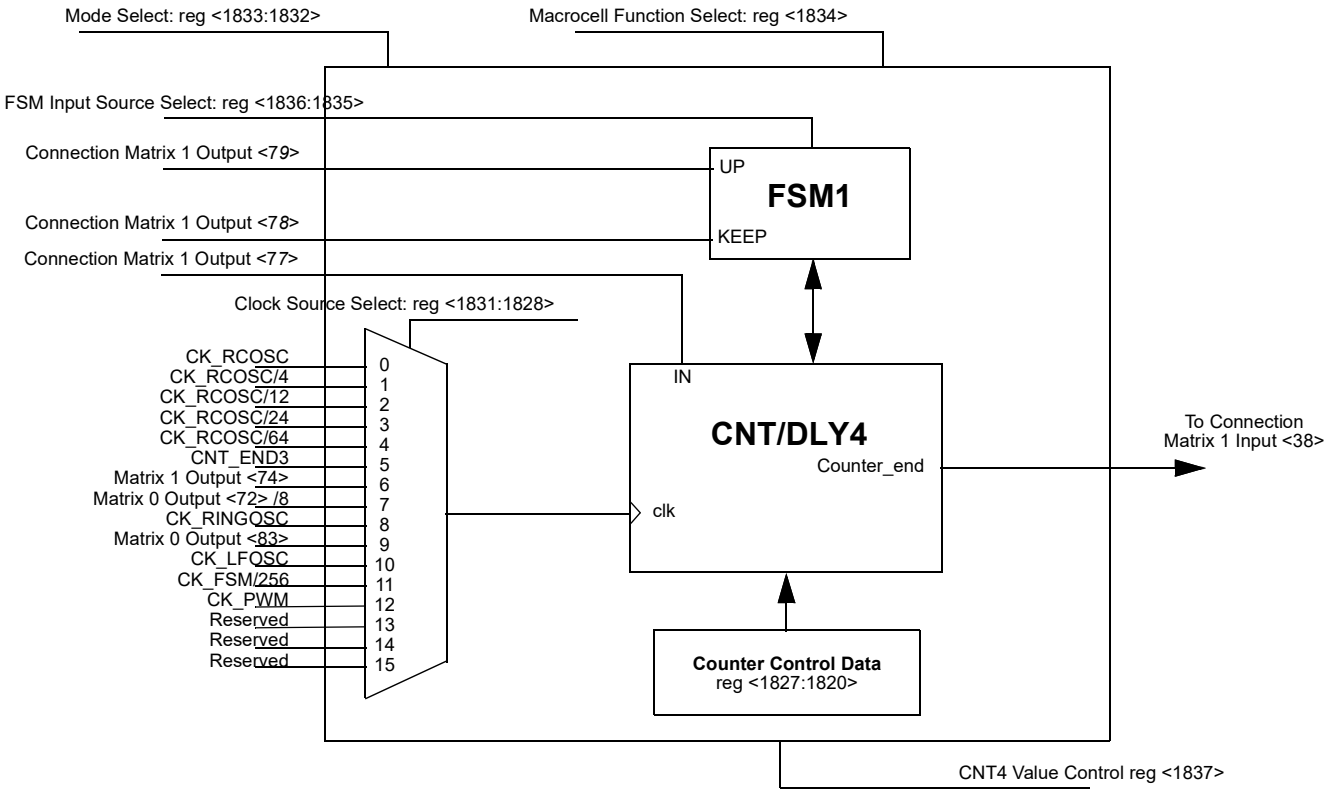


Figure 81. CNT/DLY4/FSM0

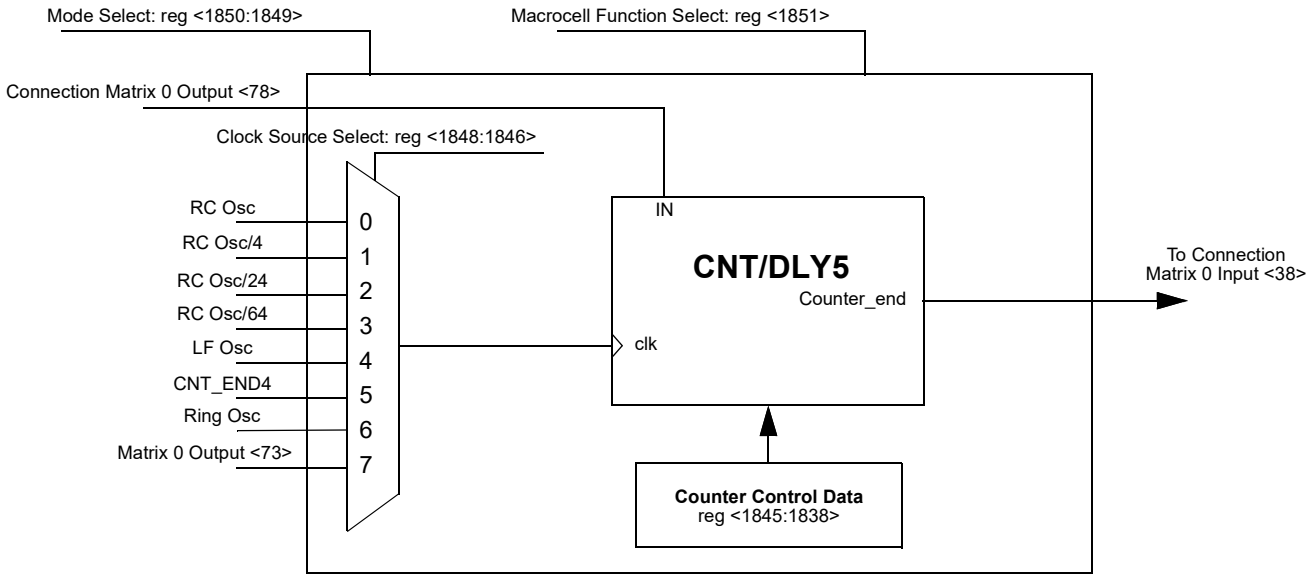


Figure 82. CNT/DLY5

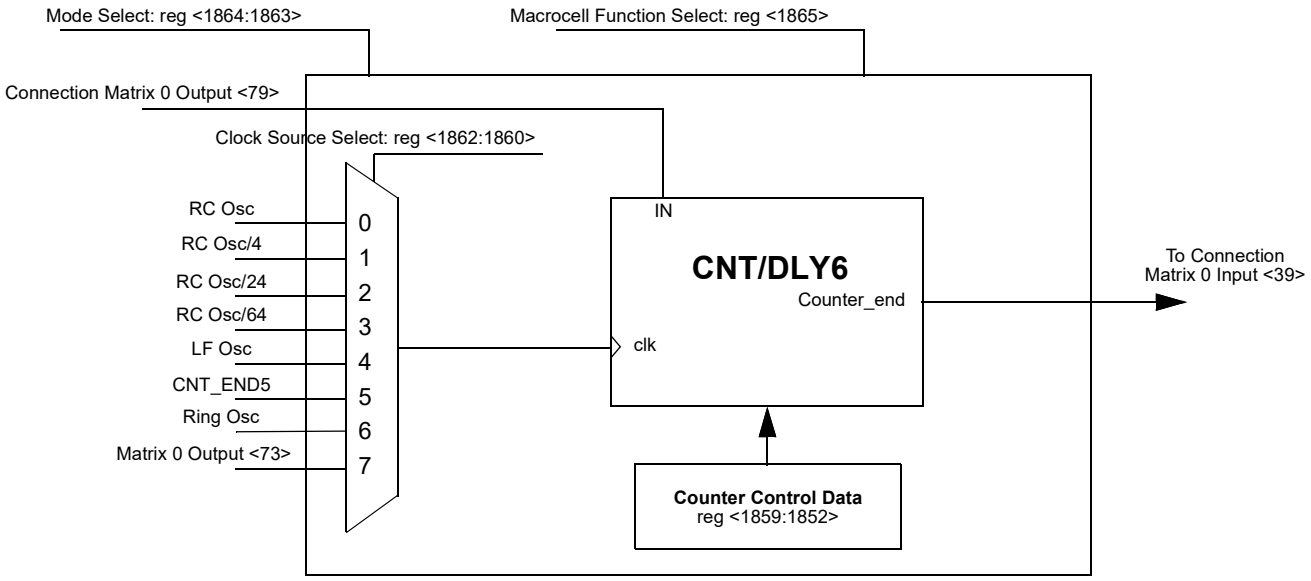


Figure 83. CNT/DLY6

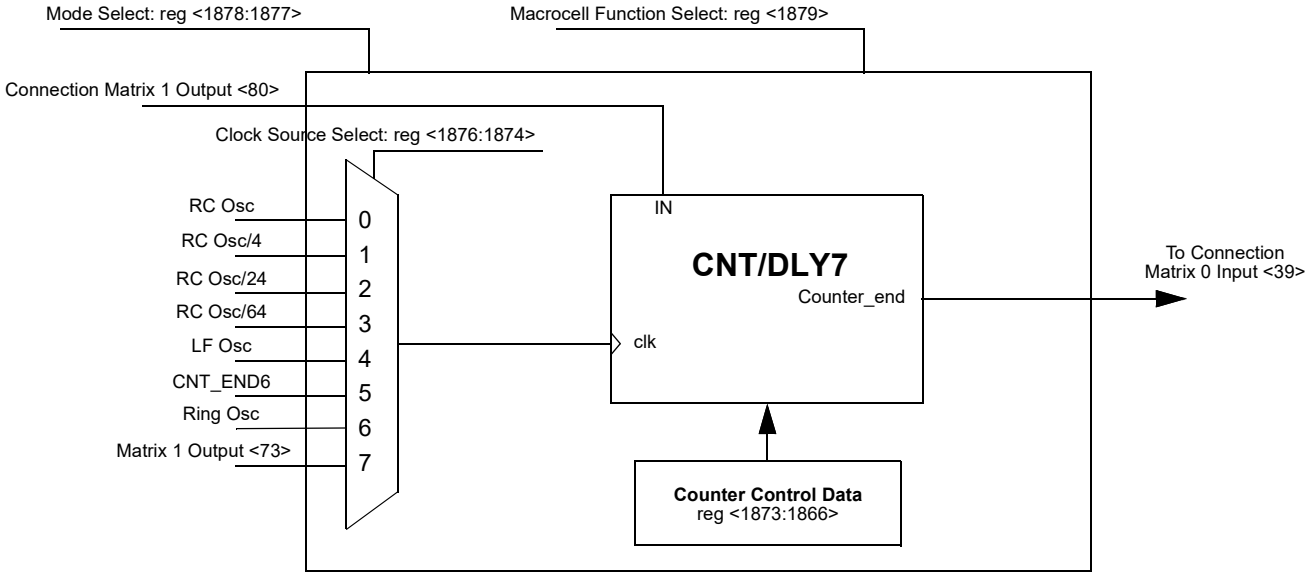


Figure 84. CNT/DLY7

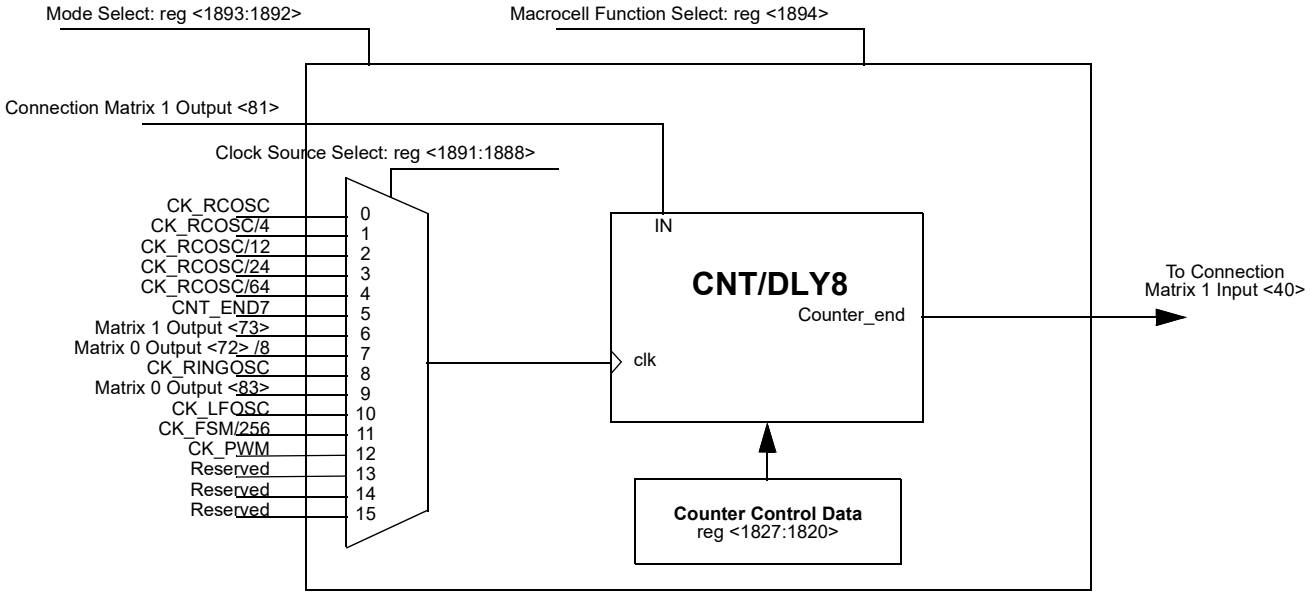


Figure 85. CNT/DLY8/PWM_RAMP

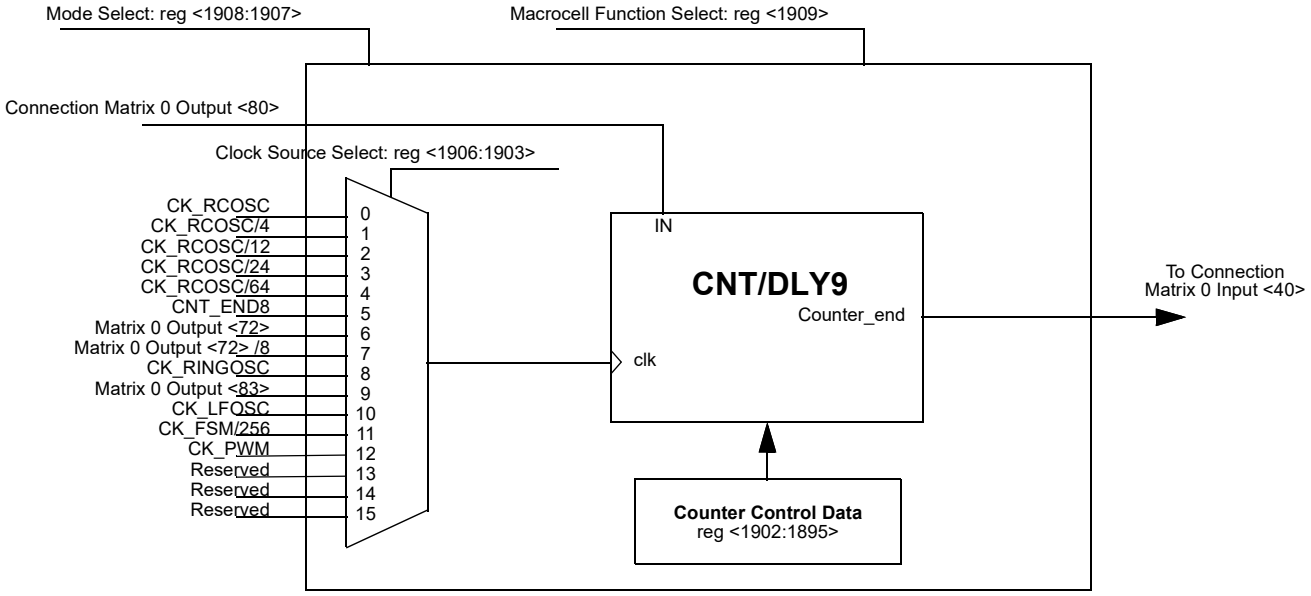


Figure 86. CNT/DLY9/PWM_RAMP

15.1 CNT/DLY Timing Diagrams

15.1.1 Delay Mode

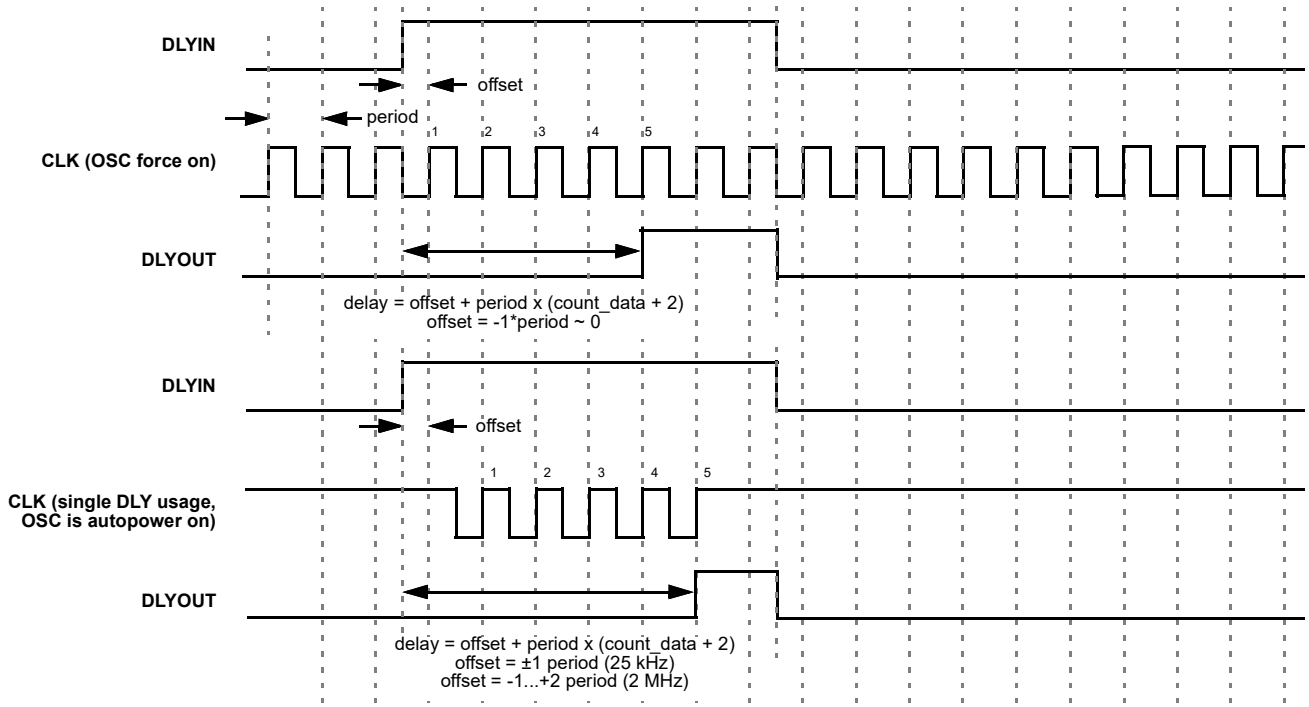


Figure 87. Timing (rising edge) for count data = 3

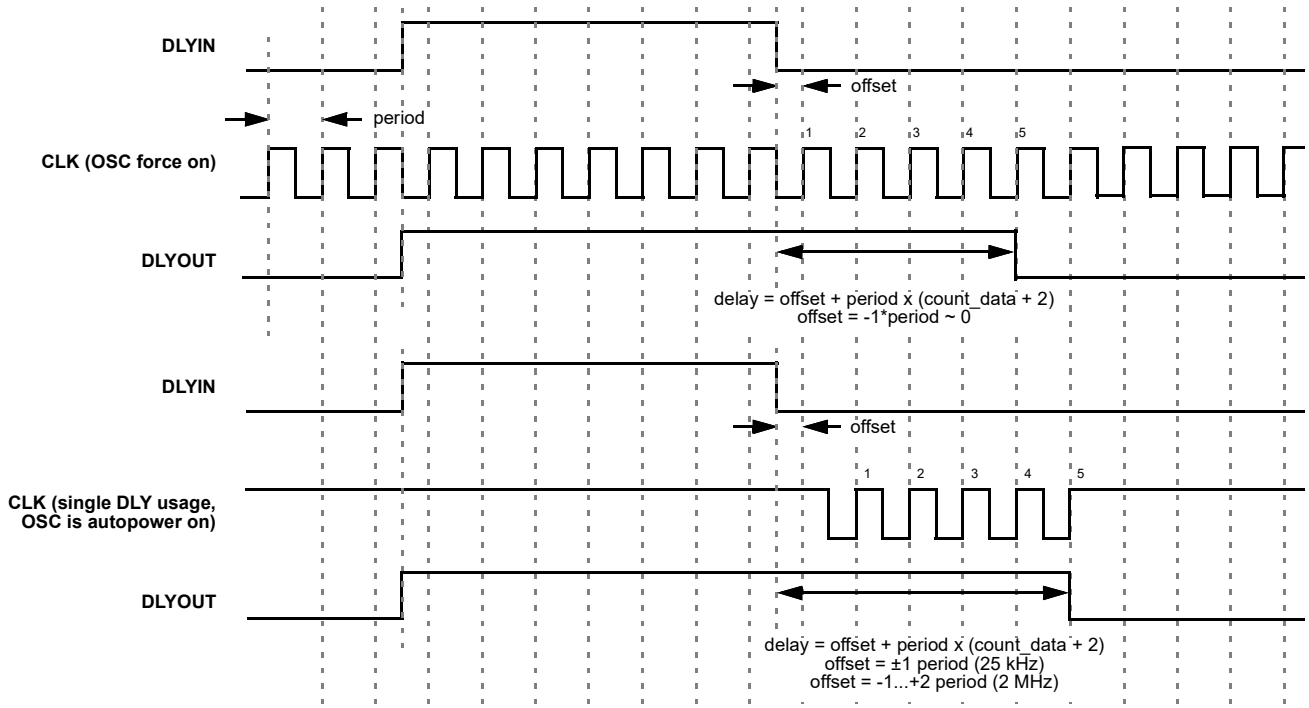


Figure 88. Timing (falling edge) for count data = 3

15.1.2 Counter Mode

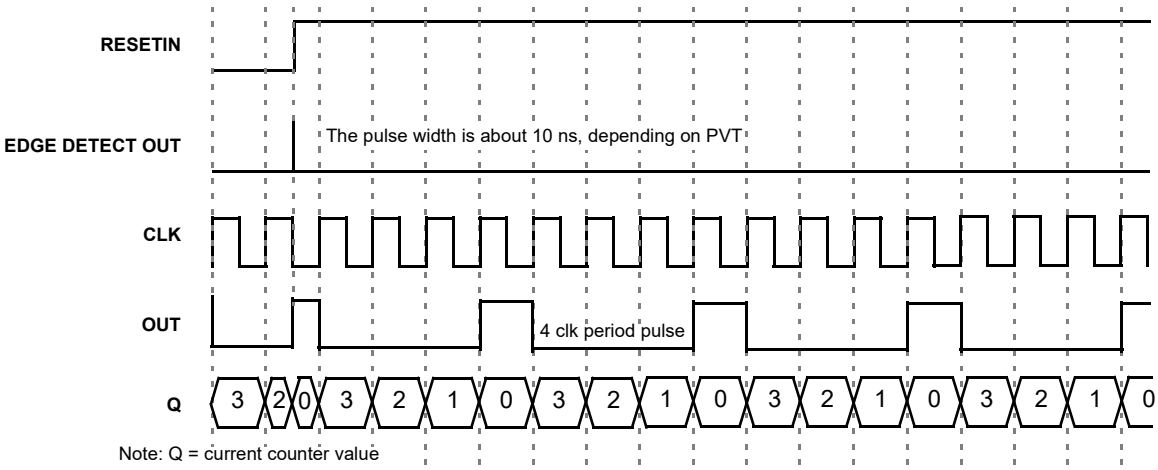


Figure 89. Timing (reset rising edge mode, oscillator is forced on) for count data = 3

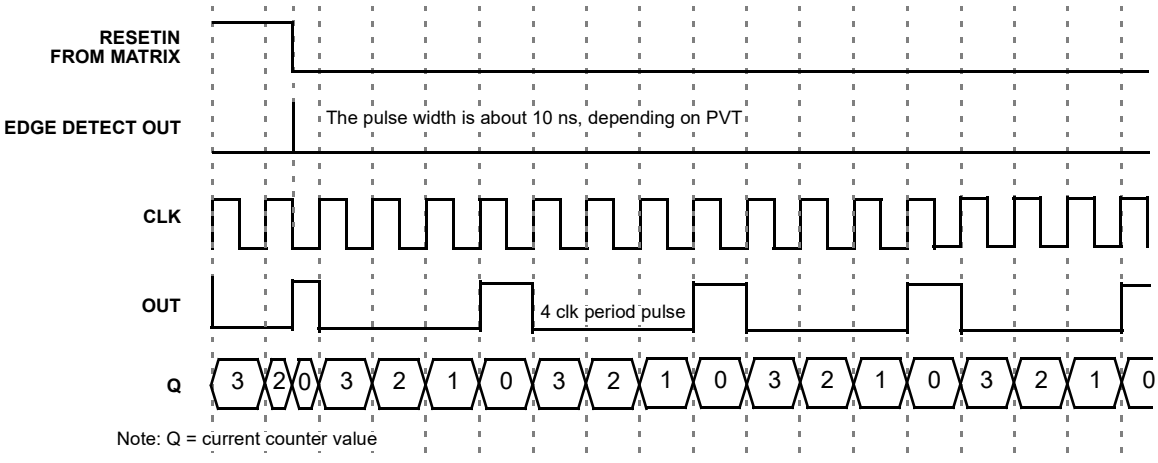


Figure 90. Timing (reset falling edge mode, oscillator is forced on) for count data = 3

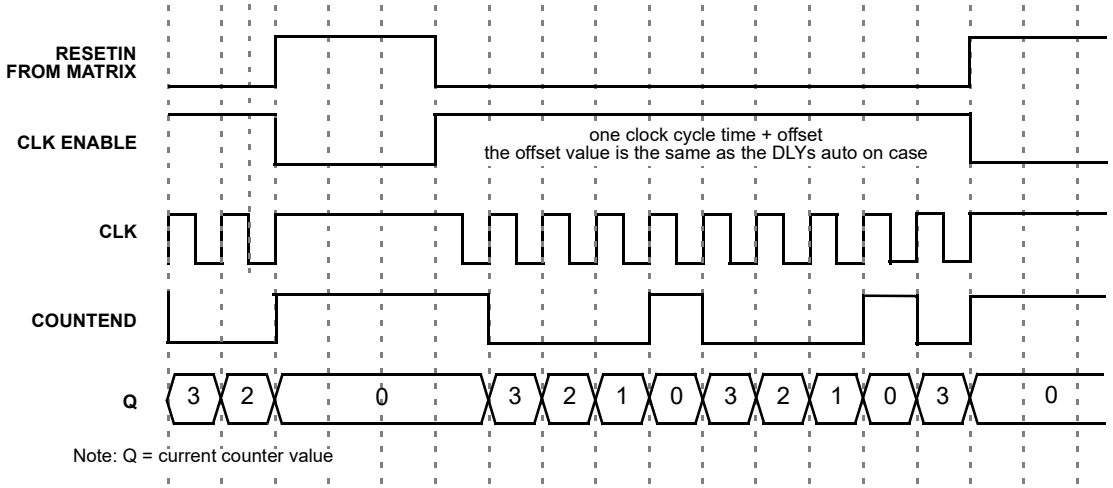


Figure 91. Timing (reset high level mode, oscillator is autopowered on (controlled by reset)) for count data = 3

15.1.3 FSM Mode

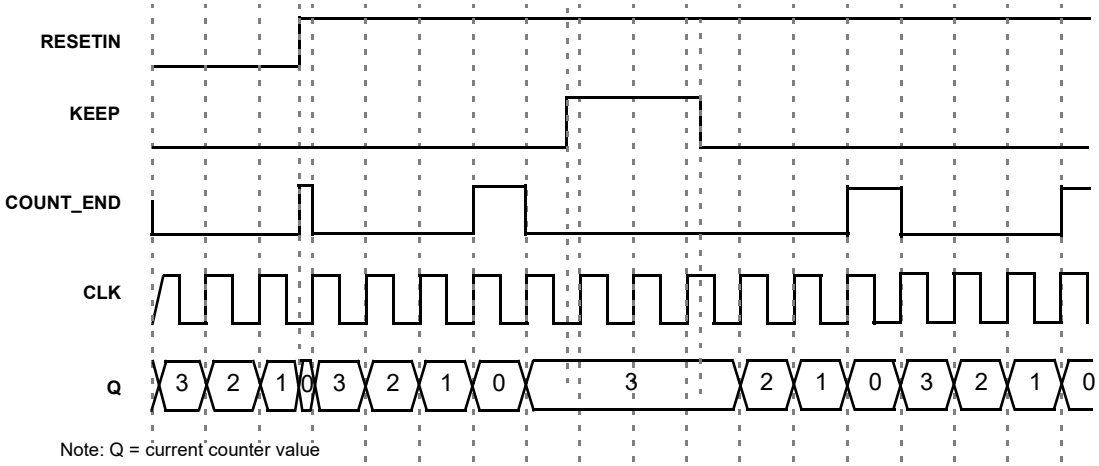


Figure 92. Timing (reset rising edge mode, oscillator is forced on, UP=0) for count data = 3

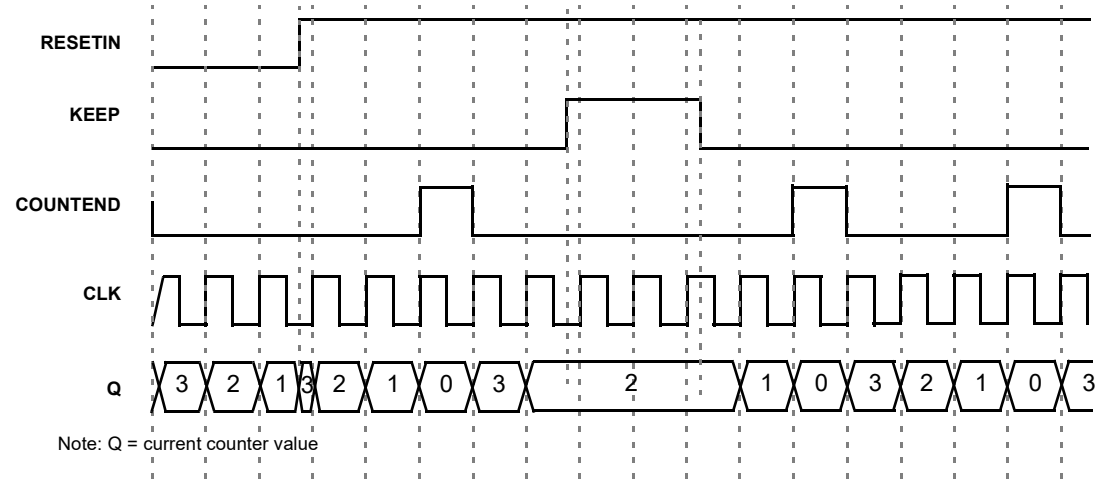


Figure 93. Timing (set rising edge mode, oscillator is forced on, UP=0) for count data = 3

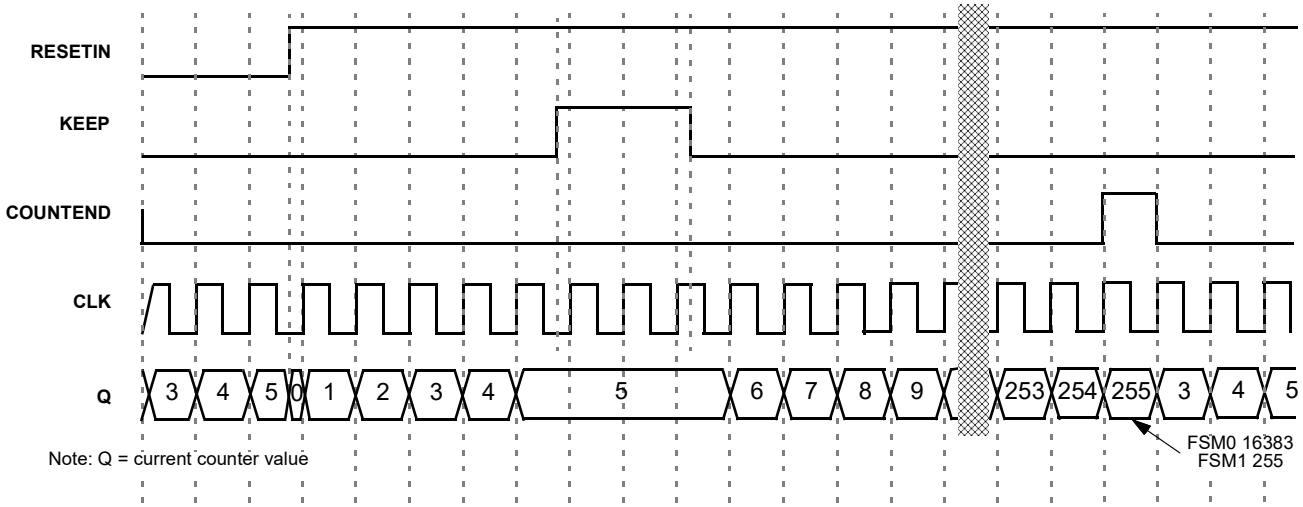


Figure 94. Timing (reset rising edge mode, oscillator is forced on, UP=1) for count data = 3

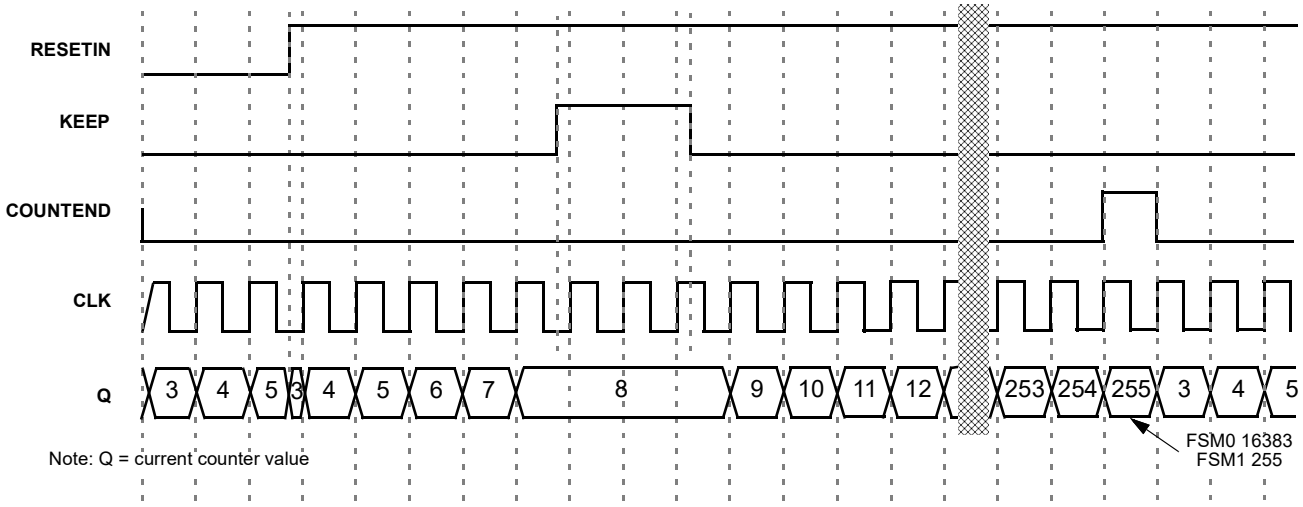


Figure 95. Timing (set rising edge mode, oscillator is forced on, UP=1) for count data = 3

15.2 CNT/DLY0 Register Settings

Table 83. CNT/DLY0 Register Settings

Signal Function	Register Bit Address	Register Definition
CNT0 14bits data From Register	reg<1744:1731>	data
CNT/DLY0 Clock Source Select	reg<1747:1745>	000: CK_RCOSC 001: CK_RCOSC_DIV4 010: CK_RCOSC_DIV24 011: CK_RCOSC_DIV64 100: CK_LFOSC 101: CNT_END9 110: CK_RINGOSC 111: Matrix0_out72
DLY0 Edge Mode Select or CNT0 Reset Mode Select	reg<1749:1748>	If DLY Mode; 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNTReset Mode; 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
CNT/DLY0 Macrocell Function Select	reg<1751:1750>	00: DLY 01: CNT 10: Edge Detect 11: Wake Sleep Ratio Control
Wake Sleep Output State When WS Oscillator is Power Down	reg<1752>	0: in Power Down Mode 1: in normal operation State

15.3 CNT/DLY1 Register Settings

Table 84. CNT/DLY1 Register Settings

Signal Function	Register Bit Address	Register Definition
CNT1 14bits data From Register	reg<1766:1753>	data
CNT/DLY1 Clock Source Select	reg<1769:1767>	000: CK_RCOSC 001: CK_RCOSC_DIV4 010: CK_RCOSC_DIV24 011: CK_RCOSC_DIV64 100: CK_LFOSC 101: CNT_END0 110: CK_RINGOSC 111: Matrix1_out74

Table 84. CNT/DLY1 Register Settings

Signal Function	Register Bit Address	Register Definition
DLY1 Edge Mode Select or CNT1 Reset Mode Select	reg<1771:1770>	If DLY Mode; 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNTReset Mode; 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
CNT/DLY1 Macrocell Function Select	reg<1773:1772>	00: DLY 01: CNT 10: Edge Detect 11: Reserved

15.4 CNT/DLY2/FSM0 Register Settings

Table 85. CNT/DLY2/FSM0 Register Settings

Signal Function	Register Bit Address	Register Definition
CNT2 14bits data From Register	reg<1787:1774>	data
CNT/DLY2/FSM0 Clock Source Select	reg<1791:1788>	0000: CK_RCOSC 0001: CK_RCOSC_DIV4 0010: CK_RCOSC_DIV12 0011: CK_RCOSC_DIV24 0100: CK_RCOSC_DIV64 0101: CNT_END1 0110: Matrix0_out72 0111: Matrix0_out72 divide by 8 1000: CK_RINGOSC 1001: Matrix0_out83(SPI_SCLK) 1010: CK_LFOSC 1011: CK_FSM_DIV256 1100: CK_PWM 1101: Reserved 1110: Reserved 1111: Reserved
DLY2 Edge Mode Select or CNT2 Reset Mode Select	reg<1793:1792>	If DLY Mode; 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNTReset Mode; 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
CNT/DLY2/FSM0 Macrocell Function Select	reg<1795:1794>	00: DLY 01: CNT/FSM 10: Edge Detect 11: None

Table 85. CNT/DLY2/FSM0 Register Settings

Signal Function	Register Bit Address	Register Definition
FSM0 Input data Source Select	reg<1797:1796>	00: 14 Bits NVM data 01: 8bits ADC data 10: 0 11: 8LSBs SPI Parallel data
CNT2 Value Control	reg<1798>	0: Reset (CNT value = 0) 1: Set (CNT value = FSM data)

15.5 CNT/DLY3 Register Settings

Table 86. CNT/DLY3 Register Settings

Signal Function	Register Bit Address	Register Definition
CNT3 14bits data From Register	reg<1812:1799>	data
CNT/DLY3 Clock Source Select	reg<1815:1813>	000: CK_RCOSC 001: CK_RCOSC_DIV4 010: CK_RCOSC_DIV24 011: CK_RCOSC_DIV64 100: CK_LFOSC 101: CNT_END2 110: CK_RINGOSC 111: Matrix1_out74
DLY3 Edge Mode Select or CNT3 Reset Mode Select	reg<1817:1816>	If DLY Mode; 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNTReset Mode; 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
CNT/DLY3 Macrocell Function Select	reg<1819:1818>	00: DLY 01: CNT 10: Edge Detect 11: CNT (the Reset From Matrix not Control the Oscillator)

15.6 CNT/DLY4/FSM1 Register Settings

Table 87. CNT/DLY4/FSM1 Register Settings

Signal Function	Register Bit Address	Register Definition
CNT4 8bits data From Register	reg<1827:1820>	data

Table 87. CNT/DLY4/FSM1 Register Settings

Signal Function	Register Bit Address	Register Definition
CNT/DLY4/FSM1 Clock Source Select	reg<1831:1828>	0000: CK_RCOSC 0001: CK_RCOSC_DIV4 0010: CK_RCOSC_DIV12 0011: CK_RCOSC_DIV24 0100: CK_RCOSC_DIV64 0101: CNT_END3 0110: Matrix1_out74 0111: Matrix0_out72 divide by 8 1000: CK_RINGOSC 1001: Matrix0_out83(SPI_SCLK) 1010: CK_LFOSC 1011: CK_FSM_DIV256 1100: CK_PWM 1101: Reserved 1110: Reserved 1111: Reserved
DLY4 Edge Mode Select or CNT4 Reset Mode Select	reg<1833:1832>	If DLY Mode; 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNTReset Mode; 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
CNT/DLY4/FSM1 Macrocell Function Select	reg<1834>	0: DLY 1: CNT/FSM
FSM1 Input data Source Select	reg<1836:1835>	00: 8 Bits NVM data 01: 8bits ADC data 10: 8MSBs SPI Parallel data 11: 0
CNT4 Value Control	reg<1837>	(0: Reset (CNT value = 0) 1: Set (CNT value = FSM data)

15.7 CNT/DLY5 Register Settings

Table 88. CNT/DLY5 Register Settings

Signal Function	Register Bit Address	Register Definition
CNT5 8bits data From Register	reg<1845:1838>	data
CNT/DLY5 Clock Source Select	reg<1848:1846>	000: CK_RCOSC 001: CK_RCOSC_DIV4 010: CK_RCOSC_DIV24 011: CK_RCOSC_DIV64 100: CK_LFOSC 101: CNT_END4 110: CK_RINGOSC 111: Matrix0_out73

Table 88. CNT/DLY5 Register Settings

Signal Function	Register Bit Address	Register Definition
DLY5 Edge Mode Select or CNT5 Reset Mode Select	reg<1850:1849>	If DLY Mode; 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNTReset Mode; 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
CNT/DLY5 Macrocell Function Select	reg<1851>	0: DLY 1: CNT

15.8 CNT/DLY6 Register Settings

Table 89. CNT/DLY6 Register Settings

Signal Function	Register Bit Address	Register Definition
CNT6 8bits data From Register	reg<1859:1852>	data
CNT/DLY6 Clock Source Select	reg<1862:1860>	000: CK_RCOSC 001: CK_RCOSC_DIV4 010: CK_RCOSC_DIV24 011: CK_RCOSC_DIV64 100: CK_LFOSC 101: CNT_END5 110: CK_RINGOSC 111: Matrix0_out73
DLY6 Edge Mode Select or CNT6 Reset Mode Select	reg<1864:1863>	If DLY Mode; 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNTReset Mode; 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
CNT/DLY6 Macrocell Function Select	reg<1865>	0: DLY 1: CNT

15.9 CNT/DLY7 Register Settings

Table 90. CNT/DLY7 Register Settings

Signal Function	Register Bit Address	Register Definition
CNT7 8bits data From Register	reg<1873:1866>	data

Table 90. CNT/DLY7 Register Settings

Signal Function	Register Bit Address	Register Definition
CNT/DLY7 Clock Source Select	reg<1876:1874>	000: CK_RCOSC 001: CK_RCOSC_DIV4 010: CK_RCOSC_DIV24 011: CK_RCOSC_DIV64 100: CK_LFOSC 101: CNT_END6 110: CK_RINGOSC 111: Matrix1_out73
DLY7 Edge Mode Select or CNT3 Reset Mode Select	reg<1878:1877>	If DLY Mode; 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNTReset Mode; 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
CNT/DLY7 Macrocell Function Select	reg<1879>	0: DLY 1: CNT

15.10 CNT/DLY8/PWM_RAMP Register Settings

Table 91. CNT/DLY8/PWM_RAMP Register Settings

Signal Function	Register Bit Address	Register Definition
CNT8 8bits data From Register	reg<1887:1880>	data
CNT/DLY8 Clock Source Select	reg<1891:1888>	0000: CK_RCOSC 0001: CK_RCOSC_DIV4 0010: CK_RCOSC_DIV12 0011: CK_RCOSC_DIV24 0100: CK_RCOSC_DIV64 0101: CNT_END7 0110: Matrix1_out73 0111: Matrix0_out72 divide by 8 1000:CK_RINGOSC 1001: Matrix0_out83(SPI_SCLK) 1010: CK_LFOSC 1011: CK_FSM_DIV256 1100: CK_PWM 1101: Reserved 1110: Reserved 1111: Reserved
DLY8 Edge Mode Select or CNT8 Reset Mode Select	reg<1893:1892>	If DLY Mode; 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNTReset Mode; 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset

Table 91. CNT/DLY8/PWM_RAMP Register Settings

Signal Function	Register Bit Address	Register Definition
CNT/DLY8 Macrocell Function Select	reg<1894>	0: DLY 1: CNT/PWM_RAMP

15.11 CNT/DLY9 Register Settings

Table 92. CNT/DLY9 Register Settings

Signal Function	Register Bit Address	Register Definition
CNT9 8bits data From Register	reg<1902:1895>	data
CNT/DLY9 Clock Source Select	reg<1906:1903>	0000: CK_RCOSC 0001: CK_RCOSC_DIV4 0010: CK_RCOSC_DIV12 0011: CK_RCOSC_DIV24 0100: CK_RCOSC_DIV64 0101: CNT_END8 0110: Matrix0_out72 0111: Matrix0_out72 divide by 8 1000: CK_RINGOSC 1001: Matrix0_out83(SPI_SCLK) 1010: CK_LFOSC 1011: CK_FSM_DIV256 1100: CK_PWM 1101: Reserved 1110: Reserved 1111: Reserved
DLY9 Edge Mode Select or CNT9 Reset Mode Select	reg<1908:1907>	If DLY Mode; 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNTReset Mode; 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
CNT/DLY9 Macrocell Function Select	reg<1909>	00: DLY 01: CNT

16.0 Digital Comparator (DCMP) / Pulse Width Modulator (PWM)

The SLG46621 has three 8-bit digital comparator (DCMP)/ pulse width modulator (PWM) logic macrocells. Each of these three logic macrocells can be either a digital comparator (DCMP) or a pulse width modulator (PWM) independently of how the other two logic macrocells are defined.

Both the DCMP and PWM logic can operate at up to a frequency of 10 MHz. The input power for the three logic macrocells is controlled independently by reg <1678> for DCMP0/PWM0, reg <1698> for DCMP1/PWM1 and reg <1718> for DCMP2/PWM2.

PWM power-down control is configured by reg <1677> which is also shared with the ADC and OSC.

16.1 DCMP Input Modes

All three DCMP logic macrocells have a positive (IN+) and a negative (IN-) input. The signal (through the IN+ input) takes the value from a 4:1 MUX selection between the following signals:

- 8-bit signal from the ADC Parallel Output
- 8-bit signal from the SPI logic cell output (SPI<15:8> for DCMP0 and DCMP2 or SPI<7:0> for DCMP1)
- 8-bit signal from the FSM (FSM0<7:0> for DCMP0 or FSM1<7:0> for DCMP1 and DCMP2)
- 8-bit user defined signal value.

The signal (through the IN- input) takes the value from a 4:1 MUX selection between the following signals:

- 8-bit signal from the CNT (CNT9'Q <7:0> for DCMP1 or CNT8'Q <7:0> for DCMP0 and DCMP2)
- 8-bit signal from the SPI logic cell output (SPI<7:0> for DCMP0 and DCMP2 or SPI<15:8> for DCMP1)
- 8-bit signal from the FSM (FSM1' Q <7:0> for DCMP0 or FSM0'Q<7:0> for DCMP1 and DCMP2)
- 8-bit user defined signal value.

16.2 DCMP Output Modes

The two 8-bit parallel data inputs from IN+ and IN- are compared within the DCMP logic macrocells to produce the output (OUT+) and an Equal signal (EQ).

There are two cases for the OUT+ signal controlled by reg <1714>, reg <1694>, reg <1673>.

If these regs = 0, then

- if *inp* > *inn, OUT*+ = 1, EQ = 0
- if *inp* < *inn*, *OUT*+ = 0, EQ = 0
- if *inp* = *inn, OUT*+ = 0, EQ = 1

If these regs = 1, then

- if *inp* > *inn, OUT*+ = 1, EQ = 0
- if *inp* < *inn, OUT*+ = 0, EQ = 0
- if *inp* = *inn, OUT*+ = 1, EQ = 1

Both the OUT+ and EQ signals are triggered by the rising or falling edge (controlled by reg <1676>, reg <1697> and reg<1717>) of the CLK OSC signal (clock source is defined by regs <1629:1628>) and result of comparison can be read in the next clock pulse, see figure below, where reg <1714>, reg <1694>, reg <1673> are equal 0.

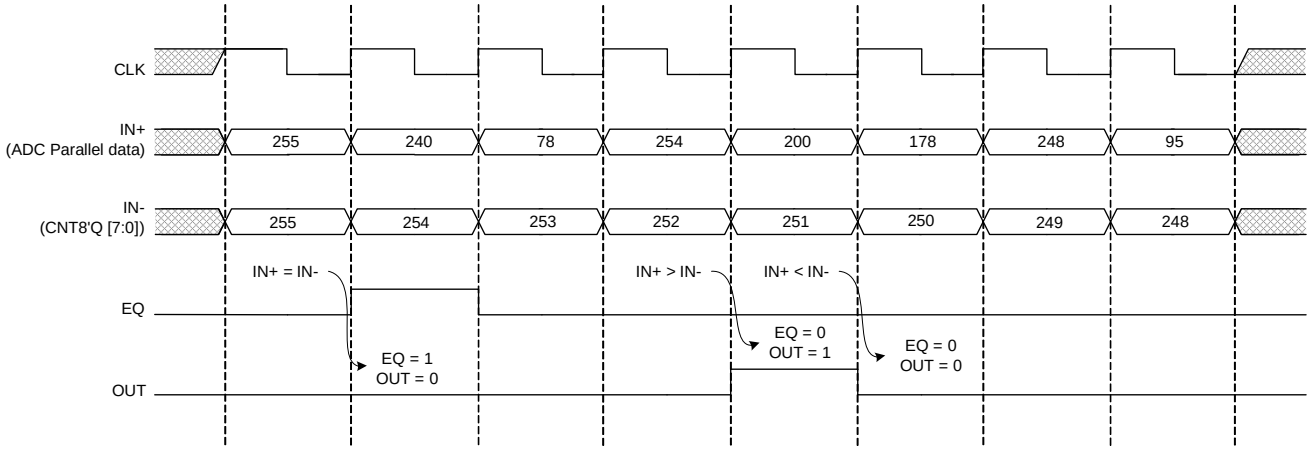


Figure 96. DCMP Timing Diagram

16.3 PWM Input Modes

IN+ for the PWM is an 8-bit data string that can be selected from one of four sources;

- 8-bit signal from the ADC Parallel Output
- 8-bit signal from the SPI logic cell output (SPI<15:8> for DCMP0 and DCMP1 or SPI<7:0> for DCMP2)
- 8-bit signal from the FSM0<7:0>
- 8-bit user defined signal value.

IN-'s 8-bit data string for all PWMs is sourced from an 8-bit signal from CNT/DLY1.

16.4 PWM Output Modes

The output (*OUT+*) duty cycle can be set to either count down to 0% or count up to 100% and each PWM is independently controlled by the value of reg<1673> (PWM0), reg<1694> (PWM1), and reg<1714> (PWM2). When both inputs are equal the output signal (*EQ*) will go high. The outputs (*OUT-* and *OUT+*) are non-overlapping.

When reg<1673/1694/1714> = “0”

- PWM output duty cycle ranges from 0% to 99.61% and is determined by: Output Duty Cycle = IN+/256
- (IN+ = 0: output duty cycle = 0/256 = 0%; IN+ = 255: output duty cycle = 255/256 = 99.61%)
- Output signals are triggered by the rising or falling edge of the *CKOSC* signal (defined by bit regs <1676>, <1697>, <1717>).

When reg<1673/1694/1714> = “1”

- PWM output duty cycle ranges from 0.39% to 100% and is determined by Output Duty Cycle = (IN+ + 1)/256
- (IN+ = 0: output duty cycle = 1/256 = 0.39%; IN+ = 255: output duty cycle = 256/256 = 100%)
- Output signals are triggered by the rising or falling edge of the *CKOSC* signal (defined by bit regs <1676>, <1697>, <1717>).

When IN+ = IN- then EQ = “1”

16.5 DCMP0/PWM0 Functional Diagram

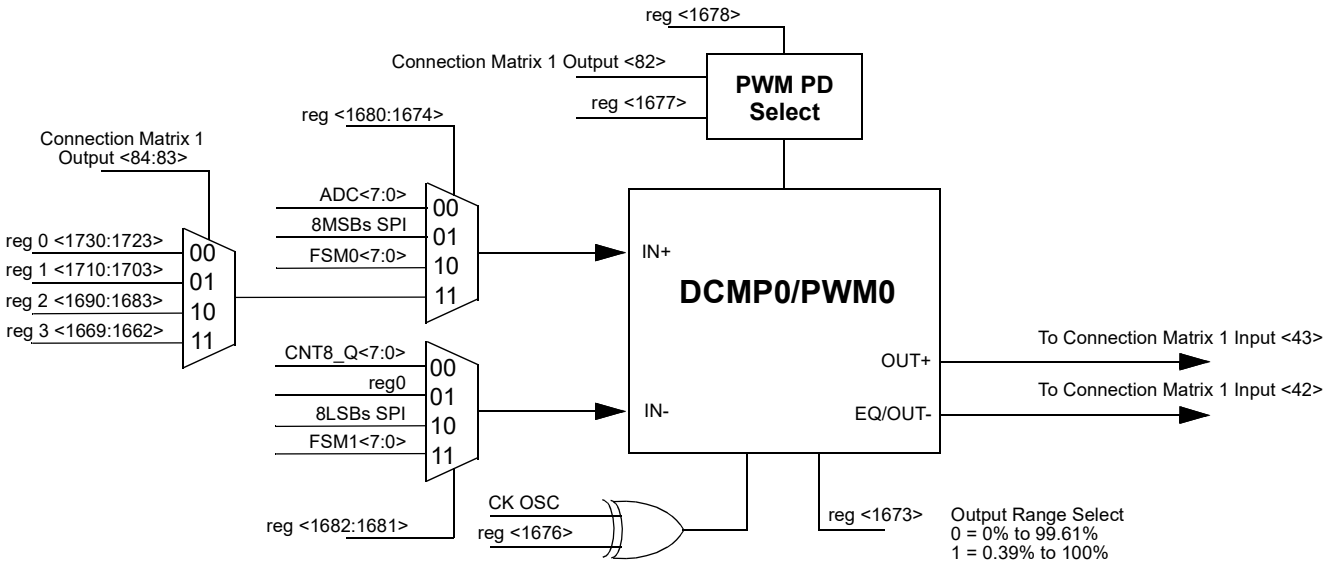


Figure 97. DCMP0/PWM0 Functional Diagram

16.6 DCMP1/PWM1 Functional Diagram

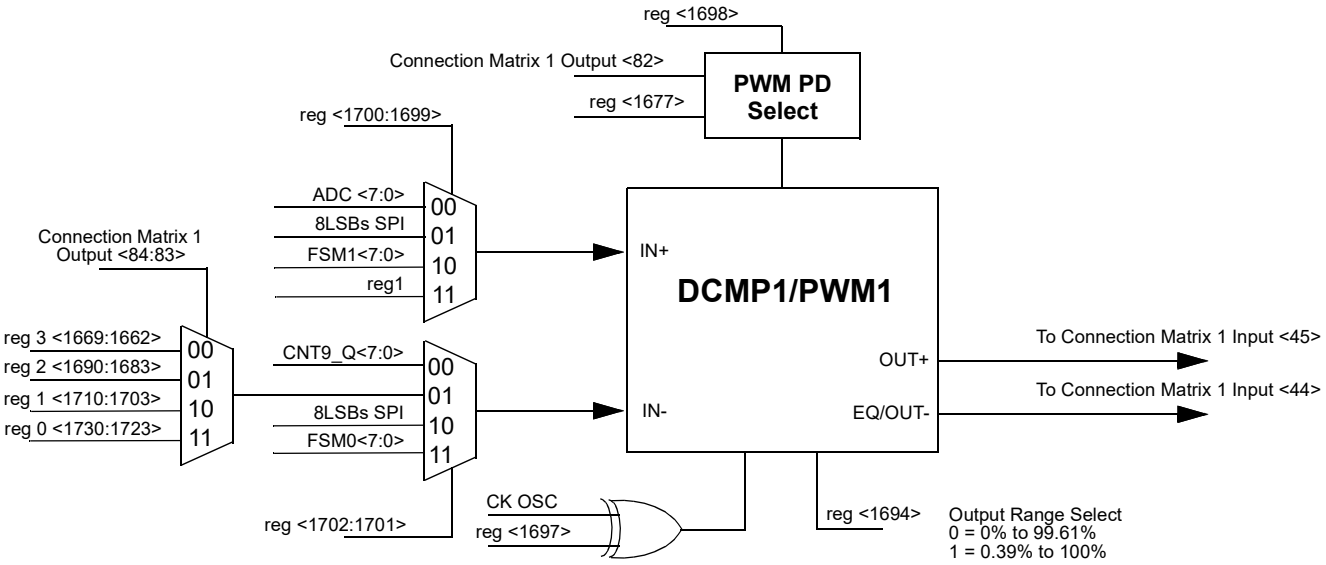


Figure 98. DCMP1/PWM1 Functional Diagram

16.7 DCMP2/PWM2 Functional Diagram

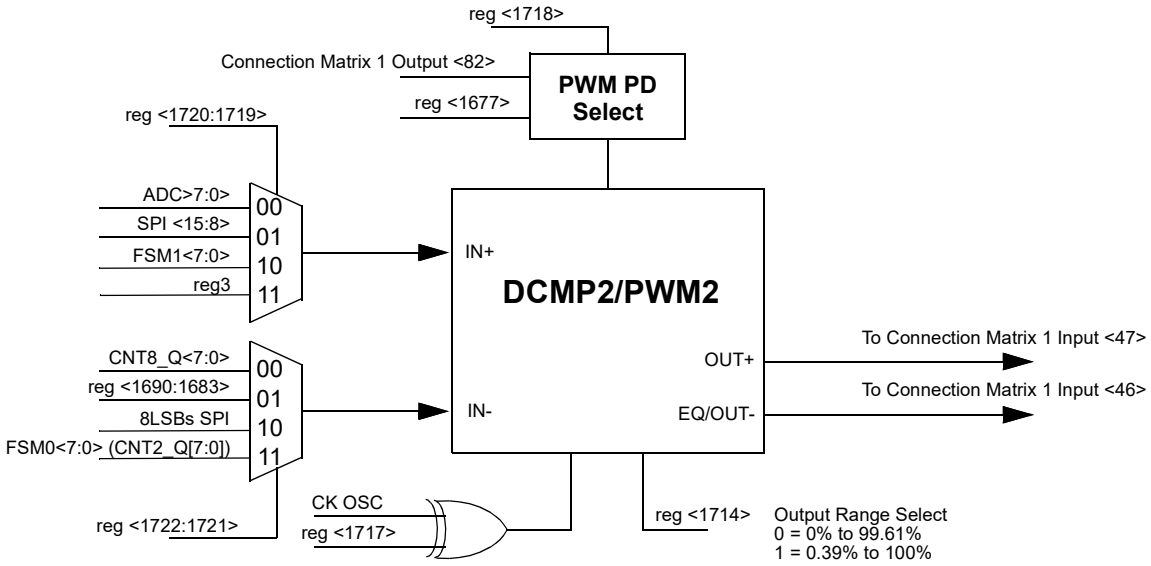


Figure 99. DCMP2/PWM2 Functional Diagram

16.8 PWM Dead Band Control

The dead band interval can be controlled with NVM bits from PWM0 reg<1722:1720>, from PWM1 reg<1693:1691>, from PWM2 reg<1713:1711>. The typical dead band time starts at 8 ns and can go to 64 ns, increasing by 8 ns intervals.

For the Delay dead band control, the dead time control range is:

$$T_D = (PWM\ Register\ bits + 1) \times 8ns$$

16.9 PWM Dead Band Control Timing Diagram

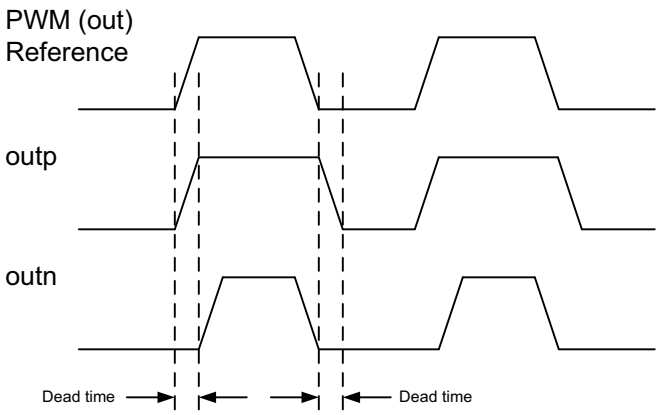


Figure 100. PWM Dead Band Control Timing Diagram

16.10 DCMP/PWM Power Down Control

The power down source for the DCMP/PWM logic cells is selected by reg <1521:1516>. The DCMP/PWM logic cells can then be turned on or off individually with the appropriate register. The power down control of each logic cell is managed by the following register settings:

- When reg<1678> = “0” DCMP0/PWM0 is powered down, when “1” logic cell is ON
- When reg<1698> = “0” DCMP1/PWM1 is powered down, when “1” logic cell is ON
- When reg<1718> = “0” DCMP2/PWM2 is powered down, when “1” logic cell is ON

16.11 DCMP/PWM Clock Invert Control

The three DCMP/PWM logic cells can invert the *CKOSC* input signal during the compare or PWM function. reg <1676>, reg < 1697>, and reg <1717 > are used to control the three logic cells clock inversion for PWM0, PWM1, and PWM2 respectively.

16.12 DCMP/PWM Register Settings

Table 93. DCMP/PWM Register Settings

Signal Function	Register Bit Address	Register Definition
Reg3, 8 bits NVM data to PWM/DCMP or DAC input	<1669:1672>	
PWM0 Deadband Zone Control	<1672:1670>	000: 10 ns 001: 20 ns 010: 30 ns 011: 40 ns 100: 50 ns 101: 60 ns 110: 70 ns 111: 80 ns
PWM/DCMP0 mode selection	<1673>	0: PWM output duty cycle down to 0% and DCMP out=1 if A>B 1: PWM output duty cycle up to 100% and DCMP out=1 if A>=B.
PWM/DCMP0 function selection	<1674>	0: PWM 1: DCMP. when in PWM mode, OUTN0 is PWM1's negative ouput. when in DCMP mode, OUTN0 is DCMP1's match output
PWM/DCMP0 clock source selection	<1675>	0: Clock from mux controlled by reg[1629:1628] 1: matrix1_73
PWM/DCMP0 clock inversion	<1676>	0: Disable 1: Enable
power down sync to clock and output state control in power down mode	<1677>	0: power down is not synchronized with clock,and output reset to 0 when PWM/DCMP is power down, 1: power down is synchronized with clock, when PD=0, the clock is enabled after 2 clock cycles, while when PD=1, the clock is gated immediatlly. and the output is kept at current state when PD=1.
PWM/DCMP0 turn on by register	<1678>	0: Disable 1: Enable
PWM/DCMP0 positive input source selection	<1680:1679>	00: ADC 01: 8MSBs SPI 10: FSM0[7:0] 11: from MUX controlled by matrix1_out[84:83]
PWM/DCMP0 negative input source selection	<1682:1681>	00: CNT8_Q[7:0] 01: reg0 10: 8LSBs SPI 11: FSM1_Q[7:0]
Reg2, 8 bits NVM data to PWM/DCMP or DAC input	<1690:1683>	
PWM1 Deadband Zone Control	<1693:1691>	000: 10 ns 001: 20 ns 010: 30 ns 011: 40 ns 100: 50 ns 101: 60 ns 110: 70 ns 111: 80 ns
PWM/DCMP1 mode selection	<1694>	0: PWM output duty cycle down to 0% and DCMP out=1 if A>B 1: PWM output duty cycle up to 100% and DCMP out=1 if A>=B
PWM/DCMP1 function selection	<1695>	0: PWM 1: DCMP When in PWM mode, OUTN1 is PWM1's negative ouput When in DCMP mode, OUTN1 is DCMP1's match output

Table 93. DCMP/PWM Register Settings

Signal Function	Register Bit Address	Register Definition
PWM/DCMP1 clock source selection	<1696>	0: clock from mux controlled by reg<1629:1628> 1: matrix1_73
PWM/DCMP1 clock inversion	<1697>	0: Disable 1: Enable
PWM/DCMP1 positive input source selection	<1700:1699>	00: ADC 01: 8LSBs SPI 10: FSM1[7:0] 11: reg1
PWM/DCMP1 negative input and DAC input source selection	<1702:1701>	00: CNT9_Q[7:0] 01: from MUX controlled by matrix1_out<84:83> 10: 8MSBs SPI 11: FSM0_Q[7:0]
Reg1, 8 bits NVM data to PWM/DCMP or DAC input	<1710:1703>	
PWM2 Deadband Zone Control	<1713:1711>	000: 10 ns 001: 20 ns 010: 30 ns 011: 40 ns 100: 50 ns 101: 60 ns 110: 70 ns 111: 80 ns
PWM/DCMP2 mode selection	<1714>	0: PWM output duty cycle down to 0% and DCMP out=1 if A>B 1: PWM output duty cycle up to 100% and DCMP out=1 if A>=B.
PWM/DCMP2 function selection	<1715>	0: PWM 1: DCMP When in PWM mode, OUTN2 is pwm2's negative ouput When in DCMP mode, OUTN2 is dcmp1's match output
PWM/DCMP2 clock source selection	<1716>	0: clock from mux controlled by reg<1629:1628> 1: matrix1_73
PWM/DCMP2 clock inversion	<1717>	0: Disable 1: Enable
PWM/DCMP2 turn on by register	<1718>	0: Disable 1: Enable
PWM/DCMP2 positive input source selection	<1720:1719>	00: ADC 01: 8MSBs SPI 10: FSM1[7:0] 11: reg3
PWM/DCMP2 negative input source selection	<1722:1721>	00: CNT8_Q[7:0] 01: reg2 10: 8LSBs SPI 11: FSM0_Q[7:0]
Reg0, 8 bits NVM data to PWM/DCMP or DAC input	<1730:1723>	

17.0 Slave SPI - Serial to Parallel / Parallel to Serial Converter (SPI)

The Slave SPI data can be communicated between the SLG46621 and the larger system design through either the serial to parallel or parallel to serial interface. The SPI has two 8-bit registers (2 bytes) that are used for data transfer. The external clock signal and the nCSB (Enable Control Signal) comes from the Connection Matrix Out.

For serial to parallel operation (S2P), the serial data in (MOSI) comes from PIN 10 of the SLG46621. The S2P will produce a 16-bit parallel data output (S2P<15:0>) where the MSB <15:8> can be used by the PWM/DCMP0_IN+, PWM/DCMP1_IN-, PWM/DCMP2_IN+ and FSM0 logic cells, while the LSB <7:0> can be used by the PWM/DCMP0_IN-, PWM/DCMP1_IN+, PWM/DCMP2_IN- and FSM1 logic cells.

In parallel to serial mode (P2S) there is an additional configuration of the length of converted code - 8-bit and 16-bit. With 8-bit configuration the parallel data from FSM0 or ADC can be converted to serial data. PIN 10 is used to output this 8-bit serial data out (MISO) signal. With 16 bit configuration the parallel data from FSM0 and FSM1 can be converted into a serial code. 8 LSB bits of FSM1 data will be sent to PAR_IN<7:0> and 8 bits of FSM0 will be sent to PAR_IN<15:8>. Same as in 8-bit mode 16 bit serial data will be output to PIN 10.

17.1 SPI Functional Diagram

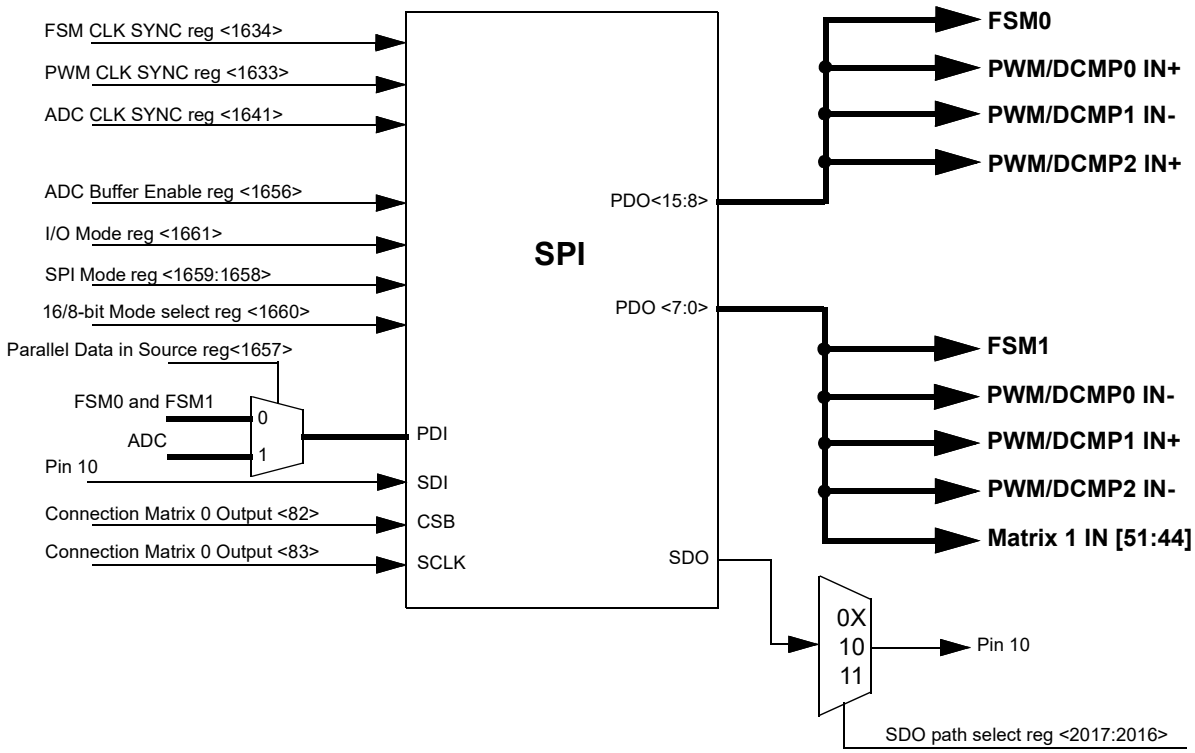


Figure 101. SPI Functional Diagram

17.2 Clock polarity and phase

In addition to setting the clock frequency, it is possible to configure the clock polarity and phase with respect to the data. This is configured by the CPOL and CPHA respectively.

Figure 90. shows the SPI timing diagram when CPHA=0; in this mode data can only be transmitted from serial to parallel, not from parallel to serial.*Figure 91.* shows the SPI timing diagram when CPHA=1; in this mode data can be transmitted both from serial to parallel and from parallel to serial.

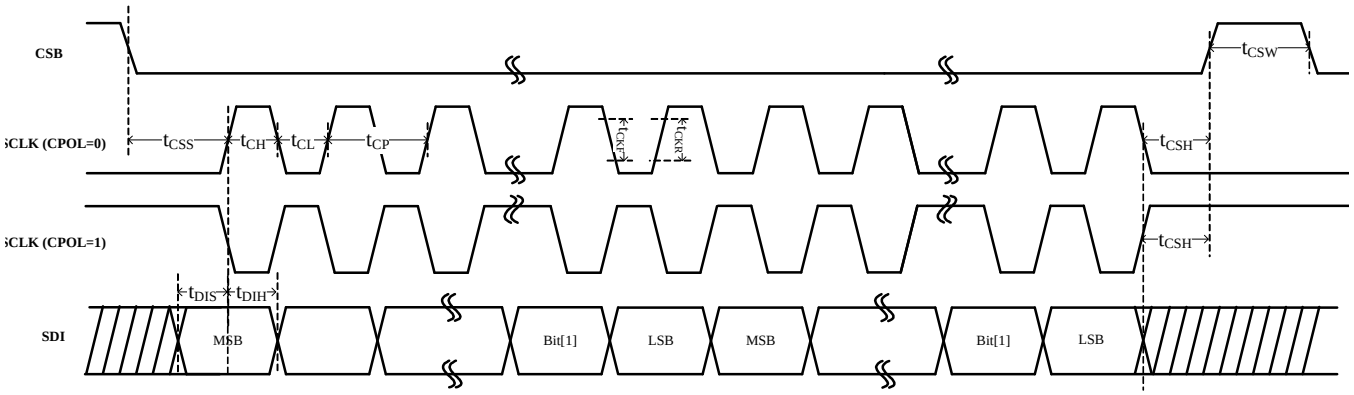


Figure 102. Timing Diagram showing Clock Polarity and Phase, CPHA=0

Table 94. CPHA = 0 Timing Characteristics

Parameter	Symbol	Min	Max	Units
SCLK period	t_{CP}	500	--	ns
SCLK pulse width high	t_{CH}	250	--	ns
SCLK pulse width low	t_{CL}	250	--	ns
CSB fall to SCLK first edge setup	t_{CSS}	250	--	ns
SCLK last edge to CSB rise hold	t_{CSH}	250	--	ns
CSB pulse width high	t_{CSW}	500	--	ns
SCLK to SDI hold	t_{DIH}	100	--	ns
SCLK to SDI setup	t_{DIS}	50	--	ns
SCLK rise/fall time	t_{CKR}	--	20	ns

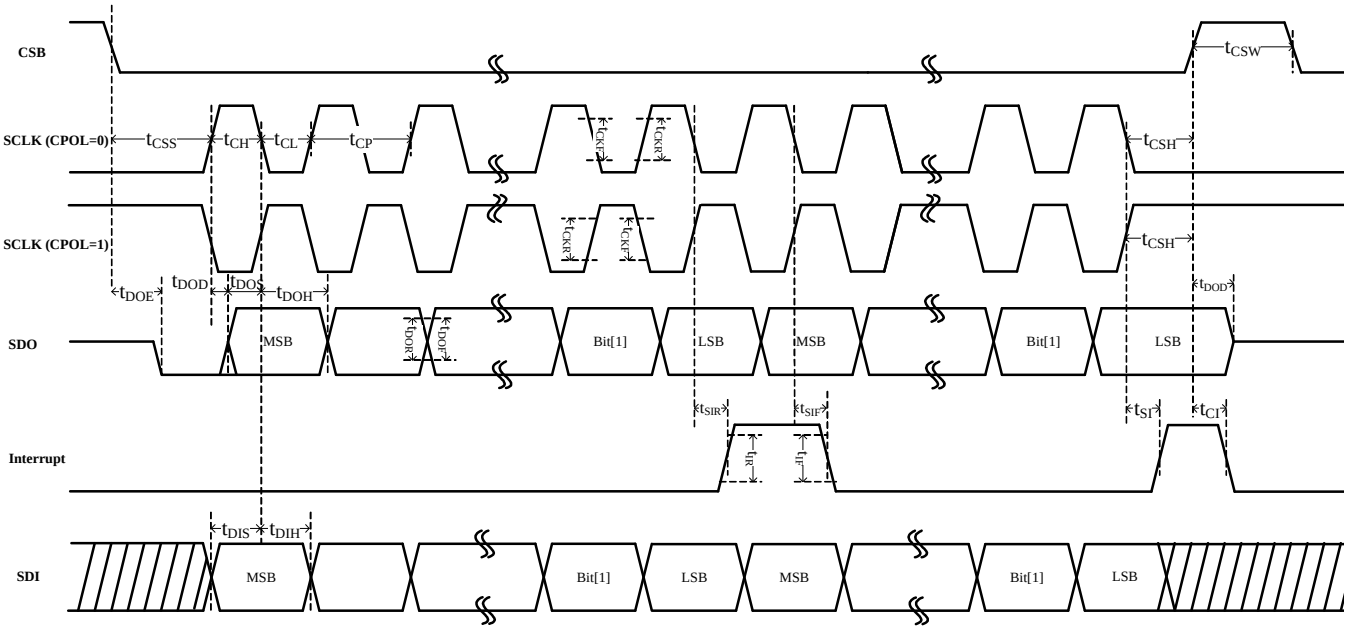


Figure 103. Timing Diagram showing Clock Polarity and Phase, CPHA = 1

Table 95. CPHA = 1 Timing Characteristics

Parameter	Symbol	Min	Max	Units
SCLK period	t_{CP}	500	--	ns
SCLK pulse width high	t_{CH}	250	--	ns
SCLK pulse width low	t_{CL}	250	--	ns
CSB fall to SCLK first edge setup	t_{CSS}	250	--	ns
SCLK last edge to CSB rise hold	t_{CSH}	250	--	ns
SCLK to SDO hold	t_{DOH}	100	--	ns
SCLK to SDO setup	t_{DOS}	100	--	ns
SCLK to SDO delay	t_{DOD}	--	150*	ns
CSB rise to SDO disable	t_{DOD}	5	150*	ns
CSB fall to SDO enable	t_{DOE}	5	150*	ns
CSB pulse width high	t_{CSW}	500	--	ns
LSB' SCLK fall to Interrupt high	t_{SIR}	5	150*	ns
MSB' SCLK fall to Interrupt low	t_{CIF}	5	150*	ns
SCLK to Interrupt high	t_{SI}	5	150*	ns
CSB rise to Interrupt low	t_{CI}	5	150*	ns
SCLK to SDI hold	t_{DIH}	100	--	ns
SCLK to SDI setup	t_{DIS}	50	--	ns
SCLK rise/fall time	t_{CKR}/t_{CKF}	--	20	ns
SDO rise/fall time	t_{DOR}/t_{DOF}	--	20*	ns
Interrupt rise/fall time	t_{IR}/t_{IF}	--	20*	ns
Note: The data is based on 50pF loading on the output PIN, and the output drive strength is 2x option.*				

- At CPOL=0 the base value of the clock is zero
  - For CPHA=0, data are captured on the clock's rising edge (LOW→HIGH transition) and data is propagated on a falling edge (HIGH→LOW clock transition).
  - For CPHA=1, data are captured on the clock's falling edge and data is propagated on a rising edge.
- At CPOL=1 the base value of the clock is one (inversion of CPOL=0)
  - For CPHA=0, data are captured on clock's falling edge and data is propagated on a rising edge.
  - For CPHA=1, data are captured on clock's rising edge and data is propagated on a falling edge.

That is, CPHA=0 means sample on the leading (first) clock edge, while CPHA=1 means sample on the trailing (second) clock edge, regardless of whether that clock edge is rising or falling. Note that with CPHA=0, the data must be stable for a half cycle before the first clock cycle.

The MOSI and MISO signals are usually stable (at their reception points) for the half cycle until the next clock transition. SPI master and slave devices may well sample data at different points in that half cycle.

This adds more flexibility to the communication channel between the master and slave.

17.3 SPI Clock synchronization

When the parallel data is going to be loaded into the buffer in SPI, the SPI will generate the "sync" signal, it will gating the ADC/PWM CLOCK or FSM CLOCK/256 to stop the running ADC, PWM, FSM or CNTs to avoid mis-catch data due to theasynchronization of SCLK and the internal clocks, see *Figure 94.* .

Note: The internal clock and SPI clock must satisfy the: 2TCLK_INT<1/2TSCK.

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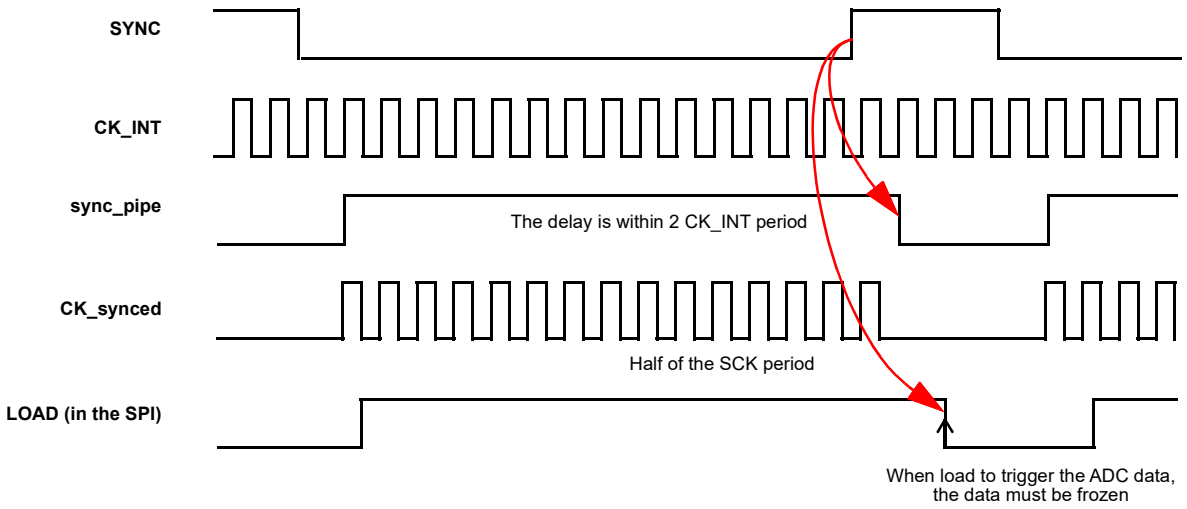


Figure 104. Timing Diagram showing SPI Clock synchronization

17.4 SPI data buffer function

SPI data buffer can be used to have DCMP compare two different ADC timing data. The ADC buffer is shared with the DFFs that are in the SPI macrocell. When the SPI is set to ADC buffer mode (reg[1656]=1), the DFF 's data inputs of SPI's parallel outputs

are from ADC and the DFF's clock source comes from matrix0_output83 which can be programmed by user. The DFF's output (SPI[7:0]) is the ADC data's buffered output which can be sent to DCMP/PWMs or FSM (CNT)s

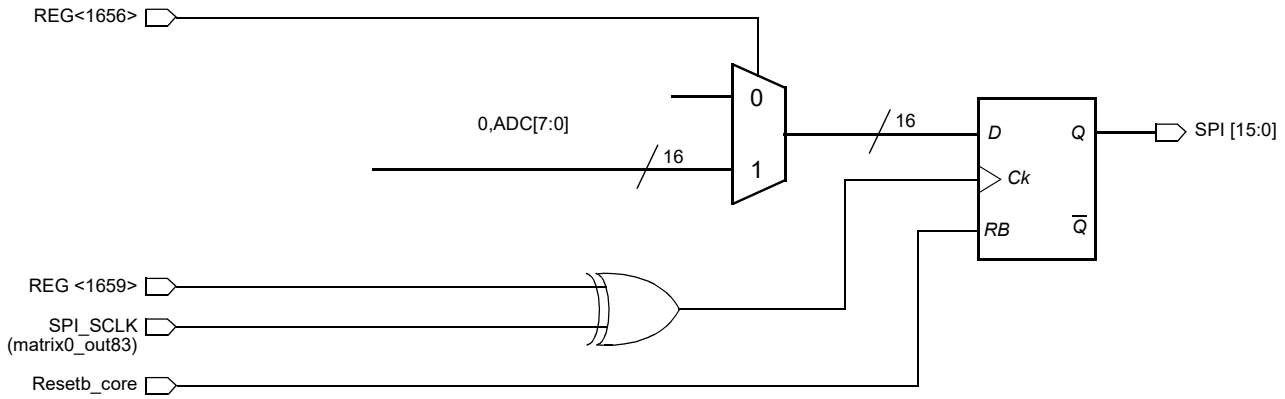


Figure 105. The SPI used as ADC data buffer diagram

17.5 SPI Register Settings

Table 96. SPI Register Settings

Signal Function	Register Bit Address	Register Definition
SPI used as ADC buffer enable (1 clock delayed)	<1656>	0: Disable 1: Enable
SPI clock phase (CPHA)	<1658>	refer to SPI spec
SPI clock polarity (CPOL)	<1659>	refer to SPI spec
Byte Selection	<1660>	0: 16bits 1: 8bits (less significant 8 bits)
SPI input/output mode selection	<1661>	0: serial in parallel out 1: parallel in serial out
SPI parallel output selection for matrix 1. (in<44> --> in<51>)	<2015>	0: matrix1_in[44] from pwm1_outn; matrix1_in[45] from pwm1_outp; matrix1_in[46] from pwm2_outn; matrix1_in[47] from pwm2_outp; matrix1_in[48] from ckringosc; matrix1_in[49] from ckrcosc; matrix1_in[50] from cklfosc; matrix1_in[51] from ground 1: matrix 1 in[51:44] from SPI parallel output LSB <7:0>
SPI SDIO output control	<2017:2016>	0x: Pin10 dout from matrix 0 (out67) 10: from SPI (SDO) 11: from ADC serial output

18.0 Pipe Delay (PD)

The SLG46621 has two 16-bit Pipe Delay Macrocells.

Each Pipe Delay has three input signals from the matrix, Input (IN), Clock (CLK) and Reset (RST). The pipe delay cell is built from 16 D Flip-Flop logic cells that provide two delay options which are user selectable. The DFF cells are tied in series where the output (Q) of each delay cell goes to the next DFF cell. The two outputs (OUT0 and OUT1) provide user selectable options for 1 – 16 stages of delay. There are delay output points for each set of the OUT0 and OUT1 outputs to a 4-input mux that is controlled by register bits. The 4-input mux is used to control the selection of the amount of delay.

The overall time of the delay is based on the clock used in the SLG46621 design. Each DFF cell has a time delay of the inverse of the clock time (either external clock or any Oscillator within the SLG46621). The sum of the number of DFF cells used will be the total time delay of the Pipe Delay logic cell.

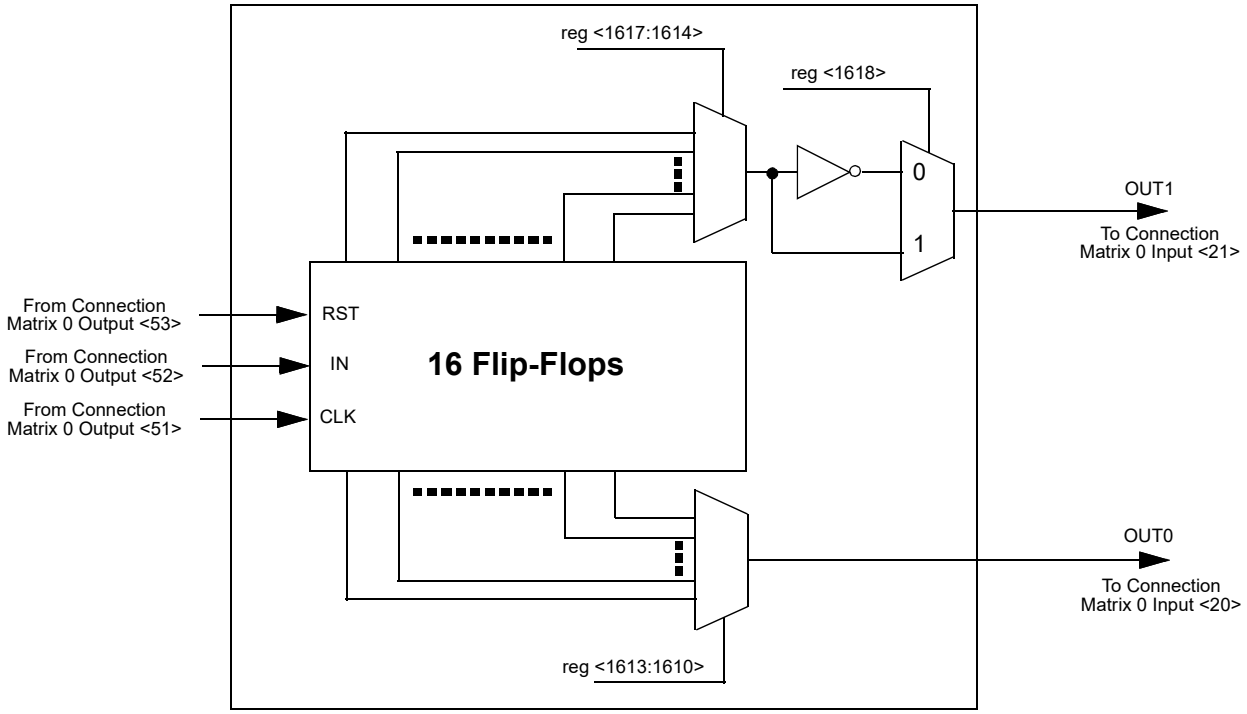


Figure 106. Pipe Delay 0

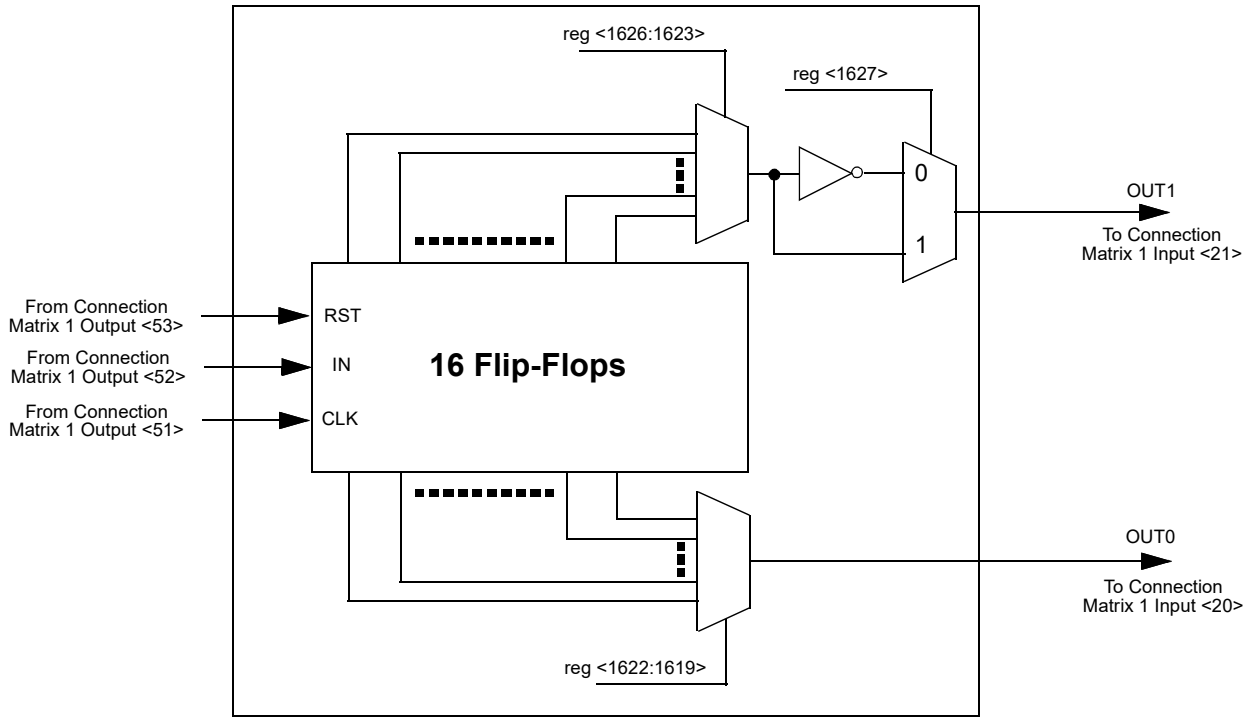


Figure 107. Pipe Delay 1

18.1 Pipe Delay Register Settings

Table 97. Pipe Delay Register Settings

Signal Function	Register Bit Address	Register Definition
Pipe Delay 0 out0 selection bits	<1613:1610>	register bits from 0 to 15, data delay from 1 to 16 pipes.
Pipe Delay 0 out1 selection bits	<1617:1614>	register bits from 0 to 15, data delay from 1 to 16 pipes.
Pipe Delay 0 out1 output polarity control	<1618>	0: no invert 1: invert.
Pipe Delay 1 out0 selection bits	<1622:1619>	register bits from 0 to 15, data delay from 1 to 16 pipes.
Pipe Delay 1 out1 selection bits	<1626:1623>	register bits from 0 to 15, data delay from 1 to 16 pipes.
Pipe Delay 1 out1 output polarity control	<1627>	0: no invert 1: invert.

19.0 Programmable Delay / Edge Detector

The SLG46621 has two programmable time delay logic cells available that can generate a delay that is selectable from one of four timings (time1) configured in the GreenPAK Designer. The programmable time delay cells can generate one of four different delay patterns, rising edge detection, falling edge detection, both edge detection and both edge delay. Three of these patterns can be further modified with the addition of delayed edge detection, which adds an extra unit of delay as well as glitch rejection during the delay period. Note that, delayed edge detection function is not available for both edge delay pattern. See the timing diagrams below for further information.

Note: *The input signal must be longer than the delay, otherwise it will be filtered out.*

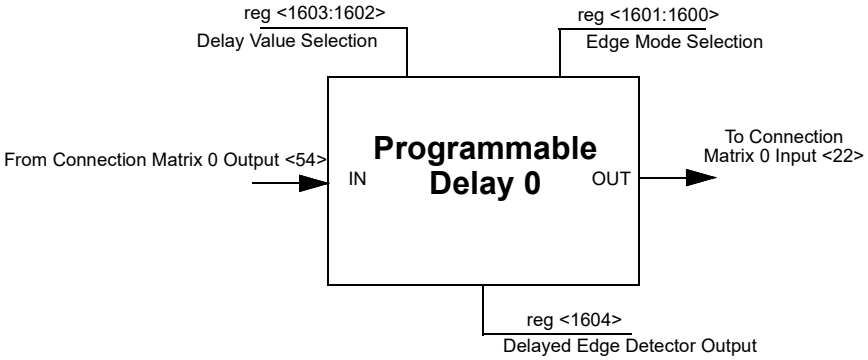


Figure 108. Programmable Delay

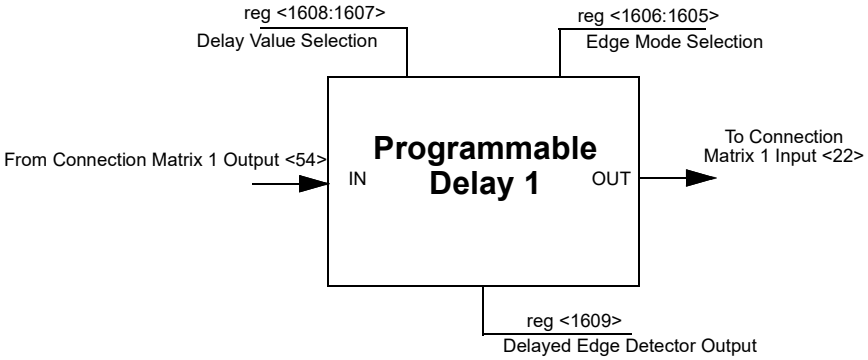


Figure 109. Programmable Delay

19.1 Programmable Delay Timing Diagram - Edge Detector Output

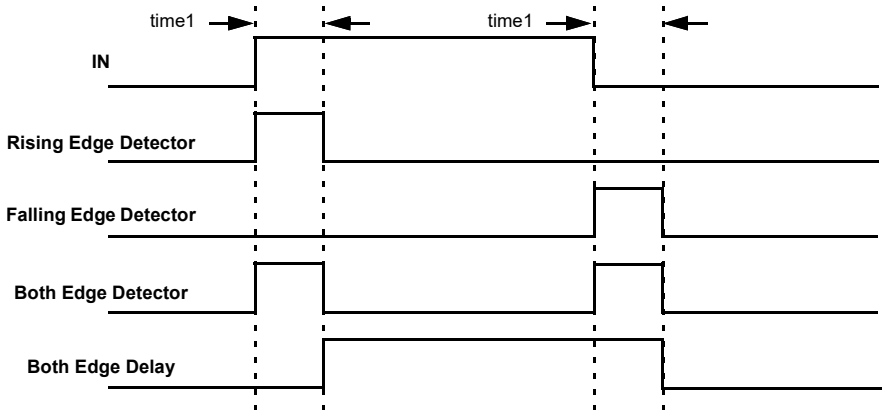


Figure 110. Edge Detector Output

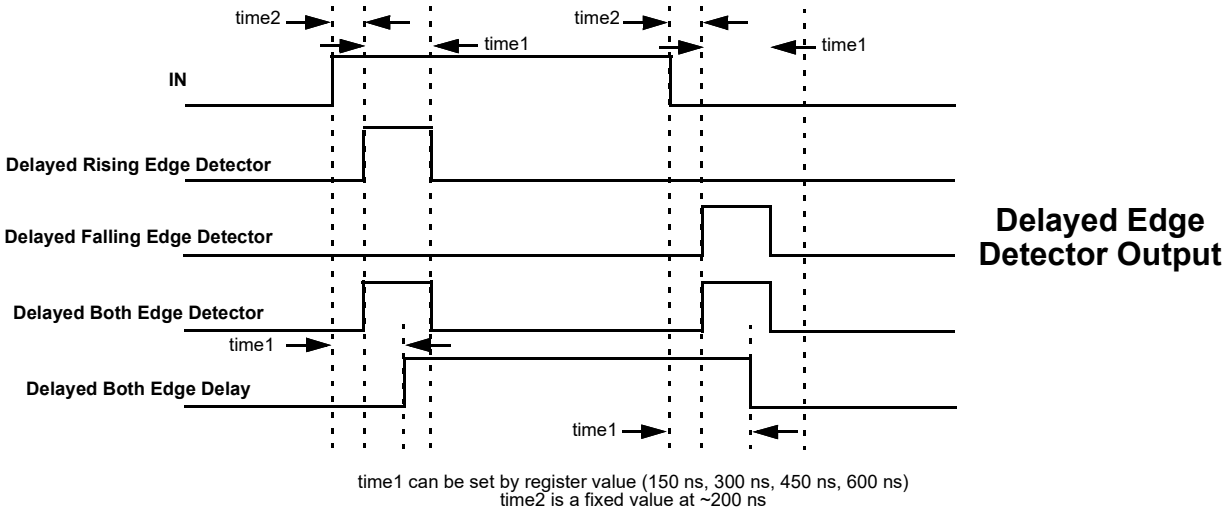


Figure 111. Delayed Edge Detector Output

19.2 Programmable Delay Timing Diagram - Glitch Filtering For Edge Detector Output

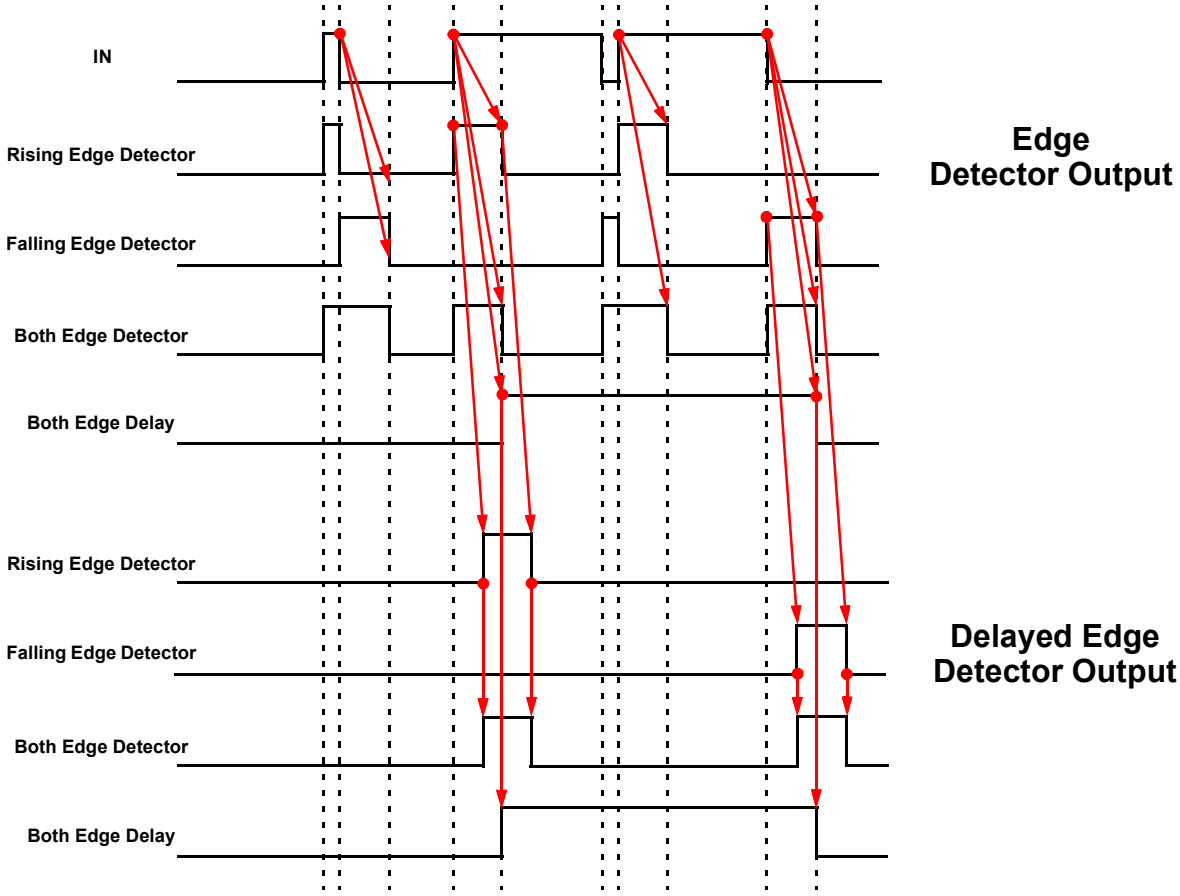


Figure 112. Glitch Filtering for Edge Detector Output

19.3 Programmable Delay 0 Register Settings

Table 98. Programmable Delay 0Register Settings

Signal Function	Register Bit Address	Register Definition
Delay value select for programmable delay & edge detector (VDD = 3.3V, typical condition)	reg<1603:1602>	00: 150 ns 01: 300 ns 10: 450 ns 11: 600 ns
Select the edge mode of programmable delay & edge detector	reg<1601:1600>	00: Rising Edge Detector 01: Falling Edge Detector 10: Both Edge Detector 11: Both Edge Delay
Select edge detector output mode	reg<1604>	0: Non-Delayed Output 1: Delayed Output

19.4 Programmable Delay 1 Register Settings

Table 99. Programmable Delay 1 Register Settings

Signal Function	Register Bit Address	Register Definition
Delay value select for programmable delay & edge detector (VDD = 3.3V, typical condition)	reg<1608:1607>	00: 150 ns 01: 300 ns 10: 450 ns 11: 600 ns
Select the edge mode of programmable delay & edge detector	reg<1606:1605>	00: Rising Edge Detector 01: Falling Edge Detector 10: Both Edge Detector 11: Both Edge Delay
Select edge detector output mode	reg<1609>	0: Non-Delayed Output 1: Delayed Output

20.0 Voltage Reference (VREF)

20.1 Voltage Reference Overview

The SLG46621 has a Voltage Reference Macrocell to provide references to the six analog comparators. This macrocell can supply a user selection of fixed voltage references, /3 and /4 reference off of the V_{DD} power supply to the device, and externally supplied voltage references from pins 5, 7,10 and 14. The macrocell also has the option to output reference voltages on pins 18 and 19. See table below for the available selections for each analog comparator. Also see *Figure 113.* below, which shows the reference output structure.VREF Selection Table

Table 100. VREF Selection Table.

reg_acmpx-ref_sel <4:0>	ACMP0_VREF	ACMP1_VREF	ACMP2_VREF	ACMP3_VREF	ACMP4_VREF	ACMP5_VREF
11111	DAC0_out	DAC0_out	DAC0_out	DAC0_out	DAC0_out	DAC0_out
11110	DAC1_out	DAC1_out	DAC1_out	DAC1_out	DAC1_out	DAC1_out
11101	vref_ext_ac-mp0 / 2	vref_ext_ac-mp0 / 2	vref_ext_ac-mp2 / 2	vref_ext_ac-mp2 / 2	vref_ext_ac-mp2 / 2	vref_ext_ac-mp5 / 2
11100	vref_ext_ac-mp1 / 2	vref_ext_ac-mp1 / 2	vref_ext_ac-mp1 / 2	vref_ext_ac-mp1 / 2	vref_ext_ac-mp1 / 2	vref_ext_ac-mp1 / 2
11011	vref_ext_acmp0	vref_ext_acmp0	vref_ext_acmp2	vref_ext_acmp2	vref_ext_acmp2	vref_ext_acmp5
11010	vref_ext_acmp1	vref_ext_acmp1	vref_ext_acmp1	vref_ext_acmp1	vref_ext_acmp1	vref_ext_acmp1
11001	vdd/4	vdd/4	vdd/4	vdd/4	vdd/4	vdd/4
11000	vdd/3	vdd/3	vdd/3	vdd/3	vdd/3	vdd/3
10111	1.20	1.20	1.20	1.20	1.20	1.20
10110	1.15	1.15	1.15	1.15	1.15	1.15
10101	1.10	1.10	1.10	1.10	1.10	1.10
10100	1.05	1.05	1.05	1.05	1.05	1.05
10011	1.00	1.00	1.00	1.00	1.00	1.00
10010	0.95	0.95	0.95	0.95	0.95	0.95
10001	0.90	0.90	0.90	0.90	0.90	0.90
10000	0.85	0.85	0.85	0.85	0.85	0.85
01111	0.80	0.80	0.80	0.80	0.80	0.80
01110	0.75	0.75	0.75	0.75	0.75	0.75
01101	0.70	0.70	0.70	0.70	0.70	0.70
01100	0.65	0.65	0.65	0.65	0.65	0.65
01011	0.60	0.60	0.60	0.60	0.60	0.60
01010	0.55	0.55	0.55	0.55	0.55	0.55
01001	0.50	0.50	0.50	0.50	0.50	0.50
01000	0.45	0.45	0.45	0.45	0.45	0.45
00111	0.40	0.40	0.40	0.40	0.40	0.40
00110	0.35	0.35	0.35	0.35	0.35	0.35
00101	0.30	0.30	0.30	0.30	0.30	0.30
00100	0.25	0.25	0.25	0.25	0.25	0.25
00011	0.20	0.20	0.20	0.20	0.20	0.20
00010	0.15	0.15	0.15	0.15	0.15	0.15
00001	0.10	0.10	0.10	0.10	0.10	0.10
00000	0.05	0.05	0.05	0.05	0.05	0.05

Table 101. VREF Range.

VDD	Practial VREF Range	Note
2.0 V - 5.5 V	50 mV ~ 1.2 V	Do not use external Vref when VDD > 5.0 V and T = 85°C
1.7 V - 2.0 V	50 mV ~ 1.1 V	Do not operate above 1.1 V

20.2 VREF Block Diagram

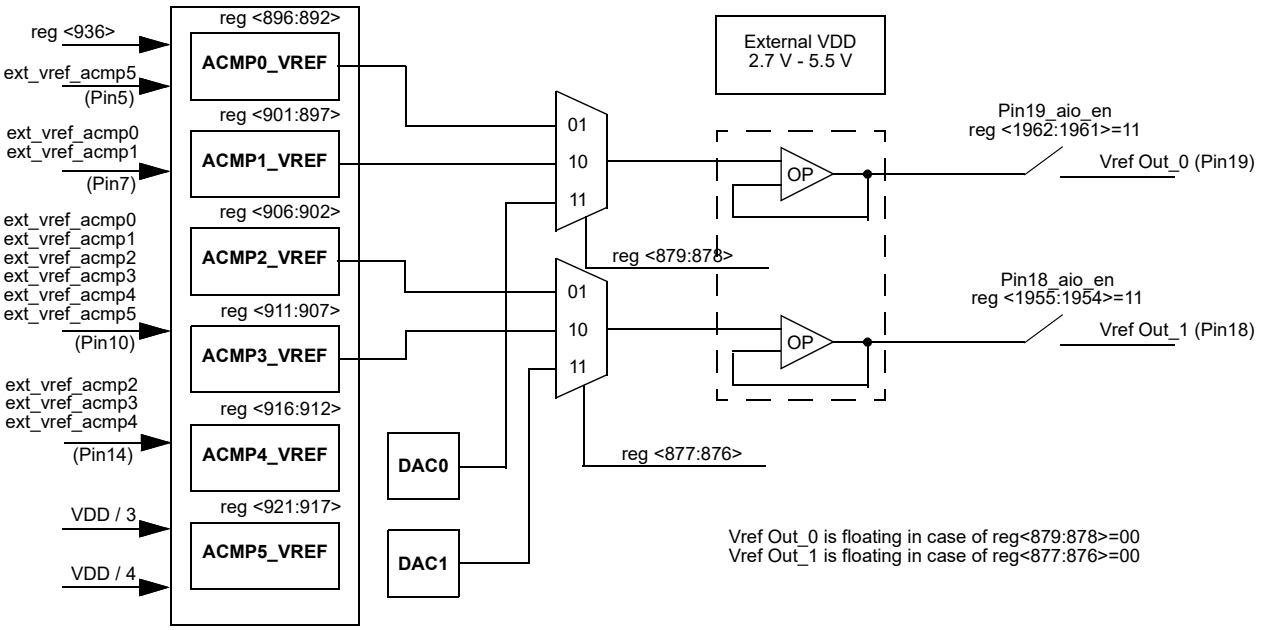


Figure 113. Voltage Reference Block Diagram

21.0 Oscillators

The SLG46621 has three internal RC oscillators (25 kHz or 2 MHz, user selectable), as well as one Low-Frequency oscillator (1.73 kHz) and one Ring oscillator (27 MHz).

There are two divider stages for the RC and Ring oscillators, one divider stage for the Low-Frequency oscillator, that gives the user flexibility for introducing clock signals to connection matrix 0 and 1, as well as various other Macrocells. The predivider (first stage) for RC Oscillator allows the selection of /1, /2, /4 or /8, for LF Osc - /1, /2, /4 or /16 and for Ring Osc - /1, /4, /8 or /16 to divide down frequency from the fundamental. The second stage divider (does not apply for LF Osc) has an input of frequency from the predivider, and outputs one of eight different frequencies on Connection Matrix Input lines <49> and <48>. The output of LF Osc Predivider goes directly on Connection Matrix Input line <50>. Please see below, for more details on the SLG46621 clock scheme.

The Matrix Power Down function allowes to switch on/off the oscillators using an external pin (reg<1648> for 25 kHz / 2 MHz OSC, reg<1652> for LF OSC and reg<1638> for Ring Osc):

- **Enable <1>**. If PWR DOWN input of oscillator is LOW, the oscillator will be turned on. If PWR DOWN input

of oscillator is HIGH the oscillator will be turned off.

- **Disable <0>**. Turns off the Matrix Power Down function.

The PWR CONTROL signal has the highest priority.

The user can select two OSC POWER MODEs (reg<1649> for 25 kHz / 2 MHz OSC, reg<1653> for LF OSC and reg<1640> for Ring Osc):

- **If FORCE POWER ON <1>** is selected, the OSC will run when the SLG46621 is powered on.
- **If AUTO POWER ON <0>** is selected, the OSC will run only when any macrocell that uses OSC is powered on.

OSC can be turned on by:

- Register control (force power on);
- Delay mode, when delay requires OSC;
- ADC;
- PWM/DCMP.

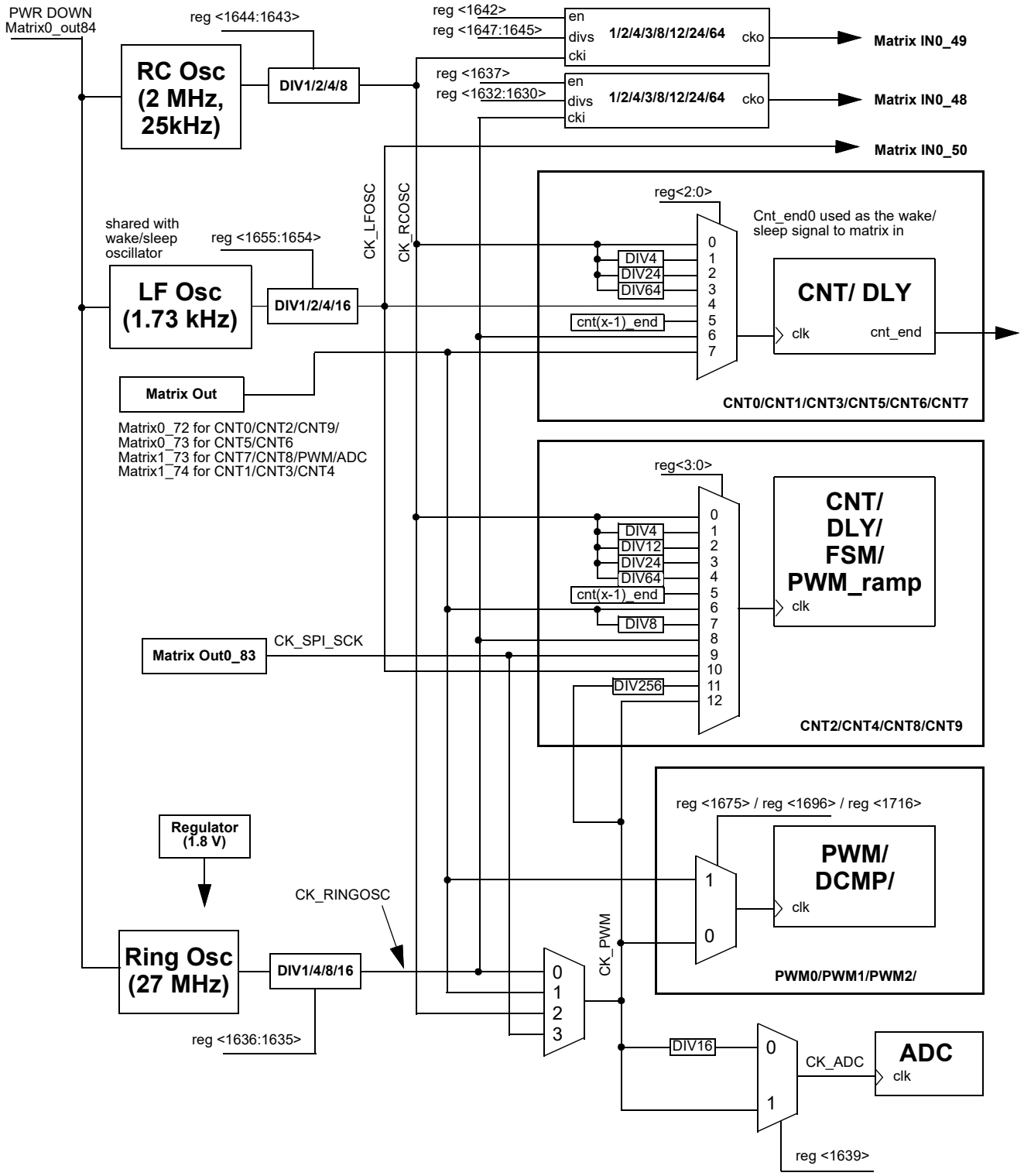


Figure 114. Oscillator Block Diagram

21.1 Oscillator Power On delay

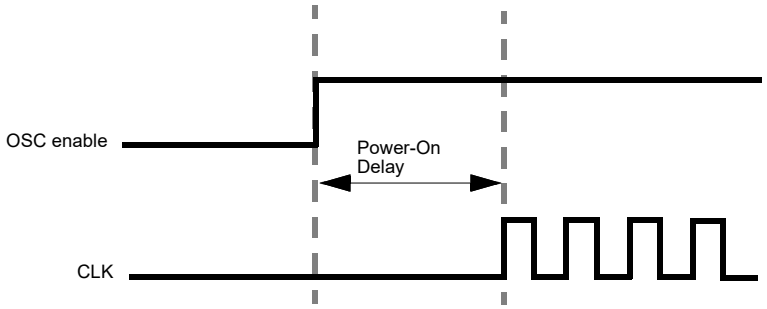


Figure 115. Oscillator Startup Diagram

Note 1: OSC power mode: "Auto Power On".

Note 2: 'OSC enable' signal appears when any block that uses OSC is powered on.

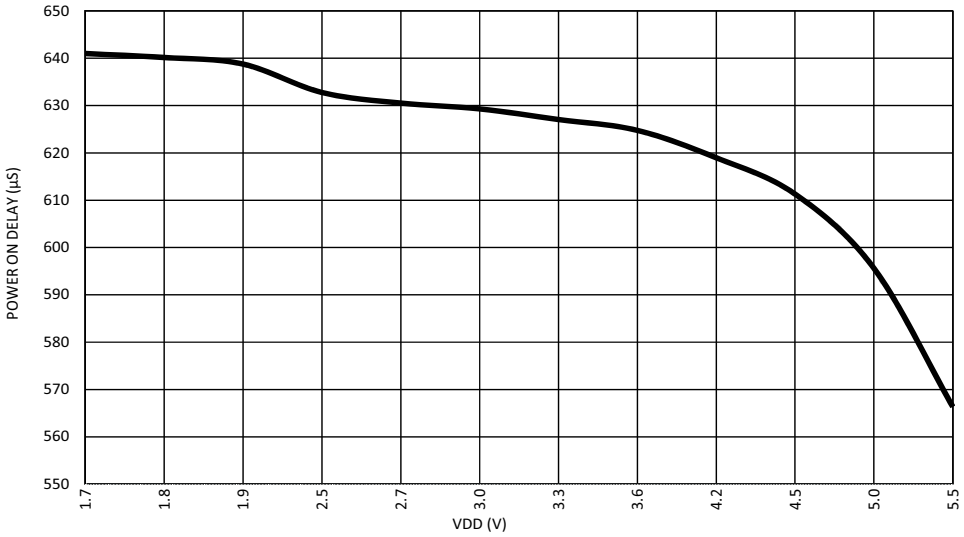


Figure 116. Low Frequency Oscillator Maximum Power On Delay vs. VDD at room temperature

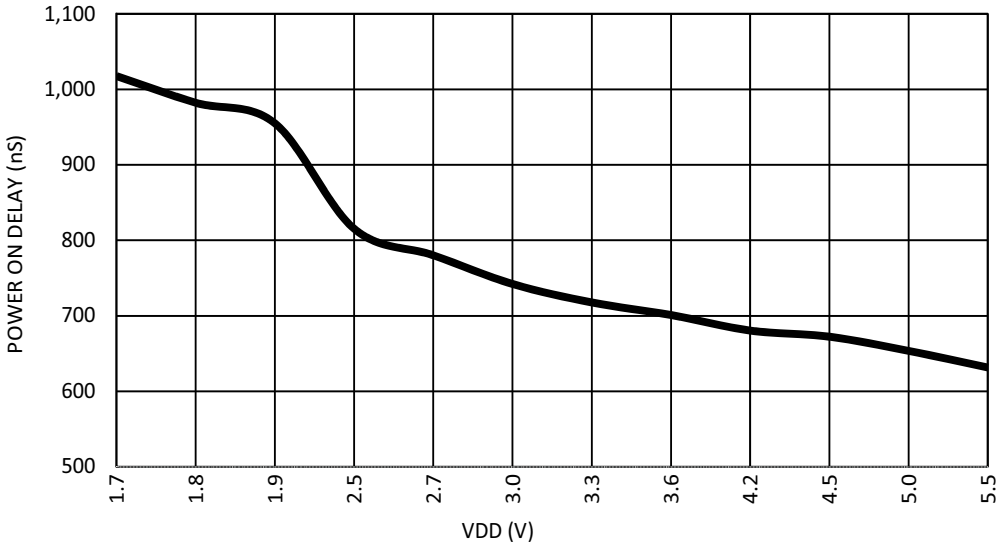


Figure 117. RC Oscillator Maximum Power On Delay vs. VDD at room temperature, RC OSC=2 MHz.

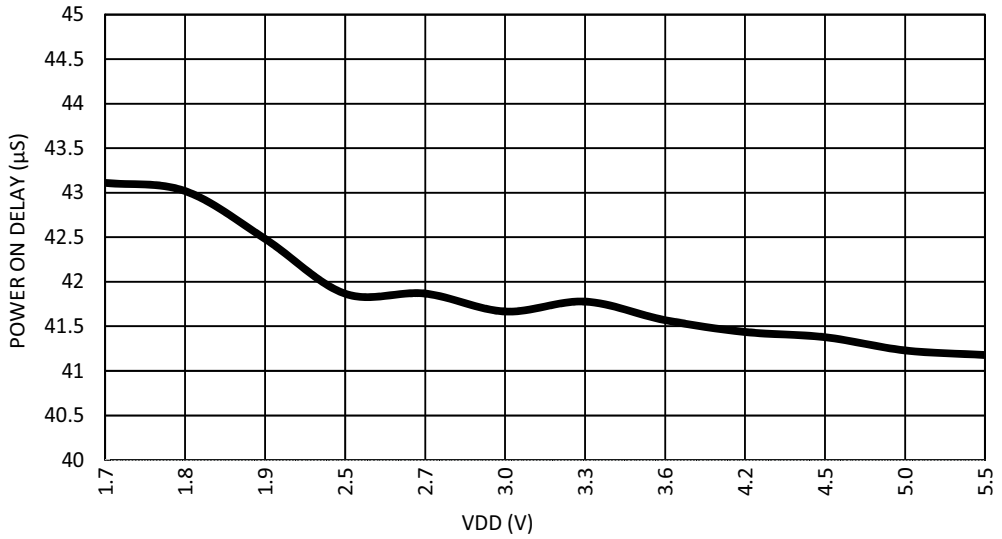


Figure 118. RC Oscillator Maximum Power On Delay vs. VDD at room temperature, RC OSC=25 kHz.

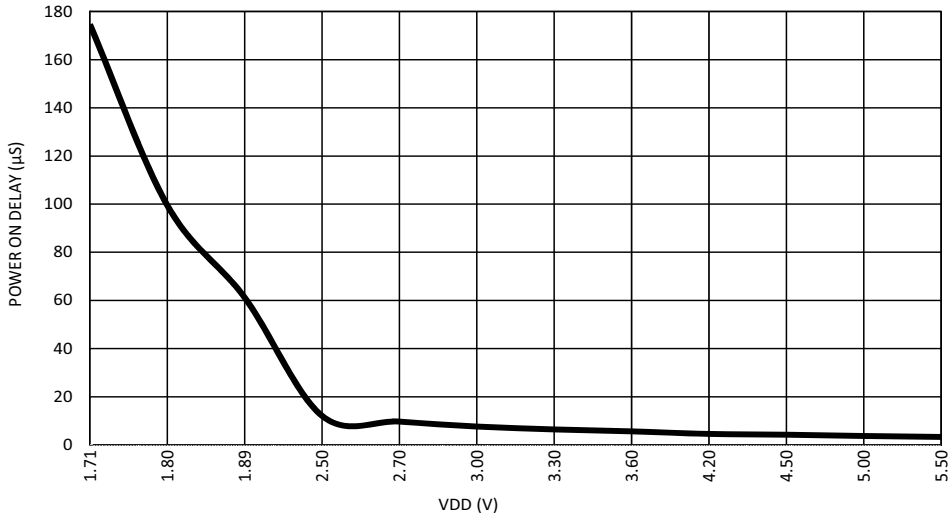


Figure 119. Ring Oscillator Maximum Power On Delay vs. VDD at room temperature.

21.2 Oscillator Accuracy

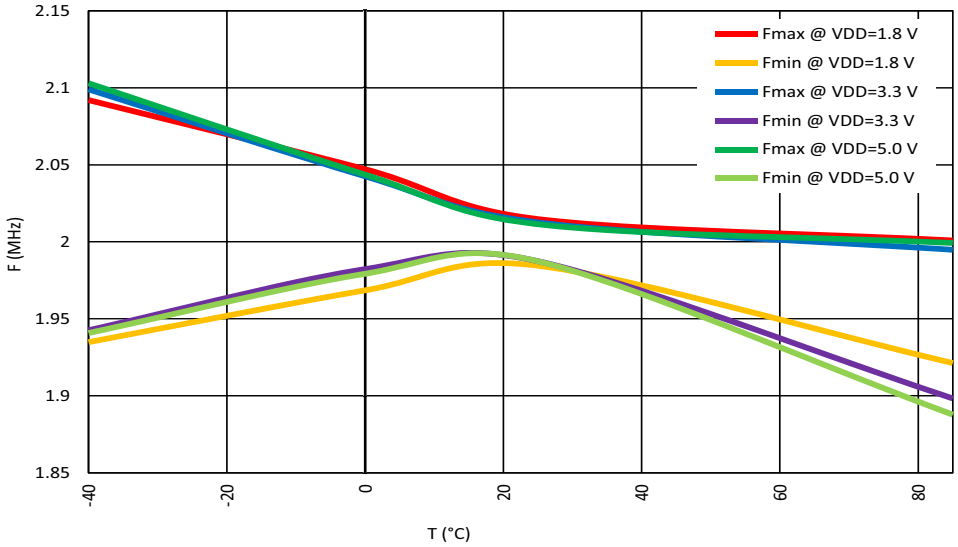


Figure 120. RC Oscillator Frequency vs. Temperature, RC OSC=2 MHz

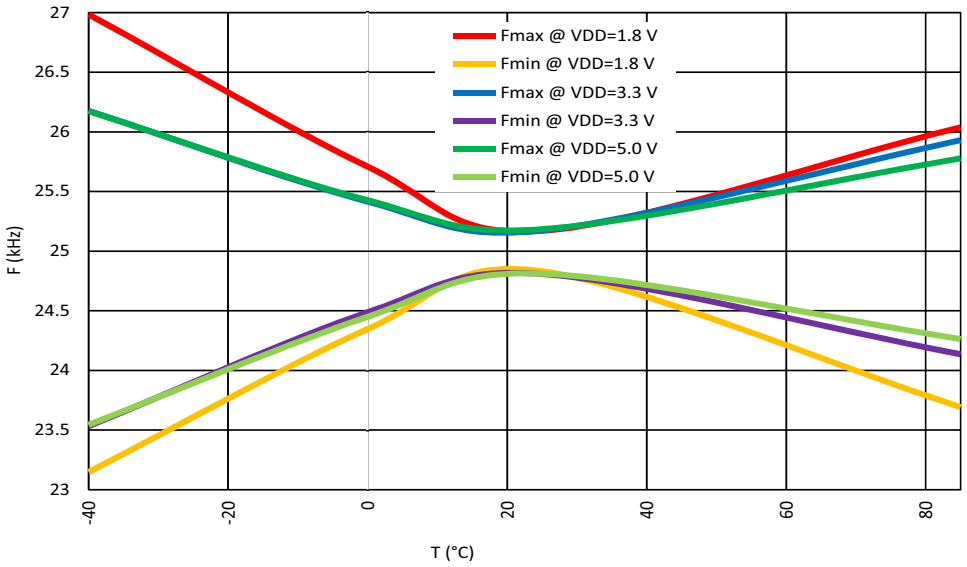


Figure 121. RC Oscillator Frequency vs. Temperature, RC OSC=25 kHz

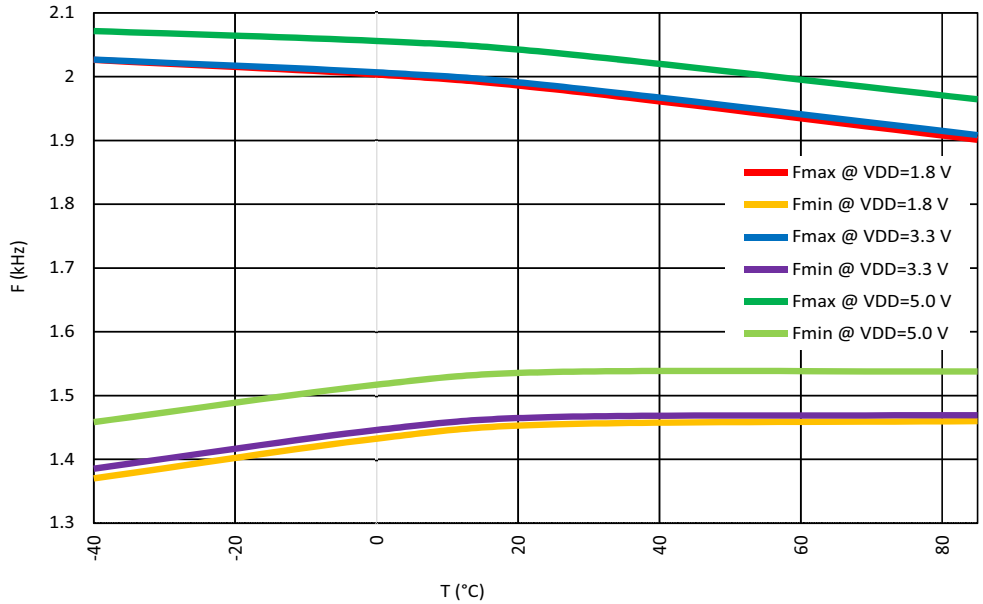


Figure 122. LF Oscillator Frequency vs. Temperature, LF OSC=1.73 kHz

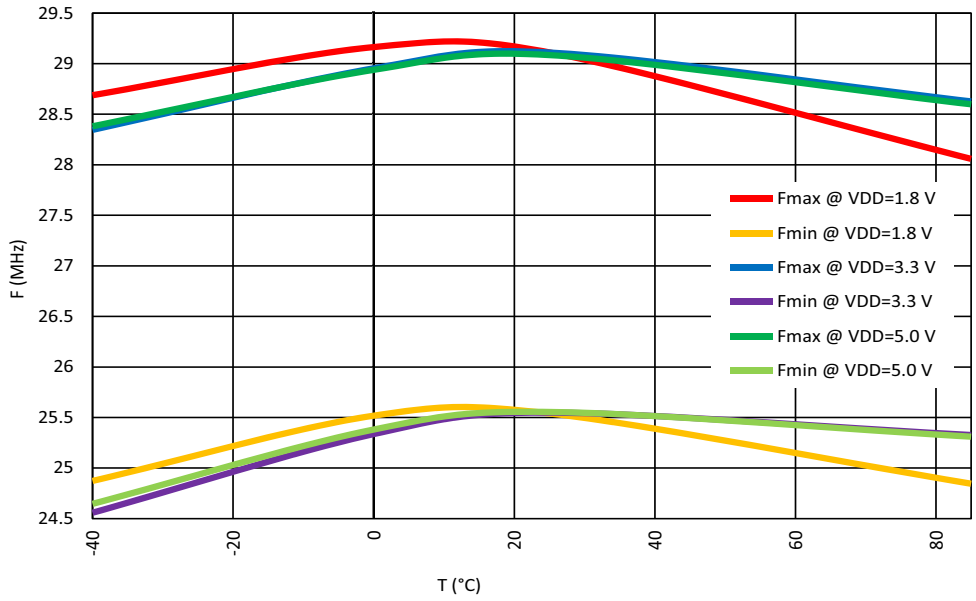


Figure 123. Ring Oscillator Frequency vs. Temperature, Ring OSC=27 MHz

Note: For more information see section 5.10 OSC Specifications.

22.0 Power On Reset (POR)

The SLG46621 has a power-on reset (POR) macrocell to ensure correct device initialization and operation of all macrocells in the device. The purpose of the POR circuit is to have consistent behavior and predictable results when the VDD power is first ramping to the device, and also while the VDD is falling during power-down. To accomplish this goal, the POR drives a defined sequence of internal events that trigger changes to the states of different macrocells inside the device, and finally to the state of the I/O pins.

22.1 General Operation

The SLG46621 is guaranteed to be powered down and nonoperational when the VDD voltage (voltage on PIN1) is less than Power Off Threshold (see in Electrical Characteristics table), but not less than -0.6V. Another essential condition for the chip to be powered down is that no voltage higher (see Note 1) than the VDD voltage is applied to any other PIN. For example, if VDD voltage is 0.3V, applying a voltage higher than 0.3V to any other PIN is incorrect, and can lead to incorrect or unexpected device behavior.

Note 1. There is a 0.6V margin due to forward drop voltage of the ESD protection diodes.

To start the POR sequence in the SLG46621, the voltage applied on the VDD should be higher than the Power_ON threshold (see Note 2). The full operational VDD range for the SLG46621 is 1.71 V – 5.5 V (1.8 V ±5% – 5 V±10%). This means that the VDD voltage must ramp up to the operational voltage value, but the POR sequence will start earlier, as soon as the VDD voltage rises to the Power_ON threshold. After the POR sequence has started, the SLG46621 will have a typical period of time to go through all the steps in the sequence (see *Figure 111.* and *Figure 112.*), and will be ready and completely operational after the POR sequence is complete.

Note 2. The Power_ON threshold is defined in Electrical Characteristics table.

Note 3. VDD ramp rising speed must be less than 0.6 V/µs after power on. Violating this specification may cause chip to restart.

To power down the chip the VDD voltage should be lower than the operational and to guarantee that chip is powered down it should be less than Power Off Threshold.

All PINs are in high impedance state when the chip is powered down and while the POR sequence is taking place. The last step in the POR sequence releases the I/O structures from the high impedance state, at which time the device is operational. The pin configuration at this point in time is defined by the design programmed into the chip. Also as it was mentioned before the voltage on PINs can't be bigger than the VDD, this rule also applies to the case when the chip is powered on.

Note that VDD2 has no influence on POR sequence, all internal macrocells are powered from VDD. It means, VDD2 can be switched on/off while VDD is on. If voltage on VDD2 appears after the POR sequence, pins 12, 13, 15, 16, 17, 18, 19, 20 become available when VDD2 reaches 0.6 V.

For proper power up sequence, make sure VDD2 will not exceed VDD at any point during startup.

For normal operation VDD should not be switched off while VDD2 is on, due to VDD2≤VDD, see section *5.0 Electrical Specifications*.

22.2 POR Sequence

The POR system generates a sequence of signals that enable certain macrocells. The sequence is shown in *Figure 124.* .

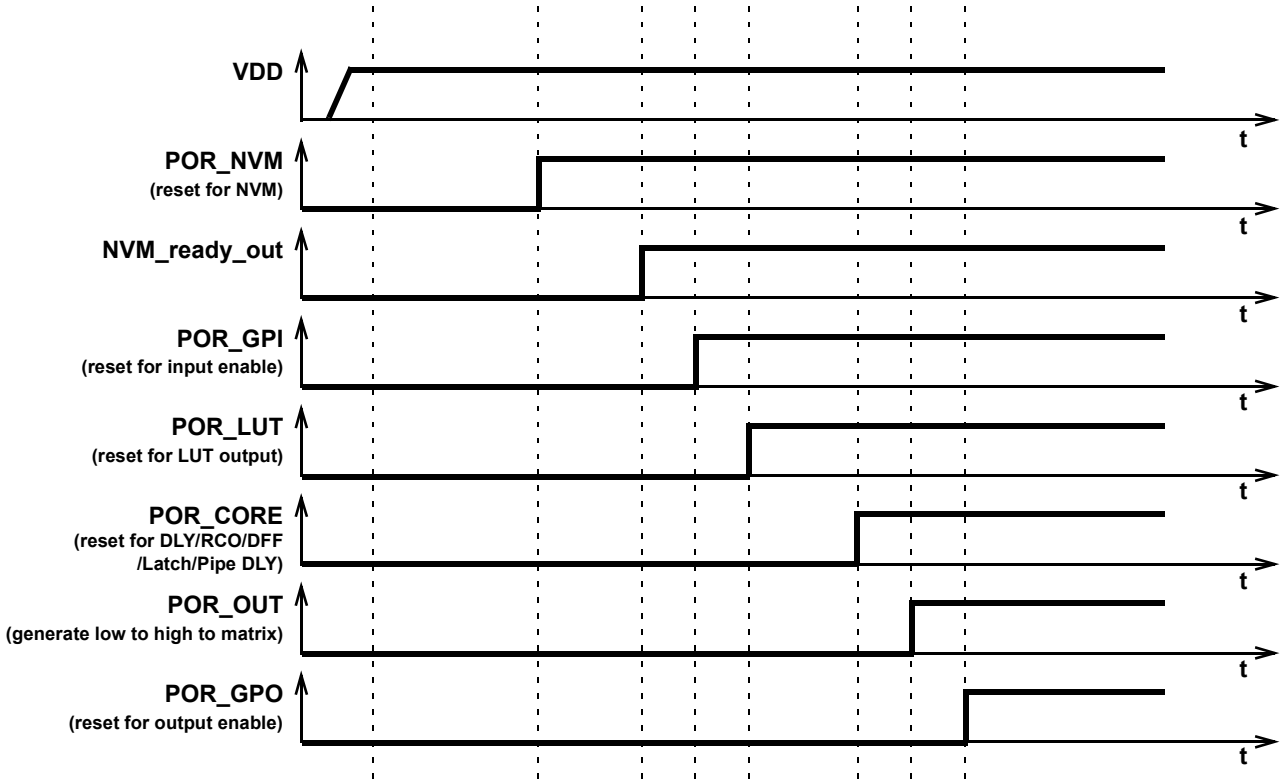


Figure 124. POR sequence

As can be seen from *Figure 124.* after the VDD has start ramping up and crosses the Power_ON threshold, first, the on-chip NVM memory is reset. Next the chip reads the data from NVM, and transfers this information to SRAM registers that serve to configure each macrocell, and the Connection Matrix which routes signals between macrocells. The third stage causes the reset of the input pins, and then to enable them. After that, the LUTs are reset and become active. After LUTs the Delay cells, RC OSC, DFFs, Latches and Pipe Delay are initialized. Only after all macrocells are initialized internal POR signal (POR macrocell output) goes from LOW to HIGH. The last portion of the device to be initialized are the output PINs, which transition from high impedience to active at this point.

The typical time that takes to complete the POR sequence varies by device type in the GreenPAK family. It also depends on many environmental factors, such as: slew rate, VDD value, temperature and even will vary from chip to chip (process influence).

22.3 Macrocells Output States During POR Sequence

To have a full picture of SLG46621 operation during powering and POR sequence, review the overview the macrocell output states during the POR sequence (*Figure 125.* describes the output signals states).

First, before the NVM has been reset, all macrocells have their output set to logic LOW (except the output PINs which are in high impedance state). Before the NVM is ready, all macrocell outputs are unpredictable (except the output PINs). On the next step, some of the macrocells start initialization: input pins output state becomes LOW; LUTs also output LOW. Only P DLY macrocell configured as edge detector becomes active at this time. After that input PINs are enabled. Next, only LUTs are configured. Next, all other macrocells are initialized. After macrocells are initialized, internal POR matrix signal switches from LOW to HIGH. The last are output PINs that become active and determined by the input signals.

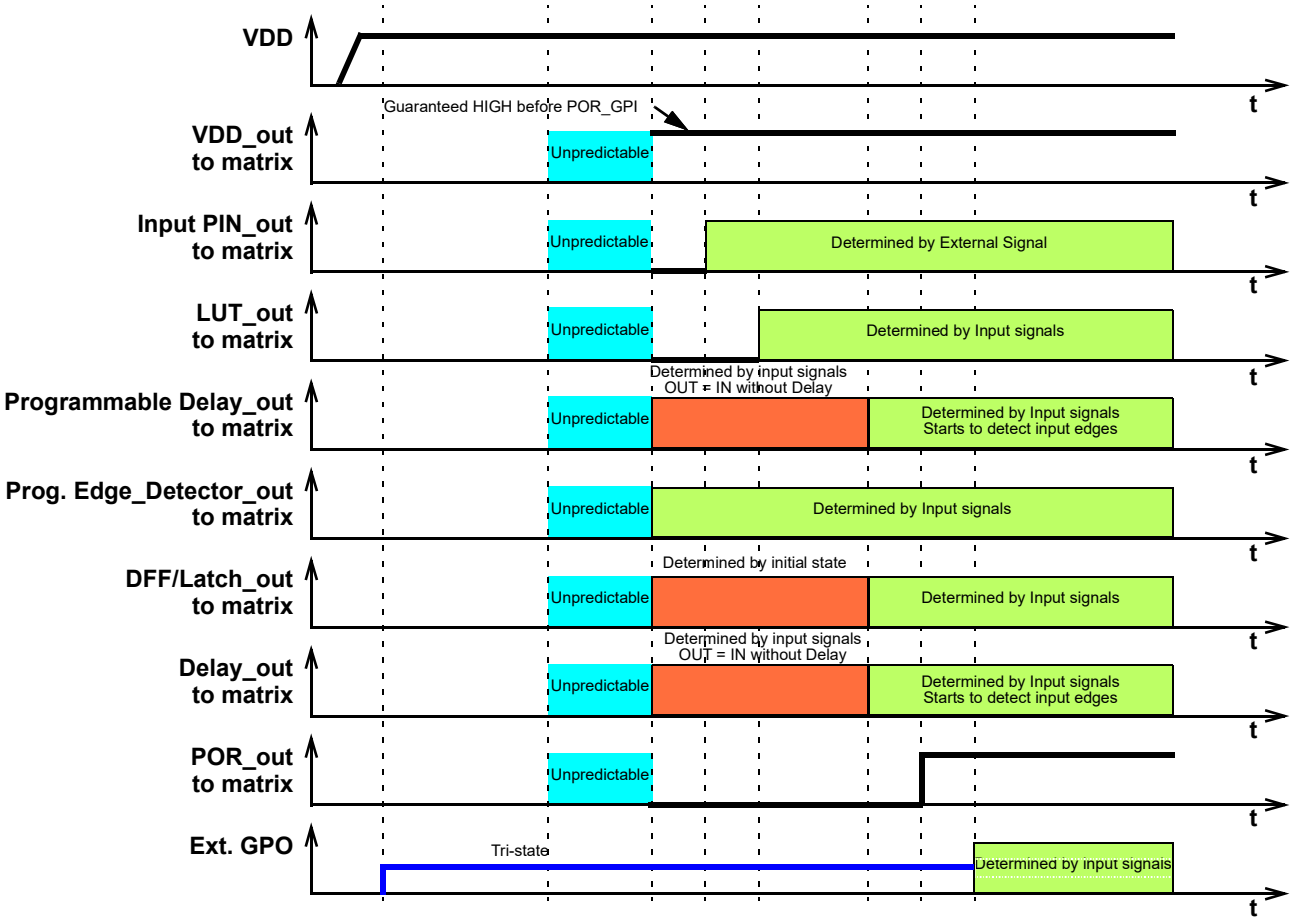


Figure 125. Internal Macrocell States during POR sequence

22.4 Initialization

All internal macrocells by default have initial low level. Starting from indicated powerup time of 1.15 V - 1.6 V, macrocells in SLG46621 are powered on while forced to the reset state, All outputs are in Hi-Z and chip starts loading data from NVM. Then the reset signal is released for internal macrocells and they start to initialize according to the following sequence:

1. Input PINs, ACMP, pull up/down;
2. LUTs;
3. DFFs, Delays/Counters, Pipe Delay;
4. POR output to matrix;
5. Output PIN corresponds to the internal logic

The VREF output pin driving signal can precede POR output signal going high by 3 µs - 5 µs. The POR signal going high indicates the mentioned powerup sequence is complete.

Note: The maximum voltage applied to any PIN should not be higher than the VDD level. There are ESD Diodes between PIN –> VDD and PIN –> GND on each PIN. So if the input signal applied to PIN is higher than VDD, then current will sink through the diode to VDD. Exceeding VDD results in leakage current on the input PIN, and VDD will be pulled up, following the voltage on the input PIN.There is no effect from input pin when input voltage is applied at the same time as VDD.

22.5 Power Down

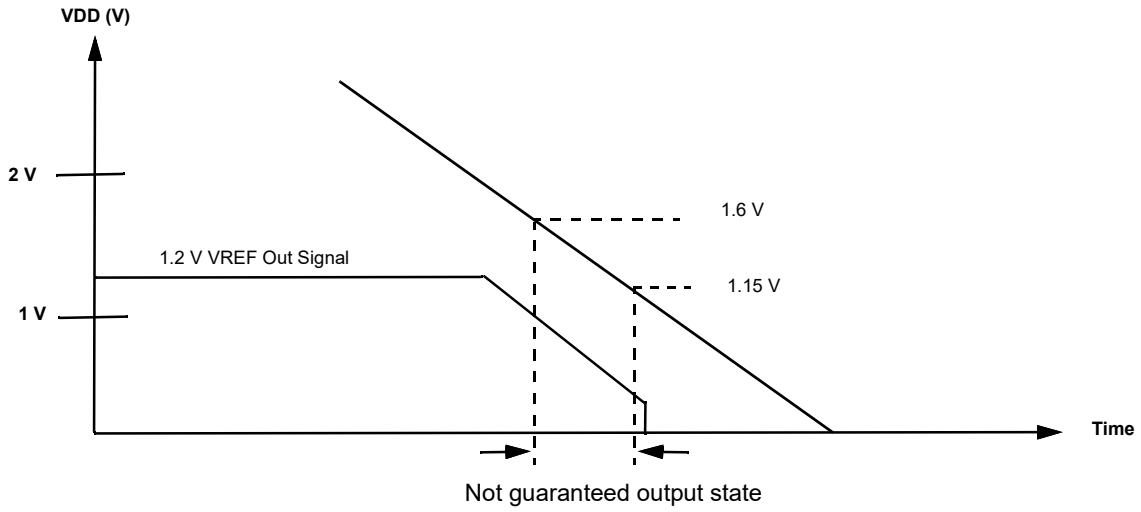


Figure 126. Power Down

During powerdown, macrocells in SLG46621 are powered off after VDD falling down below Power Off Threshold. Please note that during a slow rampdown, outputs can possibly switch state during this time.

22.6 External reset

The SLG46621 has an optional External Reset function on Pin2. It allows to reset the chip while powered on.
Pin2 must be configured as Digital Input reg<942:941> and function Reset must be enabled also, reg<2020>: 0 - disabled, 1 - enabled. Unlike POR, External Reset affects only GPI, LUTs, DLY, RC osc, DFFs, Latchs, Pipe Delay, Matrix and GPO. While NVM remains its previous state, see *Figure 116.* to *Figure 127.* .

Note: External Reset affects Pipe Delay only if its nRST is connected to POR.

Note that during External Reset the output pin's status will depend on the OE control circuits and current consumption is determined by the design.

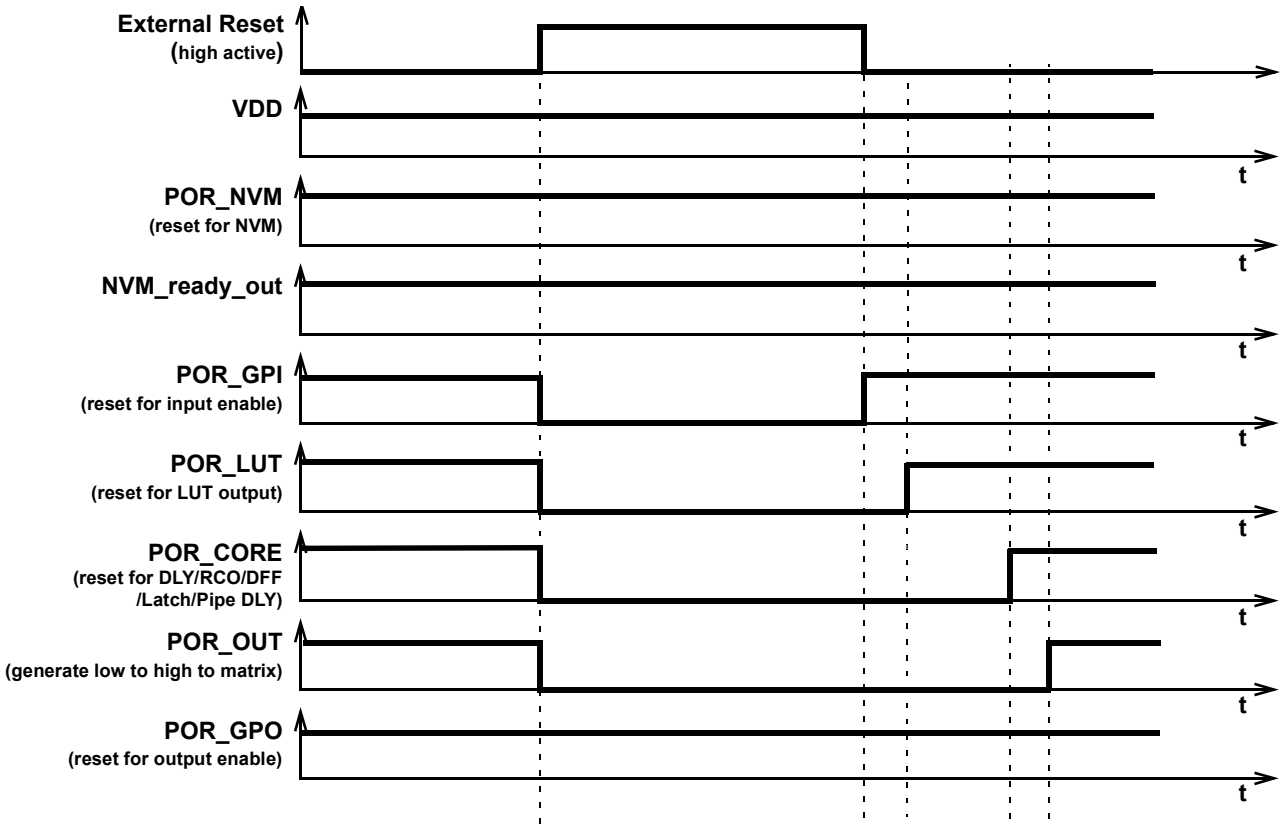


Figure 127. External reset sequence (High active).

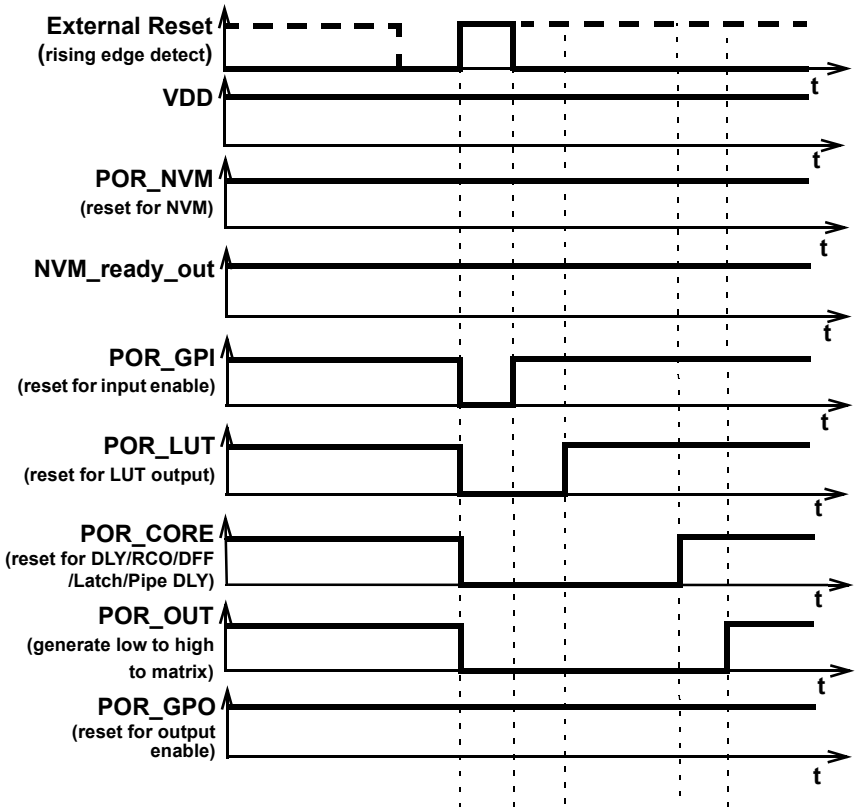


Figure 128. External reset sequence (Rising edge detect).

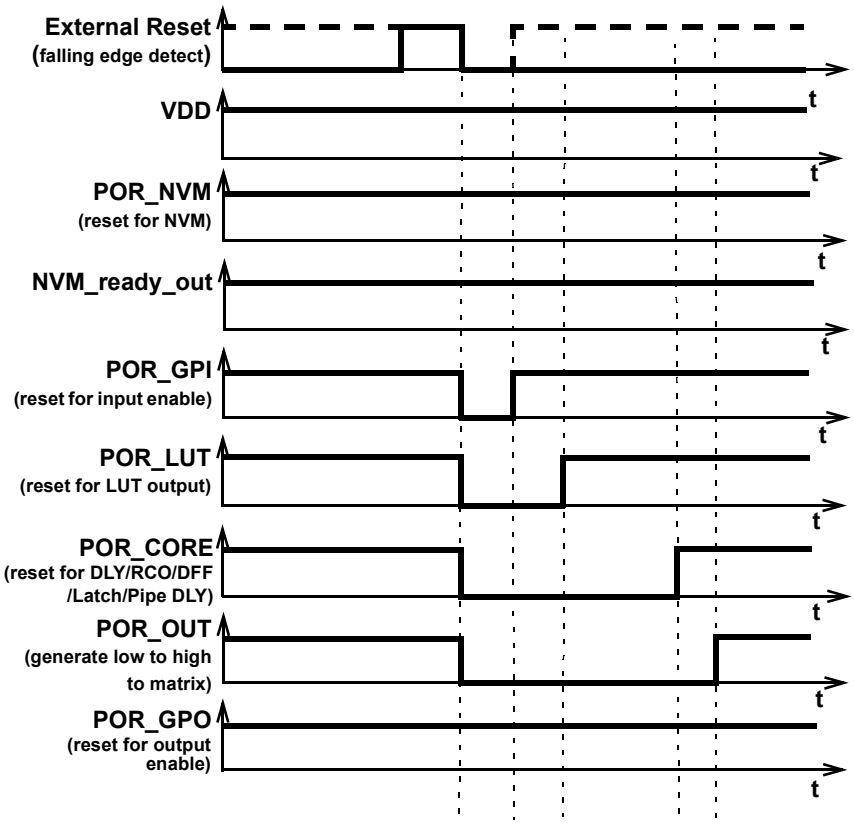


Figure 129. External reset sequence (Falling edge detect)

Table 102. External reset Register Settings

Signal Function	Register Bit Address	Register Definition
Pin2 edge reset enable	reg<2018>	0: edge reset enable (controlled by reg<2019>) 1: high level reset
Pin2 rising/falling edge reset	reg<2019>	0: rising 1: falling
Pin2 reset function	reg<2020>	0: disable 1: enable

23.0 Power Detector

The Power Detect (PWR DET) is used to monitor the state of the internal charge pump regulator. The macrocell only has one output (OUT). The PWR DET output is HIGH when V_{DD} < 2.7 V and LOW when V_{DD} > 2.7 V. In order to use the macrocell reg<2010> must be set to 0.

24.0 Additional Logic Functions

The SLG46621 has two additional logic functions that are connected directly to the Connection Matrix inputs and outputs. There are two inverters which can switch the polarity of any Connection Matrix signal.

24.1 INV_0 Gate

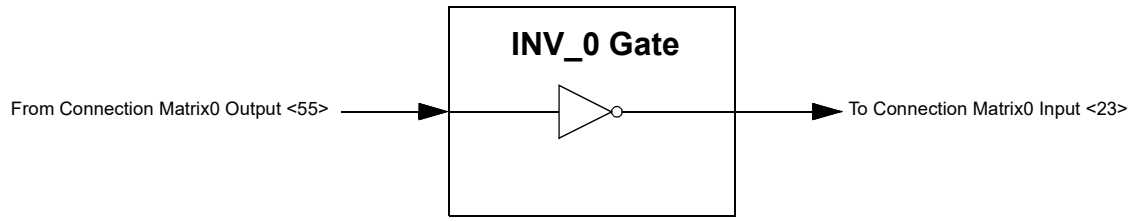


Figure 130. INV_0 Gate

24.2 INV_1 Gate

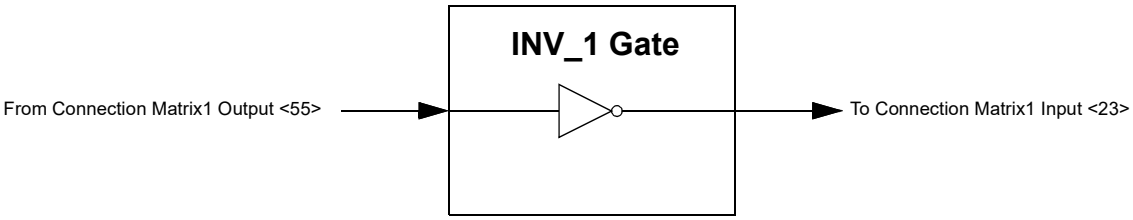


Figure 131. INV_1 Gate

25.0 Appendix A - SLG46621 Register Definition

Register Bit Address	Signal Function	Register Bit Definition
reg<5:0>	Matrix 0 Out: In0 of LUT2_0	
reg<11:6>	Matrix 0 Out: In1 of LUT2_0	
reg<17:12>	Matrix 0 Out: In0 of LUT2_1	
reg<23:18>	Matrix 0 Out: In1 of LUT2_1	
reg<29:24>	Matrix 0 Out: In0 of LUT2_2	
reg<35:30>	Matrix 0 Out: In1 of LUT2_2	
reg<41:36>	Matrix 0 Out: In0 of LUT2_3	
reg<47:42>	Matrix 0 Out: In1 of LUT2_3	
reg<53:48>	Matrix 0 Out: In0 of LUT3_0	
reg<59:54>	Matrix 0 Out: In1 of LUT3_0	
reg<65:60>	Matrix 0 Out: In2 of LUT3_0	
reg<71:66>	Matrix 0 Out: In0 of LUT3_1	
reg<77:72>	Matrix 0 Out: In1 of LUT3_1	
reg<83:78>	Matrix 0 Out: In2 of LUT3_1	
reg<89:84>	Matrix 0 Out: In0 of LUT3_2	
reg<95:90>	Matrix 0 Out: In1 of LUT3_2	
reg<101:96>	Matrix 0 Out: In2 of LUT3_2	
reg<107:102>	Matrix 0 Out: In0 of LUT3_3	
reg<113:108>	Matrix 0 Out: In1 of LUT3_3	
reg<119:114>	Matrix 0 Out: In2 of LUT3_3	
reg<125:120>	Matrix 0 Out: In0 of LUT3_4	
reg<131:126>	Matrix 0 Out: In1 of LUT3_4	
reg<137:132>	Matrix 0 Out: In2 of LUT3_4	
reg<143:138>	Matrix 0 Out: In0 of LUT3_5	
reg<149:144>	Matrix 0 Out: In1 of LUT3_5	
reg<155:150>	Matrix 0 Out: In2 of LUT3_5	
reg<161:156>	Matrix 0 Out: In0 of LUT3_6	
reg<167:162>	Matrix 0 Out: In1 of LUT3_6	
reg<173:168>	Matrix 0 Out: In2 of LUT3_6	
reg<179:174>	Matrix 0 Out: In0 of LUT3_7	
reg<185:180>	Matrix 0 Out: In1 of LUT3_7	
reg<191:186>	Matrix 0 Out: In2 of LUT3_7	
reg<197:192>	Matrix 0 Out: In0 of LUT4_0	
reg<203:198>	Matrix 0 Out: In1 of LUT4_0	
reg<209:204>	Matrix 0 Out: In2 of LUT4_0 or PGEN CLK	
reg<215:210>	Matrix 0 Out: In3 of LUT4_0 or PGEN ResetB	
reg<221:216>	Matrix 0 Out: Set or Resetb of DFF0/Latch0	
reg<227:222>	Matrix 0 Out: Data of DFF0/Latch0	
reg<233:228>	Matrix 0 Out: Clock of DFF0/Latch0	
reg<239:234>	Matrix 0 Out: Set or Resetb of DFF1/Latch1	
reg<245:240>	Matrix 0 Out: Data of DFF1/Latch1	
reg<251:246>	Matrix 0 Out: Clock of DFF1/Latch1	

Register Bit Address	Signal Function	Register Bit Definition
reg<257:252>	Matrix 0 Out: Set or Resetb of DFF2/Latch2	
reg<263:258>	Matrix 0 Out: Data of DFF2/Latch2	
reg<269:264>	Matrix 0 Out: Clock of DFF2/Latch2	
reg<275:270>	Matrix 0 Out: Data of DFF3/Latch3	
reg<281:276>	Matrix 0 Out: Clock of DFF3/Latch3	
reg<287:282>	Matrix 0 Out: Data of DFF4/Latch4	
reg<293:288>	Matrix 0 Out: Clock of DFF4/Latch4	
reg<299:294>	Matrix 0 Out: Data of DFF5/Latch5	
reg<305:300>	Matrix 0 Out: Clock of DFF5/Latch5	
reg<311:306>	Matrix 0 Out: Clock of Pipe Delay 0	
reg<317:312>	Matrix 0 Out: Input Data of Pipe Delay 0	
reg<323:318>	Matrix 0 Out: Reset of Pipe Delay 0	
reg<329:324>	Matrix 0 Out: Input of Edge Detector and Programmable Delay 0	
reg<335:330>	Matrix 0 Out: Input of Inverter 0	
reg<341:336>	Matrix 0 Out: Digital Output of PIN 3	
reg<347:342>	Matrix 0 Out: OE of PIN 3	
reg<353:348>	Matrix 0 Out: Digital Output of PIN 4	
reg<359:354>	Matrix 0 Out: Digital Output of PIN 5	
reg<365:360>	Matrix 0 Out: OE of PIN 5	
reg<371:366>	Matrix 0 Out: Digital Output of PIN 6	
reg<377:372>	Matrix 0 Out: Digital Output of PIN 7	
reg<383:378>	Matrix 0 Out: OE of PIN 7	
reg<389:384>	Matrix 0 Out: Digital Output of PIN 8	
reg<395:390>	Matrix 0 Out: Digital Output of PIN 9	
reg<401:396>	Matrix 0 Out: OE of PIN 9	
reg<407:402>	Matrix 0 Out: Digital Output of PIN 10	
reg<413:408>	Matrix 0 Out: OE of PIN 10	
reg<419:414>	Matrix 0 Out: PDB(Power Down) for ACMP0	
reg<425:420>	Matrix 0 Out: PDB(Power Down) for ACMP4	
reg<431:426>	Matrix 0 Out: PDB(Power Down) for ACMP5	
reg<437:432>	Matrix 0 Out: CNT0/CNT2/CNT9/ External Clock(CLK_Matrix0)	
reg<443:438>	Matrix 0 Out: CNT5/CNT6 External Clock(CLK_Matrix1)	
reg<449:444>	Matrix 0 Out: Input of DLY/CNT0	
reg<455:450>	Matrix 0 Out: Input of DLY/CNT2	
reg<461:456>	Matrix 0 Out: Keep of DLY/CNT2	
reg<467:462>	Matrix 0 Out: Up of DLY/CNT2	
reg<473:468>	Matrix 0 Out: Input of DLY/CNT5	
reg<479:474>	Matrix 0 Out: Input of DLY/CNT6	
reg<485:480>	Matrix 0 Out: Input of DLY/CNT9	
reg<491:486>	Matrix 0 Out: ADC Power Down	
reg<497:492>	Matrix 0 Out: CSB of SPI	
reg<503:498>	Matrix 0 Out: SCLK of SPI	

Register Bit Address	Signal Function	Register Bit Definition
reg<509:504>	Matrix 0 Out: Oscillator Power Down	
reg<515:510>	Matrix 0 Out: Cross Connection Output to Matrix 1 <0>	
reg<521:516>	Matrix 0 Out: Cross Connection Output to Matrix 1 <1>	
reg<527:522>	Matrix 0 Out: Cross Connection Output to Matrix 1 <2>	
reg<533:528>	Matrix 0 Out: Cross Connection Output to Matrix 1 <3>	
reg<539:534>	Matrix 0 Out: Cross Connection Output to Matrix 1 <4>	
reg<545:540>	Matrix 0 Out: Cross Connection Output to Matrix 1 <5>	
reg<551:546>	Matrix 0 Out: Cross Connection Output to Matrix 1 <6>	
reg<557:552>	Matrix 0 Out: Cross Connection Output to Matrix 1 <7>	
reg<563:558>	Matrix 0 Out: Cross Connection Output to Matrix 1 <8>	
reg<569:564>	Matrix 0 Out: Cross Connection Output to Matrix 1 <9>	
reg<575:570>	Reserved	
LUT Data		
reg<579:576>	LUT2_0 data	data
reg<583:580>	LUT2_1 data	data
reg<587:584>	LUT2_2 data	data
reg<591:588>	LUT2_3 data	data
reg<599:592>	LUT3_0 data	data
reg<607:600>	LUT3_1 data	data
reg<615:608>	LUT3_2 data	data
reg<623:616>	LUT3_3 data	data
reg<631:624>	LUT3_4 data	data
reg<639:632>	LUT3_5 data	data
reg<647:640>	LUT3_6 data	data
reg<655:648>	LUT3_7 data	data
LUT4_0 and PGEN		
reg<671:656>	LUT4_0 & PGEN data	data
reg<675:672>	4-bit counter data in PGEN	data
reg<676>	PGEN Enable Signal	0: LUT4 Function 1: PGEN Function
DFF/Latch 0		
reg<677>	Mode Select	0: DFF Function 1: Latch Function
reg<678>	Output Parity Control	0: Q Output 1: QB Output
reg<679>	Set or Reset Selection	0: Reset State by Matrix 1: Set State by Matrix
reg<680>	Initial State During POR	0: Initial State is 0 1: Initial State is 1
DFF/Latch 1		
reg<681>	Mode Select	0: DFF Function 1: Latch Function
reg<682>	Output Parity Control	0: Q Output 1: QB Output

Register Bit Address	Signal Function	Register Bit Definition
reg<683>	Set or Reset Selection	0: Reset State by Matrix 1: Set State by Matrix
reg<684>	Initial State During POR	0: Initial State is 0 1: Initial State is 1
DFF/Latch 2		
reg<685>	Mode Select	0: DFF Function 1: Latch Function
reg<686>	Output Parity Control	0: Q Output 1: QB Output
reg<687>	Set or Reset Selection	0: Reset State by Matrix 1: Set State by Matrix
reg<688>	Initial State During POR	0: Initial State is 0 1: Initial State is 1
DFF/Latch 3		
reg<689>	Mode Select	0: DFF Function 1: Latch Function
reg<690>	Output Parity Control	0: Q Output 1: QB Output
reg<691>	Initial State During POR	0: Initial State is 0 1: Initial State is 1
DFF/Latch 4		
reg<692>	Mode Select	0: DFF Function 1: Latch Function
reg<693>	Output Parity Control	0: Q Output 1: QB Output
reg<694>	Initial State During POR	0: Initial State is 0 1: Initial State is 1
DFF/Latch 5		
reg<695>	Mode Select	0: DFF Function 1: Latch Function
reg<696>	Output Parity Control	0: Q Output 1: QB Output
reg<697>	Initial State During POR	0: Initial State is 0 1: Initial State is 1
LUT Data		
reg<701:698>	LUT2_4 data	data
reg<705:702>	LUT2_5 data	data
reg<709:706>	LUT2_6 data	data
reg<713:710>	LUT2_7 data	data
reg<721:714>	LUT3_8 data	data
reg<729:722>	LUT3_9 data	data
reg<737:730>	LUT3_10 data	data
reg<745:738>	LUT3_11 data	data
reg<753:746>	LUT3_12 data	data
reg<761:754>	LUT3_13 data	data
reg<769:762>	LUT3_14 data	data
reg<777:770>	LUT3_15 data	data

Register Bit Address	Signal Function	Register Bit Definition
reg<793:778>	LUT4_1 data	data
DFF/Latch 6		
reg<794>	Mode Select	0: DFF Function 1: Latch Function
reg<795>	Output Parity Control	0: Q Output 1: QB Output
reg<796>	Set or Reset Selection	0: Reset State by Matrix 1: Set State by Matrix
reg<797>	Initial State During POR	0: Initial State is 0 1: Initial State is 1
DFF/Latch 7		
reg<798>	Mode Select	0: DFF Function 1: Latch Function
reg<799>	Output Parity Control	0: Q Output 1: QB Output
reg<800>	Set or Reset Selection	0: Reset State by Matrix 1: Set State by Matrix
reg<801>	Initial State During POR	0: Initial State is 0 1: Initial State is 1
DFF/Latch 8		
reg<802>	Mode Select	0: DFF Function 1: Latch Function
reg<803>	Output Parity Control	0: Q Output 1: QB Output
reg<804>	Set or Reset Selection	0: Reset State by Matrix 1: Set State by Matrix
reg<805>	Initial State During POR	0: Initial State is 0 1: Initial State is 1
DFF/Latch 9		
reg<806>	Mode Select	0: DFF Function 1: Latch Function
reg<807>	Output Parity Control	0: Q Output 1: QB Output
reg<808>	Initial State During POR	0: Initial State is 0 1: Initial State is 1
DFF/Latch 10		
reg<809>	Mode Select	0: DFF Function 1: Latch Function
reg<810>	Output Parity Control	0: Q Output 1: QB Output
reg<811>	Initial State During POR	0: Initial State is 0 1: Initial State is 1
DFF/Latch 11		
reg<812>	Mode Select	0: DFF Function 1: Latch Function
reg<813>	Output Parity Control	0: Q Output 1: QB Output
reg<814>	Initial State During POR	0: Initial State is 0 1: Initial State is 1

Register Bit Address	Signal Function	Register Bit Definition
ADC and ACMP Control		
reg<815>	ADC Native Input From Internal DAC0	0: Disable 1: Enable
reg<816>	Multichannel Input Mux Enable (State by PIN 16)	0: Disable (PIN 16 can not Control) 1: Enable
reg<817>	ADC Input Mode Control	0: Single-Ended Input 1: Differential Input
reg<820:818>	ADC PGA Gain Selection	000: 0.25x (For single-ended operation only) 001: 0.5x (For single-ended operation only) 010: 1x 011: 2x 100: 4x 101: 8x (For single-ended and differential operation) 110: 16x (For differential operation only) 111: Reserved
reg<821>	PGA Power On Signal Note: in ADC Wake Sleep/dynamic On/Off Mode, it should Set to 0	0: Power Down 1: Power On
reg<822>	ADC Pseudo Differential Mode Enable	0: Disable 1: Enable
reg<830:823>	DAC1 8 Bit Register Control	00: DAC1 Output is ADC Vref bottom Voltage FF: DAC1's Output is ADC Vref top Voltage
reg<831>	ACMP 1 Input 100u Current Source Enable	0: Disable 1: Enable
reg<832>	ACMP 0 Input 100u Current Source Enable	0: Disable 1: Enable
reg<833>	Reserved	
reg<834>	DAC1 Power On Signal	0: Power Down 1: Power On When DAC0 Used Only, need set this bit
reg<835>	Reserved	
reg<837:836>	ACMP Buffer Bandwidth Selection	00: 1 K 01: 5 K 10: 20 K 11: 50 K
reg<839:838>	ADC Speed Selection	00: Reserved 01: Reserved 10: 100 kHz 11: Reserved
reg<840>	DAC0 Power On Signal	0: Power Down 1: Power On When DAC0 Used Only, need set this bit
reg<842:841>	ADC Vref Source Select	00: ADC V_{REF} 01: Reserved 10: 1/4 Vdd 11: None
reg<843>	DAC0 Input Selection	0: From Register 1: From DCMP1's Negative Input
reg<851:844>	DAC0 8 Bit Register Control	00: DAC0 Output is 0 FF: DAC0 Output is 1 V
reg<852>	ACMP 0 Low Bandwidth Enable	0: Disable 1: Enable

Register Bit Address	Signal Function	Register Bit Definition
reg<854:853>	ACMP 0 Positive Input Gain Control	00: 1x 01: 0.5x 10: 0.33x 11: 0.25x
reg<856:855>	ACMP 0 Input Selection	00: PIN 6 Input 01: With Buffer 10: Vdd 11: None
reg<858:857>	ACMP 1 Positive Input Gain Control	00: 1x 01: 0.5x 10: 0.33x 11: 0.25x
reg<860:859>	ACMP 1 Input Selection	00: PIN 12 Input 01: ADC PGA out 10: ACMP 0 Input (before Gain) 11: None
reg<861>	ACMP 1 Low Bandwidth Enable	0: Disable 1: Enable
reg<862>	ACMP 2 Low Bandwidth Enable	0: Disable 1: Enable
reg<863>	ACMP 2 Input Selection	0: PIN 13 Input 1: ACMP 0 Input (before Gain)
reg<865:864>	ACMP 2 Positive Input Gain Control	00: 1x 01: 0.5x 10: 0.33x 11: 0.25x
reg<866>	ACMP 3 Low Bandwidth Enable	0: Disable 1: Enable
reg<868:867>	ACMP 3 Positive Input Gain Control	00: 1x 01: 0.5x 10: 0.33x 11: 0.25x
reg<870:869>	ACMP 3 Input Selection	00: PIN 15 Input 01: PIN 13 Input 10: ACMP 0 Input (before Gain) 11: None
reg<872:871>	ACMP 4 Positive Input Gain Control	00: 1x 01: 0.5x 10: 0.33x 11: 0.25x
reg<874:873>	ACMP 4 Input Selection	00: PIN 3 Input 01: PIN 15 Input 10: ACMP 0 Input (before Gain) 11: None
reg<875>	ACMP 4 Low Bandwidth Enable	0: Disable 1: Enable
reg<877:876>	Output Buffer1 Source Selection	00: Buffer Power Down 01: ACMP 2' Input 10: ACMP 3's Input 11: DAC1's Output
reg<879:878>	Output Buffer0 Source Selection	00: Buffer Power Down 01: ACMP 0' Input 10: ACMP 1's Input 11: DAC0's Output

Register Bit Address	Signal Function	Register Bit Definition
reg<880>	ACMP 5 Low Bandwidth Enable	0: Disable 1: Enable
reg<881>	Reserved	Reserved
reg<882>	ADC Wake Sleep Enable	0: Disable 1: Enable
reg<883>	DAC1 Input Selection	0: From DCMP1's Negative input 1: From Register
reg<884>	ADC Wake Sleep Enable	0: Disable 1: Enable
reg<885>	Force ADC Analog Circuit On	0: Disable 1: Enable
reg<886>	PGA Output Enable	0: Disable 1: Enable
BG, ACMP and Vref		
reg<891:887>	Reserved	
reg<896:892>	ACMP0 Vref Value Selection	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: Vdd/3 11001: Vdd/4 11010: Vref_Ext_ACMP1 11011: Vref_Ext_ACMP0 11100: Vref_Ext_ACMP1 / 2 11101: Vref_Ext_ACMP0 / 2 11110: DAC1_out 11111: DAC0_out
reg<901:897>	ACMP1 Vref Value Selection	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 11.5 V 10111: 1.2 V 11000: Vdd/3 11001: Vdd/4 11010: Vref_Ext_ACMP1 11011: Vref_Ext_ACMP0 11100: Vref_Ext_ACMP1 / 2 11101: Vref_Ext_ACMP0 / 2 11110: DAC1_out 11111: DAC0_out

Register Bit Address	Signal Function	Register Bit Definition
reg<906:902>	ACMP2 Vref Value Selection	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: Vdd/3 11001: Vdd/4 11010: Vref_Ext_ACMP1 11011: Vref_Ext_ACMP2 11100: Vref_Ext_ACMP1 / 2 11101: Vref_Ext_ACMP2 / 2 11110: DAC1_out 11111: DAC0_out
reg<911:907>	ACMP3 Vref Value Selection	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: Vdd/3 11001: Vdd/4 11010: Vref_Ext_ACMP1 11011: Vref_Ext_ACMP2 11100: Vref_Ext_ACMP1 / 2 11101: Vref_Ext_ACMP2 / 2 11110: DAC1_out 11111: DAC0_out
reg<916:912>	ACMP4 Vref Value Selection	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: Vdd/3 11001: Vdd/4 11010: Vref_Ext_ACMP1 11011: Vref_Ext_ACMP2 11100: Vref_Ext_ACMP1 / 2 11101: Vref_Ext_ACMP2 / 2 11110: DAC1_out 11111: DAC0_out

Register Bit Address	Signal Function	Register Bit Definition
reg<921:917>	ACMP5 Vref Value Selection	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: Vdd/3 11001: Vdd/4 11010: Vref_Ext_ACMP1 11011: Vref_Ext_ACMP5 11100: Vref_Ext_ACMP1 / 2 11101: Vref_Ext_ACMP5 / 2 11110: DAC1_out 11111: DAC0_out
reg<922>	Reserved	
reg<923>	Bangap OK for ADC, ACMP Output Delay Time Select, the start Time is porb_core go to High	0: 550 us 1: 100 us
reg<925:924>	ACMP5 Hystersis Control	00: 0 01: 25 mV 10: 50 mV 11: 200 mV
reg<927:926>	ACMP4 Hystersis Control	00: 0 01: 25 mV 10: 50 mV 11: 200 mV
reg<929:928>	ACMP3 Hystersis Control	00: 0 01: 25 mV 10: 50 mV 11: 200 mV
reg<931:930> >	ACMP2 Hystersis Control	00: 0 01: 25 mV 10: 50 mV 11: 200 mV
reg<933:932>	ACMP1 Hystersis Control	00: 0 01: 25 mV 10: 50 mV 11: 200 mV
reg<935:934>	ACMP0 Hystersis Control	00: 0 01: 25 mV 10: 50 mV 11: 200 mV
reg<936>	Bandgap Turn On by Register	0: Turn Off 1: Turn On (if chip is Power Down, the Bandgap will Power Down even if it is set to 1)
reg<937>	Reserved	
reg<938>	Reserved	
reg<939>	Reserved	
IO Pad		

Register Bit Address	Signal Function	Register Bit Definition
reg<940>	IO preCharge Enable Bit	0: Disable 1: Enable
PIN 2		
reg<942:941>	PIN2 Input Mode Control	00: Digital in without schmitt trigger 01: Digital in with schmitt trigger 10: Low Voltage Digital In 11: Reserved
reg<944:943>	PIN2 Pull-Up/Down Resistor Selection	00: Floating 01: 10 K 10: 100 K 11: 1 M
reg<945>	PIN2 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
PIN 3		
reg<947:946>	PIN 3 Input Mode Control	00: Digital in without schmitt trigger 01: Digital in with schmitt trigger 10: Low Voltage Digital In 11: Analog IO
reg<949:948>	PIN 3 Output Mode Control	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-Drain 11: 2x Open-Drain
reg<951:950>	PIN 3 Pull-Up/Down Resistor Selection	00: Floating 01: 10 K 10: 100 K 11: 1 M
reg<952>	PIN 3 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
PIN 4		
reg<955:953>	PIN 4 Mode Control	000: Digital in without schmitt trigger 001: Digital in with schmitt trigger 010: Low Voltage Digital In 011: Analog IO 100: Push-Pull 101: NMOS Open-Drain 110: PMOS Open-Drain 111: Analog IO & NMOS Open-Drain
reg<957:956>	PIN 4 Pull-Up/Down Resistor Selection	00: Floating 01: 10 K 10: 100 K 11: 1 M
reg<958>	PIN 4 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
reg<959>	PIN 4 Output Driver Current double	0: 1x drive 1: 2x drive
PIN 5		
reg<961:960>	PIN 5 Input Mode Control	00: Digital in without schmitt trigger 01: Digital in with schmitt trigger 10: Low Voltage Digital In 11: Analog IO

Register Bit Address	Signal Function	Register Bit Definition
reg<963:962>	PIN 5 Output Mode Control	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-Drain 11: 2x Open-Drain
reg<965:964>	PIN 5 Pull-Up/Down Resistor Selection	00: Floating 01: 10 K 10: 100 K 11: 1 M
reg<966>	PIN 5 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
PIN 6		
reg<969:967>	PIN 6 Mode Control	000: Digital in without schmitt trigger 001: Digital in with schmitt trigger 010: Low Voltage Digital In 011: Analog IO 100: Push-Pull 101: NMOS Open-Drain 110: PMOS Open-Drain 111: Analog IO & NMOS Open-Drain
reg<971:970>	PIN 6 Pull-Up/Down Resistor Selection	00: Floating 01: 10 K 10: 100 K 11: 1 M
reg<972>	PIN 6 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
reg<973>	PIN 6 Output Driver Current double	0: 1x drive 1: 2x drive
PIN 7		
reg<975:974>	PIN 7 Input Mode Control	00: Digital in without schmitt trigger 01: Digital in with schmitt trigger 10: Low Voltage Digital In 11: Analog IO
reg<977:976>	PIN 7 Output Mode Control	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-Drain 11: 2x Open-Drain
reg<979:978>	PIN 7 Pull-Up/Down Resistor Selection	00: Floating 01: 10 K 10: 100 K 11: 1 M
reg<980>	PIN 7 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
PIN 8		
reg<983:981>	PIN 8 Mode Control	000: Digital in without schmitt trigger 001: Digital in with schmitt trigger 010: Low Voltage Digital In 011: Analog IO 100: Push-Pull 101: NMOS Open-Drain 110: PMOS Open-Drain 111: Analog IO & NMOS Open-Drain

Register Bit Address	Signal Function	Register Bit Definition
reg<985:984>	PIN 8 Pull-Up/Down Resistor Selection	00: Floating 01: 10 K 10: 100 K 11: 1 M
reg<986>	PIN 8 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
reg<987>	PIN 8 Output Driver Current double	0: 1x drive 1: 2x drive
PIN 9		
reg<989:988>	PIN 9 Input Mode Control	00: Digital in without schmitt trigger 01: Digital in with schmitt trigger 10: Low Voltage Digital In 11: Analog IO
reg<991:990>	PIN 9 Output Mode Control	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-Drain 11: 2x Open-Drain
reg<993:992>	PIN 9 Pull-Up/Down Resistor Selection	00: Floating 01: 10 K 10: 100 K 11: 1 M
reg<994>	PIN 9 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
PIN 10		
reg<996:995>	PIN 10 Input Mode Control	00: Digital in without schmitt trigger 01: Digital in with schmitt trigger 10: Low Voltage Digital in 11: Analog IO
reg<998:997>	PIN 10 Output Mode Control	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-Drain 11: 2x Open-Drain
reg<1000:999>	PIN 10 Pull-Up/Down Resistor Selection	00: Floating 01: 10 K 10: 100 K 11: 1 M
reg<1001>	PIN 10 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
reg<1002>	PIN 10 4x Drive Enable	0: Disable 1: Enable
reg<1015:1003>	Reserved	Reserved
reg<1023:1016>	Die ID: Power up Sequence Bits	data Hex: 5A
Matrix 1 Output Selection		
reg<1029:1024>	Matrix 1 Out:In0 of LUT2_4	
reg<1035:1030>	Matrix 1 Out:In1 of LUT2_4	
reg<1041:1036>	Matrix 1 Out:In0 of LUT2_5	
reg<1047:1042>	Matrix 1 Out:In1 of LUT2_5	
reg<1053:1048>	Matrix 1 Out:In0 of LUT2_6	
reg<1059:1054>	Matrix 1 Out:In1 of LUT2_6	
reg<1065:1060>	Matrix 1 Out:In0 of LUT2_7	

Register Bit Address	Signal Function	Register Bit Definition
reg<1071:1066>	Matrix 1 Out:In1 of LUT2_7	
reg<1077:1072>	Matrix 1 Out:In0 of LUT3_8	
reg<1083:1078>	Matrix 1 Out:In1 of LUT3_8	
reg<1089:1084>	Matrix 1 Out:In2 of LUT3_8	
reg<1095:1090>	Matrix 1 Out:In0 of LUT3_9	
reg<1101:1096>	Matrix 1 Out:In1 of LUT3_9	
reg<1107:1102>	Matrix 1 Out:In2 of LUT3_9	
reg<1113:1108>	Matrix 1 Out:In0 of LUT3_10	
reg<1119:1114>	Matrix 1 Out:In1 of LUT3_10	
reg<1125:1120>	Matrix 1 Out:In2 of LUT3_10	
reg<1131:1126>	Matrix 1 Out:In0 of LUT3_11	
reg<1137:1132>	Matrix 1 Out:In1 of LUT3_11	
reg<1143:1138>	Matrix 1 Out:In2 of LUT3_11	
reg<1149:1144>	Matrix 1 Out:In0 of LUT3_12	
reg<1155:1150>	Matrix 1 Out:In1 of LUT3_12	
reg<1161:1156>	Matrix 1 Out:In2 of LUT3_12	
reg<1167:1162>	Matrix 1 Out:In0 of LUT3_13	
reg<1173:1168>	Matrix 1 Out:In1 of LUT3_13	
reg<1179:1174>	Matrix 1 Out:In2 of LUT3_13	
reg<1185:1180>	Matrix 1 Out:In0 of LUT3_14	
reg<1191:1186>	Matrix 1 Out:In1 of LUT3_14	
reg<1197:1192>	Matrix 1 Out:In2 of LUT3_14	
reg<1203:1198>	Matrix 1 Out:In0 of LUT3_15	
reg<1209:1204>	Matrix 1 Out:In1 of LUT3_15	
reg<1215:1210>	Matrix 1 Out:In2 of LUT3_15	
reg<1221:1216>	Matrix 1 Out:In0 of LUT4_1	
reg<1227:1222>	Matrix 1 Out:In1 of LUT4_1	
reg<1233:1228>	Matrix 1 Out:In2 of LUT4_1	
reg<1239:1234>	Matrix 1 Out:In3 of LUT4_1	
reg<1245:1240>	Matrix 1 Out:Set or Resetb of DFF6/Latch6	
reg<1251:1246>	Matrix 1 Out:Data of DFF6/Latch6	
reg<1257:1252>	Matrix 1 Out:Clock of DFF6/Latch6	
reg<1263:1258>	Matrix 1 Out:Set or Resetb of DFF7/Latch7	
reg<1269:1264>	Matrix 1 Out:Data of DFF7/Latch7	
reg<1275:1270>	Matrix 1 Out:Clock of DFF7/Latch7	
reg<1281:1276>	Matrix 1 Out:Set or Resetb of DFF8/Latch8	
reg<1287:1282>	Matrix 1 Out:Data of DFF8/Latch8	
reg<1293:1288>	Matrix 1 Out:Clock of DFF8/Latch8	
reg<1299:1294>	Matrix 1 Out:Data of DFF9/Latch9	
reg<1305:1300>	Matrix 1 Out:Clock of DFF9/Latch9	
reg<1311:1306>	Matrix 1 Out:Data of DFF10/Latch10	
reg<1317:1312>	Matrix 1 Out:Clock of DFF10/Latch10	
reg<1323:1318>	Matrix 1 Out:Data of DFF11/Latch11	
reg<1329:1324>	Matrix 1 Out:Clock of DFF11/Latch11	

Register Bit Address	Signal Function	Register Bit Definition
reg<1335:1330>	Matrix 1 Out:Clock of Pipe Delay 1	
reg<1341:1336>	Matrix 1 Out:Input Data of Pipe Delay 1	
reg<1347:1342>	Matrix 1 Out:Reset of Pipe Delay 1	
reg<1353:1348>	Matrix 1 Out:Input of Edge Detector and Programmable Delay 1	
reg<1359:1354>	Matrix 1 Out:Input of Inverter 1	
reg<1365:1360>	Matrix 1 Out:Digital Output of PIN 12	
reg<1371:1366>	Matrix 1 Out:Digital Output of PIN 13	
reg<1377:1372>	Matrix 1 Out:OE of PIN 13	
reg<1383:1378>	Reserved	
reg<1389:1384>	Reserved	
reg<1395:1390>	Matrix 1 Out:Digital Output of PIN 15	
reg<1401:1396>	Matrix 1 Out:Digital Output of PIN 16	
reg<1407:1402>	Matrix 1 Out:OE of PIN 16	
reg<1413:1408>	Matrix 1 Out:Digital Output of PIN 17	
reg<1419:1414>	Matrix 1 Out:Digital Output of PIN 18	
reg<1425:1420>	Matrix 1 Out:OE of PIN 18	
reg<1431:1426>	Matrix 1 Out:Digital Output of PIN 19	
reg<1437:1432>	Matrix 1 Out:OE of PIN 19	
reg<1443:1438>	Matrix 1 Out:Digital Output of PIN 20	
reg<1449:1444>	Matrix 1 Out:PDB(Power Down) for ACMP1	
reg<1455:1450>	Matrix 1 Out:PDB(Power Down) for ACMP2	
reg<1461:1456>	Matrix 1 Out:PDB(Power Down) for ACMP3	
reg<1467:1462>	Matrix 1 Out:CNT7/CNT8/PWM/ADC External Clock (CLK_Matrix2)	
reg<1473:1468>	Matrix 1 Out:CNT1/CNT3/CNT4 External Clock (CLK_Matrix3)	
reg<1479:1474>	Matrix 1 Out:Input of DLY/CNT1	
reg<1485:1480>	Matrix 1 Out:Input of DLY/CNT3	
reg<1491:1486>	Matrix 1 Out:Input of DLY/CNT4	
reg<1497:1492>	Matrix 1 Out:Keep of DLY/CNT4	
reg<1503:1498>	Matrix 1 Out:Up of DLY/CNT4	
reg<1509:1504>	Matrix 1 Out:Input of DLY/CNT7	
reg<1515:1510>	Matrix 1 Out:Input of DLY/CNT8	
reg<1521:1516>	Matrix 1 Out:PWM Power Down	
reg<1527:1522>	Matrix 1 Out:PWM/DCMP0 Positive Input and PWM/DCMP1 Negative Input Register Selection Bit 0	
reg<1533:1528>	Matrix 1 Out:PWM/DCMP0 Positive Input and PWM/DCMP1 Negative Input Register Selection Bit 1	
reg<1539:1534>	Matrix 1 Out:Cross Connection Output to Matrix 0 <0>	
reg<1545:1540>	Matrix 1 Out:Cross Connection Output to Matrix 0 <1>	
reg<1551:1546>	Matrix 1 Out:Cross Connection Output to Matrix 0 <2>	
reg<1557:1552>	Matrix 1 Out:Cross Connection Output to Matrix 0 <3>	
reg<1563:1558>	Matrix 1 Out:Cross Connection Output to Matrix 0 <4>	
reg<1569:1564>	Matrix 1 Out:Cross Connection Output to Matrix 0 <5>	

Register Bit Address	Signal Function	Register Bit Definition
reg<1575:1570>	Matrix 1 Out:Cross Connection Output to Matrix 0 <6>	
reg<1581:1576>	Matrix 1 Out:Cross Connection Output to Matrix 0 <7>	
reg<1587:1582>	Matrix 1 Out:Cross Connection Output to Matrix 0 <8>	
reg<1593:1588>	Matrix 1 Out:Cross Connection Output to Matrix 0 <9>	
reg<1599:1594>	Reserved	
Programmable Delay with Edge Detector 0		
reg<1601:1600>	Mode Selection	00: Rising Edge Detect 01: Falling Edge Detect 10: Both Edge Detect 11: Both Edge Delay
reg<1603:1602>	Delay Time Selection	00: 110 ns Delay 01: 220 ns Delay 10: 330 ns Delay 11: 440 ns Delay
reg<1604>	Output Delay Control	0: Output No Delay 1: Output Delay
Programmable Delay with Edge Detector 1		
reg<1606:1605>	Mode Selection	00: Rising Edge Detect 01: Falling Edge Detect 10: Both Edge Detect 11: Both Edge Delay
reg<1608:1607>	Delay Time Selection	00: 110 ns Delay 01: 220 ns Delay 10: 330 ns Delay 11: 440 ns Delay
reg<1609>	Output Delay Control	0: Output No Delay 1: Output Delay
Pipe Delay 0		
reg<1613:1610>	out0 Selection Bits	Register Bits From 0 to 15, data Delay From 1 to 16 pipes
reg<1617:1614>	out1 Selection Bits	Register Bits From 0 to 15, data Delay From 1 to 16 pipes
reg<1618>	out1 Output polarity Control	0: non-inverted 1: inverted
Pipe Delay 1		
reg<1622:1619>	out0 Selection Bits	Register Bits From 0 to 15, data Delay From 1 to 16 pipes
reg<1626:1623>	out1 Selection Bits	Register Bits From 0 to 15, data Delay From 1 to 16 pipes
reg<1627>	out1 Output polarity Control	0: non-inverted 1: inverted
Oscillator		
reg<1629:1628> >	PWM and ADC Clock Source Select	00: CK_RINGOSC 01: CK_Matrix(Matrix1_out73) 10: CK_RCOSC 11: CK_SPI_SCLK(Matrix0_out83)

Register Bit Address	Signal Function	Register Bit Definition
reg<1632:1630>	Clock divide Ratio Control for ring osc to Matrix	000: /1 001: /2 010: /4 011: /3 100: /8 101: /12 110: /24 111: /64
reg<1633>	PWM data synchronized with SPI Clock Enable	0: Disable 1: Enable
reg<1634>	FSM data synchronized with SPI Clock Enable	0: Disable 1: Enable
reg<1636:1635>	Clock divide Ratio Control for Ring Osc	00: /1 01: /4 10: /8 11: /16
reg<1637>	ring osc Clock to Matrix Input Enable	0: Disable 1: Enable
reg<1638>	Matrix Power Down (Matrix0_out84)Enable for ring Oscillator	0: Disable 1: Enable
reg<1639>	ADC Clock divide by 16 Bypass	0: Non-Bypass 1: Bypass
reg<1640>	Ring Osc Turn On by Register Note: if chip is Powered Down, the Ring Osc will Power Down even if this bit is set to 1	0: Turn Off 1: Turn On
reg<1641>	ADC data synchronized with SPI Clock Enable	0: Disable 1: Enable
reg<1642>	RC osc Clock to Matrix Input Enable	0: Disable 1: Enable
reg<1644:1643>	Clock divide Ratio Control for RC osc	00: /1 01: /2 10: /4 11: /8
reg<1647:1645>	Clock divide Ratio Control for RC osc to Matrix	000: /1 001: /2 010: /4 011: /3 100: /8 101: /12 110: /24 111: /64
reg<1648>	Matrix Power Down (Matrix0_out84)Enable for RC Oscillator	0: Disable 1: Enable
reg<1649>	RC osc Turn On by Register Note: if chip is Powered Down, the Ring Osc will Power Down even if this Bit is Set to 1	0: Turn Off 1: Turn On
reg<1650>	RC osc frequency Select	0: 25 kHz 1: 2 MHz
reg<1651>	bypass RC oscillator with external clock(matrix_out1_73)	0: Rcosc 1: external clock
reg<1652>	matrix power down (matrix0_out84) enable for LF oscillator	0: Disable 1: Enable

Register Bit Address	Signal Function	Register Bit Definition
reg<1653>	Low Frequency osc turn on by register	0: Turn Off 1: Turn On (if chip is Power Down, the LFosc will Power Down even if it is Set to 1)
reg<1655:1654>	Clock divide Ratio Control for LF osc	00: /1 01: /2 10: /4 11: /16
SPI		
reg<1656>	SPI Used as ADC Buffer Enable (1 Clock Delayed)	
reg<1657>	SPI Parallel Input data Source Selection	0: FSM0[7:0], FSM1[7:0] 1: ADC
reg<1658>	SPI Clock phase (CPHA)	
reg<1659>	SPI Clock polarity (CPOL)	
reg<1660>	byte Selection	0: 16 bits 1: 8 bits (least significant 8 Bits)
reg<1661>	SPI Input/Output Mode Selection	0: Serial In Parallel out 1: Parallel In Serial out
PWM0		
reg<1669:1662>	reg3, 8 Bits NVM data to PWM/DCMP or DAC Input	data
reg<1672:1670>	PWM0 Dead Band zone Control	000: 10 ns 001: 20 ns 010: 30 ns 011: 40 ns 100: 50 ns 101: 60 ns 110: 70 ns 111: 80 ns
reg<1673>	PWM/DCMP0 Mode Selection	0: PWM Output duty cycle Down to 0% and DCMP out=1 if A>B 1: PWM Output duty cycle up to 100% and DCMP out=1 if A>=B
reg<1674>	PWM/DCMP0 Function Selection	0: PWM 1: DCMP When in PWM Mode, OUTN0 is pwm1's Negative ouput When in DCMP Mode, OUTN0 is DCMP1's match Output
reg<1675>	PWM/DCMP0 Clock Source Selection	0: Clock From mux State by reg[1629:1628] 1: Matrix1_73
reg<1676>	PWM/DCMP0 Clock Inversion	0: Disable 1: Enable
reg<1677>	power down sync to clock and output state control in power down mode	0: power down is not synchronized with clock,and output reset to 0 when PWM/DCMP is power down, 1: power down is synchronized with clock, when PD=0, the clock is enabled after 2 clock cycles, while when PD=1, the clock is gated immediatlly. and the output is kept at current state when PD=1.
reg<1678>	PWM/DCMP0 Turn On by Register	0: Disable 1: Enable
reg<1680:1679>	PWM/DCMP0 Positive Input Source Selection	00: ADC 01: 8MSBs SPI 10: FSM0_Q[7:0] 11: From MUX State by Matrix1_out[84:83]

Register Bit Address	Signal Function	Register Bit Definition
reg<1682:1681>	PWM/DCMP0 Negative Input Source Selection	00: CNT8_Q[7:0] 01: reg0 10: 8LSBs SPI 11: FSM1_Q[7:0]
reg<1690:1683>	reg2, 8 Bits NVM data to PWM/DCMP or DAC Input	data
PWM1		
reg<1693:1691>	PWM1 Dead Band zone Control	000: 10 ns 001: 20 ns 010: 30 ns 011: 40 ns 100: 50 ns 101: 60 ns 110: 70 ns 111: 80 ns
reg<1694>	PWM/DCMP1 Mode Selection	0: PWM Output duty cycle Down to 0% and DCMP out=1 if A>B 1: PWM Output duty cycle up to 100% and DCMP out=1 if A>=B
reg<1695>	PWM/DCMP1 Function Selection	0: PWM 1: DCMP When in PWM Mode, OUTN1 is pwm1's Negative ouput When in DCMP Mode, OUTN0 is DCMP1's match Output
reg<1696>	PWM/DCMP1 Clock Source Selection	0: Clock From mux State by reg[1629:1628] 1: Matrix1_73
reg<1697>	PWM/DCMP1 Clock Inversion	0: Disable 1: Enable
reg<1698>	PWM/DCMP1 Turn On by Register	0: Disable 1: Enable
reg<1700:1699>	PWM/DCMP1 Positive Input Source Selection	00: ADC 01: 8LSBs SPI 10: FSM1[7: 0] 11: reg1
reg<1702:1701>	PWM/DCMP1 Negative Input and DAC Input Source Selection	00: CNT11_Q[7:0] 01: From MUX State by Matrix1_out[84:83] 10: 8MSBs SPI 11: FSM0_Q[7:0]
reg<1710:1703>	reg1, 8 Bits NVM data to PWM/DCMP or DAC Input	data
PWM2		
reg<1713:1711>	PWM2 Dead Band zone Control	000: 10 ns 001: 20 ns 010: 30 ns 011: 40 ns 100: 50 ns 101: 60 ns 110: 70 ns 111: 80 ns
reg<1714>	PWM/DCMP2 Mode Selection	0: PWM Output duty cycle Down to 0% and DCMP out=1 if A>B 1: PWM Output duty cycle up to 100% and DCMP out=1 if A>=B

Register Bit Address	Signal Function	Register Bit Definition
reg<1715>	PWM/DCMP2 Function Selection	0: PWM 1: DCMP When in PWM Mode, OUTN2 is pwm2's Negative ouput When in DCMP Mode, OUTN2 is DCMP1's match Output
reg<1716>	PWM/DCMP2 Clock Source Selection	0: Clock From mux State by reg<1629: 1628> 1: Matrix1_73
reg<1717>	PWM/DCMP2 Clock Inversion	0: Disable 1: Enable
reg<1718>	PWM/DCMP2 Turn On by Register	0: Disable 1: Enable
reg<1720:1719>	PWM/DCMP2 Positive Input Source Selection	00: ADC 01: 8MSBs SPI 10: FSM1[7: 0] 11: reg3
reg<1722:1721>	PWM/DCMP2 Negative Input and DAC Input Source Selection	00: CNT8_Q[7: 0] 01: reg2 10: 8LSBs SPI 11: FSM0_Q[7: 0]
reg<1730:1723>	reg0, 8 Bits NVM data to PWM/DCMP or DAC Input	data
DLY/CNT 0		
reg<1744:1731>	CNT0 14bits data From Register	data
reg<1747:1745>	DLY/CNT0 Clock Source Select	000: CK_RCOSC 001: CK_RCOSC_DIV4 010: CK_RCOSC_DIV24 011: CK_RCOSC_DIV64 100: CK_LFOSC 101: DLY_OUT9 110: CK_RINGOSC 111: Matrix0_out72
reg<1749:1748>	DLY0 Edge Mode Select or CNT0 Reset Mode Select	If DLY Mode; 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNTReset Mode; 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
reg<1751:1750>	DLY/CNT0 Macrocell Function Select	00: DLY 01: CNT 10: Edge Detect 11: Wake Sleep Ratio Control
reg<1752>	Wake Sleep Output State When WS Oscillator is Power Down	0: in Power Down Mode 1: in Normal Operation State
DLY/CNT 1		
reg<1766:1753>	CNT1 14bits data from Register	data

Register Bit Address	Signal Function	Register Bit Definition
reg<1769:1767>	DLY/CNT1 Clock Source Select	000: CK_RCOSC 001: CK_RCOSC_DIV4 010: CK_RCOSC_DIV24 011: CK_RCOSC_DIV64 100: CK_LFOSC 101: DLY_OUT0 110: CK_RINGOSC 111: Matrix1_out74
reg<1771:1770>	DLY1 Edge Mode Select	If DLY Mode; 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNTReset Mode; 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
reg<1773:1772>	DLY/CNT1 Macrocell Function Select	00: DLY 01: CNT 10: Edge Detect 11: Reserved
DLY/CNT 2/FSM0		
reg<1787:1774>	CNT2 14bits data From Register	data
reg<1791:1788>	DLY2/CNT2/FSM0 Clock Source Select	0001: CK_RCOSC_DIV4 0010: CK_RCOSC_DIV12 0011: CK_RCOSC_DIV24 0100: CK_RCOSC_DIV64 0101: DLY_OUT1 0110: Matrix0_out72 0111: Matrix0_out72 divide by 8 1000: CK_RINGOSC 1001: Matrix0_out83(SPI_SCLK) 1010: CK_LFOSC 1011: CKFSM_DIV256 1100: CKPWM 1101: Reserved 1110: Reserved 1111: Reserved
reg<1793:1792>	DLY2 Edge Mode Select	If DLY Mode; 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNTReset Mode; 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
reg<1795:1794>	DLY/CNT2 Macrocell Function Select	00: DLY 01: CNT/FSM 10: Edge Detect 11: None

Register Bit Address	Signal Function	Register Bit Definition
reg<1797:1796>	FSM0 Input data Source Select	00: 14 Bits NVM data 01: 8bits ADC data 10: 0 11: 8LSBs SPI Parallel data
reg<1798>	CNT2 Value Control	0: Reset (CNT value = 0) 1: Set (CNT value = FSM data)
DLY/CNT 3		
reg<1812:1799>	CNT3 14bits data from Register	data
reg<1815:1813>	DLY/CNT3 Clock Source Select	000: CK_RCOSC 001: CK_RCOSC_DIV4 010: CK_RCOSC_DIV24 011: CK_RCOSC_DIV64 100: CK_LFOSC 101: DLY_OUT2 110: CK_RINGOSC 111: Matrix1_out74
reg<1817:1816>	DLY3 Edge Mode Select	If DLY Mode; 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNTReset Mode; 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
reg<1819:1818>	DLY/CNT3 Macrocell Function Select	00: DLY 01: CNT 10: Edge Detect 11: CNT (the Reset From Matrix not Control the Oscillator)
DLY/CNT 4/FSM1		
reg<1827:1820>	CNT4 8bits data from Register	data
reg<1831:1828>	DLY4/CNT4/FSM1 Clock Source Select	0000: CK_RCOSC 0001: CK_RCOSC_DIV4 0010: CK_RCOSC_DIV12 0011: CK_RCOSC_DIV24 0100: CK_RCOSC_DIV64 0101: DLY_OUT3 0110: Matrix1_out74 0111: Matrix0_out72 divide by 8 1000: CK_RINGOSC 1001: Matrix0_out83(SPI_SCLK) 1010: CK_LFOSC 1011: CKFSM_DIV256 1100: CKPWM 1101: Reserved 1110: Reserved 1111: Reserved

Register Bit Address	Signal Function	Register Bit Definition
reg<1833:1832>	DLY4 Edge Mode Select	If DLY Mode; 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNTReset Mode; 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
reg<1834>	DLY4/CNT4/FSM1 Macrocell Function Select	0: DLY 1: CNT/FSM
reg<1836:1835>	FSM1 Input data Source Select	00: 8 Bits NVM data 01: 8bits ADC data 10: 8MSBs SPI Parallel data 11: 0
reg<1837>	CNT4 Value Control	0: Reset (CNT value = 0) 1: Set (CNT value = FSM data)
DLY/CNT 5		
reg<1845:1838>	CNT5 8bits data From Register	data
reg<1848:1846>	DLY/CNT5 Clock Source Select	000: CK_RCOSC 001: CK_RCOSC_DIV4 010: CK_RCOSC_DIV24 011: CK_RCOSC_DIV64 100: CK_LFOSC 101: DLY_OUT4 110: CK_RINGOSC 111: Matrix0_out73
reg<1850:1849>	DLY5 Edge Mode Select	If DLY Mode; 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNTReset Mode; 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
reg<1851>	DLY/CNT5 Macrocell Function Select	0: DLY 1: CNT
DLY/CNT 6		
reg<1859:1852>	CNT6 8bits data from Register	data
reg<1862:1860>	DLY/CNT6 Clock Source Select	000: CK_RCOSC 001: CK_RCOSC_DIV4 010: CK_RCOSC_DIV24 011: CK_RCOSC_DIV64 100: CK_LFOSC 101: DLY_OUT5 110: CK_RINGOSC 111: Matrix0_out73

Register Bit Address	Signal Function	Register Bit Definition
reg<1864:1863>	DLY6 Edge Mode Select	If DLY Mode; 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNTReset Mode; 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
reg<1865>	DLY/CNT6 Macrocell Function Select	0: DLY 1: CNT
DLY/CNT 7		
reg<1873:1866>	CNT7 8bits data from Register	data
reg<1876:1874>	DLY/CNT7 Clock Source Select	000: CK_RCOSC 001: CK_RCOSC_DIV4 010: CK_RCOSC_DIV24 011: CK_RCOSC_DIV64 100: CK_LFOSC 101: DLY_OUT6 110: CK_RINGOSC 111: Matrix1_out73
reg<1878:1877>	DLY7 Edge Mode Select	If DLY Mode; 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNTReset Mode; 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
reg<1879>	DLY/CNT7 Macrocell Function Select	0: DLY 1: CNT
DLY/CNT 8		
reg<1887:1880>	CNT8 8bits data from Register	data
reg<1891:1888>	DLY/CNT8 Clock Source Select	0000: CK_RCOSC 0001: CK_RCOSC_DIV4 0010: CK_RCOSC_DIV12 0011: CK_RCOSC_DIV24 0100: CK_RCOSC_DIV64 0101: DLY_OUT7 0110: Matrix1_out73 0111: Matrix0_out72 divide by 8 1000:CK_RINGOSC 1001: Matrix0_out83(SPI_SCLK) 1010: CK_LFOSC 1011: CKFSM_DIV256 1100: CKPWM 1101: Reserved 1110: Reserved 1111: Reserved

Register Bit Address	Signal Function	Register Bit Definition
reg<1893:1892>	DLY8 Edge Mode Select	If DLY Mode; 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNTReset Mode; 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
reg<1894>	DLY/CNT8 Macrocell Function Select	0: DLY 1: CNT/PWM_RAMP
DLY/CNT 9		
reg<1902:1895>	CNT9 8bits data from Register	data
reg<1906:1903>	DLY/CNT9 Clock Source Select	0000: CK_RCOSC 0001: CK_RCOSC_DIV4 0010: CK_RCOSC_DIV12 0011: CK_RCOSC_DIV24 0100: CK_RCOSC_DIV64 0101: DLY_OUT8 0110: Matrix0_out72 0111: Matrix0_out72 divide by 8 1000: CK_RINGOSC 1001: Matrix0_out83(SPI_SCLK) 1010: CK_LFOSC 1011: CKFSM_DIV256 1100: CKPWM 1101: Reserved 1110: Reserved 1111: Reserved
reg<1908:1907>	DLY9 Edge Mode Select	If DLY Mode; 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNTReset Mode; 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
reg<1909>	DLY/CNT9 Macrocell Function Select	0: DLY 1: CNT/PWM_RAMP
reg<1910>	Reserved	
PIN 12		
reg<1913:1911>	PIN 12 Mode Control	000: Digital in without schmitt trigger 001: Digital in with schmitt trigger 010: Low Voltage Digital In 011: Analog IO 100: Push-Pull 101: NMOS Open-Drain 110: PMOS Open-Drain 111: Analog IO & NMOS Open-Drain

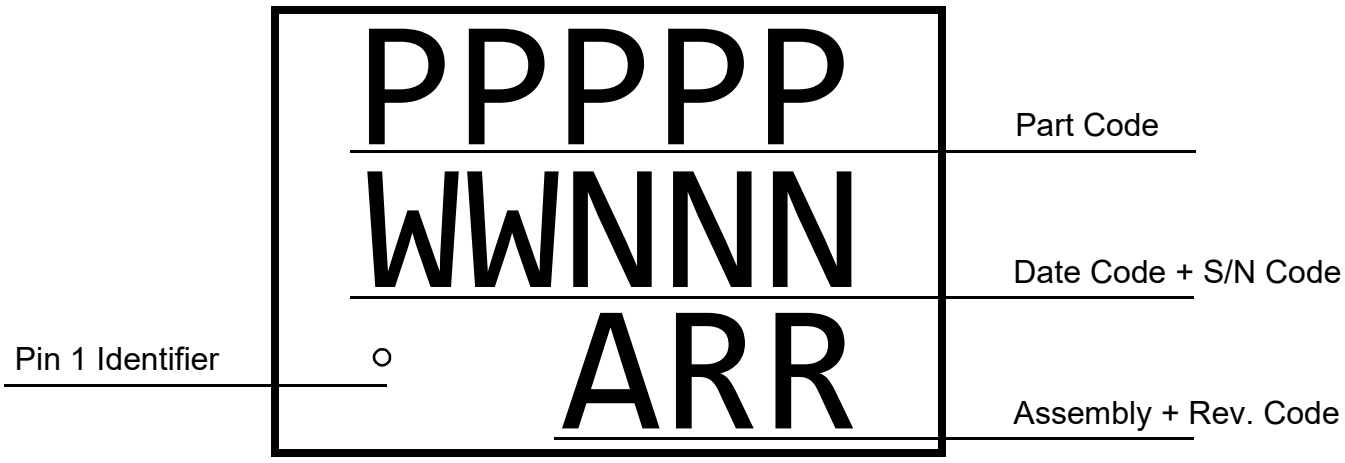
Register Bit Address	Signal Function	Register Bit Definition
reg<1915:1914>	PIN 12 Pull-Up/Down Resistor Selection	00: Floating 01: 10 K 10: 100 K 11: 1 M
reg<1916>	PIN 12 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
reg<1917>	PIN 12 Output Driver Current double	0: 1x drive 1: 2x drive
reg<1918>	PIN 12 4x Drive Enable	0: Disable 1: Enable
PIN 13		
reg<1920:1919>	PIN 13 Input Mode Control	00: Digital Input without schmitt trigger 01: Digital Input with schmitt trigger 10: Low Voltage Digital Input 11: Analog I/O
reg<1922:1921>	PIN 13 Output Mode Control	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-Drain 11: 2x Open-Drain
reg<1924:1923>	PIN 13 Pull-Up/Down Resistor Selection	00: Floating 01: 10 K 10: 100 K 11: 1 M
reg<1925>	PIN 13 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
Reserved		
reg<1927:1926>	Reserved	
reg<1929:1928>	Reserved	
reg<1931:1930>	Reserved	
reg<1932>	Reserved	
PIN 15		
reg<1935:1933>	PIN 15 Mode Control	000: Digital in without schmitt trigger 001: Digital in with schmitt trigger 010: Low Voltage Digital In 011: Analog IO 100: Push-Pull 101: NMOS Open-Drain 110: PMOS Open-Drain 111: Analog IO & NMOS Open-Drain
reg<1937:1936>	PIN 15 Pull-Up/Down Resistor Selection	00: Floating 01: 10 K 10: 100 K 11: 1 M
reg<1938>	PIN 15 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
reg<1939>	PIN 15 Output Driver Current double	0: 1x drive 1: 2x drive
PIN 16		
reg<1941:1940>	PIN 16 Input Mode Control	00: Digital Input without schmitt trigger 01: Digital Input with schmitt trigger 10: Low Voltage Digital Input 11: Analog I/O

Register Bit Address	Signal Function	Register Bit Definition
reg<1943:1942>	PIN 16 Output Mode Control	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-Drain 11: 2x Open-Drain
reg<1945:1944>	PIN 16 Pull-Up/Down Resistor Selection	00: Floating 01: 10 K 10: 100 K 11: 1 M
reg<1946>	PIN 16 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
PIN 17		
reg<1949:1947>	PIN 17 Mode Control	000: Digital in without schmitt trigger 001: Digital in with schmitt trigger 010: Low Voltage Digital In 011: Analog IO 100: Push-Pull 101: NMOS Open-Drain 110: PMOS Open-Drain 111: Analog IO & NMOS Open-Drain
reg<1951:1950>	PIN 17 Pull-Up/Down Resistor Selection	00: Floating 01: 10 K 10: 100 K 11: 1 M
reg<1952>	PIN 17 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
reg<1953>	PIN 17 Output Driver Current double	0: 1x drive 1: 2x drive
PIN 18		
reg<1955:1954>	PIN 18 Input Mode Control	00: Digital Input without schmitt trigger 01: Digital Input with schmitt trigger 10: Low Voltage Digital Input 11: Analog I/O
reg<1957:1956>	PIN 18 Output Mode Control	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-Drain 11: 2x Open-Drain
reg<1959:1958>	PIN 18 Pull-Up/Down Resistor Selection	00: Floating 01: 10 K 10: 100 K 11: 1 M
reg<1960>	PIN 18 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
PIN 19		
reg<1962:1961>	PIN 19 Input Mode Control	00: Digital Input without schmitt trigger 01: Digital Input with schmitt trigger 10: Low Voltage Digital Input 11: Analog I/O
reg<1964:1963>	PIN 10 Output Mode Control	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-Drain 11: 2x Open-Drain

Register Bit Address	Signal Function	Register Bit Definition
reg<1966:1965>	PIN 19 Pull-Up/Down Resistor Selection	00: Floating 01: 10 K 10: 100 K 11: 1 M
reg<1967>	PIN 19 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
PIN 20		
reg<1970:1968>	PIN 20 Mode Control	000: Digital in without schmitt trigger 001: Digital in with schmitt trigger 010: Low Voltage Digital In 011: Analog IO 100: Push-Pull 101: NMOS Open-Drain 110: PMOS Open-Drain 111: Analog IO & NMOS Open-Drain
reg<1972:1971>	PIN 20 Pull-Up/Down Resistor Selection	00: Floating 01: 10 K 10: 100 K 11: 1 M
reg<1973>	PIN 20 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
reg<1974>	PIN 20 Output Driver Current double	0: 1x drive 1: 2x drive
Reserved		
reg<1981:1975>	Reserved	
reg<1987:1982>	Reserved	
reg<1995:1988>	Reserved	
reg<2001:1996>	Reserved	
reg<2007:2002>	Reserved	
reg<2008>	Bypass Vdd to 1.8 V Device Only When Power is 1.8 V	0: 1.8 V Use Regulator 1: Bypass Vdd as 1.8 V Device Power
reg<2009>	Input pad Enable to Core Resetb Delay 500us Enable	0: Delay 4 us 1: Delay 500 us
reg<2010>	Power Auto Detector Function for Charge Pump	0: Enable 1: Disable
reg<2012:2011>	Reserved	
reg<2014:2013>	Reserved	
SPI top Control		
reg<2015>	SPI Parallel Output Selection for Matrix 1 (in<44> --> in<51>)	0: Matrix 1 Input From DCMP 1: Matrix 1 Input From SPI Parallel Output <7: 0>
reg<2017:2016>	SPI SDIO Output Control	0X: PIN 10 dout From Matrix 0 (out67) 10: From SPI (SDO) 11: From ADC serial Output
PIN 2 Reset Control		
reg<2018>	Bypass the PIN 2	0: PIN 2 Edge Active 1: PIN 2 High Active
reg<2019>	PIN2 Edge Detect Mode	0: Delay 4 us 1: Delay 500 us
reg<2020>	PIN2 Reset Enable	0: Enable 1: Disable

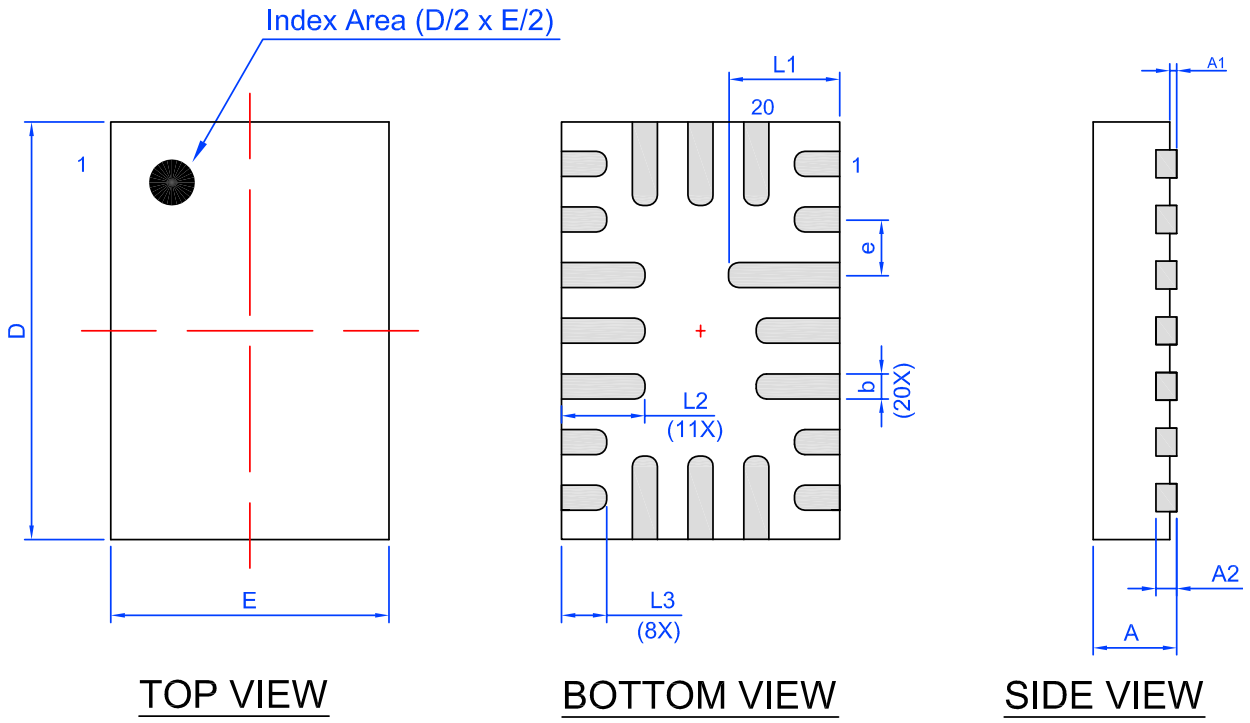
Register Bit Address	Signal Function	Register Bit Definition
reg<2027:2021>	Reserved	Reserved
NVM		
reg<2029:2028>	Reserved	
reg<2030>	Reserved	
reg<2038:2031>	Pattern ID	data Note: assigned to track code revision
reg<2039>	Read Protection	0: Protection Disable 1: Protection Enable
reg<2047:2040>	Die ID: Power up Sequence Bits	data Hex: A5

26.0 Package Top Marking System Definition



27.0 Package Drawing and Dimensions

STQFN 20L 2x3mm 0.4P COL Package
JEDEC MO-220, Variation WECE
IC Net Weight: 0.015 g



Unit: mm

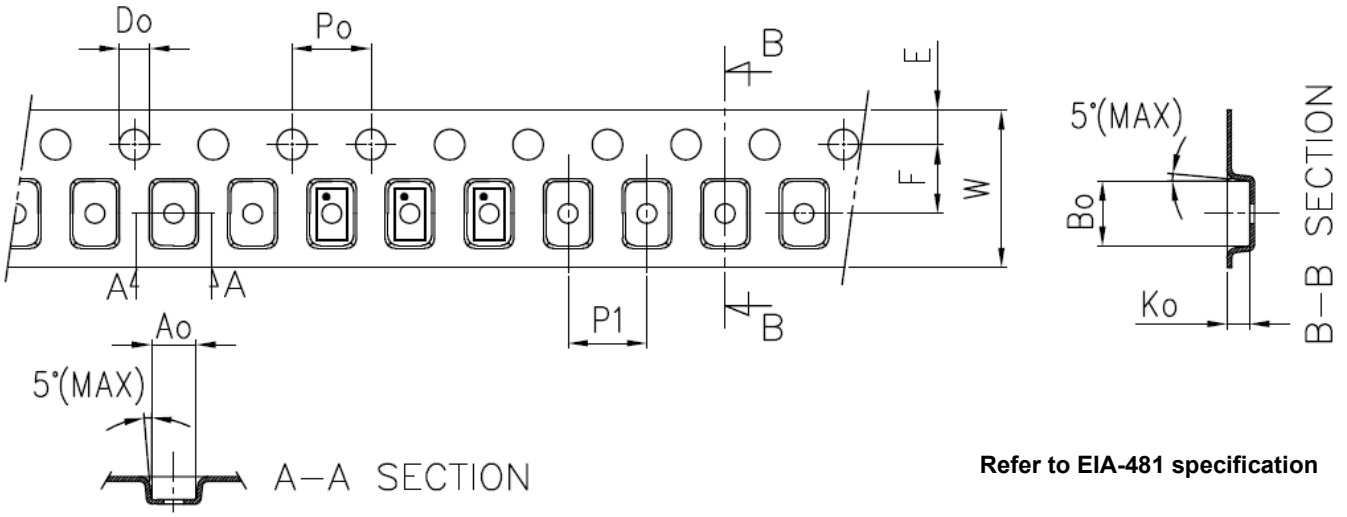
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L1	0.75	0.80	0.85
b	0.13	0.18	0.23	L2	0.55	0.60	0.65
e	0.40 BSC			L3	0.275	0.325	0.375

28.0 Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 20L 2x3 mm 0.4P COL	20	2 x 3 x 0.55	3,000	3,000	178 / 60	100	400	100	400	8	4

28.1 Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2x3 mm 0.4P COL	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8



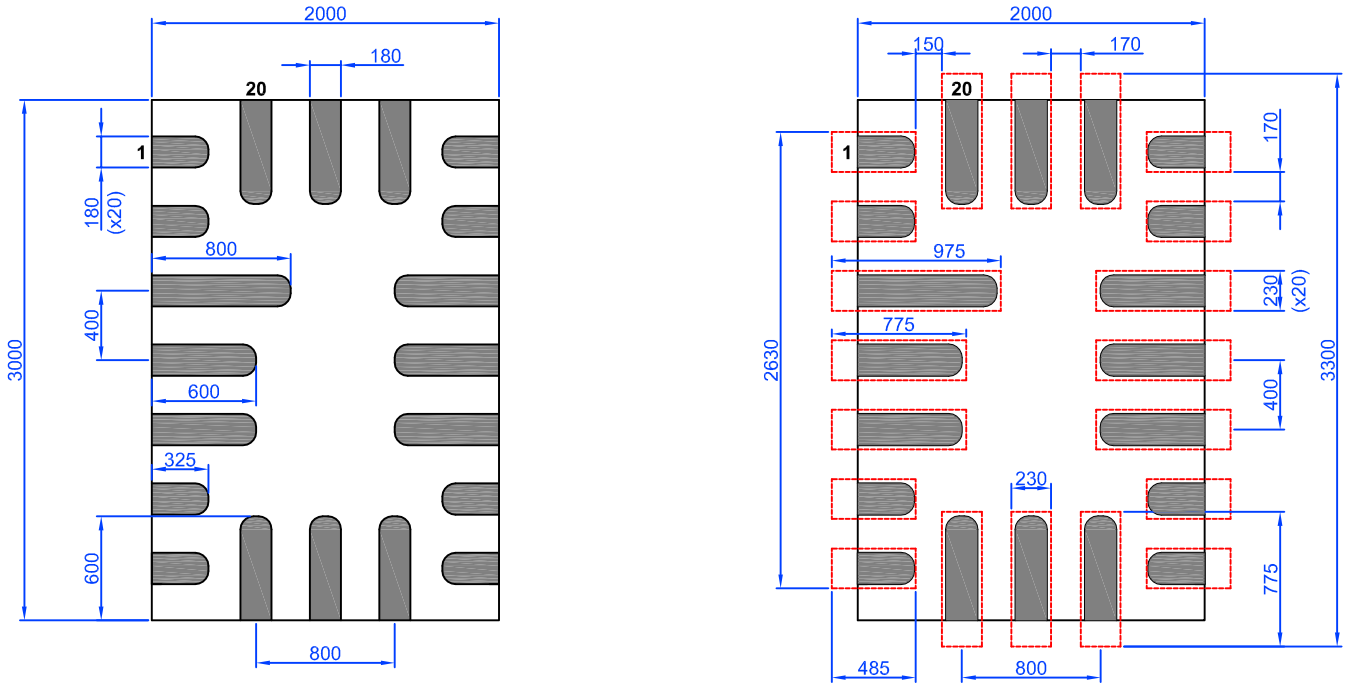
Refer to EIA-481 specification

29.0 Recommended Land Pattern

Exposed Pad
(Top View)

Recommended Land Pattern
(Top View)

Units: µm



30.0 Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.30 mm^3 (nominal). More information can be found at www.jedec.org.

31.0 Revision History

Date	Version	Change
3/6/2023	1.39	Added notes to section Ordering Information
2/16/2023	1.38	Updated ACMP0 Block Diagram
3/4/2022	1.37	Updated R_{PUP} and R_{PDWN} in section Electrical Characteristics Renesas rebranding Corrected 4-bit LUTs names Updated PIN Block Diagrams
10/28/2019	1.36	Updated disclaimer Updated Digital Comparator/Pulse Width Modulator section Fixed typos Corrected Programmable Delay / Edge Detector description and timing diagrams Corrected Oscillator Block Diagram
7/1/2019	1.35	Updated Digital Comparator description Fixed typos Updated External Reset subsection Corrected reg<1773:1772>
4/9/2019	1.34	Corrected INV_0 Gate and INV_1 Gate Figures Updated Slave SPI section Added new section Power Detector Fixed typos Corrected 4-bit LUT1 or PGEN figure Added additional information about V_{DD2} to IO Pins section
11/13/2018	1.33	Updated to Dialog style
9/7/2018	1.32	Updated Oscillator Startup Diagram Updated reg<2012:2011> Updated ADC Interrupt Output Timing Diagram
3/16/2018	1.31	Updated subsection Absolute Maximum Conditions
1/11/2018	1.30	Updated subsections ADC Outputs and ADC Interrupt Output Timing Diagram Added PGA input voltage limitation
11/22/2017	1.29	Fixed typos
10/11/2017	1.28	Updated Electrical Spec Fixed typos
10/2/2017	1.27	Updated ADC Typical Current Consumption
5/31/2017	1.26	Fixed typos Updated POR section Updated PGA Specification Conditions Updated figure PWM Dead Band Control Timing Diagram Updated Absolute Maximum Conditions and Electrical Characteristics
2/24/2017	1.25	Updated OSC Power On delay
2/17/2017	1.24	Fixed typos
1/18/2017	1.23	Updated Silego Website & Support Fixed typos Updated Section Programmable Delay / Edge Detector8
10/20/2016	1.22	Removed references to GPAK families
10/19/2016	1.21	Fixed typos
10/13/2016	1.20	Added VDD ramp rising speed Fixed typos Added subsection PGA Typical Performance Added subsection PGA Output Added table Differential or Pseudo-Differential PGA operation, ADC - Power Down
8/19/2016	1.19	Updated Input Leakage in Electrical Spec

Date	Version	Change
8/11/2016	1.18	Updated OSC Specifications for 2 MHz and 25 kHz Corrected ADC and DAC sections Added subsection ADC electrical spec Updated ADC section
6/10/2016	1.17	Corrected ACMP information Changed Superdrive to 4X Drive Updated VREF section Corrected PGA Gain Updated ADC section
4/14/2016	1.16	Updated ACMP Block Diagram Removed ACMP Speed option
4/11/2016	1.15	Updated Pipe Delay description Updated Matrix 1 Input table
4/8/2016	1.14	Updated ADC Bandgap
4/5/2016	1.13	Fixed typos Updated DAC section
4/4/2016	1.12	Updated table ACMP Electrical Spec Updated Section 13
3/25/2016	1.11	Updated VREF Range Added Table ACMP Electrical Spec Updated Input Leakage Updated Section 8-bit SAR ADC Analog-to-Digital Converter (ADC)
2/1/2016	1.10	Updated Silego Website & Support Updated Power On Reset
12/25/2015	1.09	Updated table Delayed Edge Detector Output
12/24/2015	1.08	Updated figure ADC Interrupt Output Timing Diagram
12/8/2015	1.07	Updated front page
11/19/2015	1.06	Added VDD2 information to POR section Updated pin description Updated Absolute maximum conditions
10/29/2015	1.05	Updated Input Leakage
10/27/2015	1.04	Added Input Leakage Added External Reset Subsection Added ACMP, Osc Power On delay
10/21/2015	1.03	Updated Absolute maximum conditions
10/20/2015	1.02	Added info to Osc Section
9/29/2015	1.01	Added Section DAC Added New Information, Tables, Figures, Charts to ACMP Section Corrections in ADC section
9/9/2015	1.00	Production Release

RoHS Compliance

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