GreenPAK Programmable Mixed Signal Matrix with Asynchronous State Machine and Dual Supply

General Description

The GPAK product family is based around Dialog Semiconductor's proprietary Zero Static Power ASM (Asynchronous State Machine). This machine is fault tolerant and operates continuously over a wide voltage range with very low latency. The SLG46880/81 provides a small, low power component for commonly used mixed-signal functions. The user creates their circuit design by programming the one time Non-Volatile Memory (NVM) to configure the interconnect logic, the IO Pins and the macrocells of the SLG46880/81. This highly versatile device allows a wide variety of mixed-signal functions to be designed within a very small, low power single integrated circuit.

Key Features

- Two High Speed General Purpose Rail-to-Rail Analog Comparators (ACMPxH)
- Two Low Power General Purpose Rail-to-Rail Analog Comparators (ACMPxL)
- Two Voltage References
  - Two Vref Outputs
- Twelve Combination Function Macrocells
  - One Selectable DFF/Latch or 2-bit LUT
  - Four Selectable DFF/Latches or 3-bit LUTs
  - One Selectable Pipe Delay or Ripple Counter or 3-bit LUT
  - One Selectable Programmable Pattern Generator or 2-bit LUT
  - Four Selectable 8-bit CNT/DLYs or 3-bit LUTs
  - One Selectable 16-bit CNT/DLY or 4-bit LUT
- Asynchronous State Machine
  - Twelve States
  - Four Dynamic Memory Macrocells
  - f(1) Computation Macrocell with dedicated ACMP
- Serial Communications
  - I^2C Protocol Interface
- Programmable Delay with Edge Detector Output
- Deglitch Filter or Edge Detector
- Three Oscillators
  - 2.048 kHz Oscillator
  - 2.048 MHz Oscillator
  - 25 MHz Oscillator
- Crystal Oscillator
- Analog Temperature Sensor
- Power-On Reset
- Wide Range Power Supply
  - 2.5 V (±8%) to 5 V (±10%) V_{DD}
  - 2.5 V (±8%) to 5 V (±10%) V_{DD2} ($V_{DD2} \leq V_{DD}$) for SLG46880
  - 1 V (±5%) to 1.8 V (±10%) V_{DD2} for SLG46881
- Operating Temperature Range: -40°C to 85°C
- RoHS Compliant/Halogen-Free
- 32-pin STQFN: 4 mm x 4 mm x 0.55 mm, 0.4 mm pitch

Applications

- Personal Computers and Servers
- PC Peripherals
- Consumer Electronics
- Data Communications Equipment
- Handheld and Portable Electronics
- Smartphones and Fitness Bands
- Notebook and Tablet PCs

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1 Block Diagram

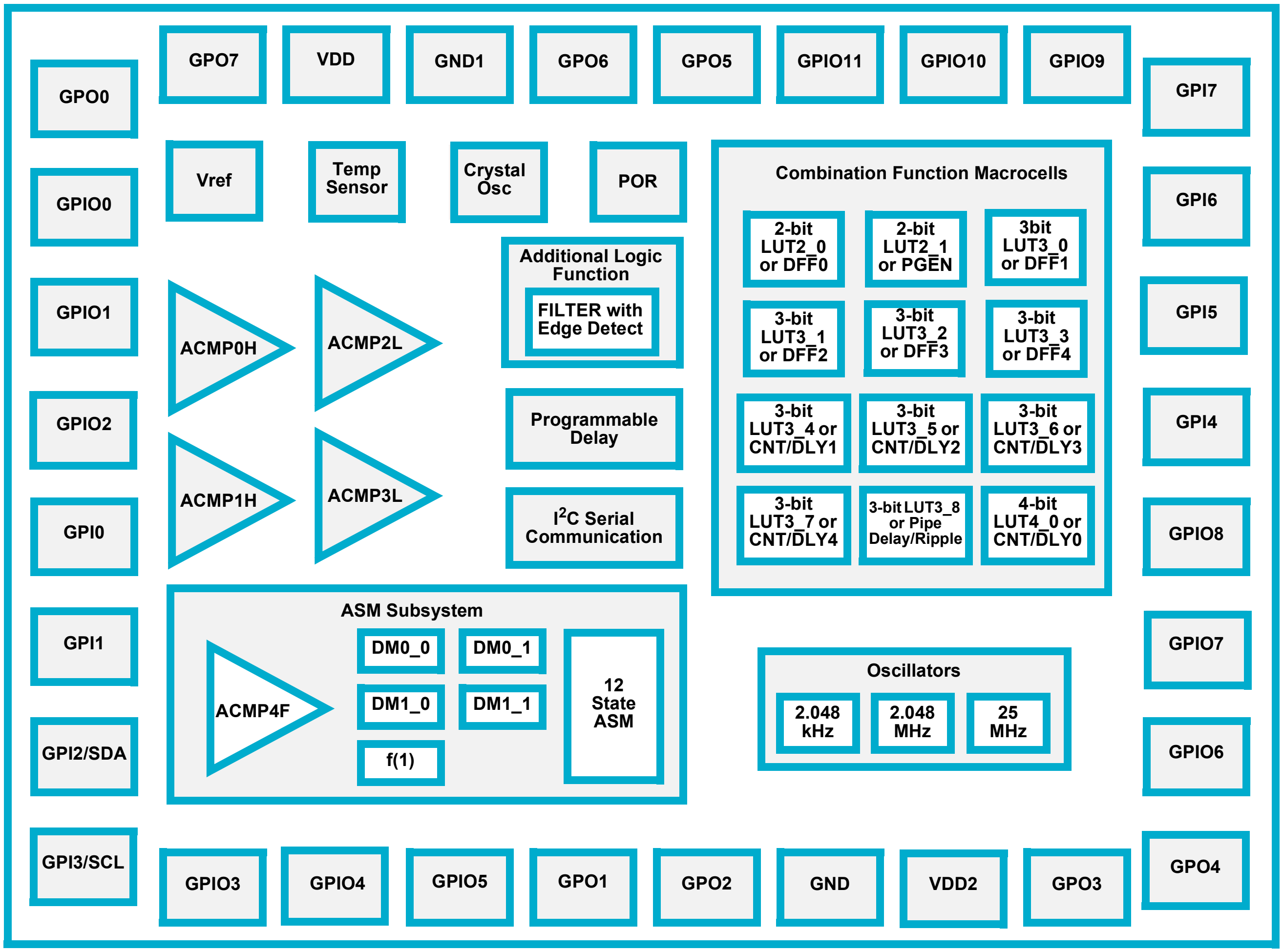
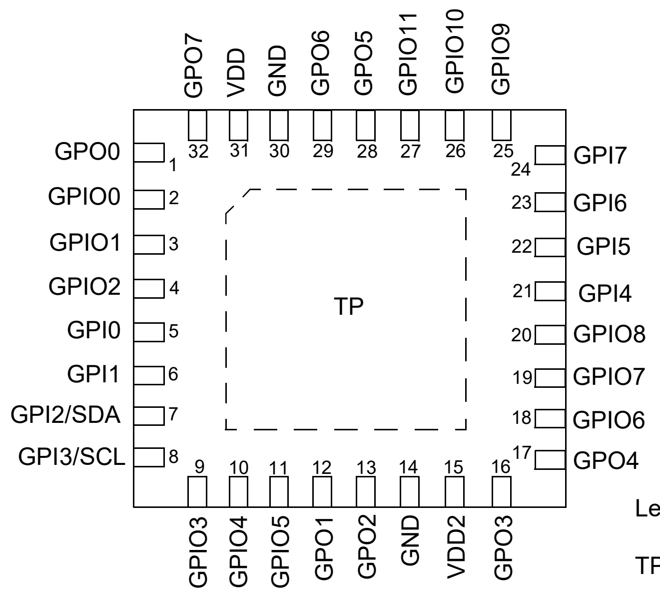


Figure 1: Block Diagram

2 Pinout

2.1 PIN CONFIGURATION - STQFN- 32L



STQFN-32
(Top View)

Legend:

TP- Thermal Pad

GPI - General Purpose Input

GPO - General Purpose Output

GPIO - General Purpose Input/ Output

Table 1: Functional Pin Description

STQFN Pin #	Pin Name	Function
1	GPO0	General Purpose Output or ACMP4F Input 1 or ASM1 output
2	GPIO0	General Purpose IO or ACMP4F Input 2
3	GPIO1	General Purpose IO or ACMP4F Input 3
4	GPIO2	General Purpose IO or VrefO1 or Din LATCH (en1)
5	GPI0	General Purpose Input or Din LATCH (en0)/ext_CLK0
6	GPI1	General Purpose Input or Din LATCH (en0)/ext_CLK1/Vref IN
7	GPI2/SDA	General Purpose Input/I^2C SDA
8	GPI3/SCL	General Purpose Input/I^2C SCL
9	GPIO3	General Purpose IO or Din LATCH (en1)
10	GPIO4	General Purpose IO or I^2C exp0 output
11	GPIO5	General Purpose IO or I^2C exp1 output
12	GPO1	General Purpose Output or ASM2 output
13	GPO2	General Purpose Output or ASM3 output
14	GND	Ground
15	V_{DD2}	Power Supply
16	GPO3	General Purpose Output or ASM4 output

Table 1: Functional Pin Description(Continued)

STQFN Pin #	Pin Name	Function
17	GPO4	General Purpose Output or ASM5 output
18	GPIO6	General Purpose IO or Din LATCH (en1) or I^2C exp2 output
19	GPIO7	General Purpose IO or Din LATCH (en1) or I^2C exp3 output
20	GPIO8	General Purpose IO or ACMP4F Input 7
21	GPI4	General Purpose Input (XTAL IN) or Din LATCH (en0)/ext_CLK2
22	GPI5	General Purpose Input (XTAL OUT) or Din LATCH (en0)/ext_CLK3
23	GPI6	General Purpose Input or ACMP4F Input 4
24	GPI7	General Purpose Input or ACMP4F Input 5
25	GPIO9	General Purpose IO or ACMP4F Input 6 or VrefO0
26	GPIO10	General Purpose IO or ACMP0H
27	GPIO11	General Purpose IO or ACMP1H
28	GPO5	General Purpose Output or ACMP2L or ASM6 output
29	GPO6	General Purpose Output or ACMP3L or ASM7 output
30	GND	Ground
31	V_{DD}	Power Supply
32	GPO7	General Purpose Output or ACMP4F Input 0 or ASM0 output
TP	TP	Thermal Pad. Must be connected to GND externally

3 Characteristics

3.1 ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 2: Absolute Maximum Ratings

Parameter	Min	Max	Unit
V_{HIGH} to GND	-0.3	7	V
Voltage at Input Pin	-0.3	7	V
Current at Input Pin	-1.0	1.0	mA
Input leakage Current (Absolute Value)	--	1000	nA
Maximum Average or DC Current (Through V_{DD} or GND pin)	--	90	mA
Storage Temperature Range	-65	150	°C
Junction Temperature	--	150	°C
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1300	--	V
Moisture Sensitivity Level	1		

3.2 RECOMMENDED OPERATING CONDITIONS

Table 3: Recommended Operating Conditions for SLG46880/81

Parameter	Condition	Min	Max	Unit
Supply Voltage (V_{DD})		2.3	5.5	V
Supply Voltage 2 (V_{DD2})	$V_{DD2} \leq V_{DD}$ for SLG46880	2.3	5.5	V
Supply Voltage 2 (V_{DD2})	$V_{DD2} \leq V_{DD}$ for SLG46881	0.95	1.98	V
Operating Temperature		-40	85	°C
Maximal Voltage Applied to any PIN in High Impedance State		--	V_{DD}+ 0.3 (Note 1)	V
Capacitor Value at V_{DD}		0.1	--	µF
Analog Input Common Mode Range	Allowable Input Voltage at Analog Pins	0	V_{DD}	V

Note 1 GPIs 0, 1, 2, 3, 4, 5, 6, 7, GPIOs 0, 1, 2, 3, 8, 9, 10, 11, GPOs 0, 5, 6, 7 are powered from V_{DD} and GPIOs 4, 5, 6, 7, GPOs 1, 2, 3, 4 are powered from V_{DD2}.

3.3 ELECTRICAL CHARACTERISTICS

Table 4: EC for SLG46880 at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{IH}	HIGH-Level Input Voltage	Logic Input **(Note 2)**	0.7x V_{DD} (Note 1)	--	V_{DD}+ 0.3 (Note 1)	V
		Logic Input with Schmitt Trigger	0.8x V_{DD} (Note 1)	--	V_{DD}+ 0.3 (Note 1)	V
		Low-Level Logic Input **(Note 2)**	1.25	--	V_{DD}+ 0.3 (Note 1)	V

Table 4: EC for SLG46880 at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{IL}	LOW-Level Input Voltage	Logic Input **(Note 2)**	GND-0.3	--	0.3x V_{DD} **(Note 1)**	V
		Logic Input with Schmitt Trigger	GND-0.3	--	0.2x V_{DD} **(Note 1)**	V
		Low-Level Logic Input **(Note 2)**	GND-0.3	--	0.5	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	V_{DD} = 2.5 V +/- 8 %	0.32	0.43	0.56	V
		V_{DD} = 3.3 V +/- 10 %	0.36	0.46	0.57	V
		V_{DD} = 5 V +/- 10 %	0.46	0.58	0.74	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull, I_{OH} = 100 µA, 1X Drive, V_{DD} = 2.5 V +/- 8%	2.286	2.292	--	V
		Push-Pull, I_{OH} = 3 mA, 1X Drive, V_{DD} = 3.3 V +/- 10%	2.704	2.790	--	V
		Push-Pull, I_{OH} = 5 mA, 1X Drive, V_{DD} = 5 V +/- 10%	4.154	4.247	--	V
		Push-Pull, I_{OH} = 100 µA, 2X Drive, V_{DD} = 2.5 V +/- 8%	2.294	2.297	--	V
		Push-Pull, I_{OH} = 3 mA, 2X Drive, V_{DD} = 3.3 V +/- 10%	2.857	2.896	--	V
		Push-Pull, I_{OH} = 5 mA, 2X Drive, V_{DD} = 5 V +/- 10%	4.329	4.373	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull, I_{OL}= 100 µA, 1X Drive, V_{DD} = 2.5 V +/- 8%	--	0.006	0.025	V
		Push-Pull, I_{OL} = 3 mA,1X Drive, V_{DD} = 3.3 V +/- 10%	--	0.158	0.217	V
		Push-Pull, I_{OL}= 5 mA, 1X Drive, V_{DD} = 5 V +/- 10%	--	0.212	0.297	V
		Push-Pull, I_{OL} = 100 µA, 2X Drive, V_{DD} = 2.5 V +/- 8%	--	0.003	0.013	V
		Push-Pull, I_{OL}= 3 mA, 2X Drive, V_{DD} = 3.3 V +/- 10%	--	0.079	0.107	V
		Push-Pull, I_{OL} = 5 mA, 2X Drive, V_{DD} = 5 V +/- 10%	--	0.099	0.136	V
		NMOS OD, I_{OL} = 100 µA, 1X Drive, V_{DD} = 2.5 V +/- 8%	--	0.003	0.011	V
		NMOS OD, I_{OL} = 3 mA, 1X Drive, V_{DD} = 3.3 V +/- 10%	--	0.063	0.087	V
		NMOS OD, I_{OL} = 5 mA, 1X Drive, V_{DD} = 5 V +/- 10%	--	0.079	0.114	V
		NMOS OD, I_{OL} = 100 µA, 2X Drive, V_{DD} = 2.5 V +/- 8%	--	0.001	0.002	V
		NMOS OD, I_{OL} = 3 mA, 2X Drive, V_{DD} = 3.3 V +/- 10%	--	0.033	0.046	V
		NMOS OD, I_{OL} = 5 mA, 2X Drive, V_{DD} = 5 V +/- 10%	--	0.041	0.061	V

Table 4: EC for SLG46880 at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{OH}	HIGH-Level Output Current	Push-Pull, V_{OH} = V_{DD} - 0.2, 1X Drive, V_{DD} = 2.5 V +/- 8%	1.55	2.14	--	mA
		Push-Pull, V_{OH} = 2.4 V, 1X Drive, V_{DD} = 3.3 V +/- 10%	5.54	7.48	--	mA
		Push-Pull, V_{OH} = 2.4 V, 1X Drive, V_{DD} = 5 V +/- 10%	19.89	24.83	--	mA
		Push-Pull, V_{OH} = V_{DD} - 0.2, 2X Drive, V_{DD} = 2.5 V +/- 8%	3.08	4.21	--	mA
		Push-Pull, V_{OH} = 2.4 V, 2X Drive, V_{DD} = 3.3 V +/- 10%	10.92	14.72	--	mA
		Push-Pull, V_{OH} = 2.4 V, 2X Drive, V_{DD} = 5 V +/- 10%	38.89	48.60	--	mA
I_{OL}	LOW-Level Output Current	Push-Pull, V_{OL} = 0.15 V, 1X Drive, V_{DD} = 2.5 V +/- 8%	1.66	2.19	--	mA
		Push-Pull, V_{OL} = 0.4 V, 1X Drive, V_{DD} = 3.3 V +/- 10%	5.26	7.00	--	mA
		Push-Pull, V_{OL} = 0.4 V, 1X Drive, V_{DD} = 5 V +/- 10%	7.15	9.76	--	mA
		Push-Pull, V_{OL} = 0.15 V, 2X Drive, V_{DD} = 2.5 V +/- 8%	3.32	4.29	--	mA
		Push-Pull, V_{OL} = 0.4 V, 2X Drive, V_{DD} = 3.3 V +/- 10%	10.40	13.69	--	mA
		Push-Pull, V_{OL} = 0.4 V, 2X Drive, V_{DD} = 5 V +/- 10%	14.06	18.98	--	mA
		NMOS OD, V_{OL} = 0.15 V, 1X Drive, V_{DD} = 2.5 V +/- 8%	4.15	5.38	--	mA
		NMOS OD, V_{OL} = 0.4 V, 1X Drive, V_{DD} = 3.3 V +/- 10%	12.90	17.14	--	mA
		NMOS OD, V_{OL} = 0.4 V, 1X Drive, V_{DD} = 5 V +/- 10%	16.98	23.70	--	mA
		NMOS OD, V_{OL} = 0.15 V, 2X Drive, V_{DD} = 2.5 V +/- 8%	7.89	10.40	--	mA
		NMOS OD, V_{OL} = 0.4 V, 2X Drive, V_{DD} = 3.3 V +/- 10%	24.47	33.02	--	mA
		NMOS OD, V_{OL} = 0.4 V, 2X Drive, V_{DD} = 5 V +/- 10%	31.20	45.10	--	mA
T_{SU}	Startup Time	From V_{DD} rising past PON_{THR}	--	1.13	1.72	ms
T_{WR}	NVM Page Write Time		--	--	20	ms
T_{ER}	NVM Page Erase Time		--	--	20	ms
PON_{THR}	Power-On Threshold	V_{DD} Level Required to Start Up the Chip	1.64	1.84	2.11	V
$POFF_{THR}$	Power-Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.98	1.25	1.49	V
R_{PULL}	Pull Up or Pull Down Resistance	1 M for Pull Up: V_{IN} = GND; for Pull Down: V_{IN} = V_{DD}	0.74	1.04	1.50	MΩ
		100 k for Pull Up: V_{IN} = GND; for Pull Down: V_{IN} = V_{DD}	87	104	132	kΩ
		10 k For Pull Up: V_{IN} = GND; for Pull Down: V_{IN} = V_{DD}	7	10	17	kΩ
C_{IN}	Input Capacitance			4		pF

Table 4: EC for SLG46880 at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
Note 1 GPIs 0, 1, 2, 3, 4, 5, 6, 7, GPIOs 0, 1, 2, 3, 8, 9, 10, 11, GPOs 0, 5, 6, 7 are powered from V_{DD} and GPIOs 4, 5, 6, 7, GPOs 1, 2, 3, 4 are powered from V_{DD2}. **Note 2** No hysteresis.						

Table 5: EC for SLG46881 at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{IH1}	HIGH-Level Input Voltage (GPIs 0, 1, 2, 3, 4, 5, 6, 7, GPIOs 0, 1, 2, 3, 8, 9, 10, 11)	Logic Input **(Note 2)**	0.7x V_{DD}	--	V_{DD}+ 0.3	V
		Logic Input with Schmitt Trigger	0.8x V_{DD}	--	V_{DD}+ 0.3	V
		Low-Level Logic Input **(Note 2)**	1.25	--	V_{DD}+ 0.3	V
		Ultra-Low Power Digital Input **(Note 2)**	0.54	--	V_{DD2}+ 0.3	
V_{IH2}	HIGH-Level Input Voltage (GPIOs 4, 5, 6, 7)	Ultra-Low Power Digital Input **(Note 2)**	0.54	--	V_{DD2}+ 0.3	V
V_{IL1}	LOW-Level Input Voltage (GPIs 0, 1, 2, 3, 4, 5, 6, 7, GPIOs 0, 1, 2, 3, 8, 9, 10, 11)	Logic Input **(Note 2)**	GND- 0.3	--	0.3x V_{DD}	V
		Logic Input with Schmitt Trigger	GND- 0.3	--	0.2x V_{DD}	V
		Low-Level Logic Input **(Note 2)**				
		Ultra-Low Power Digital Input **(Note 2)**	GND- 0.3	--	0.5	V
V_{IL2}	LOW-Level Input Voltage (GPIOs 4, 5, 6, 7)	Ultra-Low Power Digital Input **(Note 2)**	GND- 0.3	--	0.5	V
V_{HYS1}	Schmitt Trigger Hysteresis Voltage (GPIs 0, 1, 2, 3, 4, 5, 6, 7, GPIOs 0, 1, 2, 3, 8, 9, 10, 11)	V_{DD} = 2.5 V +/- 8%	0.27	0.43	0.59	V
		V_{DD} = 3.3 V +/- 10%	0.32	0.46	0.59	V
		V_{DD} = 5 V +/- 10%	0.42	0.58	0.76	V
V_{OH1}	HIGH-Level Output Voltage (GPIOs 0, 1, 2, 3, 8, 9, 10, 11, GPOs 0, 5, 6, 7)	Push-Pull, I_{OH} = 100 µA, 1X Drive, V_{DD} = 2.5 V +/- 8%	2.29	2.49	--	V
		Push-Pull, I_{OH} = 3 mA, 1X Drive, V_{DD} = 3.3 V +/- 10%	2.69	3.11	--	V
		Push-Pull, I_{OH} = 5 mA, 1X Drive, V_{DD} = 5 V +/- 10%	4.14	4.77	--	V
		Push-Pull, I_{OH} = 100 µA, 2X Drive, V_{DD} = 2.5 V +/- 8%	2.29	2.50	--	V
		Push-Pull, I_{OH} = 3 mA, 2X Drive, V_{DD} = 3.3 V +/- 10%	2.85	3.21	--	V
		Push-Pull, I_{OH} = 5 mA, 2X Drive, V_{DD} = 5 V +/- 10%	4.32	4.88	--	V

Table 5: EC for SLG46881 at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{OH2}	HIGH-Level Output Voltage (GPIOs 4, 5, 6, 7, GPOs 1, 2, 3, 4)	Push-Pull, I_{OH} = 100 µA, 1X Drive, V_{DD2} = 1.0 V +/- 5%	0.923	0.957	--	V
		Push-Pull, I_{OH} = 100 µA, 1X Drive, V_{DD2} = 1.5 V +/- 5%	1.479	1.486	--	V
		Push-Pull, I_{OH} = 100 µA, 1X Drive, V_{DD2} = 1.8 V +/- 10%	1.780	1.886	--	V
		Push-Pull, I_{OH} = 100 µA, 2X Drive, V_{DD2} = 1.0 V +/- 5%	0.937	0.966	--	V
		Push-Pull, I_{OH} = 100 µA, 2X Drive, V_{DD2} = 1.5 V +/- 5%	1.489	1.493	--	V
		Push-Pull, I_{OH} = 100 µA, 2X Drive, V_{DD2} = 1.8 V +/- 10%	1.789	1.893	--	V
V_{OL1}	LOW-Level Output Voltage (GPIOs 0, 1, 2, 3, 8, 9, 10, 11, GPOs 0, 5, 6, 7)	Push-Pull, I_{OL}= 100 µA, 1X Drive, V_{DD} = 2.5 V +/- 8%	--	0.006	0.012	V
		Push-Pull, I_{OL} = 3 mA,1X Drive, V_{DD} = 3.3 V +/- 10%	--	0.156	0.233	V
		Push-Pull, I_{OL}= 5 mA, 1X Drive, V_{DD} = 5 V +/- 10%	--	0.197	0.295	V
		Push-Pull, I_{OL} = 100 µA, 2X Drive, V_{DD} = 2.5 V +/- 8%	--	0.003	0.005	V
		Push-Pull, I_{OL}= 3 mA, 2X Drive, V_{DD} = 3.3 V +/- 10%	--	0.078	0.116	V
		Push-Pull, I_{OL} = 5 mA, 2X Drive, V_{DD} = 5 V +/- 10%	--	0.100	0.151	V
		NMOS OD, I_{OL} = 100 µA, 1X Drive, V_{DD} = 2.5 V +/- 8%	--	0.003	0.004	V
		NMOS OD, I_{OL} = 3 mA, 1X Drive, V_{DD} = 3.3 V +/- 10%	--	0.062	0.094	V
		NMOS OD, I_{OL} = 5 mA, 1X Drive, V_{DD} = 5 V +/- 10%	--	0.080	0.122	V
		NMOS OD, I_{OL} = 100 µA, 2X Drive, V_{DD} = 2.5 V +/- 8%	--	0.001	0.002	V
		NMOS OD, I_{OL} = 3 mA, 2X Drive, V_{DD} = 3.3 V +/- 10%	--	0.032	0.051	V
		NMOS OD, I_{OL} = 5 mA, 2X Drive, V_{DD} = 5 V +/- 10%	--	0.042	0.067	V

Table 5: EC for SLG46881 at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{OL2}	LOW-Level Output Voltage (GPIOs 4, 5, 6, 7, GPOs 1, 2, 3, 4)	Push-Pull, I_{OL}= 100 µA, 1X Drive, V_{DD2} = 1.0 V +/- 5%	--	0.015	0.022	V
		Push-Pull, I_{OL}= 100 µA, 1X Drive, V_{DD2} = 1.5 V +/- 5%	--	0.012	0.018	V
		Push-Pull, I_{OL}= 100 µA, 1X Drive, V_{DD2} = 1.8 V +/- 10%	--	0.011	0.017	V
		Push-Pull, I_{OL} = 100 µA, 2X Drive, V_{DD2} = 1.0 V +/- 5%	--	0.007	0.011	V
		Push-Pull, I_{OL} = 100 µA, 2X Drive, V_{DD2} = 1.5 V +/- 5%	--	0.006	0.011	V
		Push-Pull, I_{OL} = 100 µA, 2X Drive, V_{DD2} = 1.8 V +/- 10%	--	0.006	0.008	V
		NMOS OD, I_{OL} = 100 µA, 1X Drive, V_{DD2} = 1.0 V +/- 5%	--	0.015	0.022	V
		NMOS OD, I_{OL} = 100 µA, 1X Drive, V_{DD2} = 1.5 V +/- 5%	--	0.012	0.018	V
		NMOS OD, I_{OL} = 100 µA, 1X Drive, V_{DD2} = 1.8 V +/- 10%	--	0.011	0.017	V
		NMOS OD, I_{OL} = 100 µA, 2X Drive, V_{DD2} = 1.0 V +/- 5%	--	0.007	0.011	V
		NMOS OD, I_{OL} = 100 µA, 2X Drive, V_{DD2} = 1.5 V +/- 5%	--	0.006	0.010	V
		NMOS OD, I_{OL} = 100 µA, 2X Drive, V_{DD2} = 1.8 V +/- 10%	--	0.006	0.008	V
I_{OH1}	HIGH-Level Output Current (GPIOs 0, 1, 2, 3, 8, 9, 10, 11, GPOs 0, 5, 6, 7)	Push-Pull, V_{OH} = V_{DD} - 0.2, 1X Drive, V_{DD} = 2.5 V +/- 8%	1.48	2.37	--	mA
		Push-Pull, V_{OH} = 2.4 V, 1X Drive, V_{DD} = 3.3 V +/- 10%	5.30	11.12	--	mA
		Push-Pull, V_{OH} = 2.4 V, 1X Drive, V_{DD} = 5 V +/- 10%	19.27	30.24	--	mA
		Push-Pull, V_{OH} = V_{DD} - 0.2, 2X Drive, V_{DD} = 2.5 V +/- 8%	2.91	4.67	--	mA
		Push-Pull, V_{OH} = 2.4 V, 2X Drive, V_{DD} = 3.3 V +/- 10%	10.47	21.89	--	mA
		Push-Pull, V_{OH} = 2.4 V, 2X Drive, V_{DD} = 5 V +/- 10%	37.75	59.04	--	mA
I_{OH2}	HIGH-Level Output Current (GPIOs 4, 5, 6, 7, GPOs 1, 2, 3, 4)	Push-Pull, V_{OH} = 2/3 V_{DD2}, 1X Drive, V_{DD2} = 1.0 V +/- 5%	1.16	1.55	--	mA
		Push-Pull, V_{OH} = 2/3 V_{DD2}, 1X Drive, V_{DD2} = 1.5 V +/- 5%	2.84	3.40	--	mA
		Push-Pull, V_{OH} = 2/3 V_{DD2}, 1X Drive, V_{DD2} = 1.8 V +/- 10%	3.55	4.52	--	mA
		Push-Pull, V_{OH} = 2/3 V_{DD2}, 2X Drive, V_{DD2} = 1.0 V +/- 5%	2.32	3.07	--	mA
		Push-Pull, V_{OH} = 2/3 V_{DD2}, 2X Drive, V_{DD2} = 1.5 V +/- 5%	5.57	6.74	--	mA
		Push-Pull, V_{OH} = 2/3 V_{DD2}, 2X Drive, V_{DD2} = 1.8 V +/- 10%	6.99	8.95	--	mA

Table 5: EC for SLG46881 at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{OL1}	LOW-Level Output Current (GPIOs 0, 1, 2, 3, 8, 9, 10, 11, GPOs 0, 5, 6, 7)	Push-Pull, V_{OL} = 0.15 V, 1X Drive, V_{DD} = 2.5 V +/- 8%	1.58	2.26	--	mA
		Push-Pull, V_{OL} = 0.4 V, 1X Drive, V_{DD} = 3.3 V +/- 10%	4.94	7.24	--	mA
		Push-Pull, V_{OL} = 0.4 V, 1X Drive, V_{DD} = 5 V +/- 10%	6.65	9.82	--	mA
		Push-Pull, V_{OL} = 0.15 V, 2X Drive, V_{DD} = 2.5 V +/- 8%	3.07	4.43	--	mA
		Push-Pull, V_{OL} = 0.4 V, 2X Drive, V_{DD} = 3.3 V +/- 10%	9.63	14.18	--	mA
		Push-Pull, V_{OL} = 0.4 V, 2X Drive, V_{DD} = 5 V +/- 10%	12.86	19.13	--	mA
		NMOS OD, V_{OL} = 0.15 V, 1X Drive, V_{DD} = 2.5 V +/- 8%	3.83	5.55	--	mA
		NMOS OD, V_{OL} = 0.4 V, 1X Drive, V_{DD} = 3.3 V +/- 10%	11.92	17.72	--	mA
		NMOS OD, V_{OL} = 0.4 V, 1X Drive, V_{DD} = 5 V +/- 10%	15.81	23.84	--	mA
		NMOS OD, V_{OL} = 0.15 V, 2X Drive, V_{DD} = 2.5 V +/- 8%	7.18	10.72	--	mA
		NMOS OD, V_{OL} = 0.4 V, 2X Drive, V_{DD} = 3.3 V +/- 10%	22.17	34.11	--	mA
		NMOS OD, V_{OL} = 0.4 V, 2X Drive, V_{DD} = 5 V +/- 10%	28.68	45.34	--	mA
I_{OL2}	LOW-Level Output Current (GPIOs 4, 5, 6, 7, GPOs 1, 2, 3, 4)	Push-Pull, V_{OL} = 1/3 V_{DD2}, 1X Drive, V_{DD2} = 1.0 V +/- 5%	1.37	1.85	--	mA
		Push-Pull, V_{OL} = 1/3 V_{DD2}, 1X Drive, V_{DD2} = 1.5 V +/- 5%	3.26	4.00	--	mA
		Push-Pull, V_{OL} = 1/3 V_{DD2}, 1X Drive, V_{DD2} = 1.8 V +/- 10%	4.09	5.27	--	mA
		Push-Pull, V_{OL} = 1/3 V_{DD2}, 2X Drive, V_{DD2} = 1.0 V +/- 5%	2.70	3.67	--	mA
		Push-Pull, V_{OL} = 1/3 V_{DD2}, 2X Drive, V_{DD2} = 1.5 V +/- 5%	6.42	7.93	--	mA
		Push-Pull, V_{OL} = 1/3 V_{DD2}, 2X Drive, V_{DD2} = 1.8 V +/- 10%	8.08	10.44	--	mA
		NMOS OD, V_{OL} = 1/3 V_{DD2}, 1X Drive, V_{DD2} = 1.0 V +/- 5%	1.38	1.85	--	mA
		NMOS OD, V_{OL} = 1/3 V_{DD2}, 1X Drive, V_{DD2} = 1.5 V +/- 5%	3.24	4.00	--	mA
		NMOS OD, V_{OL} = 1/3 V_{DD2}, 1X Drive, V_{DD2} = 1.8 V +/- 10%	4.08	5.27	--	mA
		NMOS OD, V_{OL} = 1/3 V_{DD2}, 2X Drive, V_{DD2} = 1.0 V +/- 5%	2.70	3.67	--	mA
		NMOS OD, V_{OL} = 1/3 V_{DD2}, 2X Drive, V_{DD2} = 1.5 V +/- 5%	6.43	7.92	--	mA
		NMOS OD, V_{OL} = 1/3 V_{DD2}, 2X Drive, V_{DD2} = 1.8 V +/- 10%	8.09	10.44	--	mA
T_{SU}	Startup Time	From V_{DD} rising past PON_{THR}	--	1.13	1.72	ms
PON_{THR}	Power-On Threshold	V_{DD} Level Required to Start Up the Chip	1.64	1.84	2.11	V

Table 5: EC for SLG46881 at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.98	1.25	1.49	V
R_{PULL}	Pull Up or Pull Down Resistance	1 M for Pull Up: V_{IN} = GND; for Pull Down: V_{IN} = V_{DD}	0.85	1.048	1.32	MΩ
		100 k for Pull Up: V_{IN} = GND; for Pull Down: V_{IN} = V_{DD}	87	104.4	131	kΩ
		10 k for Pull Up: V_{IN} = GND; for Pull Down: V_{IN} = V_{DD}	7	10.36	14	kΩ
		1 M for Pull Up: V_{IN} = GND; for Pull Down: V_{IN} = V_{DD2}	0.85	1.05	1.35	MΩ
		100 k for Pull Up: V_{IN} = GND; for Pull Down: V_{IN} = V_{DD2}	88	112.5	150	kΩ
		10 k for Pull Up: V_{IN} = GND; for Pull Down: V_{IN} = V_{DD2}	9	14.14	22	kΩ
C_{IN}	Input Capacitance			4		pF

Note 1 GPIs 0, 1, 2, 3, 4, 5, 6, 7, GPIOs 0, 1, 2, 3, 8, 9, 10, 11, GPOs 0, 5, 6, 7 are powered from V_{DD} and GPIOs 4, 5, 6, 7, GPOs 1, 2, 3, 4 are powered from V_{DD2}.
Note 2 No hysteresis.

Table 6: EC of the I²C Pins at T = -40 °C to +85 °C, VDD = 2.3 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Fast-Mode		Fast-Mode Plus		Unit
			Min	Max	Min	Max	
V_{IL}	LOW-level Input Voltage		-0.5	$0.3V_{DD}$	-0.5	$0.3\ V_{DD}$	V
V_{IH}	HIGH-level Input Voltage		$0.7V_{DD}$	5.5	$0.7V_{DD}$	5.5	V
V_{HYS}	Hysteresis of Schmitt Trigger Inputs		$0.05V_{DD}$	--	$0.05V_{DD}$	--	V
V_{OL1}	LOW-Level Output Voltage 1	(open drain or open collector) at 3mA sink current V_{DD} > 2 V	0	0.4	0	0.4	V
V_{OL2}	LOW-Level Output Voltage 2	(open drain or open collector) at 2 mA sink current $V_{DD} \le 2$ V	0	$0.2V_{DD}$	0	$0.2V_{DD}$	V
I_{OL}	LOW-Level Output Current **(Note 1)**	V_{OL} = 0.4 V, V_{DD} = 2.3 V	3	--	19.28	--	mA
		V_{OL} = 0.4 V, V_{DD} = 3.0 V	3	--	20	--	mA
		V_{OL} = 0.4 V, V_{DD} = 4.5 V	3	--	20	--	mA
		V_{OL}= 0.6 V	6	--	--	--	mA
t_{of}	Output Fall Time from V_{IHmin} to V_{ILmax} **(Note 1)**		14x (V_{DD}/5.5V)	250	10x (V_{DD}/5.5V)	120	ns
t_{SP}	Pulse Width of Spikes that must be suppressed by the Input Filter		0	50	0	50	ns

Table 6: EC of the I²C Pins at T = -40 °C to +85 °C, VDD = 2.3 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Fast-Mode		Fast-Mode Plus		Unit
			Min	Max	Min	Max	
I_i	Input Current each IO Pin	$0.1V_{DD} < V_I < 0.9V_{DDmax}$	-10	+10	-10	+10	µA
C_i	Capacitance for each IO Pin		--	10	--	10	pF
Note 1 Does not meet standard I²C specifications: t_{of} = 20x(VDD/5.5V) (min); For Fast-mode Plus I_{OL} = 20 mA (min) at V_{OL} = 0.4 V. **Note 2** For Fast-mode Plus SDA pin must be configured as 2x NMOS open drain, see registers [737:736] in section 21.							

Table 7: I²C Pins Timing Characteristics at T = -40 °C to +85 °C, VDD = 2.3 V to 5.5 V Unless Otherwise Noted

Symbol	Parameter	Condition/Note	Fast-Mode		Fast-Mode Plus		Unit
			Min	Max	Min	Max	
F_{SCL}	Clock Frequency, SCL		--	400	--	1000	kHz
t_{LOW}	Clock Pulse Width Low		1300	--	500	--	ns
t_{HIGH}	Clock Pulse Width High		600	--	260	--	ns
t_I	Input Filter Spike Suppression (SCL, SDA)	V_{DD} = 2.5 V ± 8%	--	95	--	168	ns
		V_{DD} = 3.3 V ± 10%	--	95	--	157	
		V_{DD} = 5.0 V ± 10%	--	111	--	156	
t_{AA}	Clock Low to Data Out Valid		--	900	--	450	ns
t_{BUF}	Bus Free Time between Stop and Start		1300	--	500	--	ns
t_{HD_STA}	Start Hold Time		600	--	260	--	ns
t_{SU_STA}	Start Set-up Time		600	--	260	--	ns
t_{HD_DAT}	Data Hold Time		0	--	0	--	ns
t_{SU_DAT}	Data Set-up Time		100	--	50	--	ns
t_R	Inputs Rise Time		--	300	--	120	ns
t_F	Inputs Fall Time		--	300	--	120	ns
t_{SU_STD}	Stop Set-up Time		600	--	260	--	ns
t_{DH}	Data Out Hold Time		50	--	50	--	ns
Note 1 Timing diagram can be found in the Figure 112.							

Table 8: Asynchronous State Machine Specifications at T = 25°C

Parameter	Description	Condition	Min	Typ	Max	Unit
$t_{st\_out\_delay}$	Asynchronous State Machine Output Delay Time	V_{DD} = 2.5 V ± 8 %	133	--	277	ns
		V_{DD} = 3.3 V ± 10%	96		190	
		V_{DD} = 5.0 V ± 10 %	70	--	123	

Table 8: Asynchronous State Machine Specifications at T = 25°C(Continued) (Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
t_{st_out}	Asynchronous State Machine Output Transition Time	V_{DD} = 2.5 V ± 8 %	--	--	165	ns
		V_{DD} = 3.3 V ± 10%	--	--	70	
		V_{DD} = 5.0 V ± 10 %	--	--	46	
t_{st_pulse}	Asynchronous State Machine Input Pulse Acceptance Time	V_{DD} = 2.5 V ± 8 %	28	--	--	ns
		V_{DD} = 3.3 V ± 10%	19	--	--	
		V_{DD} = 5.0 V ± 10 %	12	--	--	
t_{st_comp}	Asynchronous State Machine Input Compete Time	V_{DD} = 2.5 V ± 8 %	--	--	10	ns
		V_{DD} = 3.3 V ± 10%	--	--	7	
		V_{DD} = 5.0 V ± 10 %	--	--	5	
$t_{st\_sequential\_delay}$	Asynchronous State Machine Sequential Output Delay Time	V_{DD} = 2.5 V ± 8 %	229	--	485	ns
		V_{DD} = 3.3 V ± 10%	162	--	330	
		V_{DD} = 5.0 V ± 10 %	119	--	208	
$t_{st\_dmlatch\_delay}$	Asynchronous State Machine Dynamic Memory Latch Delay	V_{DD} = 2.5 V ± 8 %	229	--	485	ns
		V_{DD} = 3.3 V ± 10%	162	--	330	
		V_{DD} = 5.0 V ± 10 %	119	--	208	

Table 9: Typical Current Estimated for Each Macrocell at T = -40 °C to +85 °C

Parameter	Description	Note	V_{DD} = 2.5 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
I	Current	Chip Quiescent (I^2C enable)	0.11	0.13	0.20	µA
		Chip Quiescent (I^2C disable)	0.10	0.12	0.20	µA
		Vref (SourceNone, SourceTempSensor)	0.39	0.43	0.53	µA
		Vref (ACMPxH or ACMPxL, 0.32 mV)	4.03	4.16	4.43	µA
		ACMP0H, 100 µA disabled, hysteresis disabled, gain 1 or 0.25, +IN - GPIO10, Vref = 32 mV	21.21	21.59	22.87	µA
		ACMP0H, 100 µA disabled, hysteresis disabled, gain 1, Buffered +IN - GPIO10, Vref = 32 mV	24.59	24.99	26.40	µA
		ACMP0,1H, 100 µA disabled, hysteresis disabled, gain 1, +IN - GPIO10, GPIO11, Vref = 32 mV	34.97	35.67	38.02	µA
		ACMP0,1H 100 µA disabled, ACMP2, 3L, hysteresis disabled, gain 1, +IN - GPIO10, GPIO11, GPO5, GPO6, Vref = 32 mV	36.32	36.96	39.37	µA
		ACMP0H, 100 µA disabled, hysteresis disabled, gain 1, +IN - V_{DD}, Vref = 32 mV	37.06	38.41	41.99	µA
		ACMP0H, 100 µA enabled, hysteresis disabled, gain 1, +IN - GPIO10, Vref = 32 mV	46.59	48.00	51.52	µA
		ACMP2L, hysteresis disabled, gain 1 or 0.25, +IN - GPO5, Vref = 32 mV	1.61	1.65	1.78	µA
		ACMP2,3L, hysteresis disabled, gain 1, +IN - GPO5, GPO6, Vref = 32 mV	1.86	1.91	2.04	µA
		OSC2 25 MHz, pre-divider = 1	111.45	150.85	244.34	µA
		OSC2 25 MHz, pre-divider = 4	42.67	54.93	84.46	µA
		OSC2 25 MHz, pre-divider = 8	30.94	38.56	57.16	µA
		OSC1 2.048 MHz, pre-divider = 1	16.20	17.52	20.42	µA
		OSC1 2.048 MHz, pre-divider = 4	13.83	14.37	15.60	µA
		OSC1 2.048 MHz, pre-divider = 8	13.42	13.83	14.78	µA
		OSC0 2.048 kHz, pre-divider = 1 or 4 or 8	0.39	0.43	0.53	µA
		1x push-pull + 4 pF @ 25 kHz	0.4	5	16	µA
		1x push-pull + 4 pF @ 2 MHz	22	47	106	µA
		Temperature Sensor, range 0.75 to 1.2, Source Matrix	4.64	4.74	4.85	µA
		Temperature Sensor, range 0.62 to 0.99, Source Matrix or Register	4.60	4.71	4.82	µA
		Temperature Sensor, range 0.62 to 0.99, Source Matrix or GPIO11	4.15	4.41	6.73	µA

3.4 TIMING CHARACTERISTICS

Table 10: Typical Delay Estimated for Each Macrocell at T = 25°C

Symbol	Parameter	Note	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V		Unit
			rising	falling	rising	falling	rising	falling	
tpd	Delay	Digital Input to PP 1X	42	45	17	19	12	13	ns
tpd	Delay	Digital Input with Schmitt Trigger to PP 1X	42	43	16	17	18	12	ns
tpd	Delay	Low Voltage Digital input to PP 1X	45	428	17	177	12	120	ns
tpd	Delay	Digital input to NMOS output	-	80	-	27	-	18	ns
tpd	Delay	Output enable from Pin, OE Hi-Z to 1	53	-	21	-	15	-	ns
tpd	Delay	Output enable from Pin, OE Hi-Z to 0	50	-	20	-	14	-	ns
tpd	Delay	LUT2bit(LATCH)	34	33	14	13	10	9	ns
tpd	Delay	LATCH(LUT2bit)	30	34	14	13	10	9	ns
tpd	Delay	LUT3bit(LATCH)	38	37	18	15	13	10	ns
tpd	Delay	LATCH+nRESET(LUT3bit)	45	42	21	17	15	12	ns
tpd	Delay	LUT4bit	28	33	14	13	10	9	ns
tpd	Delay	LUT2bt	19	26	10	10	7	7	ns
tpd	Delay	LUT3bit	28	34	14	13	10	9	ns
tpd	Delay	CNT/DLY Logic	40	38	18	15	13	11	ns
tpd	Delay	P_DLY1C	380	377	166	163	123	120	ns
tpd	Delay	P_DLY2C	720	718	314	312	233	231	ns
tpd	Delay	P_DLY3C	1061	1060	462	460	343	341	ns
tpd	Delay	P_DLY4C	1396	1400	609	609	451	451	ns
tpd	Delay	Filter	200	200	78	78	53	53	ns

Table 11: Programmable Delay Expected Delays and Widths (Typical) T = 25 °C

Parameter	Description	Note	V_{DD} = 2.5 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
time1	Pulse Width, 1 cell	mode: (any) edge detect, edge detect output	325	150	110	ns
time1	Pulse Width, 2 cell	mode: (any) edge detect, edge detect output	740	300	225	ns
time1	Pulse Width, 3 cell	mode: (any) edge detect, edge detect output	1020	450	340	ns
time1	Pulse Width, 4 cell	mode: (any) edge detect, edge detect output	1350	600	450	ns
time2	Delay, 1 cell	mode: (any) edge detect, edge detect output	44	18	14	ns
time2	Delay, 2 cell	mode: (any) edge detect, edge detect output	44	18	14	ns
time2	Delay, 3 cell	mode: (any) edge detect, edge detect output	44	18	14	ns
time2	Delay, 4 cell	mode: (any) edge detect, edge detect output	44	18	14	ns
time1	Pulse Width, 1 cell	mode: delayed (any) edge detect, delayed edge detect output	340	150	110	ns
time1	Pulse Width, 2 cell	mode: delayed (any) edge detect, delayed edge detect output	670	300	220	ns
time1	Pulse Width, 3 cell	mode: delayed (any) edge detect, delayed edge detect output	1000	450	335	ns
time1	Pulse Width, 4 cell	mode: delayed (any) edge detect, delayed edge detect output	1340	600	450	ns
time2	Delay, 1 cell	mode: delayed (any) edge detect, delayed edge detect output	570	220	140	ns

Table 11: Programmable Delay Expected Delays and Widths (Typical) T = 25 °C(Continued)

Parameter	Description	Note	V_{DD} = 2.5 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
time2	Delay, 2 cell	mode: delayed (any) edge detect, delayed edge detect output	570	220	140	ns
time2	Delay, 3 cell	mode: delayed (any) edge detect, delayed edge detect output	570	220	140	ns
time2	Delay, 4 cell	mode: delayed (any) edge detect, delayed edge detect output	570	220	140	ns
time2	Delay, 1 cell	mode: both edge delay, edge detect output	382	375	126	ns
time2	Delay, 2 cell	mode: both edge delay, edge detect output	713	169	237	ns
time2	Delay, 3 cell	mode: both edge delay, edge detect output	1045	318	350	ns
time2	Delay, 4 cell	mode: both edge delay, edge detect output	1370	466	460	ns
time2	Delay, 1 cell	mode: both edge delay, delayed edge detect output	900	613	250	ns
time2	Delay, 2 cell	mode: both edge delay, delayed edge detect output	1250	520	360	ns
time2	Delay, 3 cell	mode: both edge delay, delayed edge detect output	1600	680	480	ns
time2	Delay, 4 cell	mode: both edge delay, delayed edge detect output	1900	815	600	ns

Table 12: Typical Filter Rejection Pulse Width at T = 25°C

Parameter	V_{DD} = 2.5 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
Filtered Pulse Width	< 123	< 84	< 52	ns

Table 13: Typical Counter/Delay Offset Measurements at T = 25°C

Parameter	OSC Freq	OSC Power	V_{DD} = 2.5 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
Power-ON time	25 MHz	auto	0.13	0.13	0.13	µs
Power-ON time	2.048 MHz	auto	0.3	0.4	0.4	µs
Power-ON time	2.048 kHz	auto	660	570	480	µs
frequency settling time	25 MHz	auto	4	4	8	µs
frequency settling time	2.048 MHz	auto	0.3	0.4	0.4	µs
frequency settling time	2.048 kHz	auto	660	570	480	µs
variable (CLK period)	25 MHz	forced	0-40	0-40	0-40	µs
variable (CLK period)	2.048 MHz	forced	0-0.5	0-0.5	0-0.5	µs
variable (CLK period)	2.048 kHz	forced	0-488	0-488	0-488	µs
tpd (non-delayed edge)	25 MHz/ 2.048 kHz	either	35	14	10	ns

3.5 OSCILLATOR CHARACTERISTICS

Table 14: Oscillator0 2.048 kHz Frequency Limits

Power Supply Range (V_{DD}), V	Temperature Range			
	+25 °C		-40 °C to +85 °C	
	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz
2.5 V ±8 %	2.026	2.071	1.907	2.088
3.3 V ±10 %	2.025	2.070	1.906	2.088
5 V ±10 %	2.025	2.071	1.905	2.087
2.5 V to 4.5 V	2.026	2.071	1.906	2.088
2.3 V to 5.5 V	2.025	2.071	1.905	2.088

Table 15: Oscillator0 2.048 kHz Frequency Error (Error Calculated Relative to Nominal Value)

Power Supply Range (V_{DD}), V	Temperature Range			
	+25 °C		-40 °C to +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
2.5 V ±8 %	-1.07 %	1.12 %	-6.91 %	1.95 %
3.3 V ±10 %	-1.09 %	1.09 %	-6.94 %	1.94 %
5 V ±10 %	-1.12 %	1.11 %	-6.96 %	1.92 %
2.5 V to 4.5 V	-1.09 %	1.10 %	-6.96 %	1.95 %
2.3 V to 5.5 V	-1.12 %	1.12 %	-6.96 %	1.95 %

Table 16: Oscillator1 2.048 MHz Frequency Limits

Power Supply Range (V_{DD}), V	Temperature Range			
	+25 °C		-40 °C to +85 °C	
	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz
2.5 V ±8 %	2.021	2.068	1.987	2.088
3.3 V ±10 %	2.024	2.069	1.990	2.089
5 V ±10 %	2.026	2.072	1.994	2.092
2.5 V to 4.5 V	2.022	2.071	1.988	2.090
2.3 V to 5.5 V	2.021	2.072	1.987	2.092

Table 17: Oscillator1 2.048 MHz Frequency Error (Error Calculated Relative to Nominal Value)

Power Supply Range (V_{DD}), V	Temperature Range			
	+25 °C		-40 °C to +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
2.5 V ±8 %	-1.32 %	0.96 %	-2.98 %	1.93 %
3.3 V ±10 %	-1.14 %	1.01 %	-2.80 %	2.01 %

Table 17: Oscillator1 2.048 MHz Frequency Error (Error Calculated Relative to Nominal Value)(Continued)

Power Supply Range (V_{DD}), V	Temperature Range			
	+25 °C		-40 °C to +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
5 V ±10 %	-1.03 %	1.18 %	-2.61 %	2.13 %
2.5 V to 4.5 V	-1.27 %	1.09 %	-2.91 %	2.04 %
2.3 V to 5.5 V	-1.32 %	1.18 %	-2.98 %	2.13 %

Table 18: Oscillator2 25 MHz Frequency Limits

Power Supply Range (V_{DD}), V	Temperature Range			
	+25 °C		-40 °C to +85 °C	
	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz
2.5 V ±8 %	24.588	25.238	23.622	25.669
3.3 V ±10 %	24.668	25.261	23.678	25.732
5 V ±10 %	24.736	25.353	23.723	25.803
2.5 V to 4.5 V	24.620	25.288	23.656	25.769
2.3 V to 5.5 V	24.588	25.353	23.622	25.803

Table 19: Oscillator2 25 MHz Frequency Error (Error Calculated Relative to Nominal Value)

Power Supply Range (V_{DD}), V	Temperature Range			
	+25 °C		-40 °C to +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
2.5 V ±8 %	-1.65 %	0.96 %	-5.51 %	2.68 %
3.3 V ±10 %	-1.33 %	1.05 %	-5.29 %	2.93 %
5 V ±10 %	-1.06 %	1.42 %	-5.11 %	3.21 %
2.5 V to 4.5 V	-1.52 %	1.16 %	-5.38 %	3.08 %
2.3 V to 5.5 V	-1.65 %	1.42 %	-5.51 %	3.21 %

3.5.1 OSC Power-On Delay

Table 20: Oscillators Power-On Delay at T = 25 °C, OSC Power Mode: "Auto Power-On"

Power Supply Range (V_{DD}), V	Oscillator2 25 MHz		Oscillator2 25 MHz Start with delay		Oscillator1 2.048 MHz		Oscillator0 2.048 kHz	
	Typical Value, µs	Maximum Value, µs	Typical Value, µs	Maximum Value, µs	Typical Value, µs	Maximum Value, µs	Typical Value, µs	Maximum Value, µs
2.30	0.033	0.044	0.132	0.146	0.319	0.657	706.144	908.371
2.50	0.029	0.038	0.130	0.146	0.332	1.045	668.258	855.197
2.70	0.025	0.034	0.129	0.146	0.336	0.792	638.228	811.718
3.00	0.021	0.028	0.128	0.148	0.345	0.972	602.986	759.657
3.30	0.018	0.025	0.127	0.150	0.366	0.842	575.778	718.414

Table 20: Oscillators Power-On Delay at T = 25 °C, OSC Power Mode: "Auto Power-On"(Continued)

Power Supply Range (V_{DD}), V	Oscillator2 25 MHz		Oscillator2 25 MHz Start with delay		Oscillator1 2.048 MHz		Oscillator0 2.048 kHz	
	Typical Value, µs	Maximum Value, µs	Typical Value, µs	Maximum Value, µs	Typical Value, µs	Maximum Value, µs	Typical Value, µs	Maximum Value, µs
3.60	0.016	0.022	0.127	0.150	0.368	0.464	553.969	685.120
4.00	0.013	0.018	0.128	0.151	0.357	0.451	530.866	648.916
4.20	0.012	0.015	0.128	0.151	0.355	0.540	521.049	633.638
4.50	0.011	0.015	0.128	0.152	0.355	0.732	507.787	613.429
5.00	0.010	0.015	0.129	0.154	0.382	0.881	486.721	582.113
5.50	0.010	0.012	0.130	0.155	0.386	0.774	462.127	551.579

3.6 ANALOG COMPARATOR CHARACTERISTICS

Table 21: Analog Comparator Specifications at T = -40 °C to +85 °C, VDD = 2.3 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Note	Condition	Min	Typ	Max	Unit
V_{ACMP}	ACMP0H, ACMP1H, ACMP2L, ACMP3L Input Voltage Range	Positive Input	V_{DD} = 2.5 V ± 5 %	0	--	V_{DD}	V
		Negative Input		0	--	2.016	V
		Positive Input	V_{DD} = 3.3 V ± 10 %	0	--	V_{DD}	V
		Negative Input		0	--	2.016	V
		Positive Input	V_{DD} = 5.0 V ± 10 %	0	--	V_{DD}	V
		Negative Input		0	--	2.016	V
V_{offset}	ACMP0H, ACMP1H Input Offset Voltage	Vhys = 0 mV, Gain = 1, Vref = 32 mV to 2016 mV	T = 25°C	0	--	5.68	mV
				0	--	6.33	mV
	ACMP2L, ACMP3L Input Offset Voltage		T = 25°C	0	--	5.09	mV
				0	--	5.55	mV
t_{start}	ACMP0H, ACMP1H Start Time	ACMP Power-On delay, Minimal required wake time for the "Wake and Sleep function"	T = 25°C	--	25.0	36.3	µS
				--	26.2	51.4	µS
	ACMP2L, ACMP3L Start Time		T = 25°C	--	139.3	233.3	µS
				--	144.6	326.6	µS
V_{HYS}	ACMP0H, ACMP1H Built-in Hysteresis	V_{HYS} = 32 mV	T = 25°C	23.60	--	36.74	mV
		V_{HYS} = 64 mV	T = 25°C	56.32	--	66.79	mV
		V_{HYS} = 196 mV	T = 25°C	189.50	--	196.00	mV
		V_{HYS} = 32 mV		21.16	--	38.84	mV
		V_{HYS} = 64 mV		52.77	--	67.32	mV
		V_{HYS} = 196 mV		180.62	--	196.00	mV
	ACMP2L, ACMP3L Built-in Hysteresis	V_{HYS} = 32 mV	T = 25°C	26.46	--	34.43	mV
		V_{HYS} = 64 mV	T = 25°C	56.58	--	67.38	mV
		V_{HYS} = 196 mV	T = 25°C	185.24	--	197.32	mV
		V_{HYS} = 32 mV		22.28	--	36.86	mV
		V_{HYS} = 64 mV		54.49	--	68.02	mV
		V_{HYS} = 196 mV		183.47	--	197.32	mV

Table 21: Analog Comparator Specifications at T = -40 °C to +85 °C, VDD = 2.3 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Note	Condition	Min	Typ	Max	Unit
R_{sin}	Series Input Resistance	Gain = 1x		--	100.0	--	MΩ
		Gain = 0.5x		--	1.0	--	MΩ
		Gain = 0.33x		--	0.8	--	MΩ
		Gain = 0.25x		--	1.0	--	MΩ
PROP	Propagation Delay, Response Time for ACMP0H, ACMP1H	Gain = 1, Vref = 32 mV to 2016 mV, Overdrive = 5 mV	Low to High	--	2.53	4.73	μS
			High to Low	--	1.88	9.48	μS
		Gain = 1, Vref = 32 mV to 2016 mV, Overdrive =10 mV	Low to High	--	1.75	3.20	μS
			High to Low	--	1.36	2.30	μS
		Gain = 1, Vref = 32 mV to 2016 mV, Overdrive = 100 mV	Low to High	--	0.81	7.42	μS
			High to Low	--	0.55	0.84	μS
	Propagation Delay, Response Time for ACMP2L, ACMP3L	Gain = 1, Vref = 32 mV to 2016 mV, Overdrive = 5 mV	Low to High	--	74.91	139.75	μS
			High to Low	--	72.28	213.26	μS
		Gain = 1, Vref = 32 mV to 2016 mV, Overdrive =10 mV	Low to High	--	49.54	70.23	μS
			High to Low	--	46.92	68.44	μS
		Gain = 1, Vref = 32 mV to 2016 mV, Overdrive = 100 mV	Low to High	--	18.41	29.06	μS
			High to Low	--	16.54	26.87	μS
G	Gain error (including threshold and internal Vref error)	G = 1,		--	1	--	
		G = 0.5,		0.497	--	0.504	
		G = 0.33,		0.330	--	0.337	
		G = 0.25,		0.247	--	0.253	
Vref	Vref0 Output Capacitance Loading		Resistance Load = 1 MΩ	--	--	5	pF
			Resistance Load = 560 κΩ	--	--	10	pF
			Resistance Load = 100 kΩ	--	--	40	pF
			Resistance Load = 10 κΩ	--	--	80	pF
			Resistance Load = 2 κΩ	--	--	120	pF
			Resistance Load = 1 κΩ, Vref = 32 mV to 1024 mV	--	--	150	pF

Table 21: Analog Comparator Specifications at T = -40 °C to +85 °C, VDD = 2.3 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Note	Condition	Min	Typ	Max	Unit
Vref	Vref1 Output Capacitance Loading		Resistance Load = 1 MΩ	--	--	15	pF
			Resistance Load = 560 κΩ	--	--	27	pF
			Resistance Load = 100 kΩ	--	--	64	pF
			Resistance Load = 10 κΩ	--	--	120	pF
			Resistance Load = 2 κΩ	--	--	180	pF
			Resistance Load = 1 κΩ, Vref = 32 mV to 1024 mV	--	--	210	pF

3.7 ANALOG TEMPERATURE SENSOR CHARACTERISTICS

Table 22: TS Output vs Temperature (Output Range 1)

T, °C	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V	
	Typical, mV	Accuracy, %	Typical, mV	Accuracy, %	Typical, mV	Accuracy, %
-40	1186	±0.54	1187	±0.50	1187	±0.60
-30	1158	±0.29	1158	±0.29	1158	±0.29
-20	1131	±0.26	1131	±0.27	1131	±0.27
-10	1104	±0.26	1104	±0.26	1104	±0.25
0	1076	±0.37	1076	±0.37	1076	±0.37
10	1049	±0.36	1049	±0.37	1049	±0.37
20	1021	±0.36	1021	±0.35	1021	±0.37
30	994	±0.24	994	±0.25	994	±0.25
40	966	±0.34	966	±0.33	966	±0.33
50	938	±0.46	938	±0.47	938	±0.47
60	910	±0.63	910	±0.64	910	±0.64
70	881	±0.75	881	±0.75	881	±0.75
80	852	±0.93	852	±0.93	852	±0.92
85	838	±1.02	838	±1.03	838	±1.02

Table 23: TS Output vs Temperature (Output range 2)

T, °C	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V	
	Typical, mV	Accuracy, %	Typical, mV	Accuracy, %	Typical, mV	Accuracy, %
-40	997	±0.45	997	±0.45	997	±0.45
-30	973	±0.22	973	±0.22	973	±0.22
-20	950	±0.28	950	±0.28	950	±0.29
-10	927	±0.21	927	±0.20	927	±0.21
0	905	±0.30	905	±0.30	905	±0.30
10	882	±0.28	882	±0.28	882	±0.28
20	859	±0.27	859	±0.27	859	±0.28

Table 23: TS Output vs Temperature (Output range 2)(Continued)

T, °C	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V	
	Typical, mV	Accuracy, %	Typical, mV	Accuracy, %	Typical, mV	Accuracy, %
30	836	±0.21	836	±0.21	836	±0.21
40	813	±0.29	813	±0.28	813	±0.28
50	790	±0.32	790	±0.32	790	±0.32
60	766	±0.52	766	±0.52	766	±0.51
70	743	±0.62	743	±0.62	743	±0.61
80	719	±0.82	719	±0.82	719	±0.82
85	707	±0.82	707	±0.82	707	±0.82

Table 24: TS Output Error (Output Range 1)

V_{DD}, V	Error at T							
	-40°C, %	-20°C, %	0°C, %	20°C, %	40°C, %	60°C, %	80°C, %	85°C, %
2.30	±0.62	±0.27	±0.37	±0.35	±0.34	±0.63	±0.94	±1.02
2.50	±0.54	±0.26	±0.37	±0.36	±0.34	±0.63	±0.93	±1.02
2.70	±0.72	±0.26	±0.37	±0.36	±0.34	±0.62	±0.94	±1.03
3.00	±0.41	±0.26	±0.37	±0.36	±0.33	±0.64	±0.93	±1.02
3.30	±0.50	±0.27	±0.37	±0.35	±0.33	±0.64	±0.93	±1.03
3.60	±0.66	±0.26	±0.37	±0.36	±0.34	±0.64	±0.93	±1.02
4.00	±0.82	±0.26	±0.37	±0.36	±0.34	±0.64	±0.93	±1.03
4.20	±0.43	±0.27	±0.37	±0.36	±0.34	±0.64	±0.92	±1.02
4.50	±0.72	±0.27	±0.37	±0.37	±0.34	±0.64	±0.92	±1.02
5.00	±0.60	±0.27	±0.37	±0.37	±0.33	±0.64	±0.92	±1.02
5.50	±0.58	±0.27	±0.37	±0.36	±0.34	±0.64	±0.93	±1.03

Table 25: TS Output Error (Output Range 2)

V_{DD}, V	Error at T							
	-40°C, %	-20°C, %	0°C, %	20°C, %	40°C, %	60°C, %	80°C, %	85°C, %
2.30	±0.44	±0.28	±0.30	±0.28	±0.29	±0.52	±0.82	±0.82
2.50	±0.45	±0.28	±0.30	±0.27	±0.29	±0.52	±0.82	±0.82
2.70	±0.46	±0.28	±0.30	±0.27	±0.28	±0.52	±0.84	±0.84
3.00	±0.45	±0.29	±0.30	±0.27	±0.28	±0.53	±0.82	±0.82
3.30	±0.45	±0.28	±0.30	±0.27	±0.28	±0.52	±0.82	±0.82
3.60	±0.45	±0.28	±0.31	±0.27	±0.28	±0.53	±0.82	±0.82
4.00	±0.45	±0.28	±0.30	±0.27	±0.28	±0.52	±0.82	±0.82
4.20	±0.44	±0.28	±0.30	±0.28	±0.28	±0.52	±0.82	±0.82
4.50	±0.45	±0.28	±0.30	±0.27	±0.28	±0.51	±0.82	±0.82
5.00	±0.45	±0.29	±0.30	±0.28	±0.28	±0.51	±0.82	±0.82
5.50	±0.44	±0.28	±0.30	±0.28	±0.28	±0.51	±0.82	±0.83

4 User Programmability

The SLG46880/81 is a user programmable device with a One-Time-Programmable (OTP) memory array that is used to configure the 12 state ASM, logic, and mixed signal circuits. Three of the IO Pins provide a connection for the bit patterns into the OTP on board memory. A programming development kit allows the user the ability to create initial devices. Once the design is finalized, the programming code (.gpx file) is forwarded to Dialog Semiconductor to integrate into a production process.

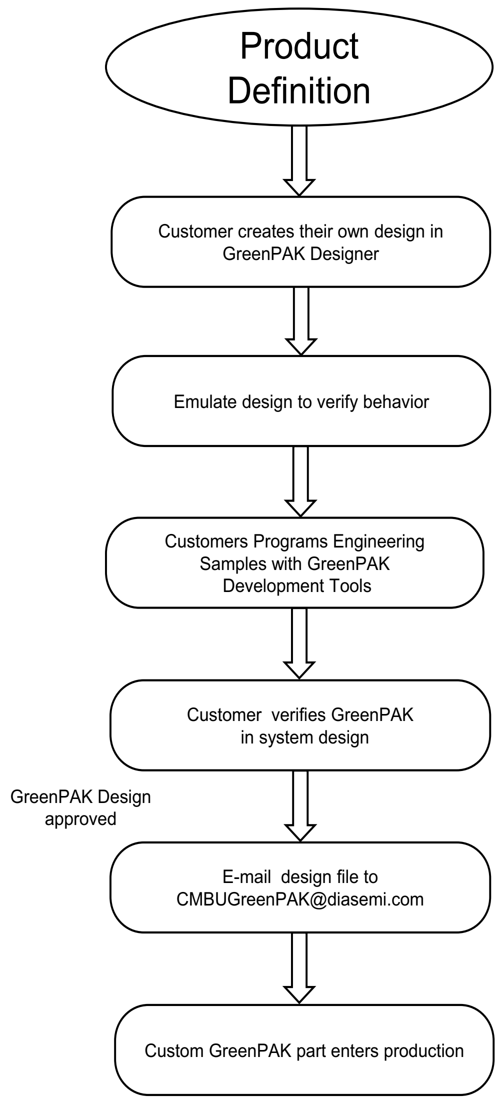


Figure 2: Steps to Create a Custom GreenPAK Device

5 IO Pins

5.1 IO PINS

The SLG46880/81 has a total of 12 GPIO, 8 GPI, and 8 GPO pins, which can function either as a user defined Input or Output, or as a special function (such as outputting the voltage reference), as well as a signal for programming of the on-chip Non Volatile Memory (NVM). Refer to Section 2 for pin definitions.

5.2 PULL UP/DOWN RESISTORS

All IO Pins have the option of user-selectable resistors that can be connected to the pin structure. The selectable values on these resistors are 10 kΩ, 100 kΩ and 1 MΩ. The internal resistors can be configured as either pull-up or pull-downs.

5.3 100 NS DEBOUNCE DELAY

100 ns debounce can be enabled for GPI0, GPI1, GPI5, and GPI6 by setting registers [536], [537], [538], and [539], respectively.

5.4 FAST PULL-UP/DOWN DURING POWER UP

During power-up, IO pull-up/down resistance will switch to 2.6 kΩ initially and then it will switch to normal setting value. This function is enabled by register [670].

5.5 DIGITAL INPUT LATCH

Digital Input Latch can be enabled for GPI0, GPI1, GPI4, GPI5, GPIO2, GPIO3, GPIO6, GPIO7. For timing diagram refer to Figure 3.

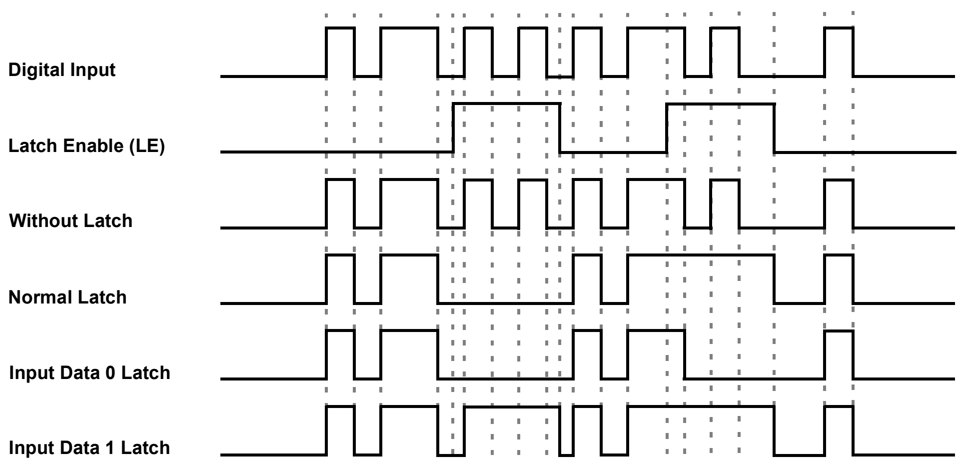


Figure 3: Digital Input Latch Timing Diagram

5.6 GPO OUTPUT SKEW

Output Skew function can be enabled for GPOs 0 to 7. Once enabled for any GPO (register [671]), Output Skew becomes valid for all GPOs. All eight GPOs are grouped in pairs: GPO0 and GPO7, GPO1 and GPO2, GPO3 and GPO4, GPO5 and GPO6. Output Skew allows to delay each pair before setting HIGH or LOW consequently. See Figure 4.

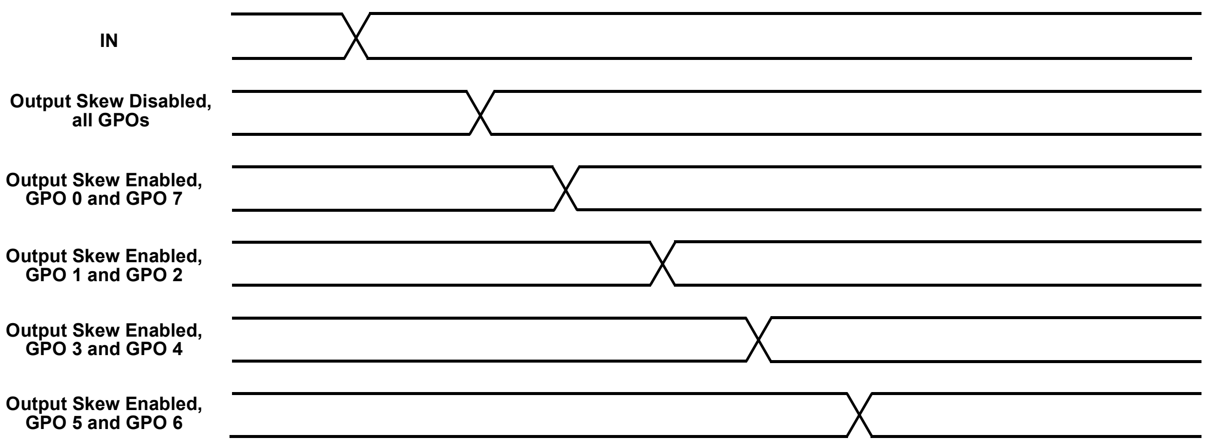


Figure 4: Output Skew Timing Diagram

5.7 ULTRA-LOW POWER DIGITAL INPUT (SLG46881 ONLY)

SLG46881 has an Ultra-Low Power Digital Input option that can be applied to GPIOs 0 to 11 and GPIs 1 to 7. Note that when Ultra-Low Power Digital Input is enabled, pull-up resistors for GPIOs 0 to 3, 8 to 11, GPIs 1 to 7 switch from V_{DD} to V_{DD2}.

5.8 GPI IO STRUCTURE (V_{DD})

5.8.1 SLG46880 GPI IO Structure (for GPIs 6, 7)

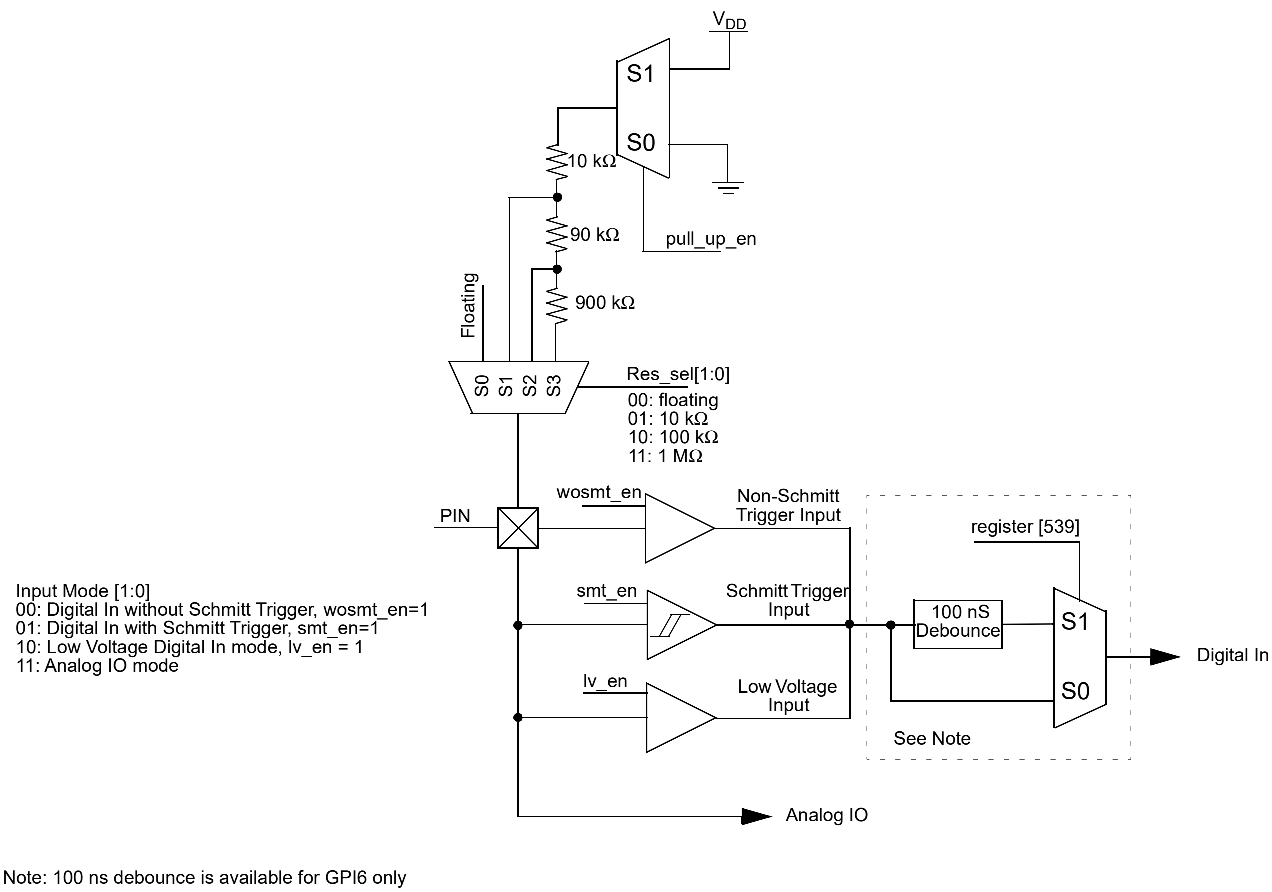


Figure 5: SLG46880 GPI IO Structure Diagram

5.8.2 SLG46881 GPI IO Structure (for GPIs 6, 7)

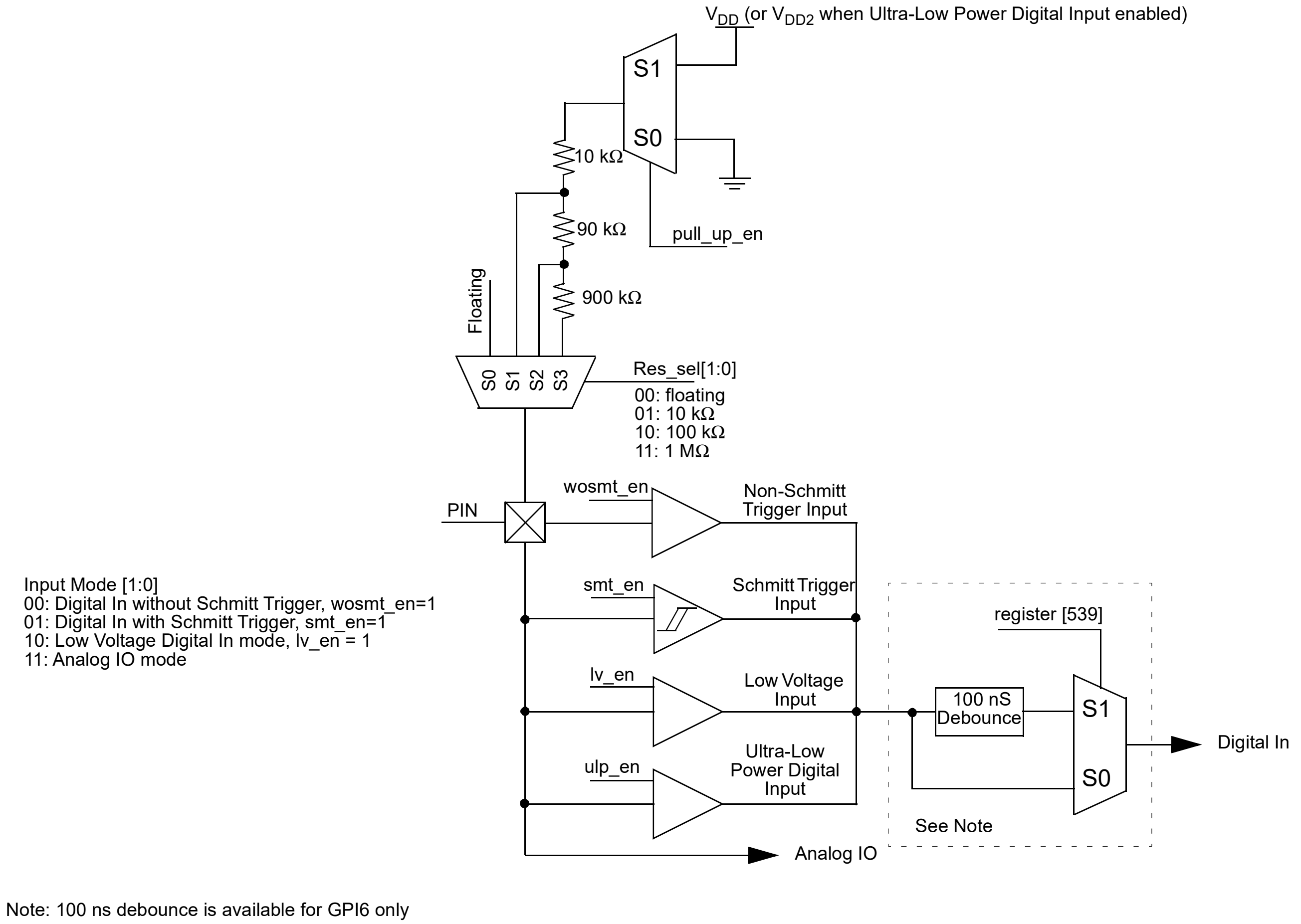


Figure 6: SLG46881 GPI IO Structure Diagram

5.9 GPI WITH INPUT LATCH IO STRUCTURE (V_{DD})

5.9.1 SLG46880 GPI with Input Latch IO Structure (for GPIs 0, 1)

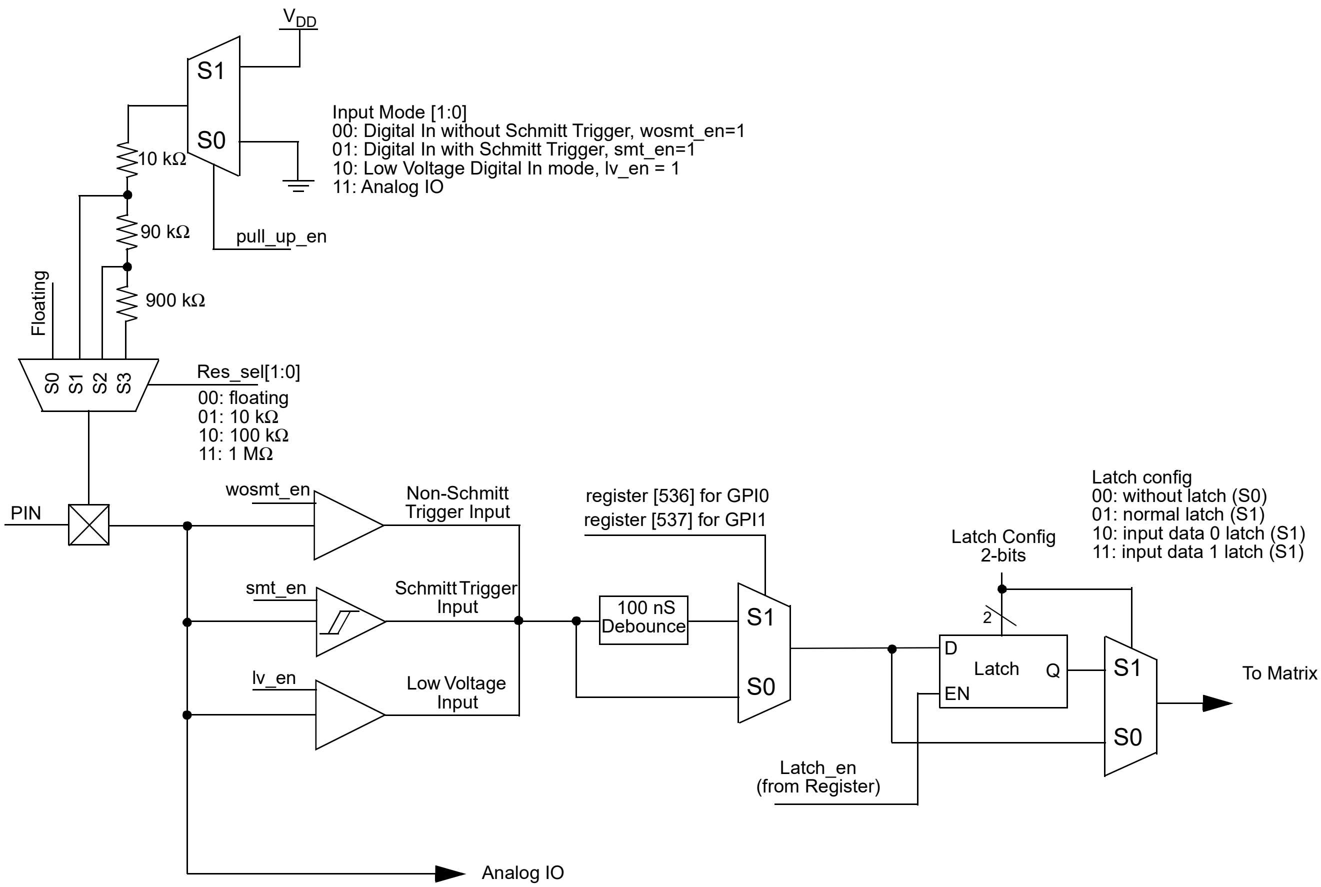


Figure 7: SLG46880 GPI with Input Latch Structure Diagram

5.9.2 SLG46881 GPI with Input Latch IO Structure (for GPIs 0, 1)

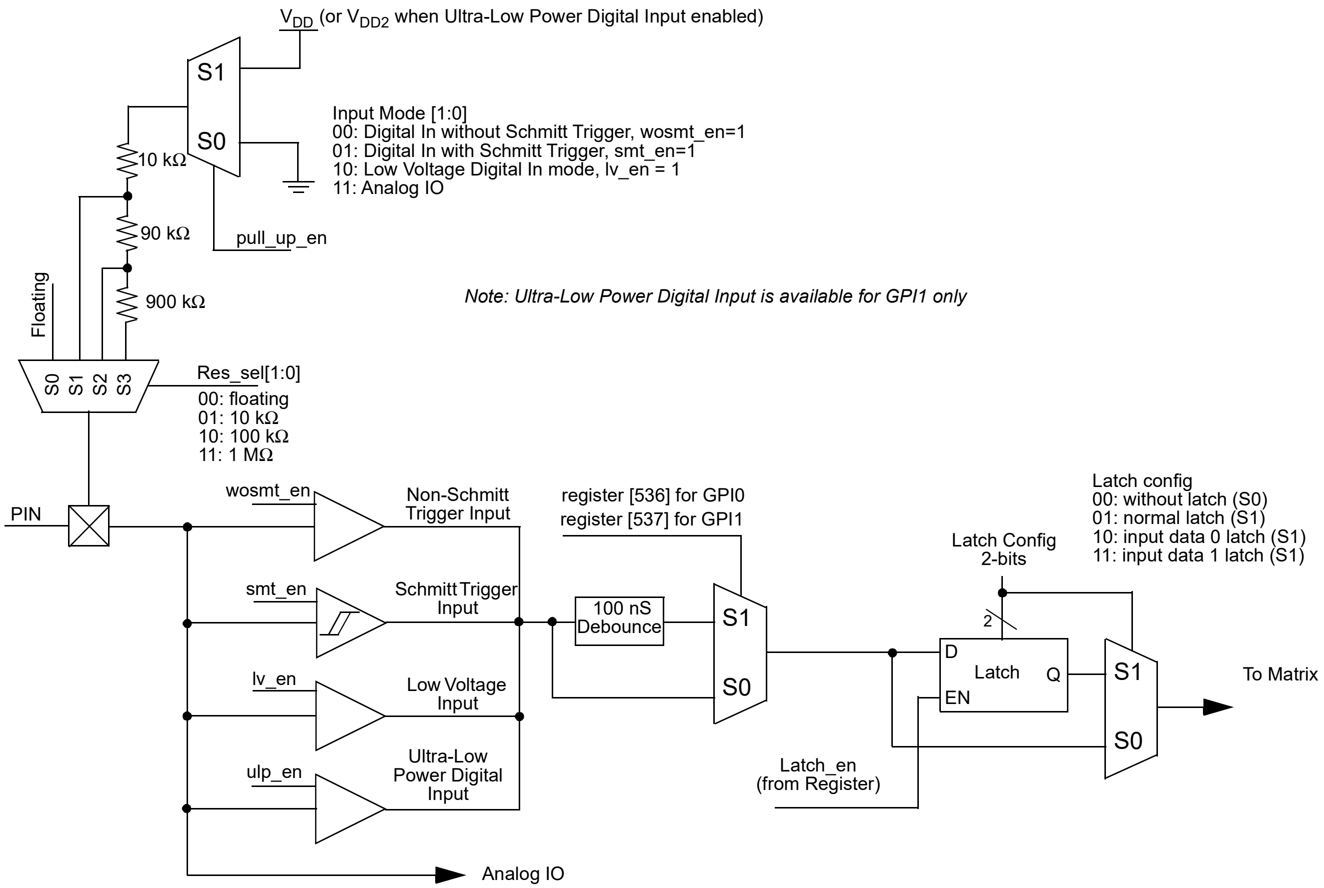


Figure 8: SLG46881 GPI with Input Latch Structure Diagram

5.10 GPI WITH I^{2}C MODE IO STRUCTURE (V_{DD})

5.10.1 SLG46880 GPI with I^{2}C Mode Structure (for GPIs 2, 3)

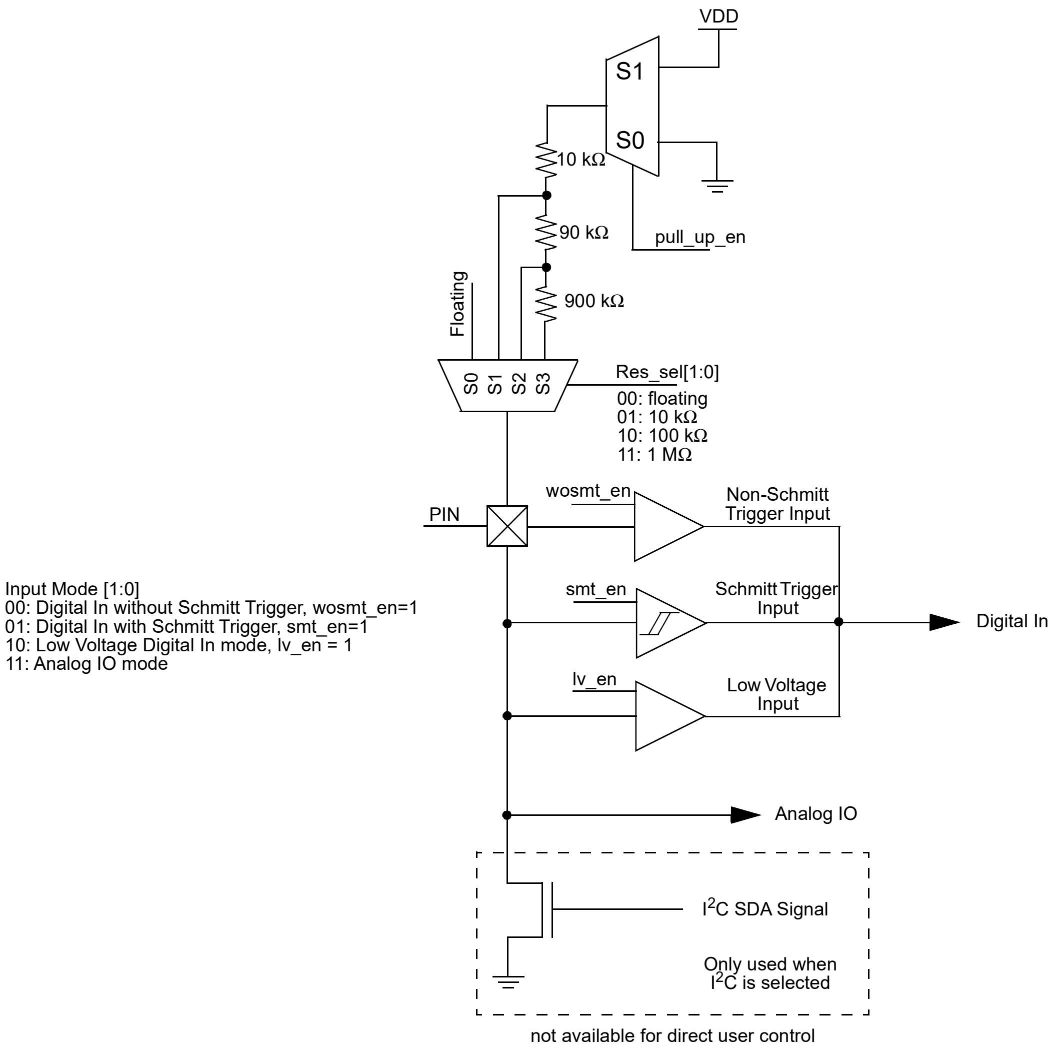


Figure 9: SLG46880 GPI with I^{2}C Mode IO Structure Diagram

5.10.2 SLG46881 GPI with I²C Mode Structure (for GPIs 2, 3)

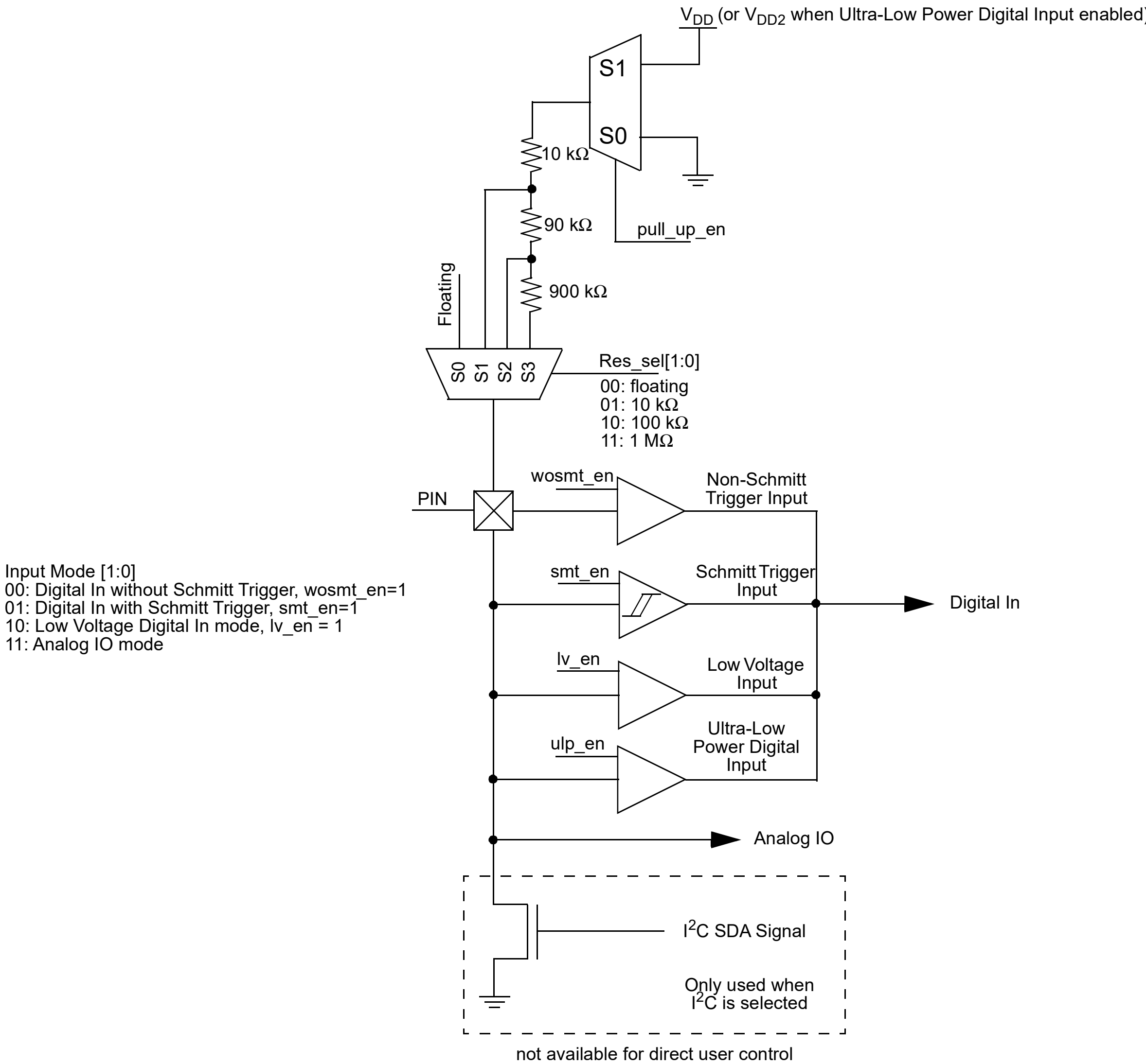


Figure 10: SLG46881 GPI with I²C Mode IO Structure Diagram

5.11 GPIO WITH MATRIX OE IO STRUCTURE (V_{DD} OR V_{DD2})

5.11.1 SLG46880 GPIO with Matrix OE IO Structure (for GPIOs 0, 1, 8, 9, 10, 11 with V_{DD}, and GPIOs 4, 5 with V_{DD2})

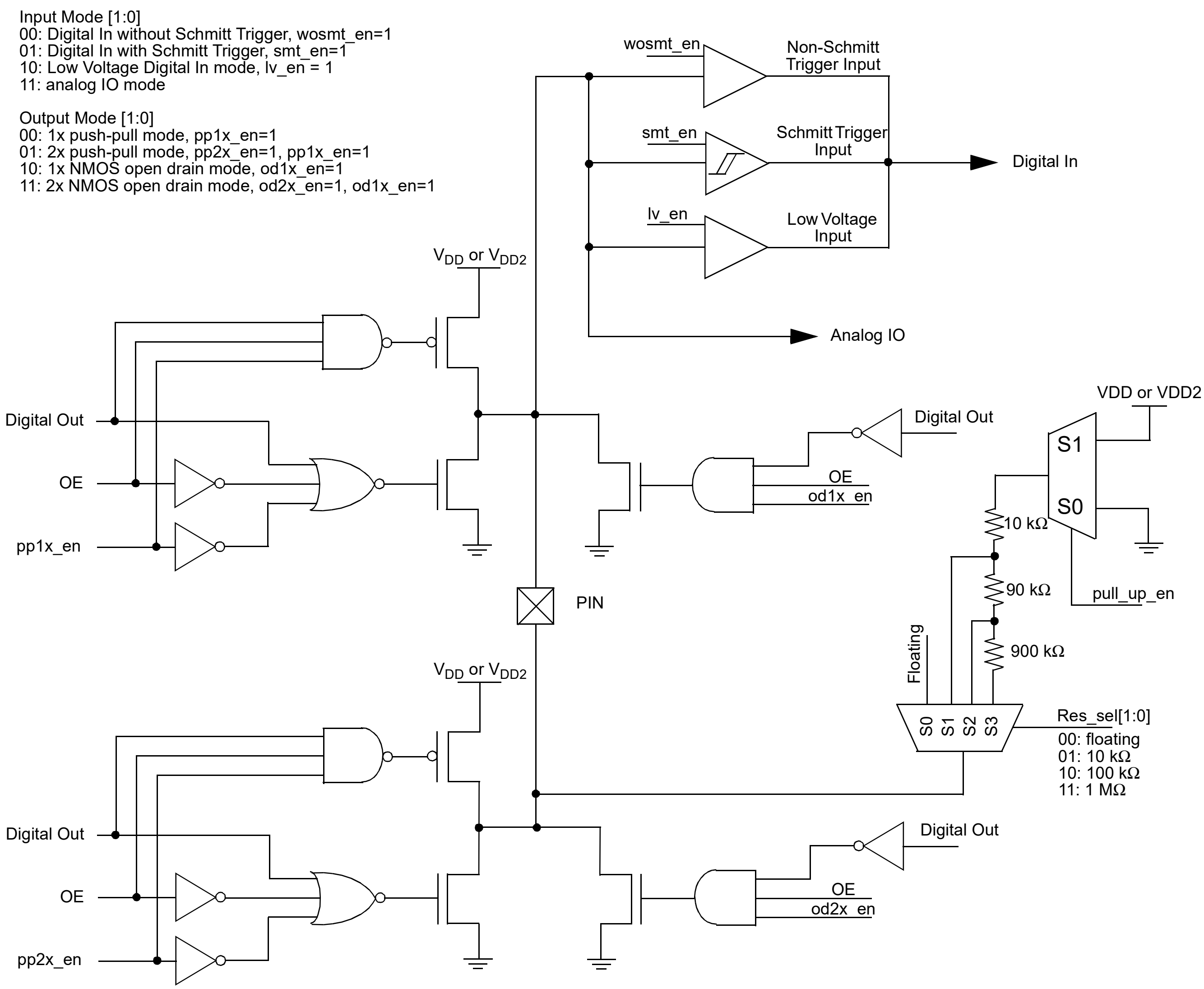
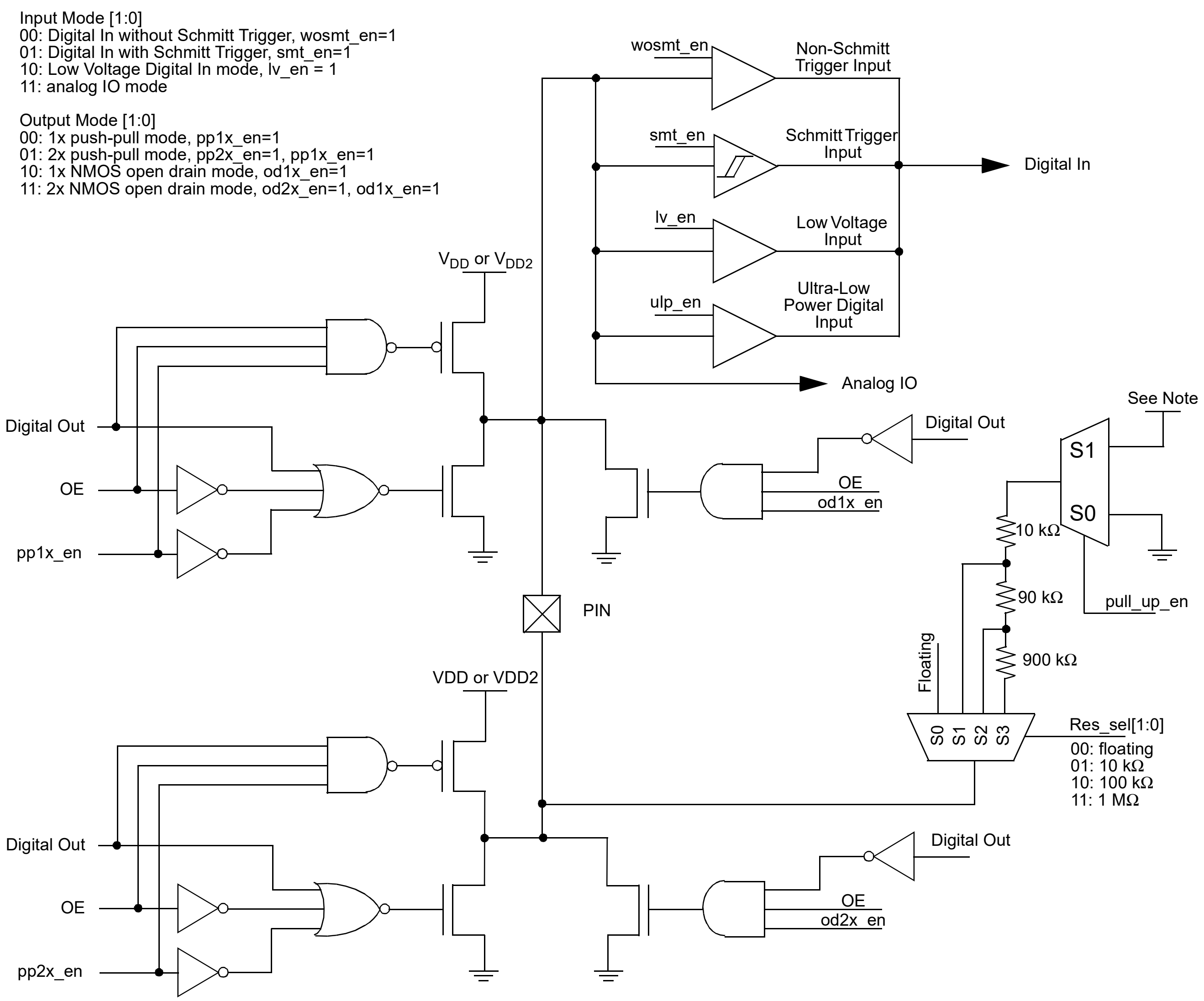


Figure 11: SLG46880 GPIO with Matrix OE IO Structure Diagram

5.11.2 SLG46881 GPIO with Matrix OE IO Structure (for GPIOs 0, 1, 8, 9, 10, 11 with V_{DD}, and GPIOs 4, 5 with V_{DD2})



Note: V_{DD} for GPIOs 0, 1, 8, 9, 10, 11 when Ultra-Low Power Digital Input disabled or V_{DD2} when Ultra-Low Power Digital Input enabled.
V_{DD2} for GPIOs 4 and 5.

Figure 12: SLG46881 GPIO with Matrix OE IO Structure Diagram

5.12 GPIO WITH MATRIX OE AND INPUT LATCH IO STRUCTURE (V_{DD} OR V_{DD2})

5.12.1 SLG46880 GPIO with Matrix OE and Input Latch IO Structure (for GPIOs 2, 3 with V_{DD}, GPIOs 6, 7 with V_{DD2})

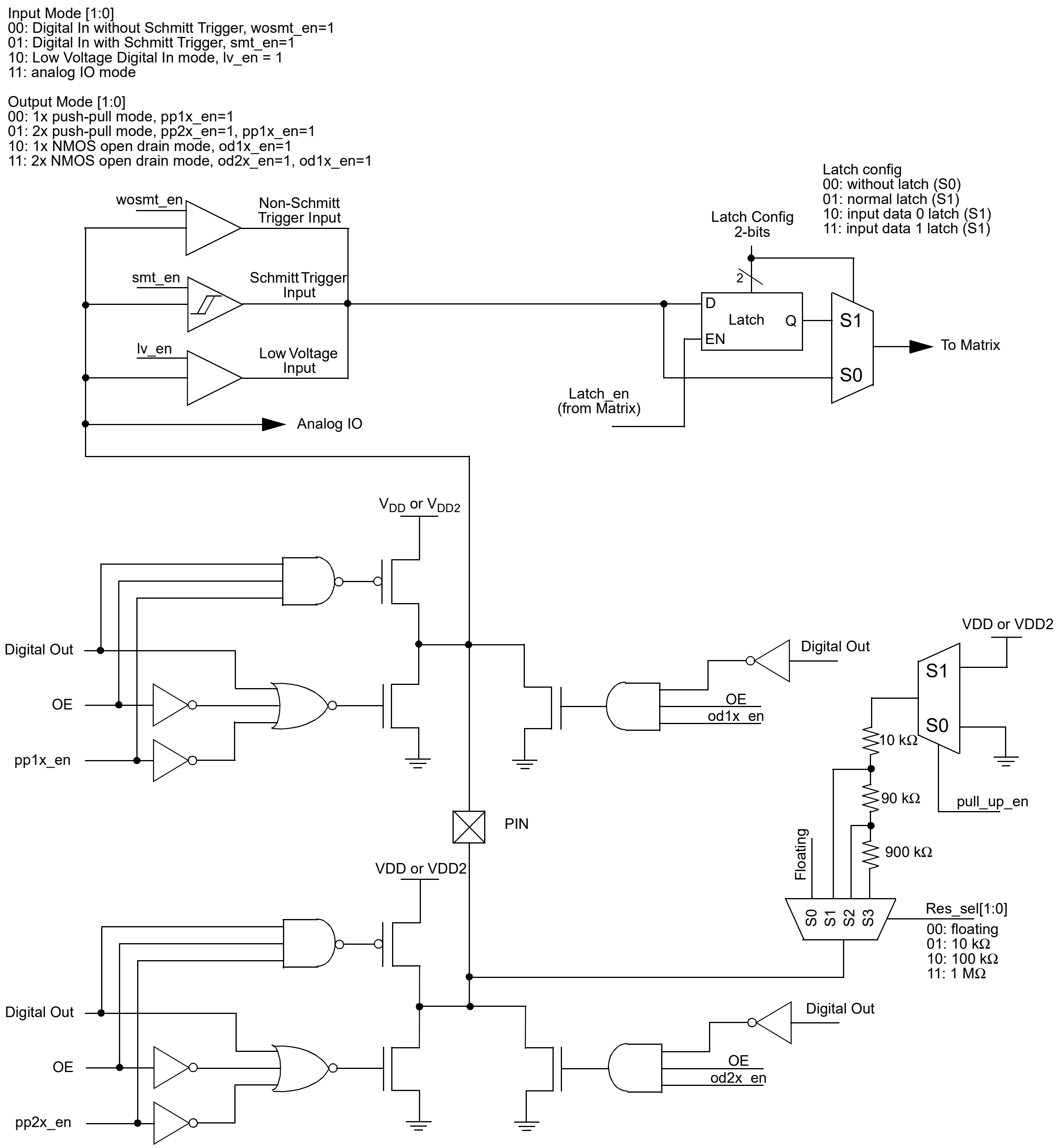


Figure 13: SLG46880 GPIO with Matrix OE and Input Latch IO Structure Diagram

5.12.2 SLG46881 GPIO with Matrix OE and Input Latch IO Structure (for GPIOs 2, 3 with V_{DD}, GPIOs 6, 7 with V_{DD2})

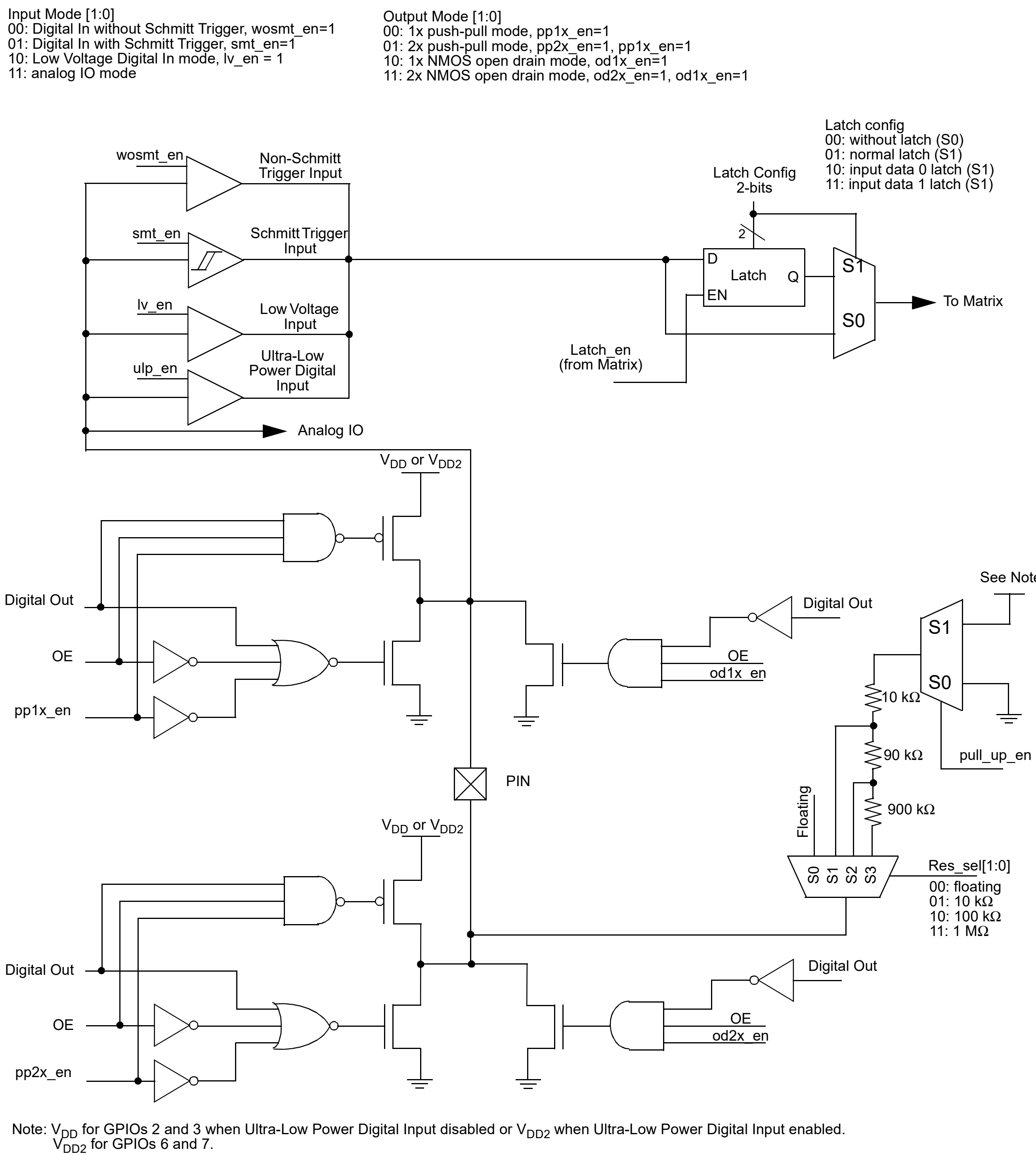
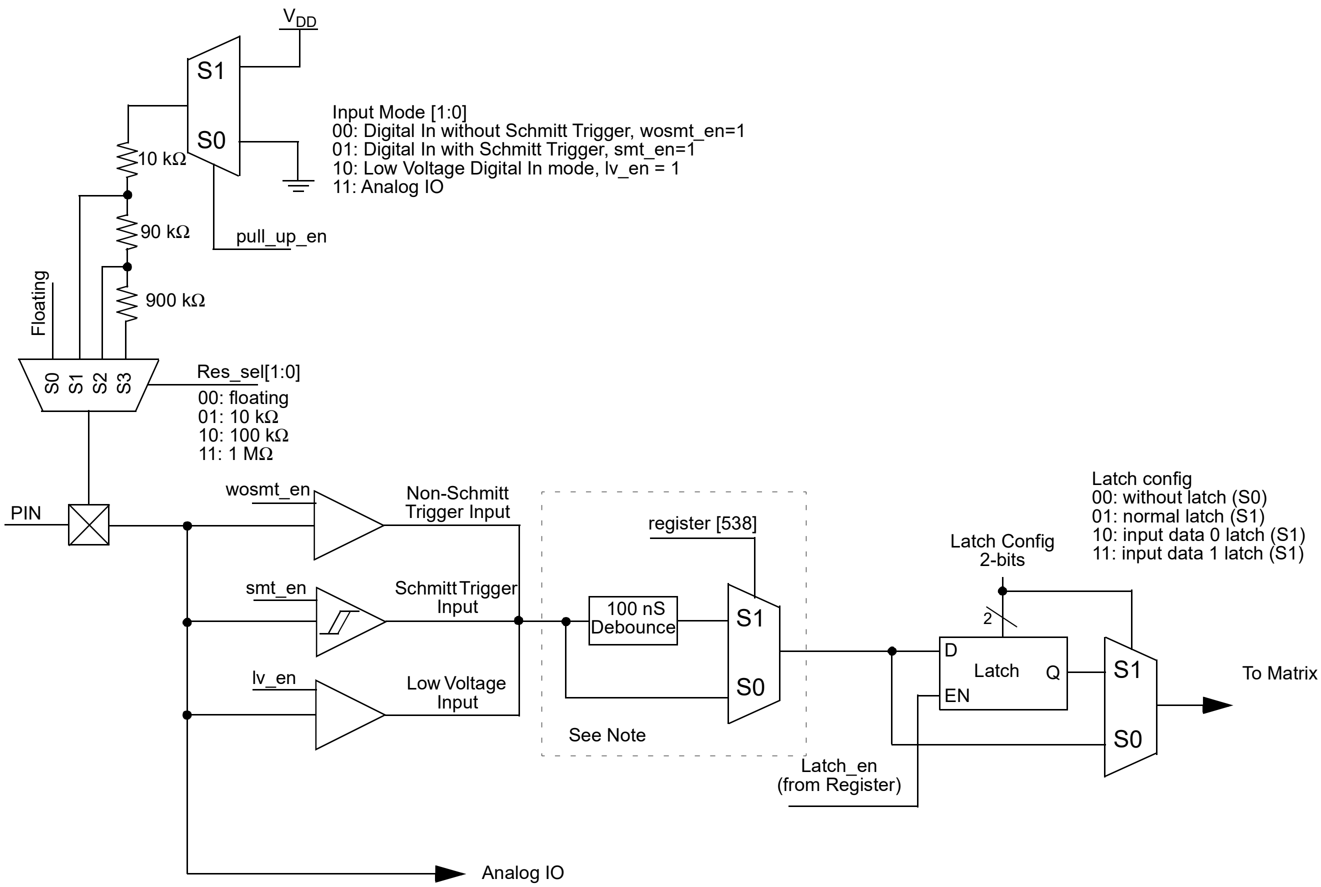


Figure 14: SLG46881 GPIO with Matrix OE and Input Latch IO Structure Diagram

5.13 GPI WITH INPUT LATCH AND CRYSTAL INPUT IO STRUCTURE (V_{DD})

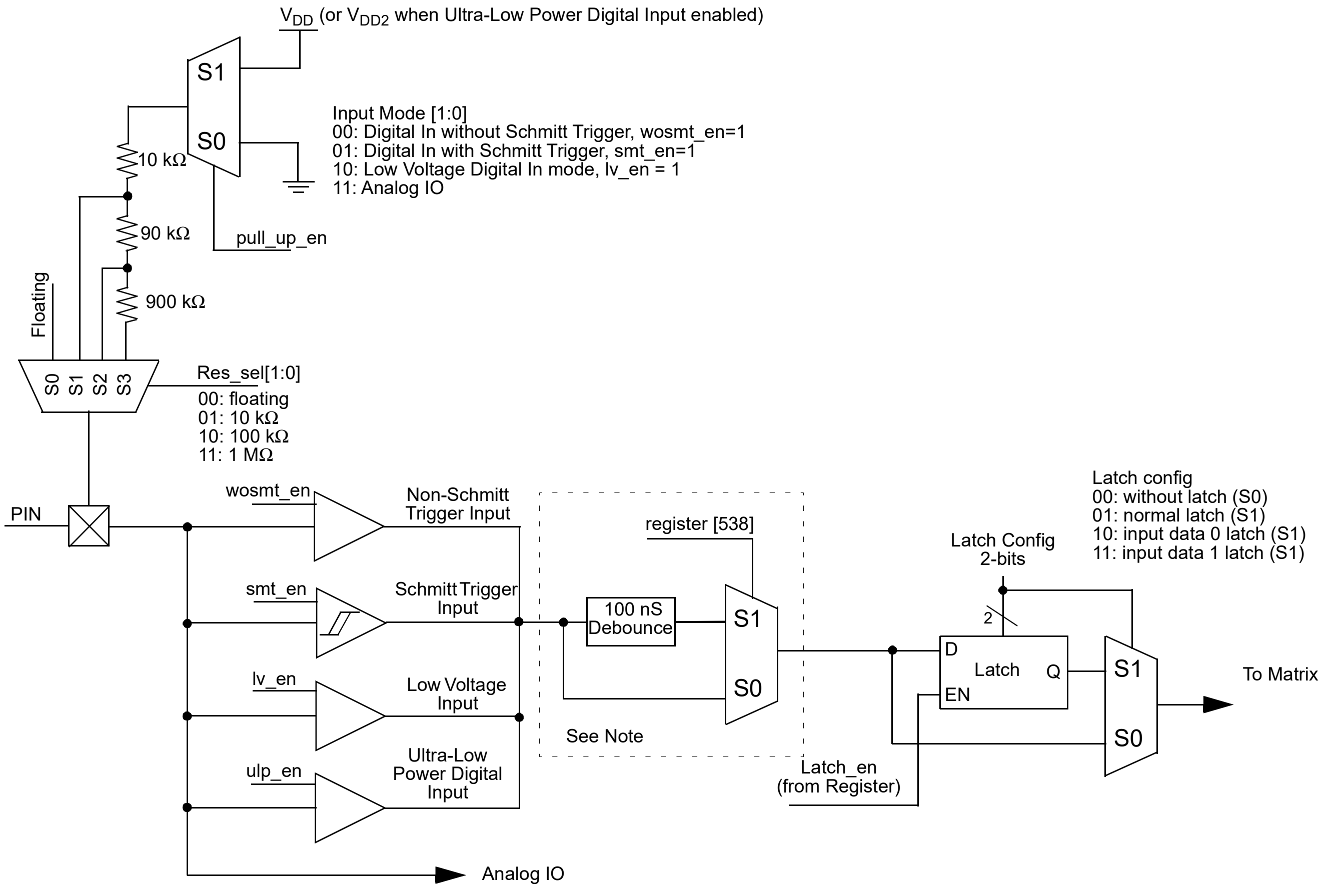
5.13.1 SLG46880 GPI with Input Latch and Crystal Input IO Structure (for GPIs 4, 5)



Note: 100 ns debounce is available for GPI5 only

Figure 15: SLG46880 GPI with Input Latch and Crystal Input IO Structure Diagram

5.13.2 SLG46881 GPI with Input Latch and Crystal Input IO Structure (for GPIs 4, 5)



Note: 100 ns debounce is available for GPI5 only

Figure 16: SLG46881 GPI with Input Latch and Crystal Input IO Structure Diagram

5.14 GPO REGISTER OE IO STRUCTURE (V_{DD} OR V_{DD2})

5.14.1 GPO Register OE IO Structure (for GPOs 0, 5, 6, 7 for V_{DD}, and GPOs 1, 2, 3, 4 for V_{DD2})

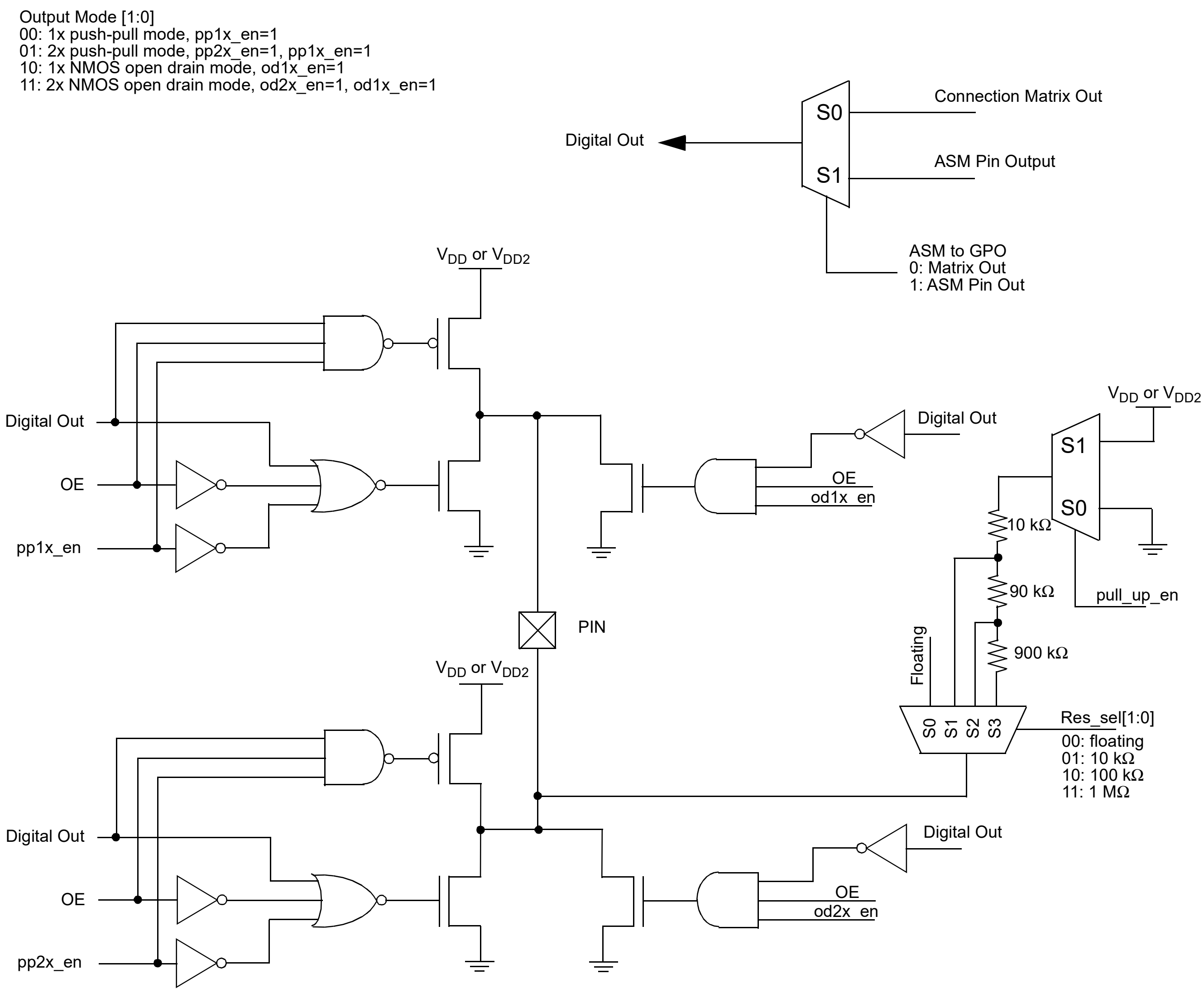


Figure 17: SLG46880/81 GPO Register OE IO Structure Diagram

6 Connection Matrix

The Connection Matrix in the SLG46880/81 is used to create the internal routing for internal functional macrocells of the device once it is programmed. The registers are programmed from the one-time NVM cell during Test Mode Operation. The output of each functional macrocell within the SLG46880/81 has a specific digital bit code assigned to it that is either set to active “High” or inactive “Low” based on the design that is created. Once the 4096 register bits within the SLG46880/81 are programmed a fully custom circuit will be created.

The Connection Matrix has 64 inputs, 84 outputs and 17 state dependent outputs. Each of the 64 inputs to the Connection Matrix is hard-wired to the digital output of a particular source macrocell, including IO pins, LUTs, analog comparators, other digital resources and V_{DD} and GND. The input to a digital macrocell uses a 6-bit register to select one of these 64 input lines.

For a complete list of the SLG46880/81’s register table, see Section 21.

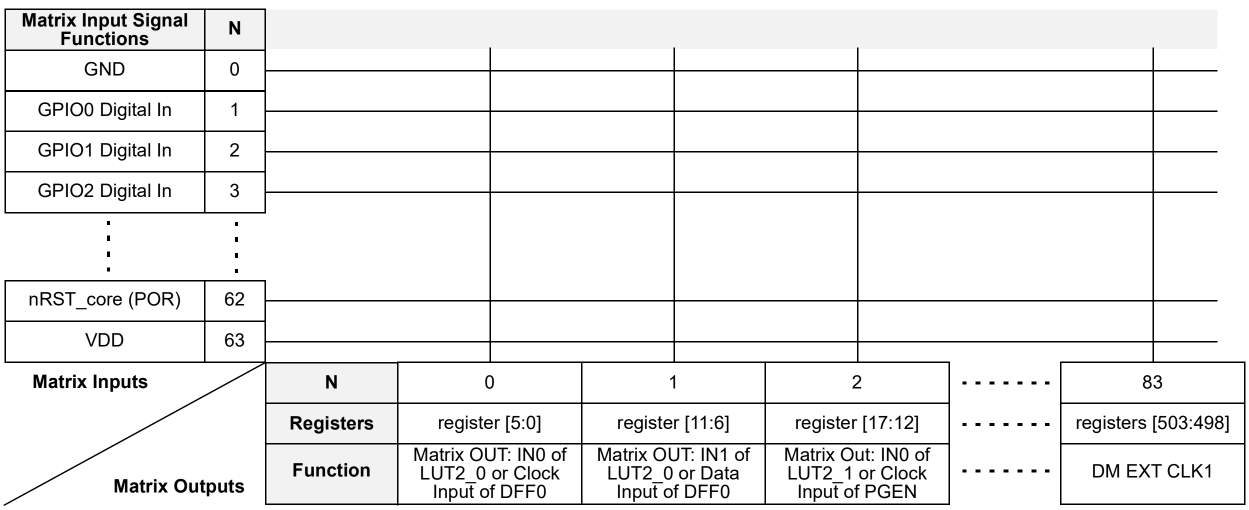


Figure 18: Connection Matrix

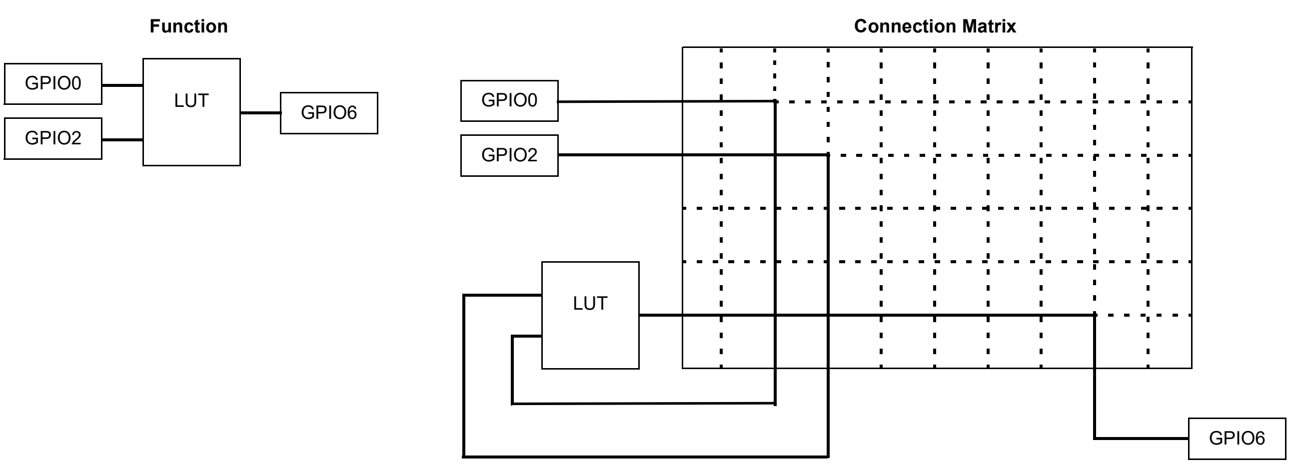


Figure 19: Connection Matrix Example

6.1 MATRIX INPUT TABLE

Table 26: Matrix Input Table

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
0	GND	0	0	0	0	0	0
1	GPIO0 Digital Input	0	0	0	0	0	1
2	GPIO1 Digital Input	0	0	0	0	1	0
3	GPIO2 Digital Input	0	0	0	0	1	1
4	GPI0 Digital Input	0	0	0	1	0	0
5	GPI1 Digital Input	0	0	0	1	0	1
6	GPIO3 Digital Input	0	0	0	1	1	0
7	GPIO4 Digital Input	0	0	0	1	1	1
8	LUT2_0/DFF0 Output	0	0	1	0	0	0
9	LUT2_1/PGEN Output	0	0	1	0	0	1
10	LUT3_0/DFF1 Output	0	0	1	0	1	0
11	LUT3_1/DFF2 Output	0	0	1	0	1	1
12	LUT3_2/DFF3 Output	0	0	1	1	0	0
13	LUT3_3/DFF4 Output	0	0	1	1	0	1
14	LUT3_4/CNT_DLY1(8bit) Output	0	0	1	1	1	0
15	LUT3_5/CNT_DLY2(8bit) Output	0	0	1	1	1	1
16	LUT3_6/CNT_DLY3(8bit) Output	0	1	0	0	0	0
17	LUT3_7/CNT_DLY4(8bit) Output	0	1	0	0	0	1
18	LUT4_0/CNT_DLY0(16bit) Output	0	1	0	0	1	0
19	LUT3_8/Pipe Delay Output0/Ripple CNT Output0	0	1	0	0	1	1
20	Pipe Delay Output1/Ripple CNT Output1	0	1	0	1	0	0
21	Internal 2.048 MHz Osc Output	0	1	0	1	0	1
22	Internal 2.048 kHz Osc Output	0	1	0	1	1	0
23	Internal 25 MHz Osc Output	0	1	0	1	1	1
24	Filter/Edge Detect Output/Ripple CNT Output2	0	1	1	0	0	0
25	Programmable Delay with Edge Detector Output	0	1	1	0	0	1
26	F(1) Function Output0	0	1	1	0	1	0
27	F(1) Function Output1	0	1	1	0	1	1
28	F(1) Function Output2	0	1	1	1	0	0
29	DM0_0 Macrocell Output0	0	1	1	1	0	1
30	DM0_0 Macrocell Output1	0	1	1	1	1	0
31	DM0_0 Macrocell Output2	0	1	1	1	1	1
32	GPI2/SDA Digital Input or I^2C_virtual_0 Input	1	0	0	0	0	0
33	GPI3/SCL Digital Input or I^2C_virtual_1 Input	1	0	0	0	0	1
34	I^2C_virtual_2 Input	1	0	0	0	1	0
35	I^2C_virtual_3 Input	1	0	0	0	1	1
36	I^2C_virtual_4 Input	1	0	0	1	0	0
37	I^2C_virtual_5 Input	1	0	0	1	0	1

Table 26: Matrix Input Table(Continued)

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
38	I^2C_virtual_6 Input	1	0	0	1	1	0
39	I^2C_virtual_7 Input	1	0	0	1	1	1
40	DM0_1 Macrocell Output0	1	0	1	0	0	0
41	DM0_1 Macrocell Output1	1	0	1	0	0	1
42	DM0_1 Macrocell Output2	1	0	1	0	1	0
43	ASM Connection Matrix Output RAM 0	1	0	1	0	1	1
44	ASM Connection Matrix Output RAM 1	1	0	1	1	0	0
45	ASM Connection Matrix Output RAM 2	1	0	1	1	0	1
46	ASM Connection Matrix Output RAM 0	1	0	1	1	1	0
47	GPIO5 Digital Input	1	0	1	1	1	1
48	GPIO6 Digital Input	1	1	0	0	0	0
49	GPIO7 Digital Input	1	1	0	0	0	1
50	GPIO8 Digital Input	1	1	0	0	1	0
51	GPI4 Digital Input/Crystal OSC	1	1	0	0	1	1
52	GPI5 Digital Input	1	1	0	1	0	0
53	GPI6 Digital Input	1	1	0	1	0	1
54	GPI7 Digital Input	1	1	0	1	1	0
55	GPIO9 Digital Input	1	1	0	1	1	1
56	ACMP0H Output	1	1	1	0	0	0
57	ACMP1H Output	1	1	1	0	0	1
58	ACMP2L Output	1	1	1	0	1	0
59	ACMP3L output	1	1	1	0	1	1
60	GPIO10 Digital Input	1	1	1	1	0	0
61	GPIO11 Digital Input	1	1	1	1	0	1
62	nRST_core (POR) as matrix input	1	1	1	1	1	0
63	V_{DD}	1	1	1	1	1	1

6.2 MATRIX OUTPUT TABLE

Table 27: Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[5:0]	Matrix Out 0: IN0 of LUT2_0 or Clock Input of DFF0	0
[11:6]	Matrix Out 1: IN1 of LUT2_0 or Data Input of DFF0	1
[17:12]	Matrix Out 2: IN0 of LUT2_1 or Clock Input of PGEN	2
[23:18]	Matrix Out 3: IN1 of LUT2_1 or nRST of PGEN	3
[29:24]	Matrix Out 4: IN0 of LUT3_0 or Clock Input of DFF1	4
[35:30]	Matrix Out 5: IN1 of LUT3_0 or Data Input of DFF1	5
[41:36]	Matrix Out 6: IN2 of LUT3_0 or nRST (nSET) of DFF1	6
[47:42]	Matrix Out 7: IN0 of LUT3_1 or Clock Input of DFF2	7
[53:48]	Matrix Out 8: IN1 of LUT3_1 or Data Input of DFF2	8

Table 27: Matrix Output Table(Continued)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[59:54]	Matrix Out 9: IN2 of LUT3_1 or nRST (nSET) of DFF2	9
[65:60]	Matrix Out 10: IN0 of LUT3_2 or Clock Input of DFF3	10
[71:66]	Matrix Out 11: IN1 of LUT3_2 or Data Input of DFF3	11
[77:72]	Matrix Out 12: IN2 of LUT3_2 or nRST (nSET) of DFF3	12
[83:78]	Matrix Out 13: IN0 of LUT3_3 or Clock Input of DFF4	13
[89:84]	Matrix Out 14: IN1 of LUT3_3 or Data Input of DFF4	14
[95:90]	Matrix Out 15: IN2 of LUT3_3 or nRST (nSET) of DFF4	15
[101:96]	Matrix Out 16:IN0 of LUT3_4 or Delay1 Input (or Counter1 nRST Input)	16
[107:102]	Matrix Out 17:IN1 of LUT3_4 or External Clock1 Input of Delay1 (or Counter1)	17
[113:108]	Matrix Out 18:IN2 of LUT3_4	18
[119:114]	Matrix Out 19:IN0 of LUT3_5 or Delay2 Input (or Counter2 nRST Input)	19
[125:120]	Matrix Out 20:IN1 of LUT3_5 or External Clock1 Input of Delay2 (or Counter2)	20
[131:126]	Matrix Out 21:IN2 of LUT3_5	21
[137:132]	Matrix Out 22:IN0 of LUT3_6 or Delay3 Input (or Counter3 nRST Input)	22
[143:138]	Matrix Out 23:IN1 of LUT3_6 or External Clock1 Input of Delay3 (or Counter3)	23
[149:144]	Matrix Out 24:IN2 of LUT3_6	24
[155:150]	Matrix Out 25:IN0 of LUT3_7 or Delay4 Input (or Counter4 nRST Input)	25
[161:156]	Matrix Out 26:IN1 of LUT3_7 or External Clock1 Input of Delay4 (or Counter4)	26
[167:162]	Matrix Out 27:IN2 of LUT3_7	27
[173:168]	Matrix Out 28:IN0 of LUT3_8 or Input of Pipe Delay	28
[179:174]	Matrix Out 29:IN1 of LUT3_8 or nRST of Pipe Delay	29
[185:180]	Matrix Out 30:IN2 of LUT3_8 or Clock of Pipe Delay	30
[191:186]	Matrix Out 31:IN0 of LUT4_0 or Delay0 Input (or Counter0 nRST Input)	31
[197:192]	Matrix Out 32:IN1 of LUT4_0 or External Clock Input of Delay0 (or Counter0)	32
[203:198]	Matrix Out 33:IN2 of LUT4_0 or UP Input of FSM0	33
[209:204]	Matrix Out 34:IN3 of LUT4_0 or KEEP Input of FSM0	34
[215:210]	Matrix Out 35: ACMP0H Power Down	35
[221:216]	Matrix Out 36: ACMP1H Power Down	36
[227:222]	Matrix Out 37: ACMP2L Power Down	37
[233:228]	Matrix Out 38: ACMP3L Power Down	38
[239:234]	Matrix Out 39: GPO7 DOUT	39
[245:240]	Matrix Out 40: GPO0 DOUT	40
[251:246]	Matrix Out 41: GPIO0 DOUT	41
[257:252]	Matrix Out 42: GPIO0 DOUT OE	42
[263:258]	Matrix Out 43: GPIO1 DOUT	43
[269:264]	Matrix Out 44: GPIO1 DOUT OE	44
[275:270]	Matrix Out 45: GPIO2 DOUT	45
[281:276]	Matrix Out 46: GPIO2 DOUT OE	46
[287:282]	Matrix Out 47: GPIO3 DOUT	47

Table 27: Matrix Output Table(Continued)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[293:288]	Matrix Out 48: GPIO3 DOUT OE	48
[299:294]	Matrix Out 49: GPIO4 DOUT	49
[305:300]	Matrix Out 50: GPIO4 DOUT OE	50
[311:306]	Matrix Out 51: GPIO5 DOUT	51
[317:312]	Matrix Out 52: GPIO5 DOUT OE	52
[323:318]	Matrix Out 53: GPO1 DOUT	53
[329:324]	Matrix Out 54: GPO2 DOUT	54
[335:330]	Matrix Out 55: GPO3 DOUT	55
[341:336]	Matrix Out 56: GPO4 DOUT	56
[347:342]	Matrix Out 57: GPIO6 DOUT OE	57
[353:348]	Matrix Out 58: GPIO6 DOUT	58
[359:354]	Matrix Out 59: GPIO7 DOUT	59
[365:360]	Matrix Out 60: GPIO7 DOUT OE	60
[371:366]	Matrix Out 61: GPIO8 DOUT OE	61
[377:372]	Matrix Out 62: GPIO8 DOUT	62
[383:378]	Matrix Out 63: GPIO9 DOUT OE	63
[389:384]	Matrix Out 64: GPIO9 DOUT	64
[395:390]	Matrix Out 65: GPIO10 DOUT OE	65
[401:396]	Matrix Out 66: GPIO10 DOUT	66
[407:402]	Matrix Out 67: GPIO11 DOUT OE	67
[413:408]	Matrix Out 68: GPIO11 DOUT	68
[419:414]	Matrix Out 69: GPO5 DOUT	69
[425:420]	Matrix Out 70: GPO6 DOUT	70
[431:426]	Matrix Out 71: ASM nRST	71
[437:432]	Matrix Out 72: OSC0 ENABLE	72
[443:438]	Matrix Out 73: OSC1 ENABLE	73
[449:444]	Matrix Out 74: OSC2 ENABLE	74
[455:450]	Matrix Out 75: Filter/Edge detect input	75
[461:456]	Matrix Out 76: F1 interrupt	76
[467:462]	Matrix Out 77: Programmable delay/edge detect input	77
[473:468]	Matrix Out 78: Temp sensor/Crystal OSC Power Down	78
[479:474]	Matrix Out 79: GPI Latch enable	79
[485:480]	Matrix Out 80: GPIO Latch enable	80
[491:486]	Matrix Out 81: BG enable	81
[497:492]	DM EXT CLK0	82
[503:498]	DM_EXT_CLK1	83
Note: For each Address, the two most significant bits are unused.		

6.3 CONNECTION MATRIX VIRTUAL INPUTS

As mentioned previously, the Connection Matrix inputs come from the outputs of various digital macrocells on the device. Eight of the Connection Matrix inputs have the special characteristic that the state of these signal lines comes from a corresponding data bit written as a register value via I^2C. This gives the user the ability to write data via the serial channel, and have this information translated into signals that can be driven into the Connection Matrix and from the Connection Matrix to the digital inputs of other macrocells on the device. The I^2C address for reading and writing these register values is at 0x1DB (475).

Six of the eight Connection Matrix Virtual Inputs are dedicated to this virtual input function. An I^2C write command to these register bits will set the signal values going into the Connection Matrix to the desired state. A read command to these register bits will read either the original data values coming from the NVM memory bits (that were loaded during the initial device startup), or the values from a previous write command (if that has happened).

Two of the eight Connection Matrix Virtual Inputs are shared with Pin digital inputs (GPI3/SCL Digital Input or I^2C_virtual_1 Input), and (GPI2/SDA Digital Input or I^2C_virtual_0 Input). If the virtual input mode is selected, an I^2C write command to these register bits will set the signal values going into the Connection Matrix to the desired state. A read command to these register bits will read either the original data values coming from the NVM memory bits (that were loaded during the initial device startup), or the values from a previous write command (if that has happened). The I^2C disable/enable register bit [4084] selects whether the Connection Matrix input comes from the Pin input or from the virtual register.

- Select SCL & Virtual Input 1 or GPI3/SCL.
- Select SDA & Virtual Input 0 or GPI2/SDA.

See Table 28 for Connection Matrix Virtual Inputs.

Table 28: Connection Matrix Virtual Inputs

Matrix Input Number	Matrix Input Signal Function	Register Bit Addresses (d)
32	I^2C_virtual_0 Input	[3800]
33	I^2C_virtual_1 Input	[3801]
34	I^2C_virtual_2 Input	[3802]
35	I^2C_virtual_3 Input	[3803]
36	I^2C_virtual_4 Input	[3804]
37	I^2C_virtual_5 Input	[3805]
38	I^2C_virtual_6 Input	[3806]
39	I^2C_virtual_7 Input	[3807]

6.4 CONNECTION MATRIX VIRTUAL OUTPUTS

The digital outputs of the various macrocells are routed to the Connection Matrix to enable interconnections to the inputs of other macrocells in the device. At the same time, it is possible to read the state of each of the macrocell outputs as a register value via I^2C. This option, called Connection Matrix Virtual Outputs, allows the user to remotely read the values of each macrocell output. The I^2C addresses for reading these register values are 0x1D7 (471) to 0x1DE (478). Write commands to these same register values will be ignored (with the exception of the Virtual Input register bits at 0x1DB (475)).

7 Combination Function Macrocells

The SLG46880/81 has 12 combination function macrocells that can serve more than one logic or timing function. In each case, they can serve as a Look Up Table (LUT), or as another logic or timing function. See the list below for the functions that can be implemented in these macrocells.

- One macrocell that can serve as either 2-bit LUT or as D Flip Flop
- Four macrocells that can serve as either 3-bit LUTs or as D Flip Flops with Set/Reset Input
- One macrocell that can serve as either 3-bit LUT or as Pipe Delay/Ripple Counter
- One macrocell that can serve as either 2-bit LUT or as Programmable Pattern Generator (PGEN)
- One macrocell that can serve as either 4-bit LUT or as 16-Bit Counter/Delay/FSM
- Four macrocells that can serve as either 3-bit LUTs or as 8-Bit Counter/Delays

Inputs/Outputs for the 12 combination function macrocells are configured from the connection matrix with specific logic functions which are defined by the state of NVM bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR). Inputs/Outputs for the 11 combination function macrocells are configured from the connection matrix with specific logic functions being defined by the state of NVM bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

7.1 2-BIT LUT OR D FLIP-FLOP MACROCELLS

There is one macrocell that can serve as either 2-bit LUT or as D Flip Flop. When used to implement LUT functions, the 2-bit LUT takes in two input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used to implement D Flip Flop function, the two input signals from the connection matrix go to the data (D) and clock (CLK) inputs for the Flip Flop, with the output going back to the connection matrix.

The operation of the D Flip-Flop and Latch will follow the functional descriptions below:

- DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change
- Latch: when CLK is Low, then Q = D; otherwise Q remains its previous value (input D has no effect on the output, when CLK is High)

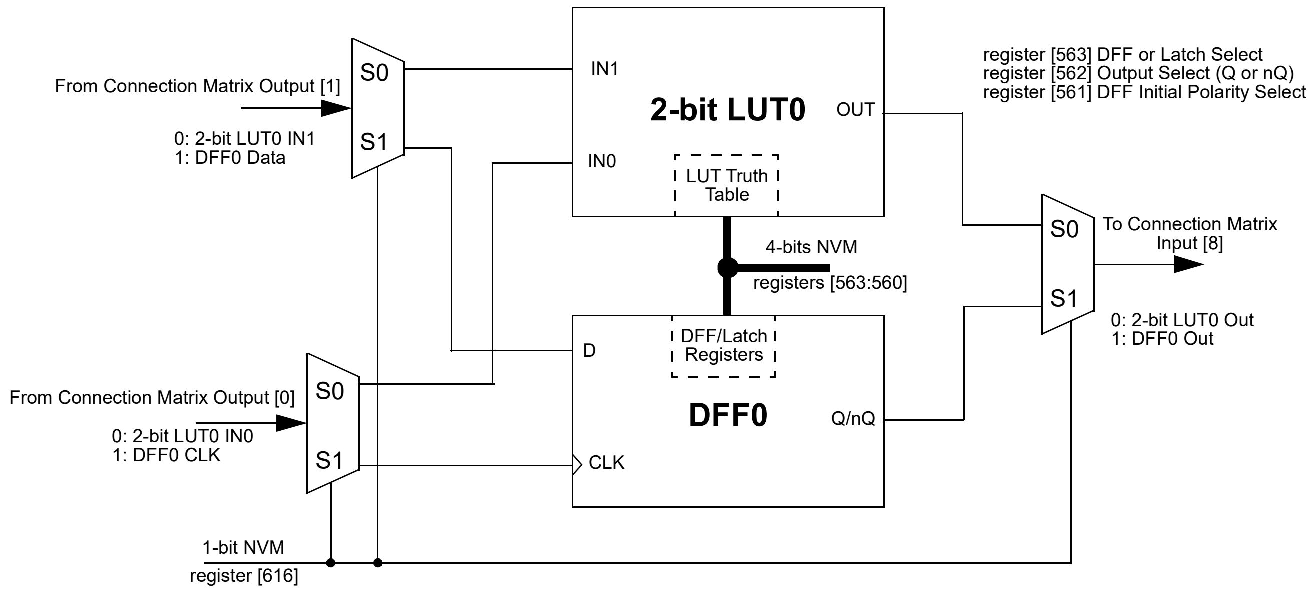


Figure 20: 2-bit LUT0 or DFF0

7.1.1 2-Bit LUT or D Flip-Flop Macrocell Used as 2-Bit LUT

Table 29: 2-bit LUT0 Truth Table

IN1	IN0	OUT	
0	0	register [560]	LSB
0	1	register [561]	
1	0	register [562]	
1	1	register [563]	MSB

This Macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

2-Bit LUT0 is defined by registers [563:560]

The Table 30 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 2-bit LUT logic cells.

Table 30: 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

7.1.2 Initial Polarity Operations

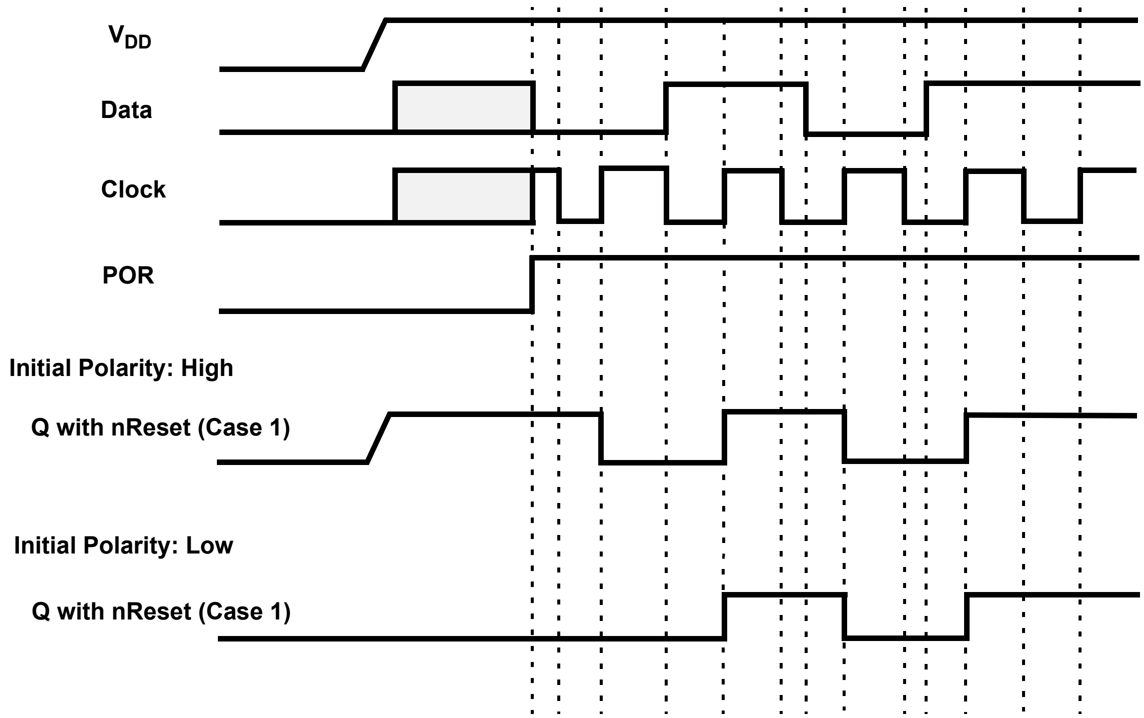


Figure 21: DFF Polarity Operations

7.2 2-BIT LUT OR PROGRAMMABLE PATTERN GENERATOR

The SLG46880/81 has one combination function macrocell that can serve as a logic or timing function. This macrocell can serve as a Look Up Table (LUT), or Programmable Pattern Generator (PGEN).

When used to implement LUT functions, the 2-bit LUT takes in two input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used as a LUT to implement combinatorial logic functions, the outputs of the LUT can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR). The user can also define the combinatorial relationship between inputs and outputs to be any selectable function.

When operating as a Programmable Pattern Generator, the output of the macrocell with clock out a sequence of two to sixteen bits that are user selectable in their bit values, and user selectable in the number of bits (up to sixteen) that are output before the pattern repeats.

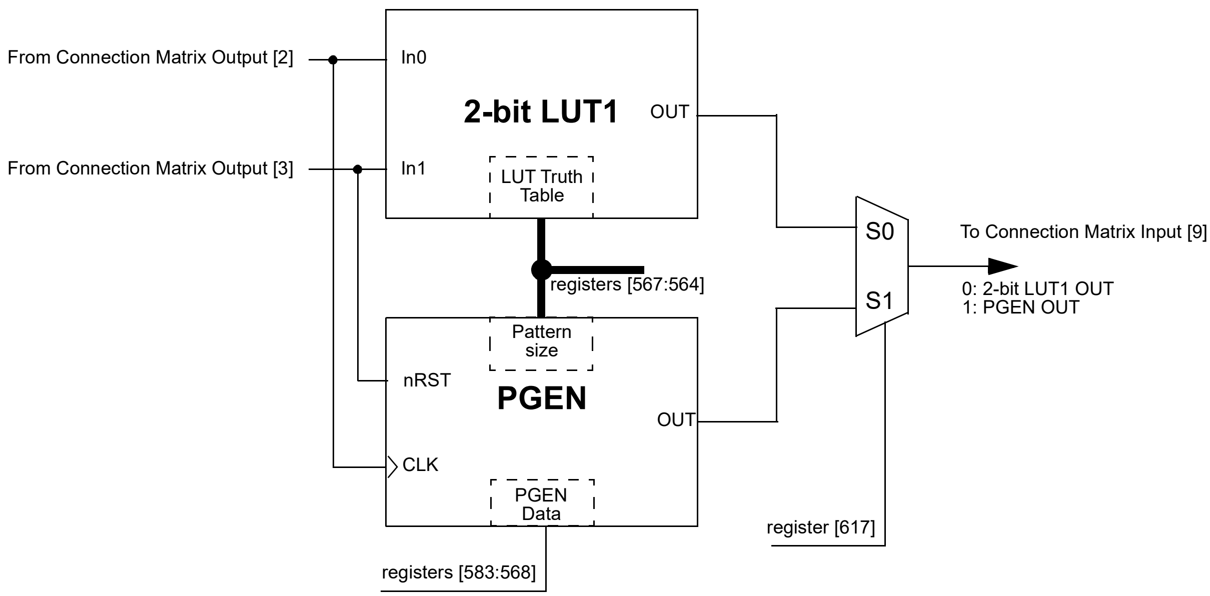


Figure 22: 2-bit LUT1 or PGEN

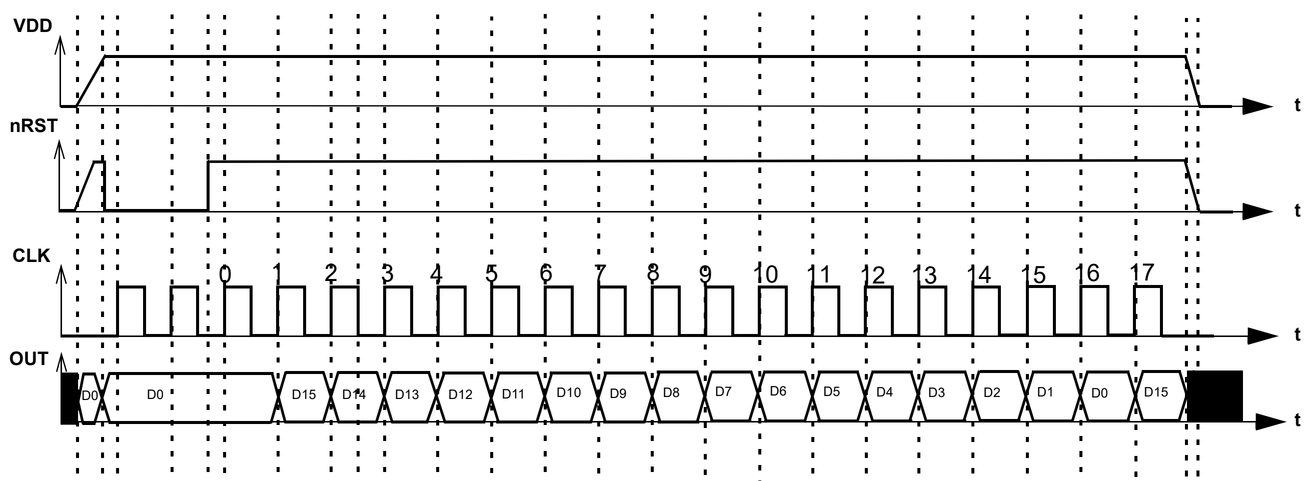


Figure 23: PGEN Timing Diagram

7.2.1 2-Bit LUT or PGEN Macrocell Used as 2-Bit LUT

Table 31: 2-bit LUT1 Truth Table

IN1	IN0	OUT	
0	0	register [564]	LSB
0	1	register [565]	
1	0	register [566]	
1	1	register [567]	MSB

This Macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

2-Bit LUT1 is defined by registers [567:564]

The Table 32 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 2-bit LUT logic cells.

Table 32: 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

7.3 3-BIT LUT OR D FLIP-FLOP WITH SET/RESET MACROCELLS

There are four macrocells that can serve as either 3-bit LUTs or as D Flip Flops with Set/Reset inputs. When used to implement LUT functions, the 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip Flop function, the three input signals from the connection matrix go to the data (D) and clock (CLK) and Set/Reset (nRST/nSET) inputs for the Flip Flop, with the output going back to the connection matrix.

DFF1 functionality is different from the other DFFs. DFF1 operation will flow the functional description below:

- if register [619] = 0, and the CLK is rising edge triggered, then Q=D, otherwise Q will not change
- if register [619] = 1, then data from D is written into the DFF by the rising edge on CLK and output to Q by the falling edge on CLK

Latch: when CLK is Low, then Q = D; otherwise Q remains its previous value (input D has no effect on the output, when CLK is High).

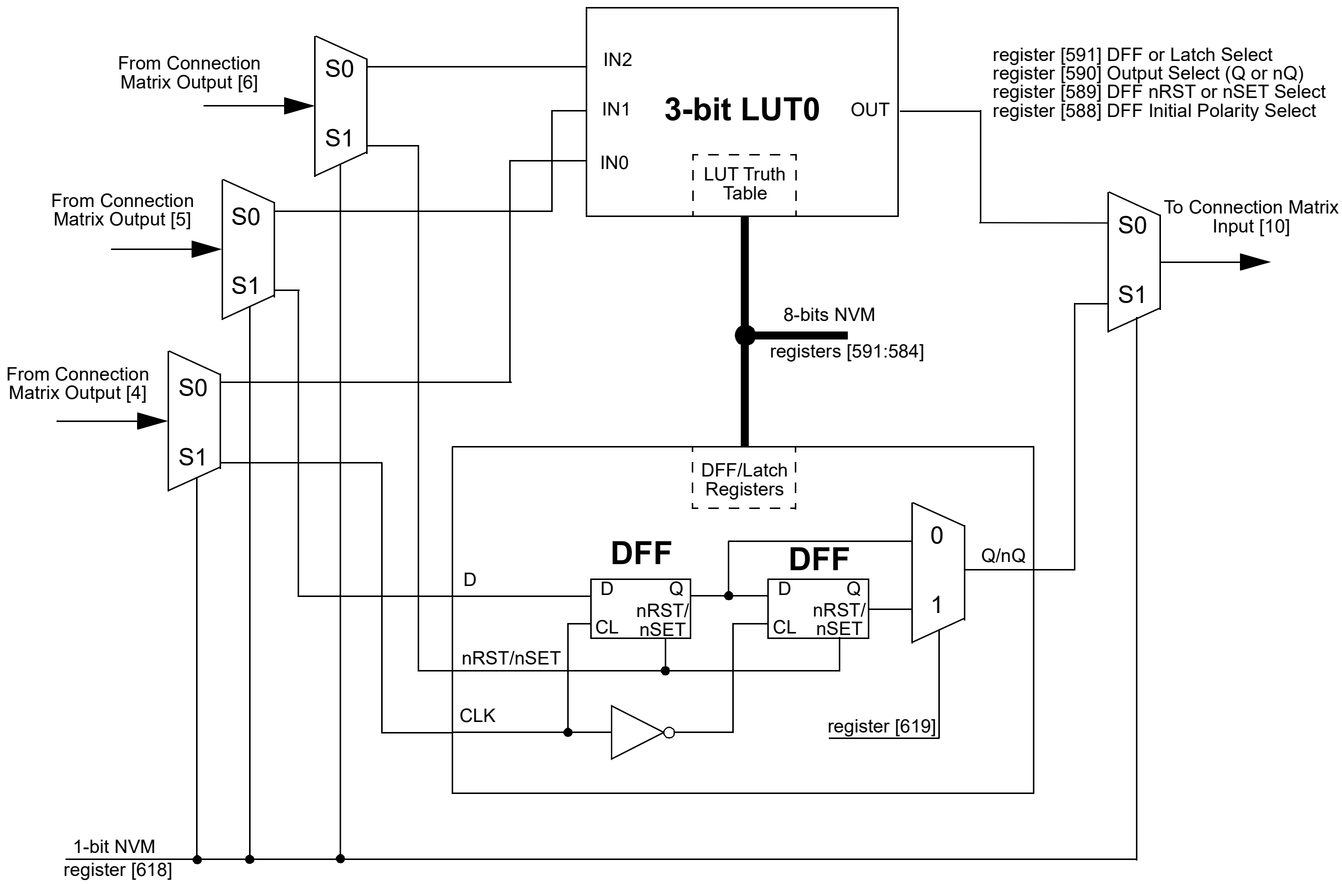


Figure 24: 3-bit LUT0 or DFF1

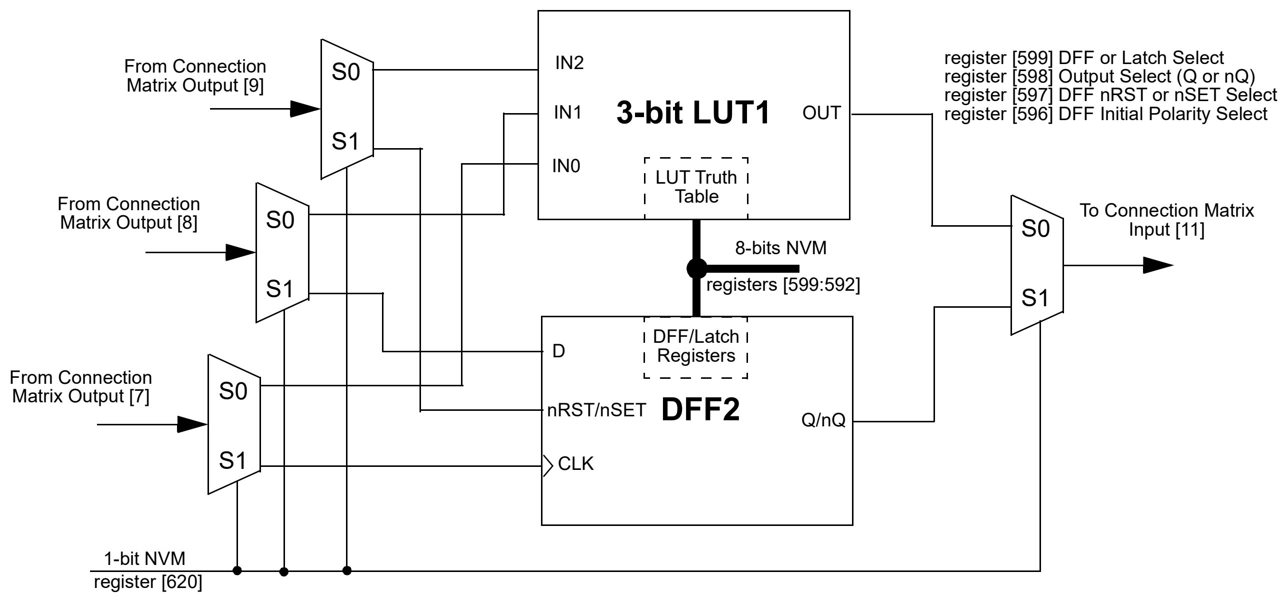


Figure 25: 3-bit LUT1 or DFF2

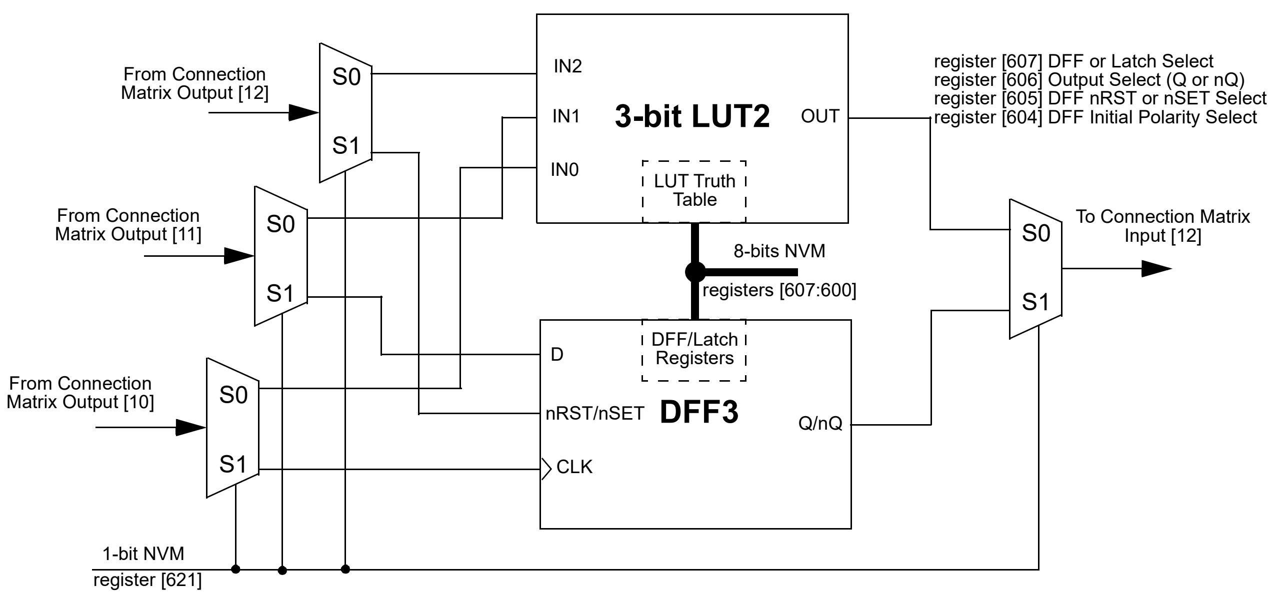


Figure 26: 3-bit LUT2 or DFF3

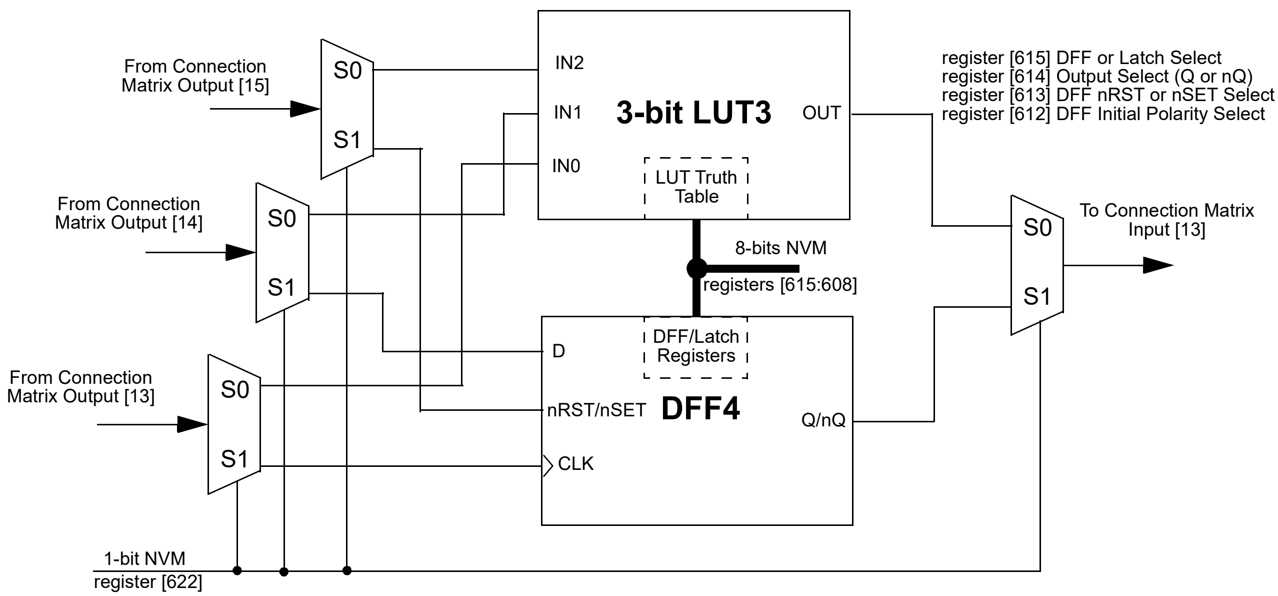


Figure 27: 3-bit LUT3 or DFF4

7.3.1 3-Bit LUT or D Flip-Flop Macrocells Used as 3-Bit LUTs

Table 33: 3-bit LUT0 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [584]	LSB
0	0	1	register [585]	
0	1	0	register [586]	
0	1	1	register [587]	
1	0	0	register [588]	
1	0	1	register [589]	
1	1	0	register [590]	
1	1	1	register [591]	MSB

Table 34: 3-bit LUT1 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [592]	LSB
0	0	1	register [593]	
0	1	0	register [594]	
0	1	1	register [595]	
1	0	0	register [596]	
1	0	1	register [597]	
1	1	0	register [598]	
1	1	1	register [599]	MSB

Table 35: 3-bit LUT2 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [600]	LSB
0	0	1	register [601]	
0	1	0	register [602]	
0	1	1	register [603]	
1	0	0	register [604]	
1	0	1	register [605]	
1	1	0	register [606]	
1	1	1	register [607]	MSB

Table 36: 3-bit LUT3 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [608]	LSB
0	0	1	register [609]	
0	1	0	register [610]	
0	1	1	register [611]	
1	0	0	register [612]	
1	0	1	register [613]	
1	1	0	register [614]	
1	1	1	register [615]	MSB

Each Macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT0 is defined by registers [591:584]

3-Bit LUT1 is defined by registers [599:592]

3-Bit LUT2 is defined by registers [607:600]

3-Bit LUT3 is defined by registers [615:608]

The Table 37 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the four 3-bit LUT logic cells.

Table 37: 3-bit LUT Standard Digital Functions

Function	MSB						LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

7.3.2 Initial Polarity Operations

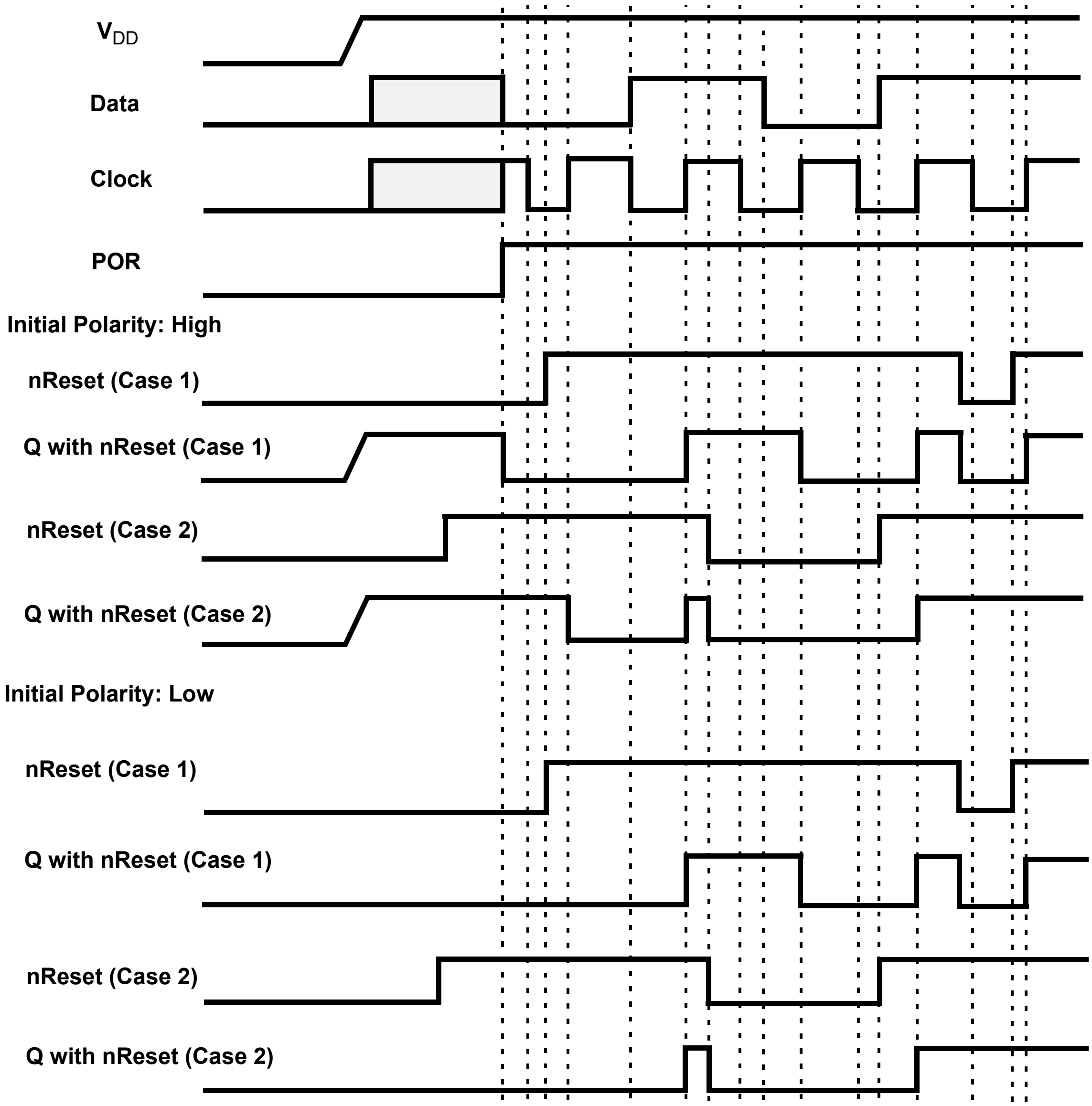


Figure 28: DFF Polarity Operations with nReset

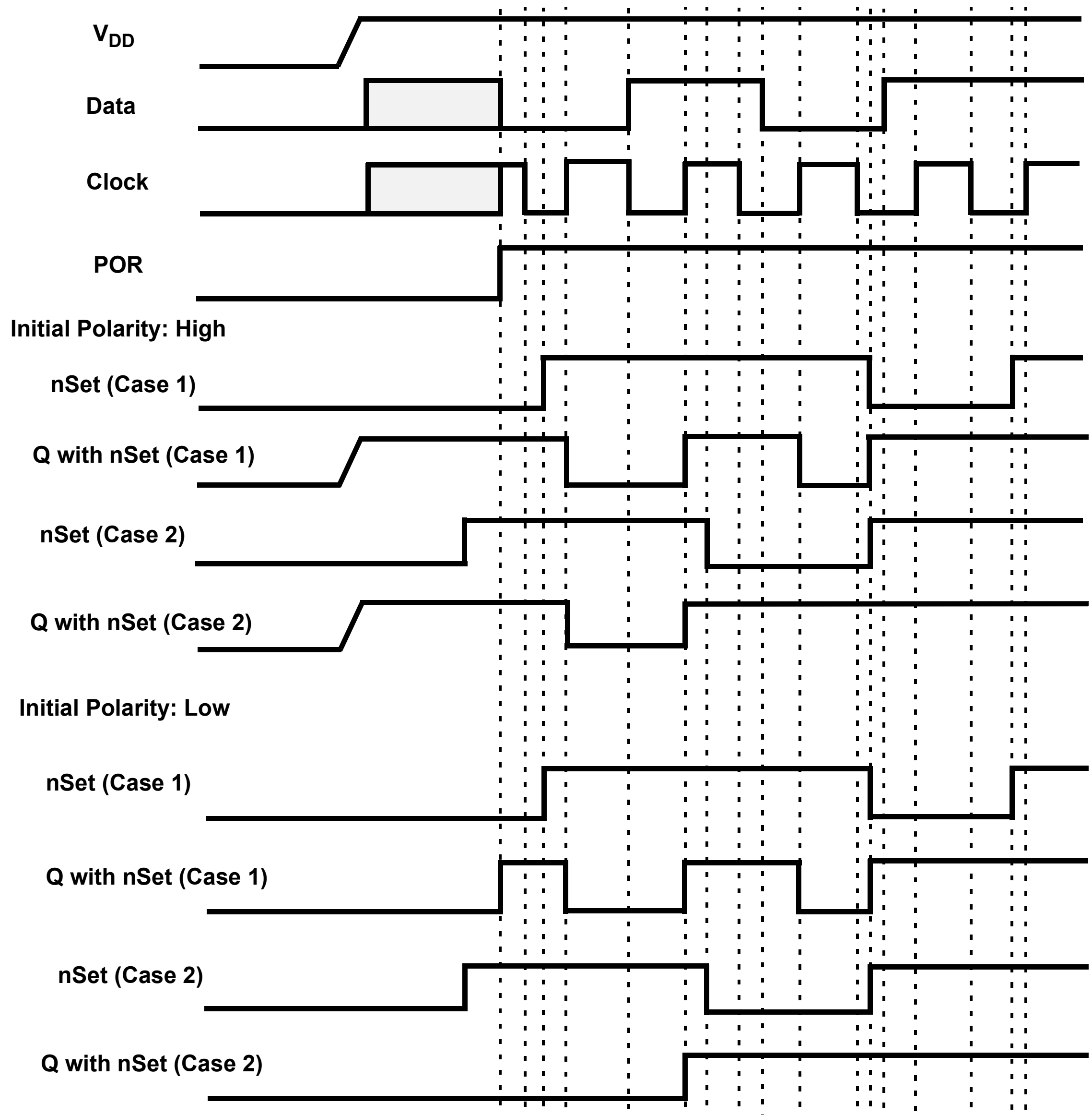


Figure 29: DFF Polarity Operations with nSet

7.4 3-BIT LUT OR PIPE DELAY/RIPPLE COUNTER MACROCELL

There is one macrocell that can serve as either a 3-bit LUT or as a Pipe Delay/Ripple Counter.

When used to implement LUT functions, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix.

When used as a pipe delay, there are three inputs signals from the matrix, Input (IN), Clock (CLK) and Reset (nRST). The pipe delay cell is built from 16 D Flip-Flop logic cells that provide the three delay options, two of which are user selectable. The DFF cells are tied in series where the output (Q) of each delay cell goes to the next DFF cell input (IN). Both of the two outputs (OUT0 and OUT1) provide user selectable options for 1 to 16 stages of delay There are delay output points for each set of the OUT0 and OUT1 outputs to a 4-input mux that is controlled by registers [547:544] for OUT0 and registers [551:548] for OUT1. The 4-input mux is used to control the selection of the amount of delay.

The overall time of the delay is based on the clock used in the SLG46880/81 design. Each DFF cell has a time delay of the inverse of the clock time (either external clock or the Oscillator within the SLG46880/81). The sum of the number of DFF cells used will be the total time delay of the Pipe Delay logic cell. OUT1 Output can be inverted (as selected by register [552]).

In the Ripple Counter mode there are 3 options for setting, which use 7 bits. There are 3 bits to set **nSET value (SV)** in range from 0 to 7. It is a value, which will be set into the Ripple Counter outputs when nSET input goes LOW. **End value (EV)** will use 3 bits for setting outputs code, which will be last code in the cycle. After reaching the EV, the Ripple Counter goes to the first code by the rising edge on CLK input. The **Functionality mode** option uses 1 bit. This setting defines how exactly Ripple Counter will operate.

The user can select one of the functionality modes by register: RANGE or FULL. If the RANGE option is selected, the count starts from SV. If UP input is LOW the count goes down: SV→EV→EV-1….SV+1→SV etc (if SV is smaller than EV) or SV→SV-1….EV+1→EV→SV (if SV is bigger than EV). If UP input is HIGH, count starts from SV up to EV etc.

In the FULL range configuration the Ripple Counter functions as follows. If UP input is LOW, the count starts from SV and goes down to 0. Then current counter value jumps to EV and goes down to 0 etc.

If UP input is HIGH, count goes up starting from SV. Then current counter value jumps to 0 and counts up to EV etc. see Ripple counter functionality example in Figure 31.

Every step is executed by the rising edge on CLK input.

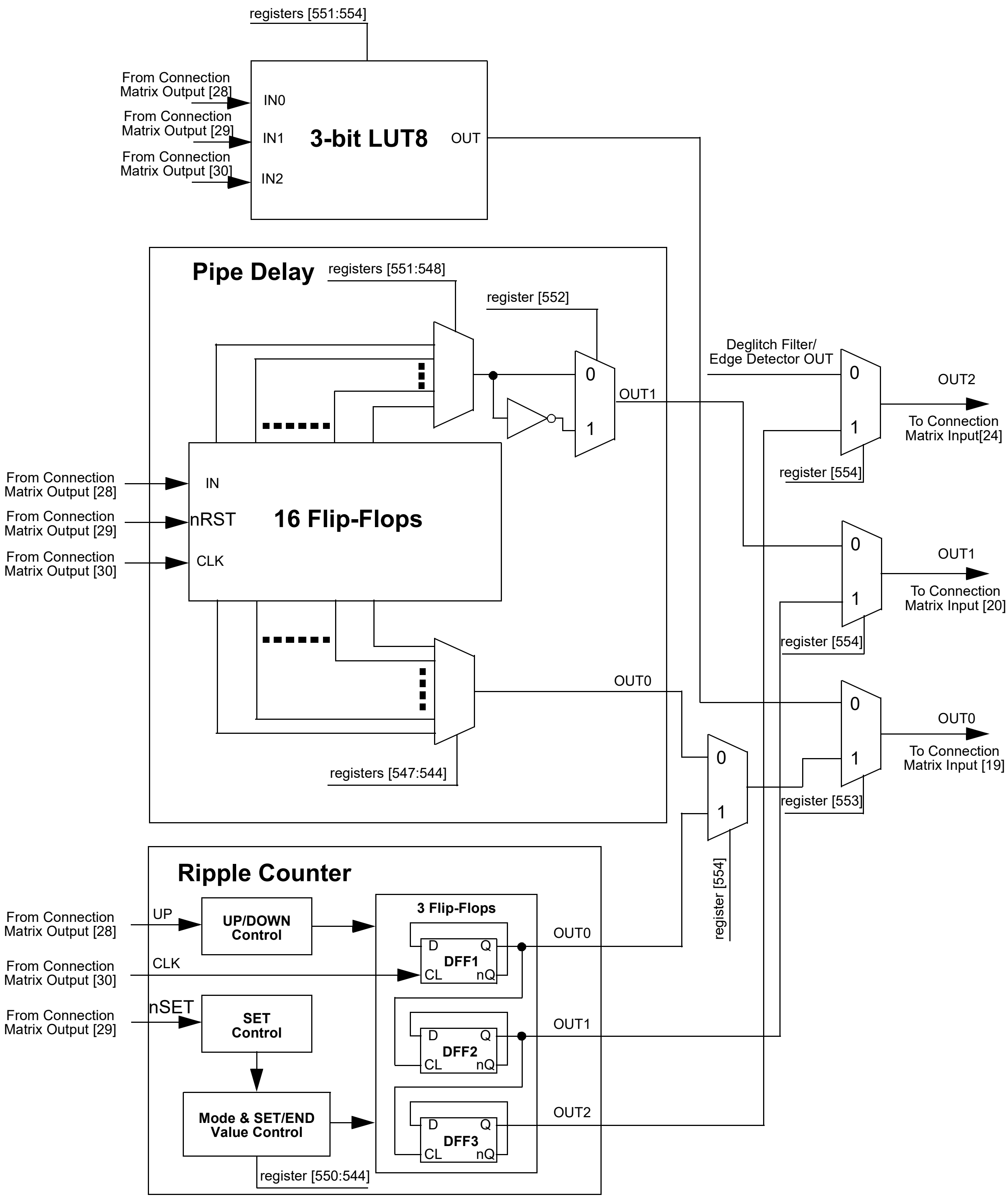


Figure 30: 3-bit LUT8/Pipe Delay/Ripple Counter

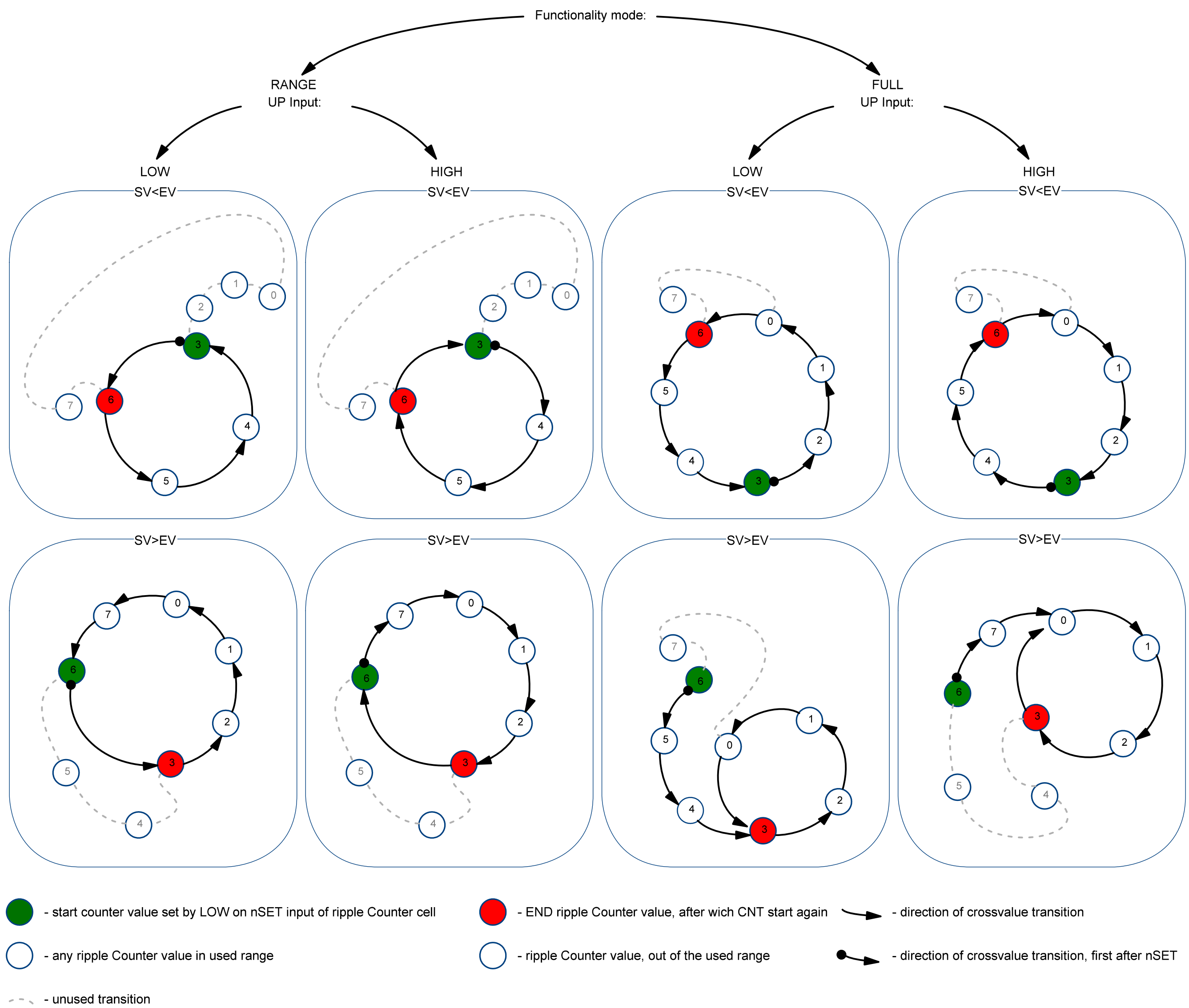


Figure 31: Example: Ripple Counter Functionality

7.4.1 3-Bit LUT or Pipe Delay Macrocells Used as 3-Bit LUT

Table 38: 3-bit LUT6 Truth Table

IN2	IN1	IN0	OUT
0	0	0	register [544]
0	0	1	register [545]
0	1	0	register [546]
0	1	1	register [547]
1	0	0	register [548]
1	0	1	register [549]
1	1	0	register [550]
1	1	1	register [551]

Each Macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT8 is defined by registers [551:544]

7.5 3-BIT LUT OR 8-BIT COUNTER/DELAY MACROCELLS

There are four macrocells that can serve as either 3-bit LUTs or as Counter/Delays. When used to implement LUT function, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used to implement 8-Bit Counter/Delay function, two of the three input signals from the connection matrix go to the external clock (ext_CLK) and reset (DLY_in/CNT_Reset) inputs for the counter/delay, with the output going back to the connection matrix.

Counter/Delay macrocell has an initial value, which define its initial value after GPAK is powered up. It is possible to select initial Low or initial High, as well as initial value defined by a Delay In signal.

For example, in case initial LOW option is used, the rising edge delay will start operation.

These macrocells can also operate in a frequency detection mode.

Delay time and Output Period can be calculated using the following formulas:

- Delay time: [(Counter data + 2)/CLK input frequency – Offset (Note)]
- Output Period: [(Counter data + 1)/CLK input frequency – Offset (Note)]

One Shot pulse width can be calculated using formula:

- Pulse width = [(Counter Data + 2)/CLK input frequency – Offset (Note)]

Note: Offset is the asynchronous time offset between the input signal and the first clock pulse.

Three of the four macrocells can have their active count value read via I^2C (CNT0, CNT2 and CNT4). See Section 19.4.6.3 for further details.

7.5.1 3-Bit LUT or 8-Bit CNT/DLY Block Diagrams

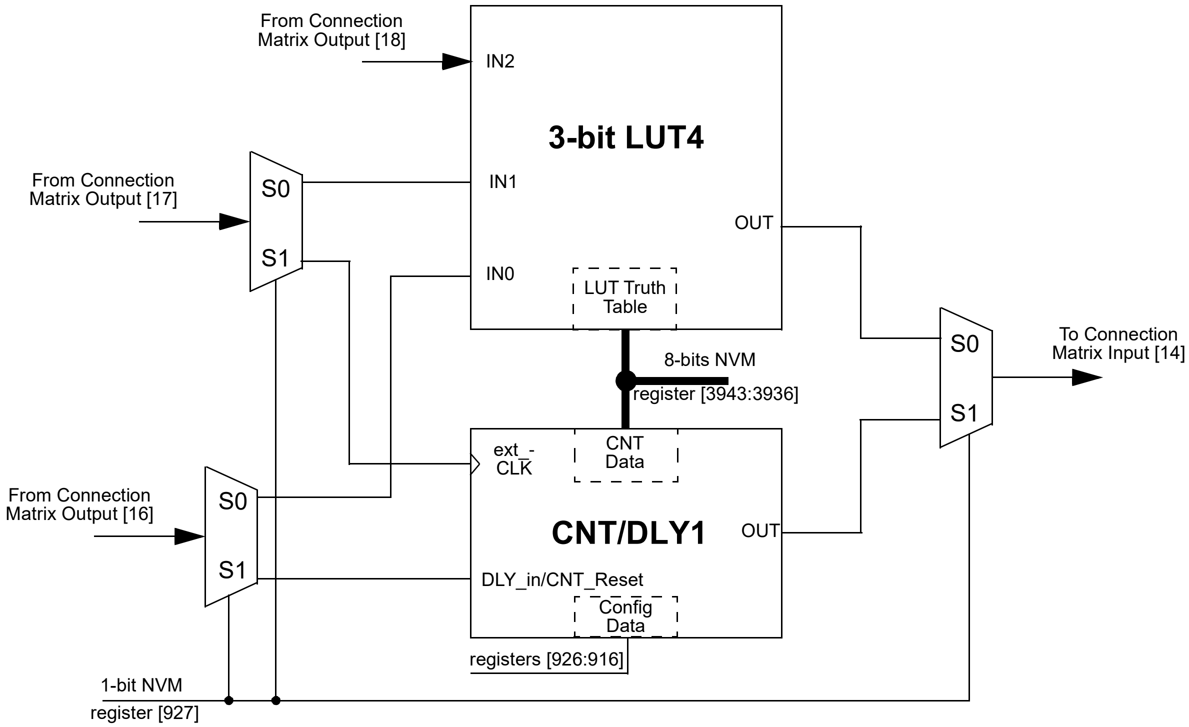


Figure 32: 3-bit LUT4 or CNT/DLY1

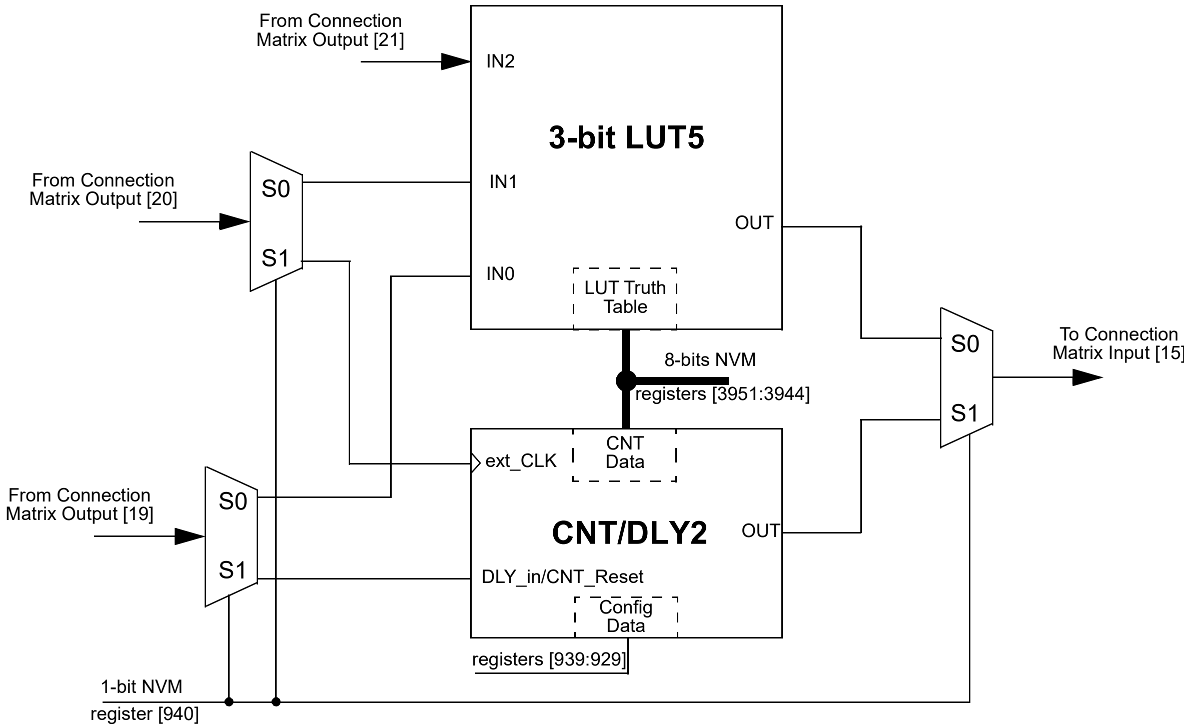


Figure 33: 3-bit LUT5 or CNT/DLY2

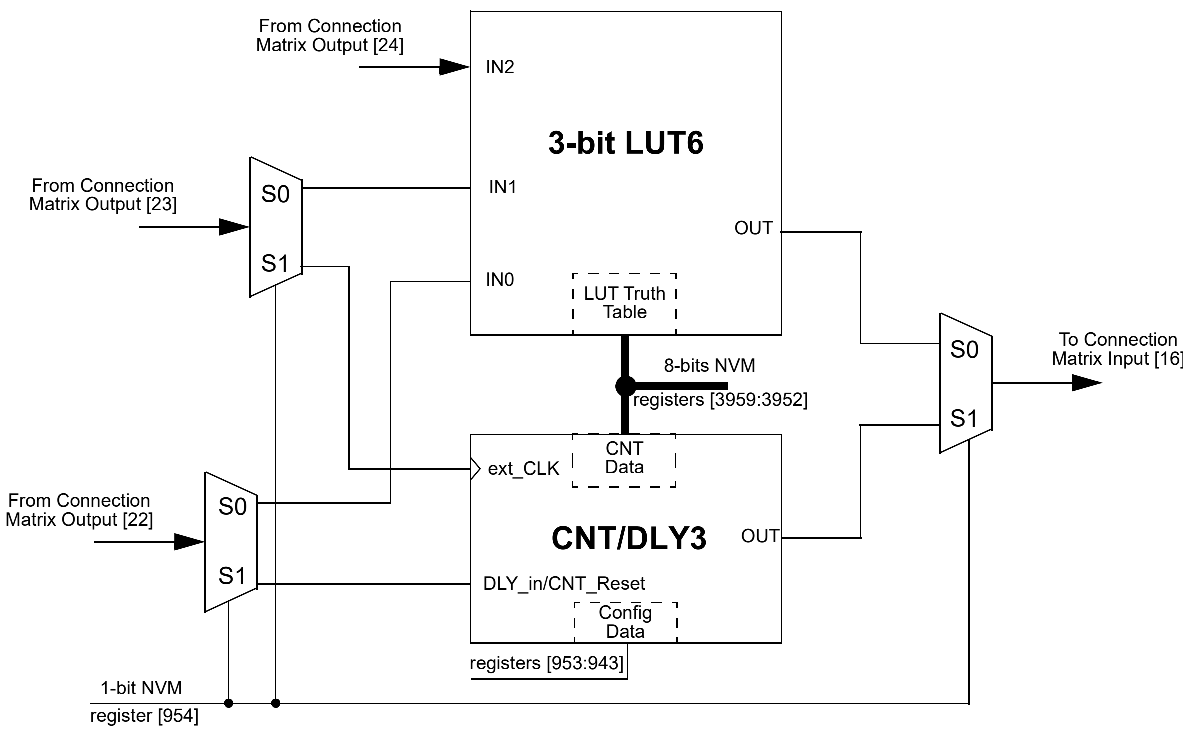


Figure 34: 3-bit LUT6 or CNT/DLY3

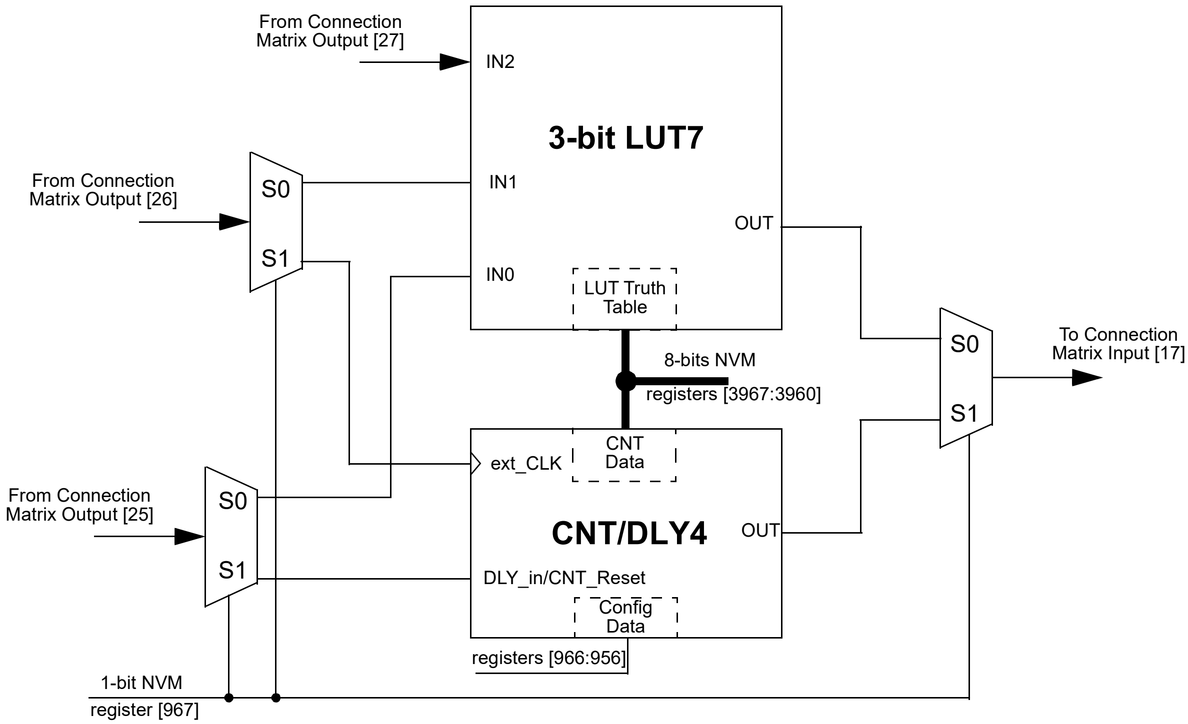


Figure 35: 3-bit LUT7 or CNT/DLY4

7.5.2 3-Bit LUT or CNT/DLYs Used as 3-Bit LUTs

Table 39: 3-bit LUT4 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [3936]	LSB
0	0	1	register [3937]	
0	1	0	register [3938]	
0	1	1	register [3939]	
1	0	0	register [3940]	
1	0	1	register [3941]	
1	1	0	register [3942]	
1	1	1	register [3943]	MSB

Table 40: 3-bit LUT5 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [3944]	LSB
0	0	1	register [3945]	
0	1	0	register [3946]	
0	1	1	register [3947]	
1	0	0	register [3948]	
1	0	1	register [3949]	
1	1	0	register [3950]	
1	1	1	register [3951]	MSB

Table 41: 3-bit LUT6 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [3952]	LSB
0	0	1	register [3953]	
0	1	0	register [3954]	
0	1	1	register [3955]	
1	0	0	register [3956]	
1	0	1	register [3957]	
1	1	0	register [3958]	
1	1	1	register [3959]	MSB

Table 42: 3-bit LUT7 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [3960]	LSB
0	0	1	register [3961]	
0	1	0	register [3962]	
0	1	1	register [3963]	
1	0	0	register [3964]	
1	0	1	register [3965]	
1	1	0	register [3966]	
1	1	1	register [3967]	MSB

Each Macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT4 is defined by registers [3943:3936]

3-Bit LUT5 is defined by registers [3951:3944]

3-Bit LUT6 is defined by registers [3959:3952]

3-Bit LUT7 is defined by registers [3967:3960]

7.6 CNT/DLY/FSM TIMING DIAGRAMS

7.6.1 Delay mode (Edge Select: Both, Counter Data: 3) CNT/DLY2...CNT/DLY6

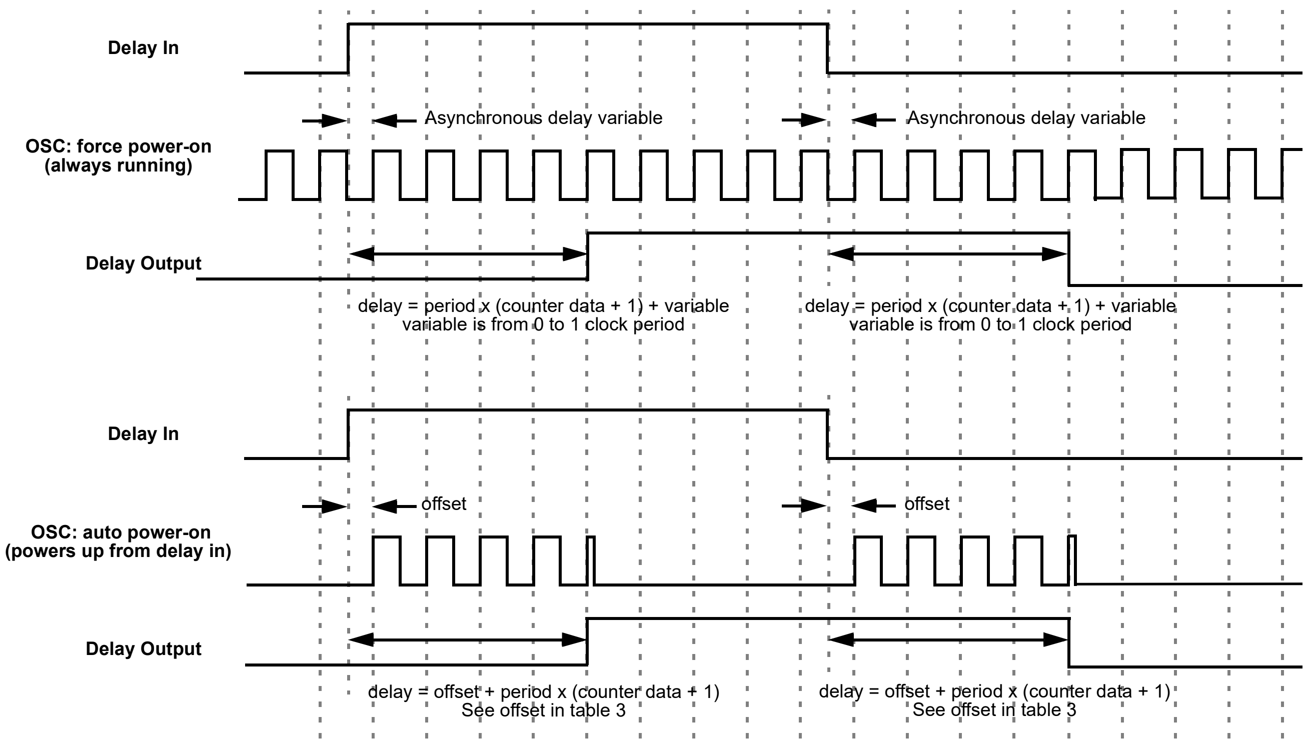


Figure 36: Delay Mode Timing Diagram

7.6.2 Count mode (Count Data: 3), Counter Reset (Rising Edge Detect) CNT/DLY2...CNT/DLY6

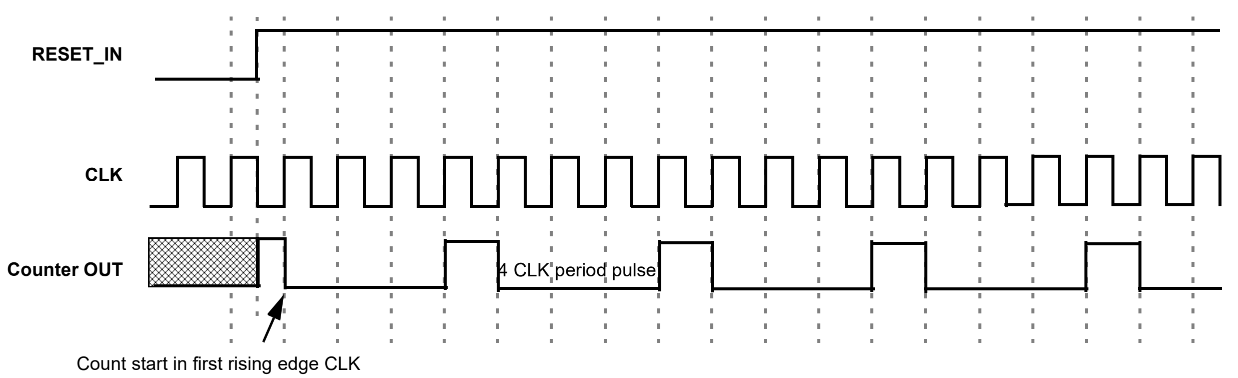


Figure 37: Counter Mode Timing Diagram without two DFFs Synced up

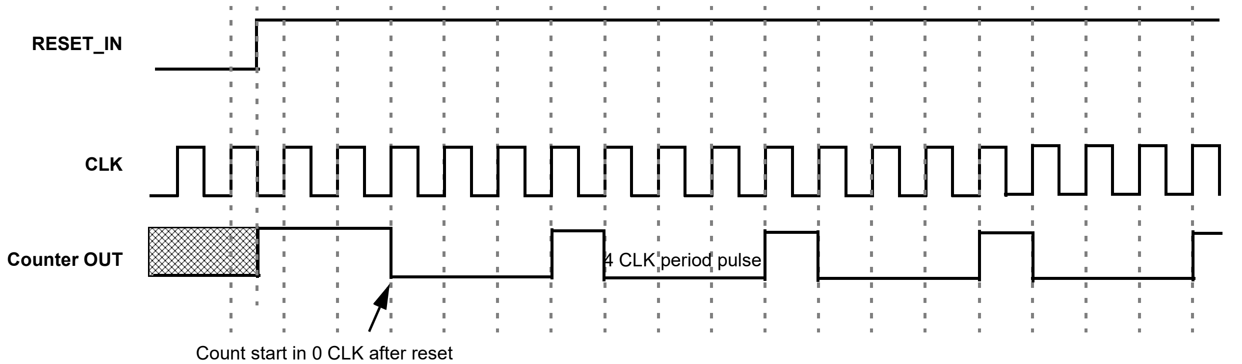


Figure 38: Counter Mode Timing Diagram with two DFFs Synced up

7.6.3 One-Shot Mode CNT/DLY0 to CNT/DLY6

This macrocell will generate a pulse whenever a selected edge is detected on its input. Register bits set the edge selection. The pulse width determines by counter data and clock selection properties. The output pulse polarity (non-inverted or inverted) is selected by register bit. Any incoming edges will be ignored during the pulse width generation. The following diagram shows one-shot function for non-inverted output.

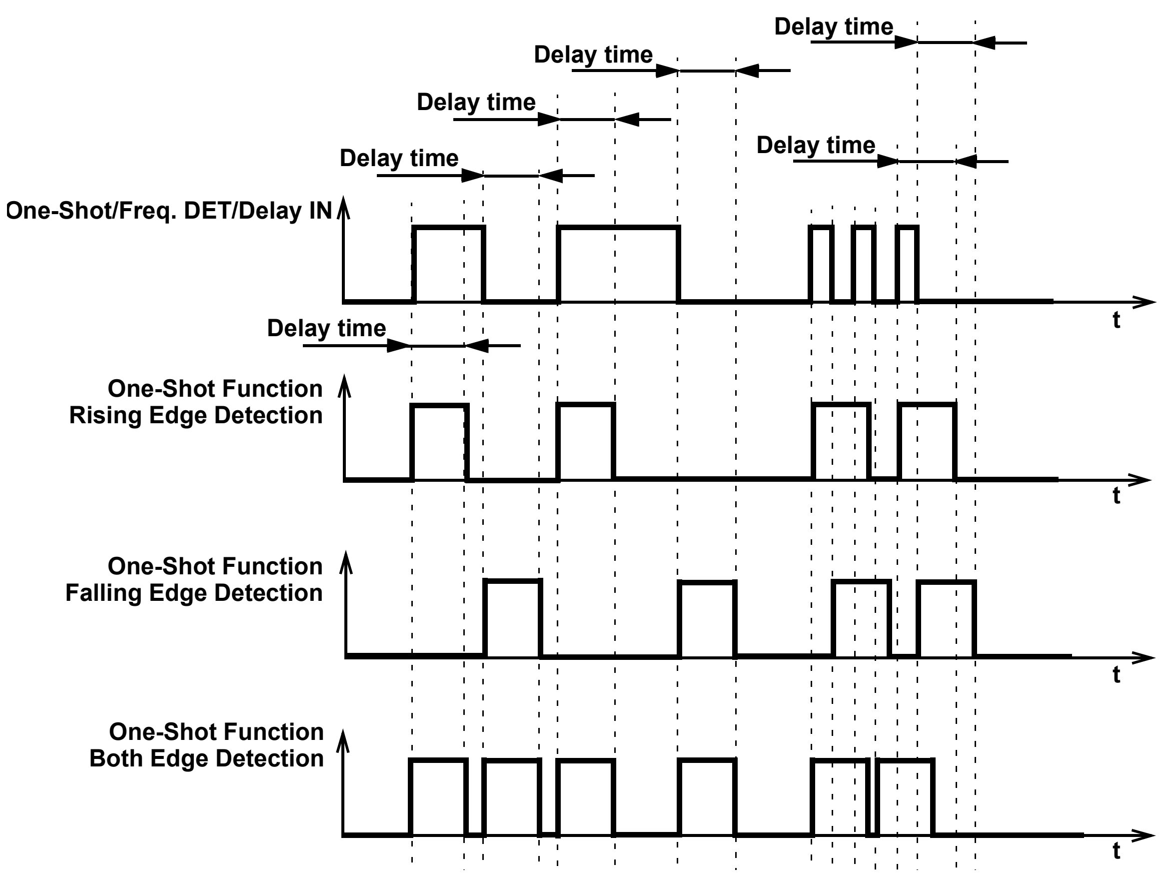


Figure 39: One-Shot Function Timing Diagram

This macrocell generates a high level pulse with a set width (defined by counter data) when detecting the respective edge. It does not restart while pulse is high.

7.6.4 Frequency Detection Mode CNT/DLY0...CNT/DLY6

Rising Edge: The output goes high if the time between two successive edges is less than the delay. The output goes low if the second rising edge has not come after the last rising edge in specified time.

Falling Edge: The output goes high if the time between two falling edges is less than the set time. The output goes low if the second falling edge has not come after the last falling edge in specified time.

Both Edge: The output goes high if the time between the rising and falling edges is less than the set time, which is equivalent to the length of the pulse. The output goes low if after the last rising/falling edge and specified time, the second edge has not come.

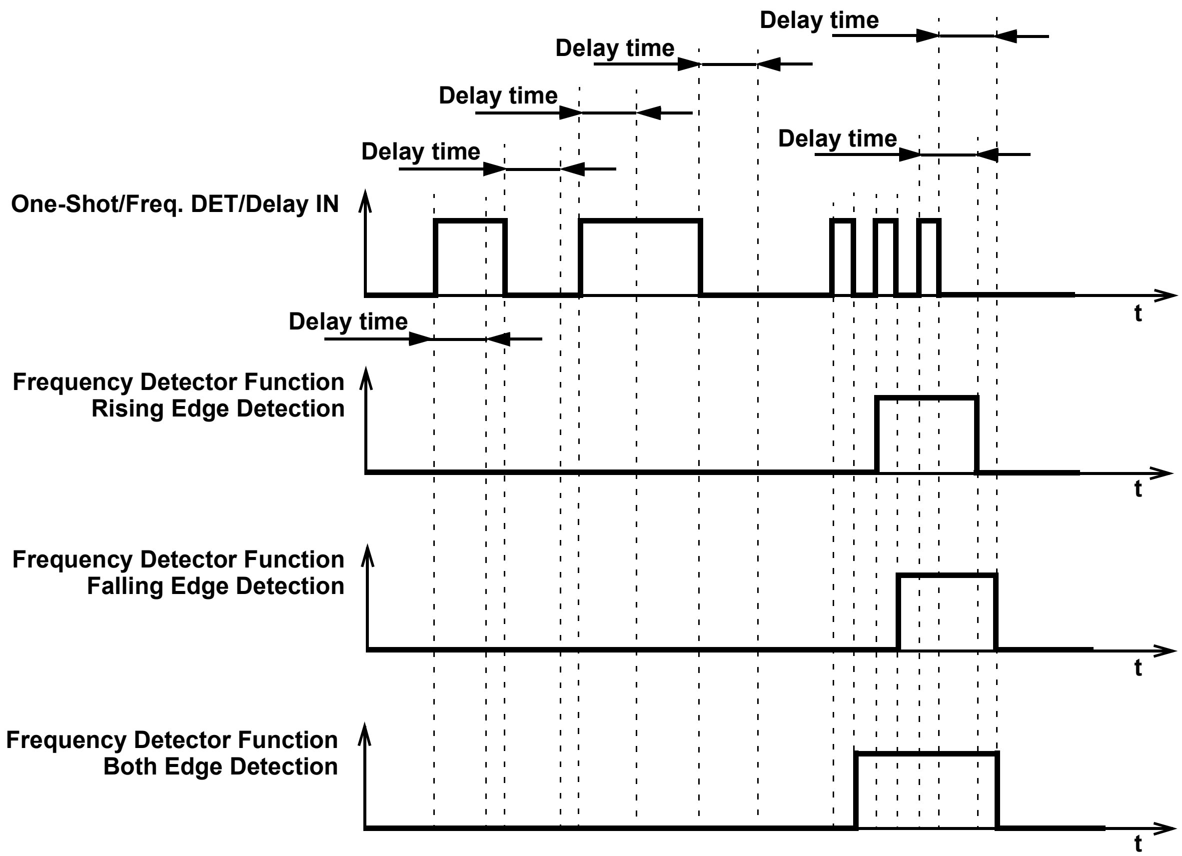


Figure 40: Frequency Detection Mode Timing Diagram

7.6.5 Edge Detection Mode CNT/DLY2...CNT/DLY6

The macrocell generates high level short pulse when detecting the respective edge. See Table 11.

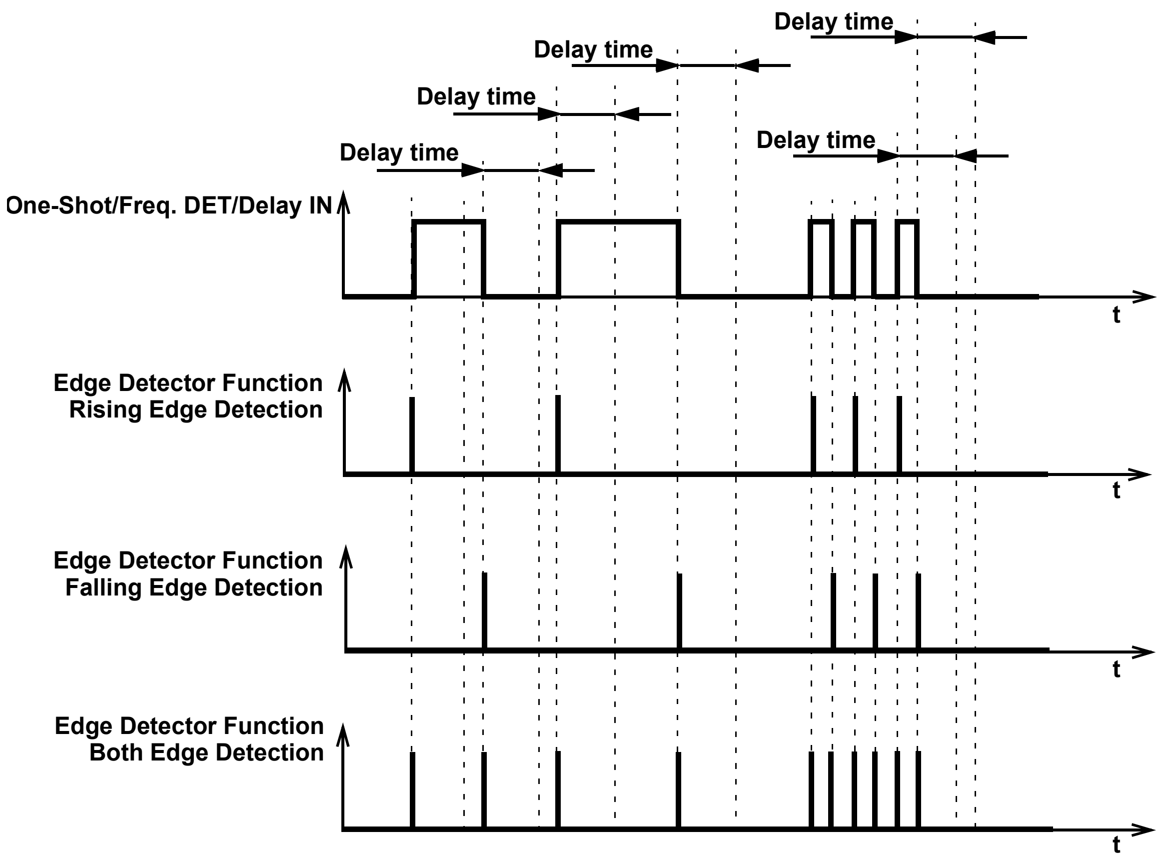


Figure 41: Edge Detection Mode Timing Diagram

7.6.5.1 Delayed Edge Detection Mode

In Delayed Edge Detection Mode, High level short pulses are generated on the macrocell output after the configured delay time if the corresponding edge was detected on the input.

If the input signal is changed during the set delay time, the pulse will not be generated. See Figure 42

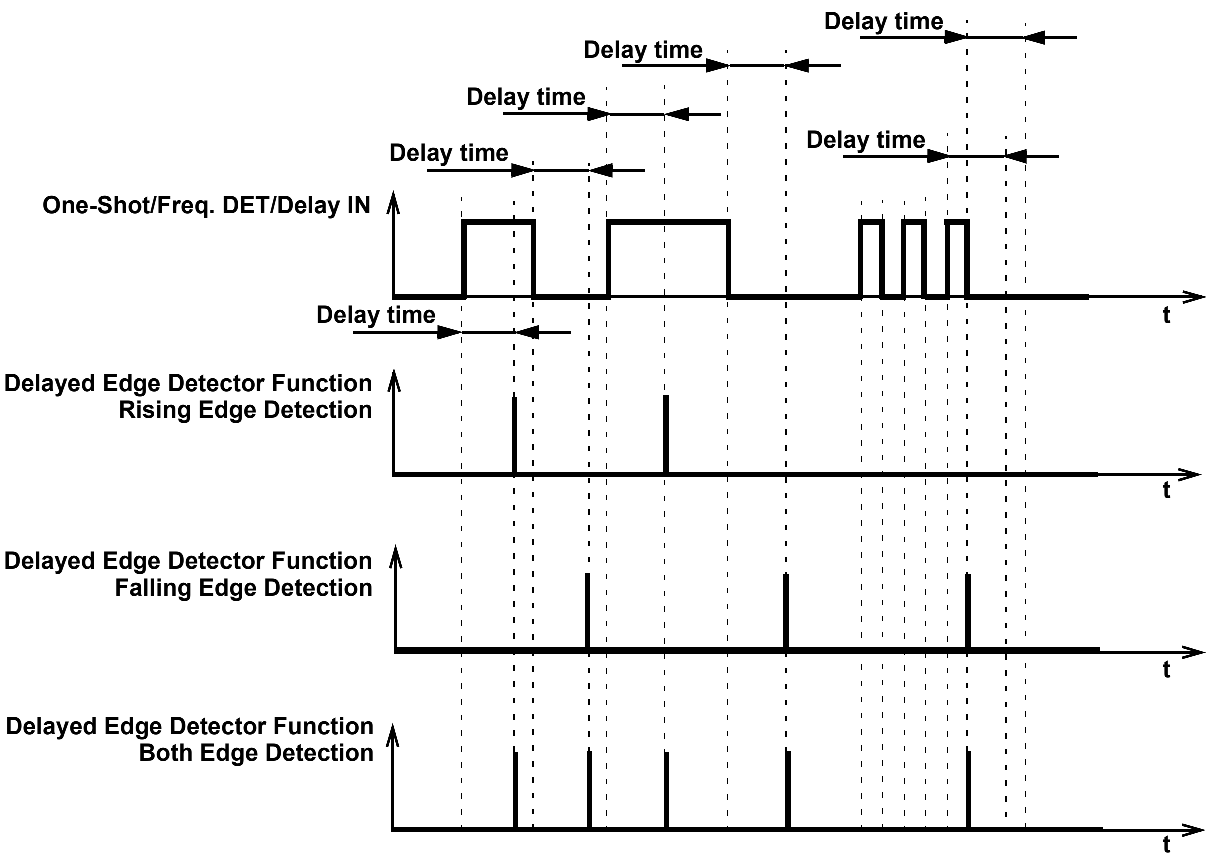


Figure 42: Delayed Edge Detection Mode

7.6.6 Delay Mode CNT/DLY0...CNT/DLY6

The macrocell shifts the respective edge to a set time and restarts by appropriate edge. It works as a filter if the input signal is shorter than the delay time.

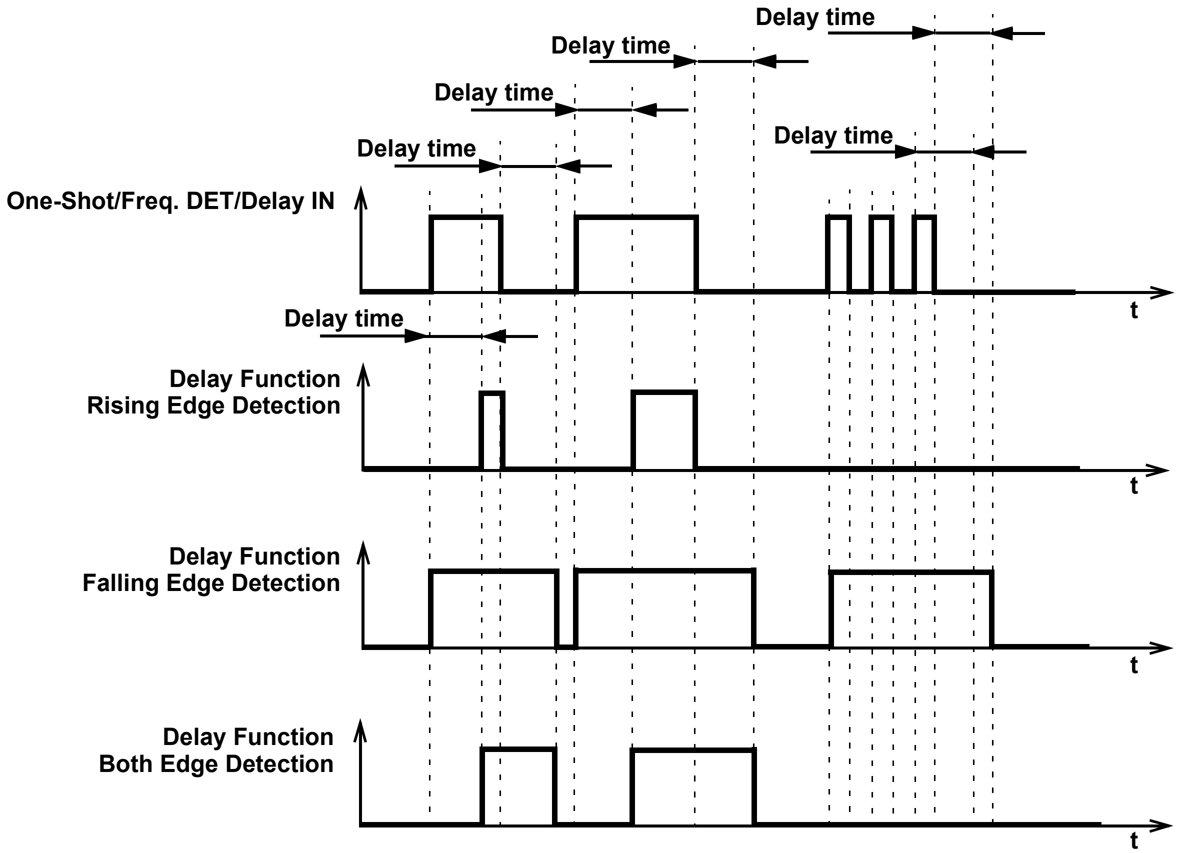


Figure 43: Delay Mode Timing Diagram

7.6.7 CNT/FSM Mode CNT/DLY0, CNT/DLY1

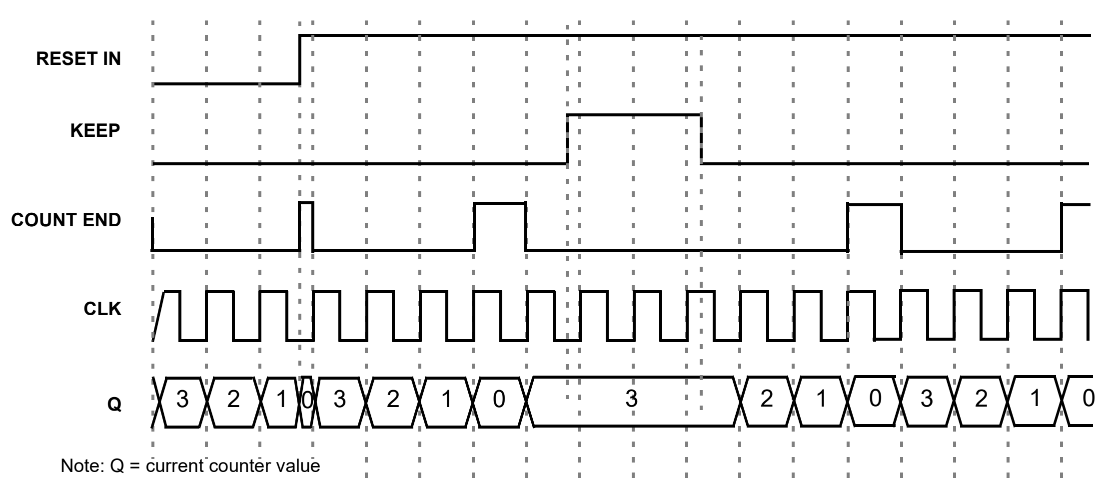


Figure 44: CNT/FSM Timing Diagram (Reset Rising Edge Mode, Oscillator is Forced On, UP=0) for Counter Data = 3

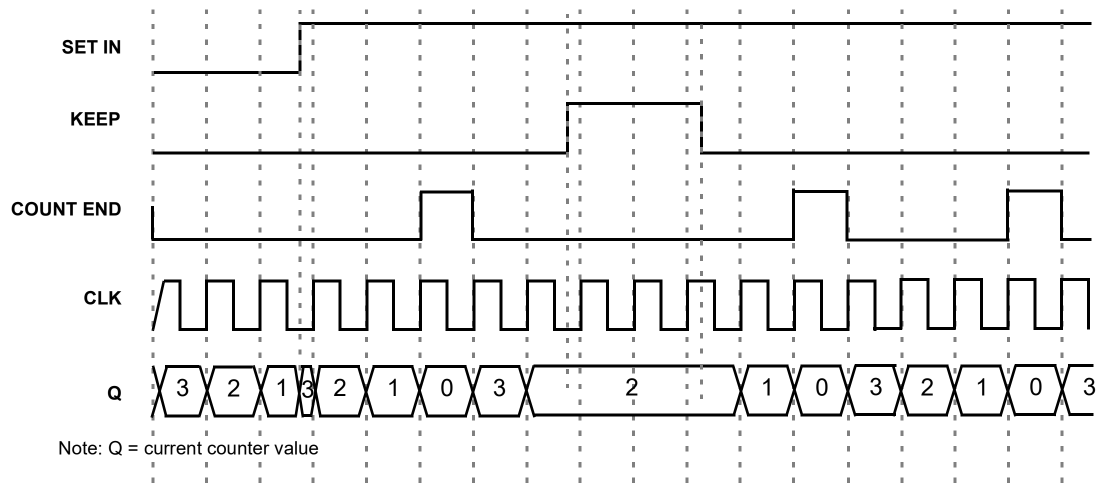


Figure 45: CNT/FSM Timing Diagram (Set Rising Edge Mode, Oscillator is Forced On, UP=0) for Counter Data = 3

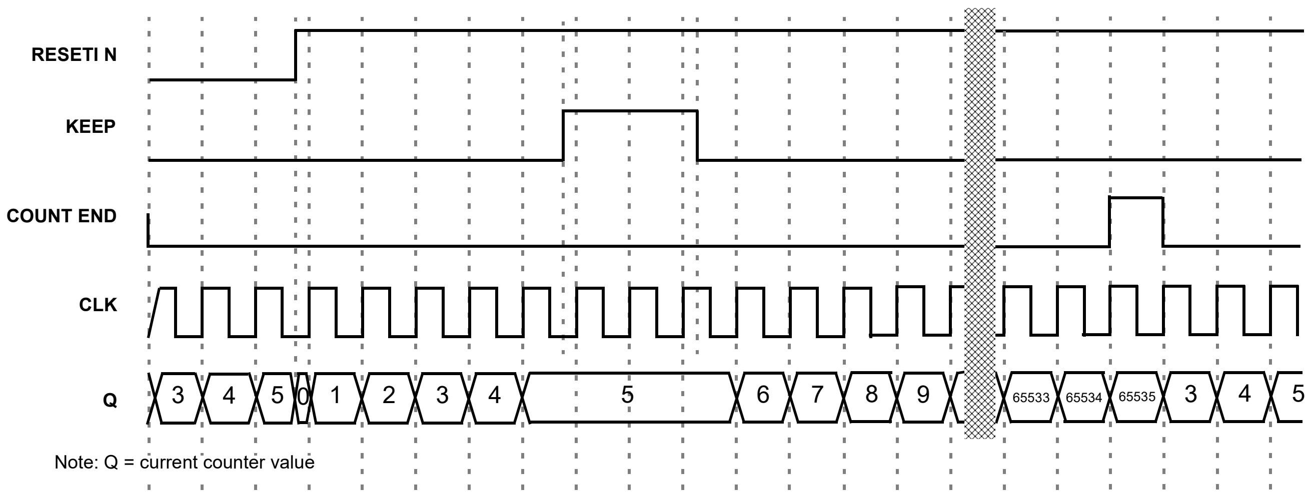


Figure 46: CNT/FSM Timing Diagram (Reset Rising Edge Mode, Oscillator is Forced On, UP=1) for Counter Data = 3

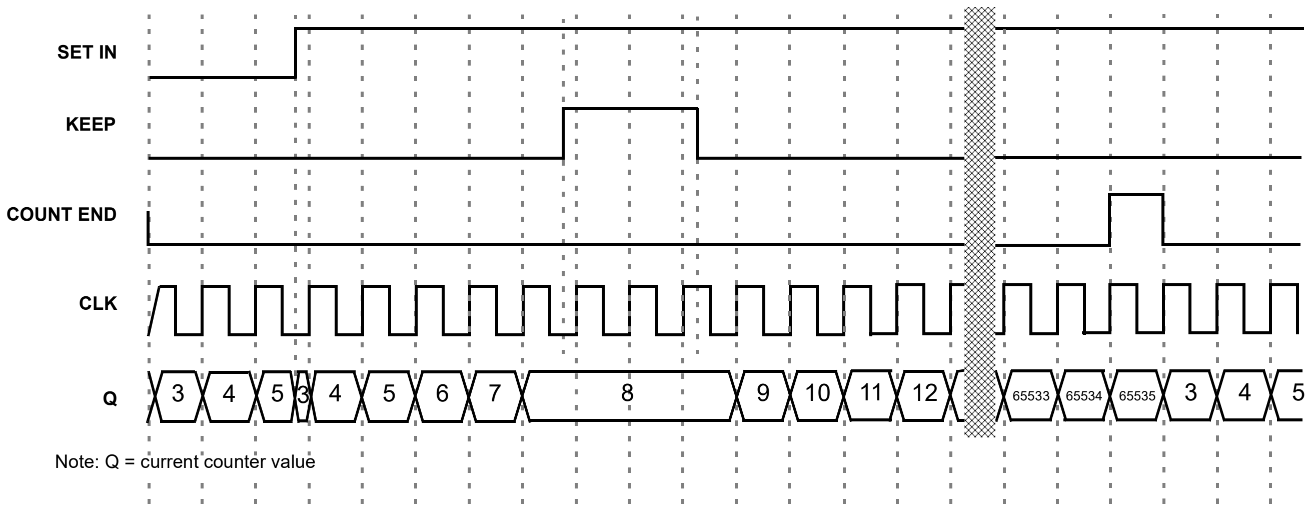


Figure 47: CNT/FSM Timing Diagram (Set Rising Edge Mode, Oscillator is Forced On, UP=1) for Counter Data = 3

7.6.8 Difference in Counter Value for Counter, Delay, One-Shot and Frequency Detect Modes

There is a difference in counter value for Counter and Delay/One-Shot/Frequency Detect modes. The counter value is shifted for two rising edges of the clock signal in Delay/One-Shot/Frequency Detect modes compared to Counter mode. See Figure 48

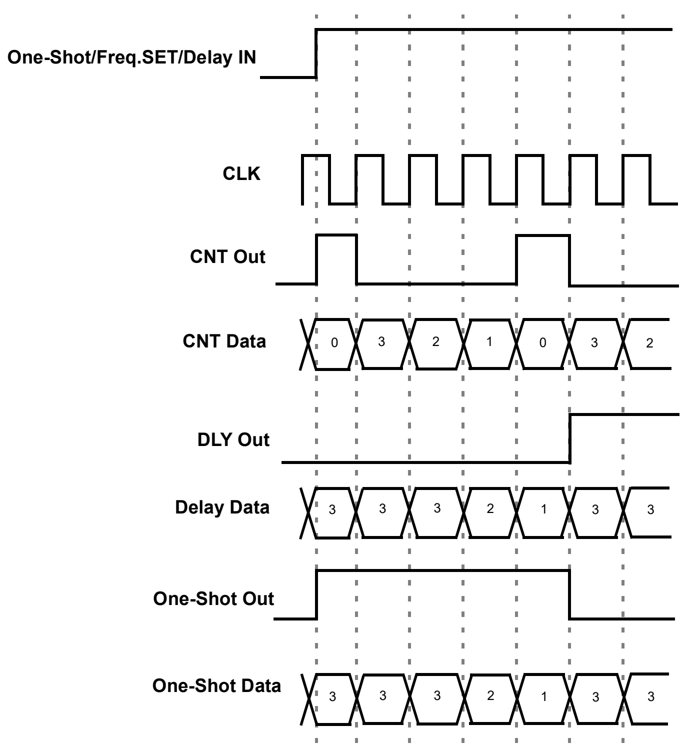


Figure 48: Counter Value, Counter Data = 3

7.7 4-BIT LUT OR 16-BIT COUNTER/DELAY MACROCELL

There is one macrocell that can serve as either 4-bit LUT or as 16-bit Counter/Delay. When used to implement LUT function, the 4-bit LUT takes in four input signals from the Connection Matrix and produces a single output, which goes back into the Connection Matrix. When used to implement 16-Bit Counter/Delay function, two of the four input signals from the connection matrix go to the external clock (ext_CLK) and reset (DLY_in/CNT_Reset) for the counter/delay, with the output going back to the connection matrix.

This macrocell has an optional Finite State Machine (FSM) function. There are two additional matrix inputs for Up and Keep to support FSM functionality.

This macrocell can also operate in a one-shot mode, which will generate an output pulse of user-defined width.

This macrocell can also operate in a frequency detection or edge detection mode.

This macrocell can have its active count value read via I^2C. See Section 19.4.6.3 for further details.

7.7.1 4-Bit LUT or 16-Bit CNT/DLY Block Diagram

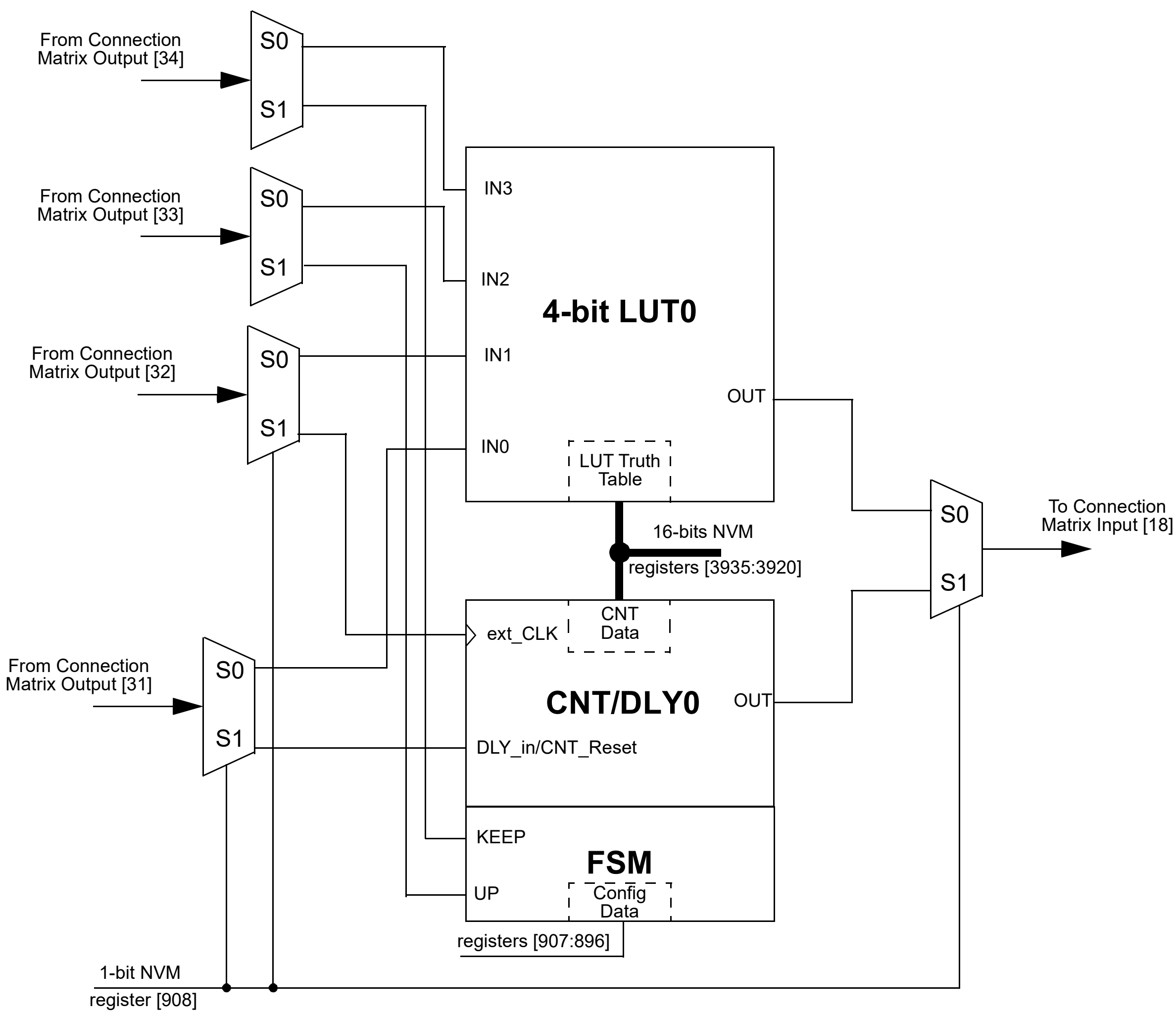


Figure 49: 4-bit LUT0 or CNT/DLY0

7.7.2 4-Bit LUT or 16-Bit Counter/Delay Macrocells Used as 4-Bit LUTs

Table 43: 4-bit LUT0 Truth Table

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	register [3920]	LSB
0	0	0	1	register [3921]	
0	0	1	0	register [3922]	
0	0	1	1	register [3923]	
0	1	0	0	register [3924]	
0	1	0	1	register [3925]	
0	1	1	0	register [3926]	
0	1	1	1	register [3927]	
1	0	0	0	register [3928]	
1	0	0	1	register [3929]	
1	0	1	0	register [3930]	
1	0	1	1	register [3931]	
1	1	0	0	register [3932]	
1	1	0	1	register [3933]	
1	1	1	0	register [3934]	
1	1	1	1	register [3935]	MSB

This Macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

4-Bit LUT0 is defined by registers [3935:3920]

Table 44: 4-bit LUT Standard Digital Functions

Function	MSB														LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1

7.8 WAKE AND SLEEP CONTROLLER

The SLG46880/81 has a Wake and Sleep (WS) function for ACMP0H and ACMP1H. The microcell CNT/DLY0 can be reconfigured for this purpose registers [897:896]=11 and register [910]=1. The WS serves for power saving, it allows to switch on and off selected ACMPs on selected bit of 16-bit counter.

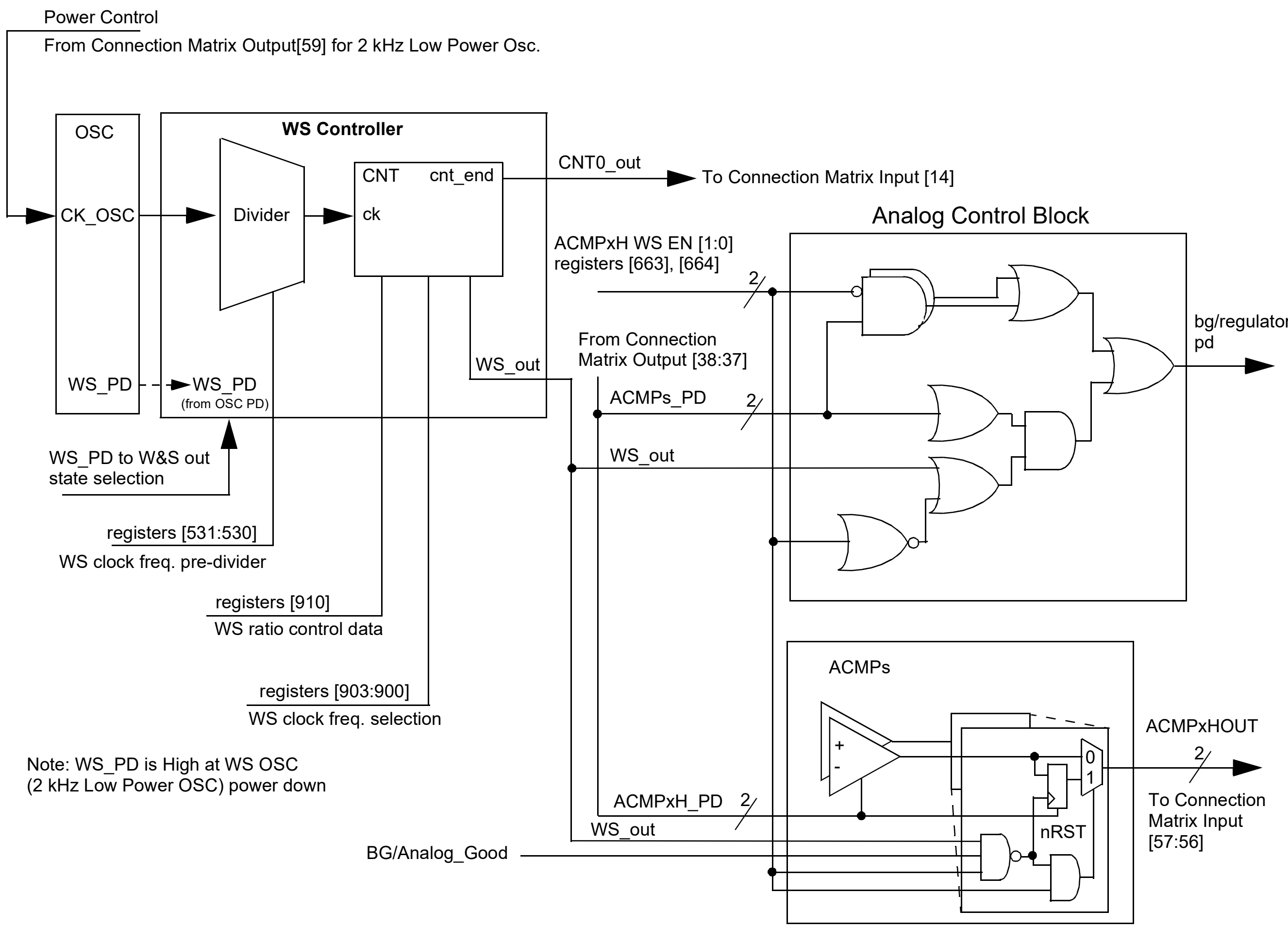


Figure 50: WS Controller

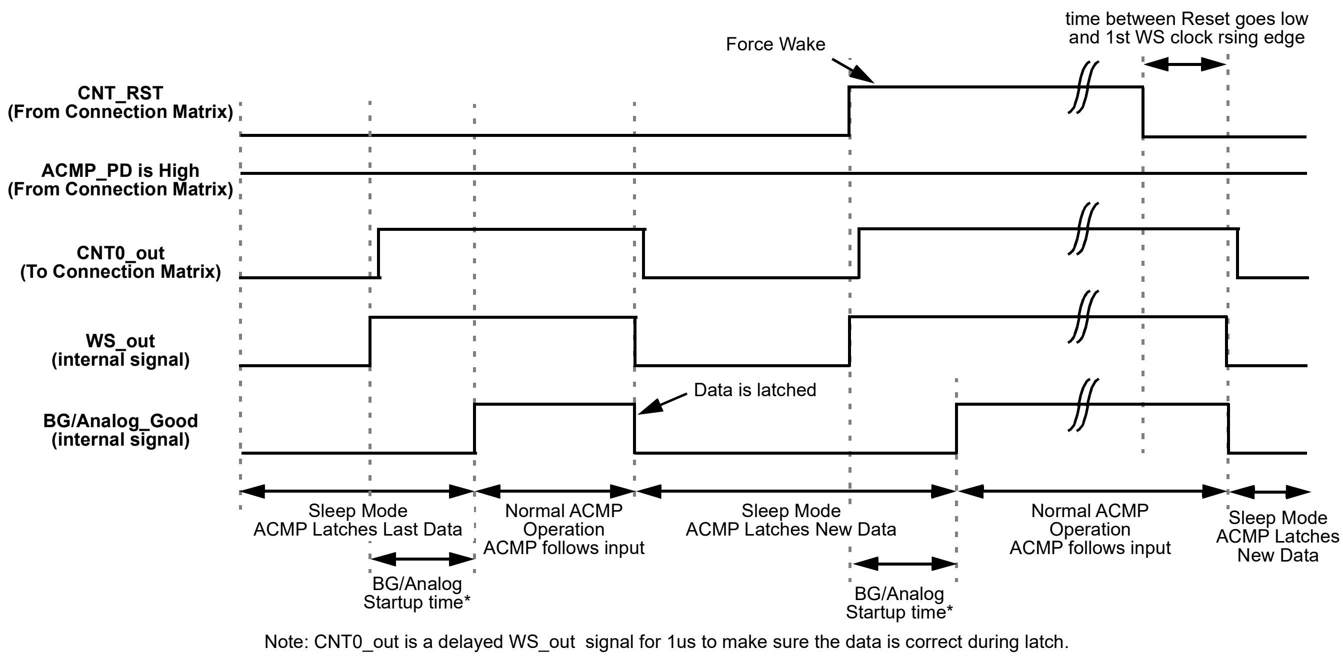


Figure 51: Wake/Sleep Timing Diagram, Normal Wake Mode, Counter Reset is Used

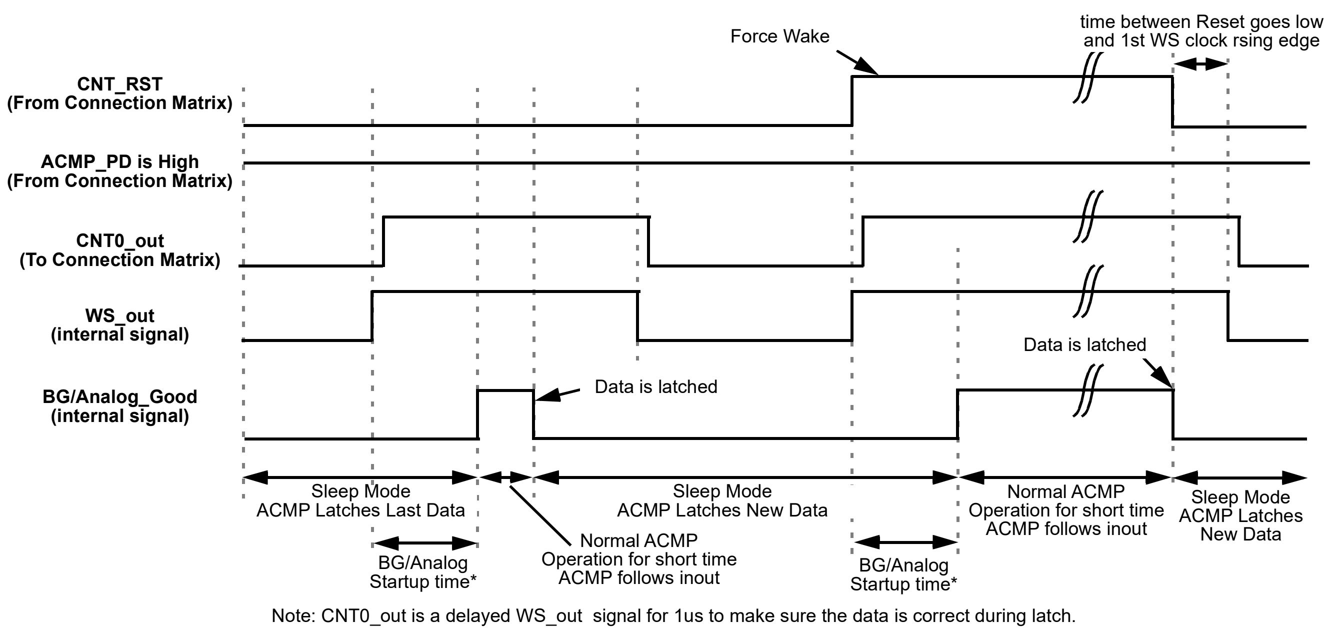


Figure 52: Wake/Sleep Timing Diagram, Short Wake Mode, Counter Reset is Used

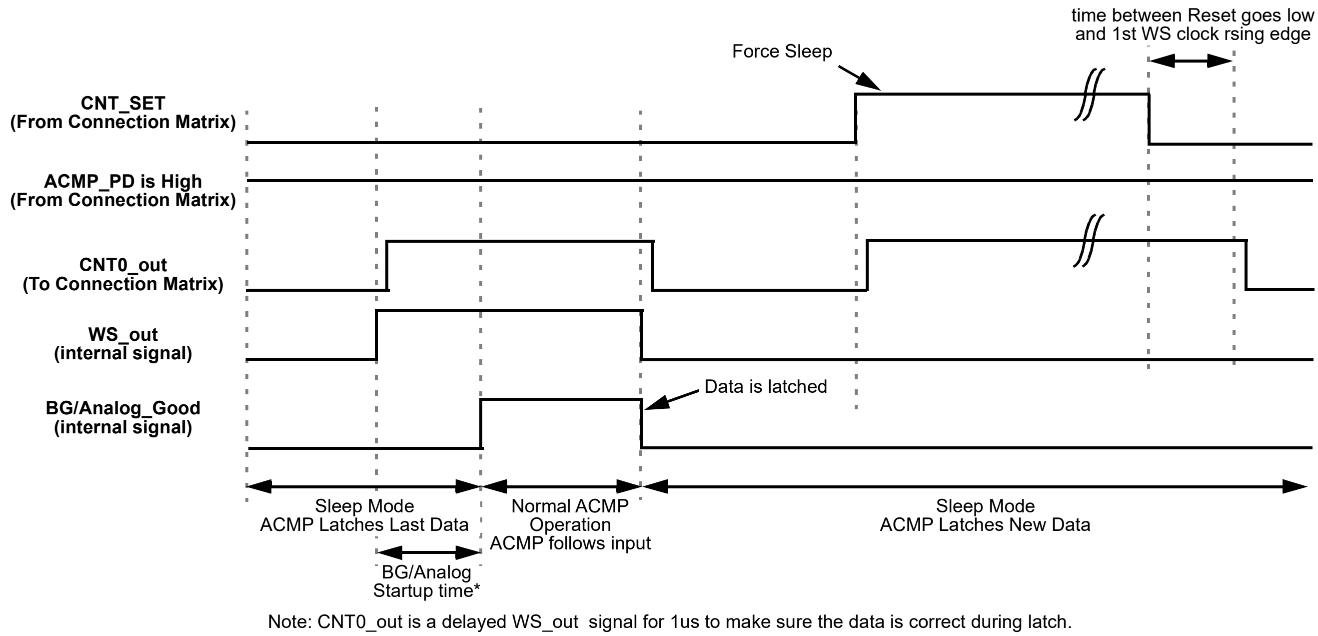


Figure 53: Wake/Sleep Timing Diagram, Normal Wake Mode, Counter Set is Used

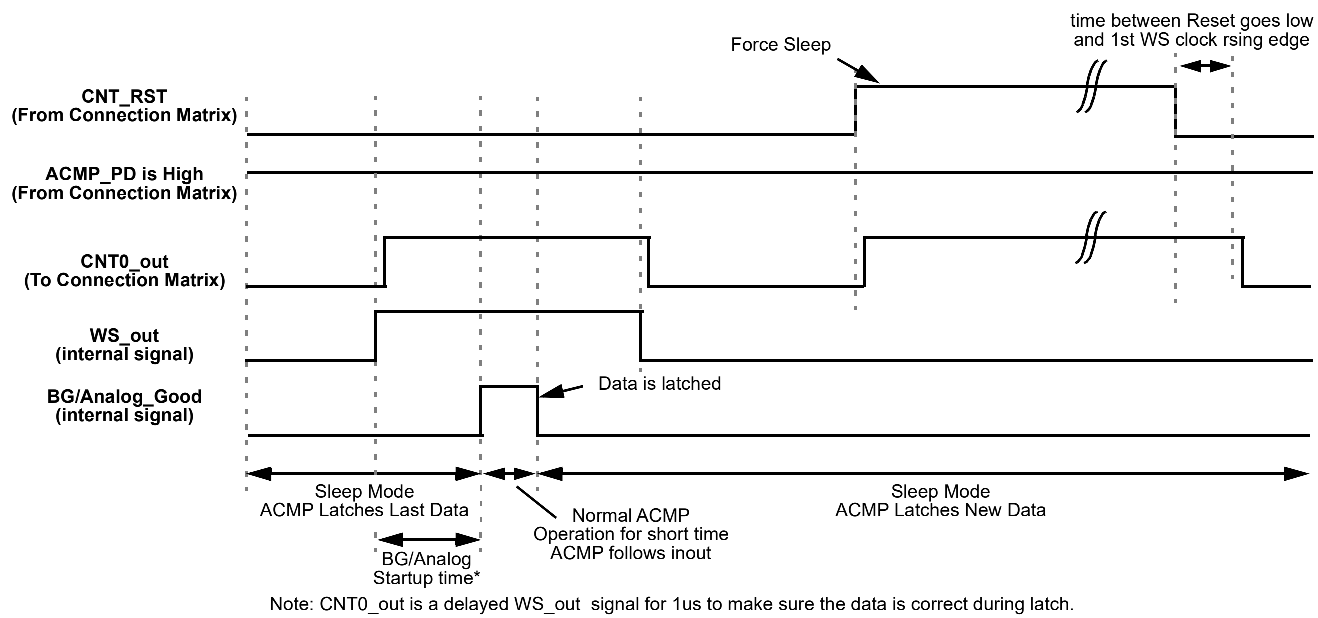


Figure 54: Wake/Sleep Timing Diagram, Short Wake Mode, Counter Set is Used

Note: If low power BG is powered on/off by w/s, the wake time should be longer than 2.1 ms. The BG/analog start up time will take maximal 2 ms. If low power BG is always on, LFOSC period is longer than required wake time. The short wake mode can be used to reduce the current consumption.

To use any ACMPxH under WS controller the following settings must be done:

- ACMPxH Power Up Input from matrix = 1 (for each ACMPxH separately).

- CNT/DLY0 must be set to Wake and Sleep Controller function (for all ACMPxH).
- Register WS → enable (for each ACMPxH separately).
- CNT/DLY0 set/reset input = 0 (for all ACMPxH).

As the OSC any oscillator with any pre-divider can be used. The user can select a period of time while the ACMPxH is sleeping in a range of 1 to 65535 clock cycles. Before they are sent to sleep their outputs are latched so the ACMPs remain their state (High or Low) while sleeping.

WS controller has the following settings:

- Wake and Sleep Output State (High/Low)
  If OSC is powered off (Power Down option is selected; power down input = 1) and Wake and Sleep Output State = High, the ACMPxH is continuously on.
  If OSC is powered off (Power Down option is selected; power down input = 1) and Wake and Sleep Output State = Low, the ACMPxH is continuously off.
  Both cases WS function is turned off.

- Counter Data (Range: 1 to 65535)
  User can select wake and sleep ratio of the ACMP; counter data = sleep time, one clock = wake time.

- Q mode - defines the state of WS counter data when Set/Reset signal appears Reset - when active signal appears, the WS counter will reset to zero and High level signal on its output will turn on the ACMPs. When Reset signal goes out, the WS counter will go Low and turn off the ACMPxH until the counter counts up to the end. Set - when active signal appears, the WS counter will stop and Low level signal on its output will turn off the ACMPxH. When Set signal goes out, the WS counter will go on counting and High level signal will turn on the ACMPxH while counter is counting up to the end.

Note: The LFOSC matrix power down to control ACMP W/S is not supported for short wait time option.

- Edge Select defines the edge for Q mode
  High level Set/Reset - switches mode Set/Reset when level is High

Note: Q mode operates only in case of "High Level Set/Reset".

- Wake time selection - time required for wake signal to turn the ACMPxH on

  Normal Wake Time - when WS signal is High, it takes BG/analog start up time to turn the ACMPs on They will stay on until WS signal is Low again. Wake time is one clock period. It should be longer than BG turn on time and minimal required comparing time of the ACMP.

  Short Wake Time - when WS signal is High, it takes BG/analog start up time to turn the ACMPs on. They will stay on for 1 µs and turn off regardless of WS signal. The WS signal width does not matter.
- Keep - pauses counting while Keep = 1
- Up - reverses counting

  If Up = 1, CNT is counting up from user selected value to 65535.

  If Up = 0, CNT is counting down from user selected value to 0.

7.8.1 WS Register Settings

Table 45: WS Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/delay0 Clock Source Select	registers [903:900]	0000: OSC2 0001: OSC2 /4 0010: OSC1 0011: OSC1 /8 0100: OSC1 /64 0101: OSC1 /512 0110: OSC0 0111: OSC0 /8 1000: OSC0 /64 1001: OSC0 /512 1010: OSC0 /4096 1011: OSC0 /32768 1100: OSC0 /262144 1101: CNT4 Overflow 1110: External 1111: Reserved
ACMP0H Wake & Sleep function Enable	register [663]	0: Disable 1: Enable
ACMP1H Wake & Sleep function Enable	register [664]	0: Disable 1: Enable
Wake Sleep Output State When WS Oscillator is Power Down if DLY/CNT0 Mode Selection is "11"	register [909]	0: Low 1: High
DLY/CNT0 (16bits, [15:0] = [3935:3920]) Control Data	registers [3935:3920]	1 - 65535

8 Analog Comparators

There are four General Purpose Rail-to-Rail Analog Comparator (ACMP) macrocells in the SLG46880/81. In order for the ACMP cells to be used in a GreenPAK design, the power up signals (ACMP0H_pd, ACMP1H_pd, ACMP2L_pd and ACMP3L_pd) need to be active. By connecting to signals coming from the Connection Matrix, it is possible to have each ACMP be on continuously, off continuously, or switched on periodically based on a digital signal coming from the Connection Matrix. When ACMP is powered down, output is low.

Two of the four General Purpose Rail-to-Rail Analog Comparators are optimized for high speed operation (ACMP0H and ACMP1H), and two of the four are optimized for low power operation (ACMP2L and ACMP3L).

Each of the ACMP cells has a positive input signal that can be provided by a variety of external sources, and can also have a selectable gain stage before connection to the analog comparator. Each of the ACMP cells has a negative input signal that is either created from an internal Vref or provided by way of the external sources.

PWR UP = 1 → ACMP is powered up.

PWR UP = 0 → ACMP is powered down.

During power-up, the ACMP output will remain LOW, and then become valid 51.4 μs (max) after power up signal goes high for ACMP0H and ACMP1H, and become valid 326.6 μs (max) after power up signal goes high for ACMP2L and ACMP3L. Input bias current < 1 nA (typ). The Gain divider is unbuffered and consists of 2 MΩ resistors.

Each cell also has a hysteresis selection, to offer hysteresis of (0, 32, 64, 192) mV.

ACMP0H IN+ options are GPIO10, buffered GPIO10, V_{DD}
ACMP1H IN+ options are GPIO11, buffered GPIO11, ACMP0H IN+ MUX output
ACMP2L IN+ options are GPO5, ACMP0H IN+ MUX output, ACMP1H IN+ MUX output
ACMP3L IN+ options are GPO6, ACMP2L IN+ MUX output, Temp Sensor OUT

8.1 ACMP0H BLOCK DIAGRAM

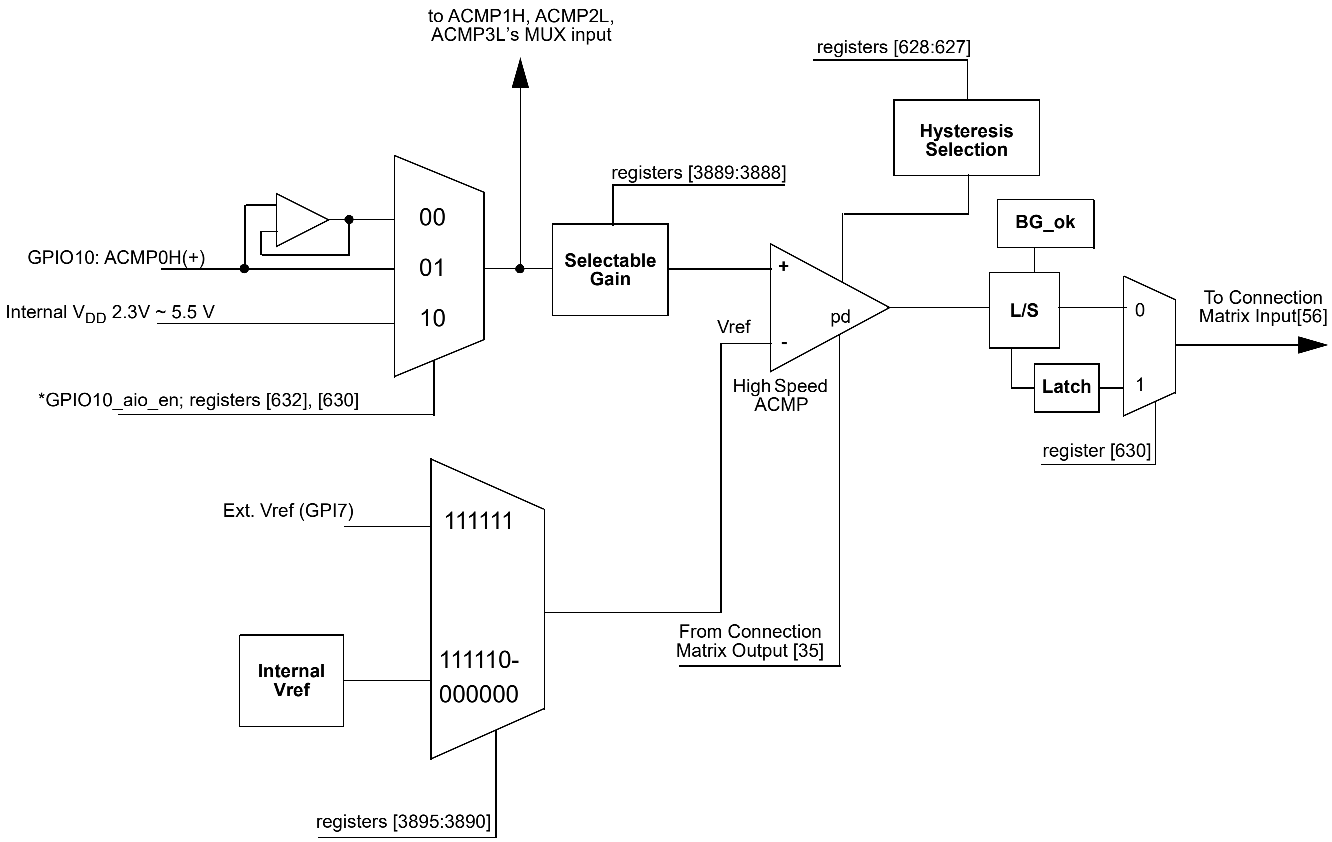


Figure 55: ACMP0H Block Diagram

8.2 ACMP1H BLOCK DIAGRAM

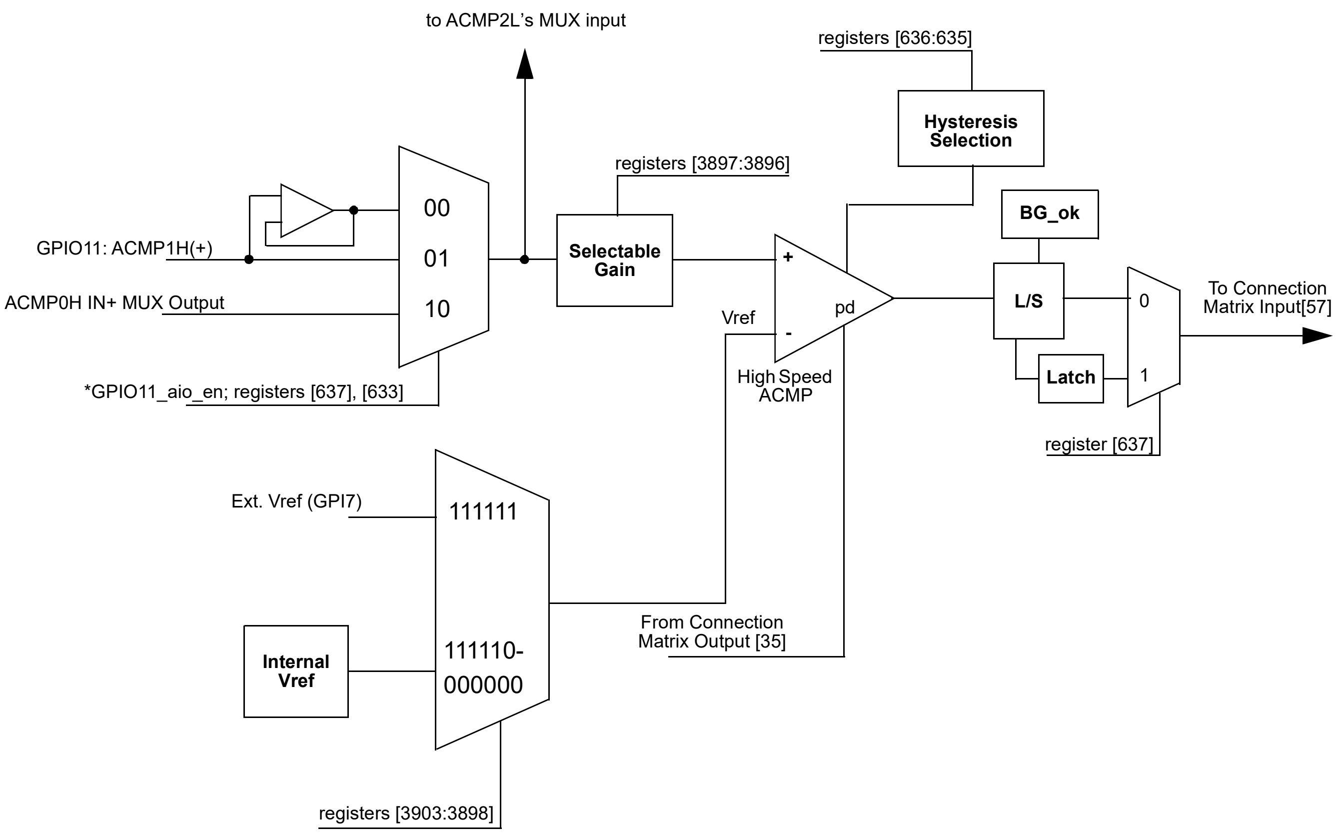


Figure 56: ACMP1H Block Diagram

8.3 ACMP2L BLOCK DIAGRAM

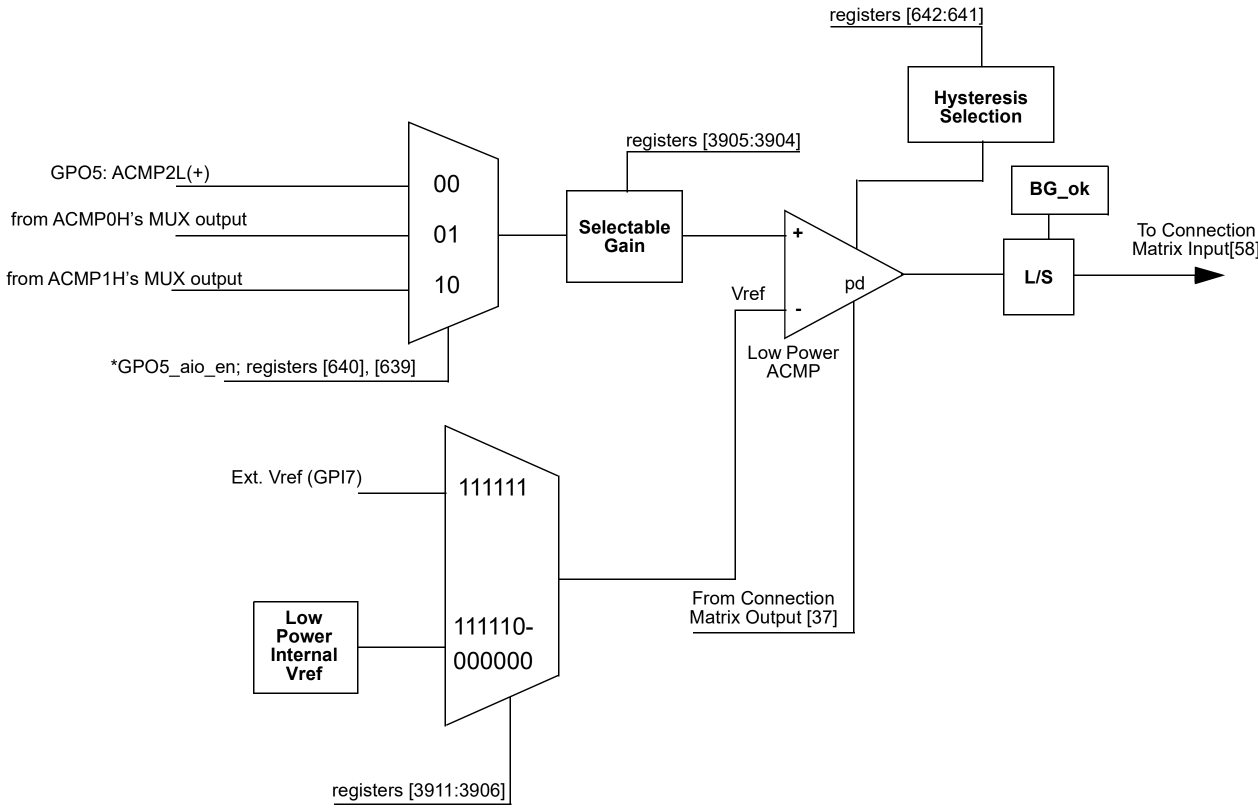


Figure 57: ACMP2L Block Diagram

8.4 ACMP3L BLOCK DIAGRAM

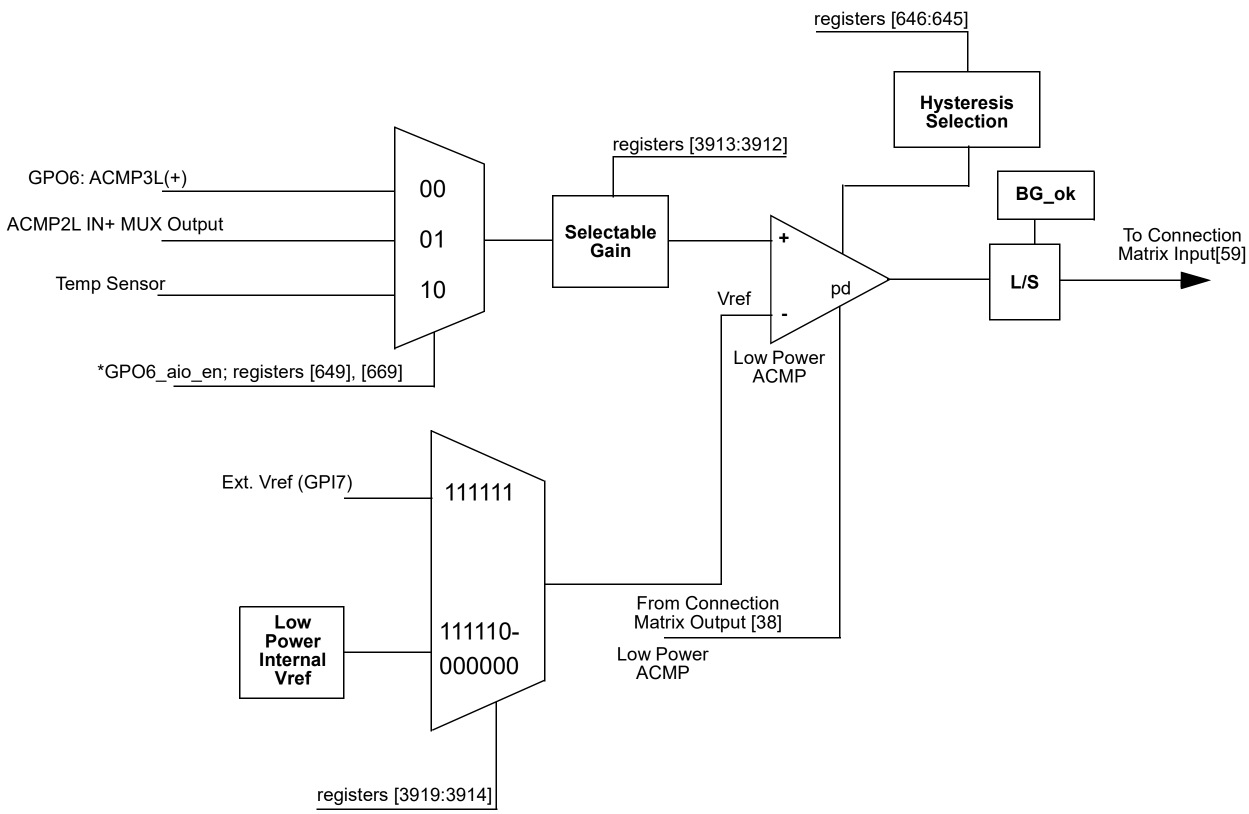


Figure 58: ACMP3L Block Diagram

9 Programmable Delay/Edge Detector

The SLG46880/81 has a programmable time delay logic cell available that can generate a delay that is selectable from one of four timings (time1) configured in the GreenPAK Designer. The programmable time delay cell can generate one of four different delay patterns, rising edge detection, falling edge detection, both edge detection and both edge delay. These four patterns can be further modified with the addition of delayed edge detection, which adds an extra unit of delay as well as glitch rejection during the delay period. See Figure 60 for further information.

Note: The input signal must be longer than the delay, otherwise it will be filtered out.

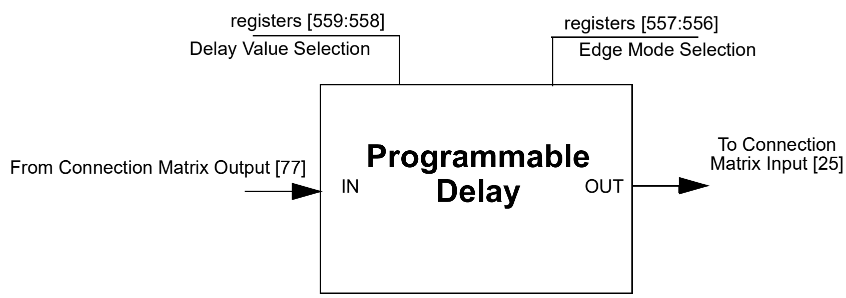


Figure 59: Programmable Delay

9.1 PROGRAMMABLE DELAY TIMING DIAGRAM - EDGE DETECTOR OUTPUT

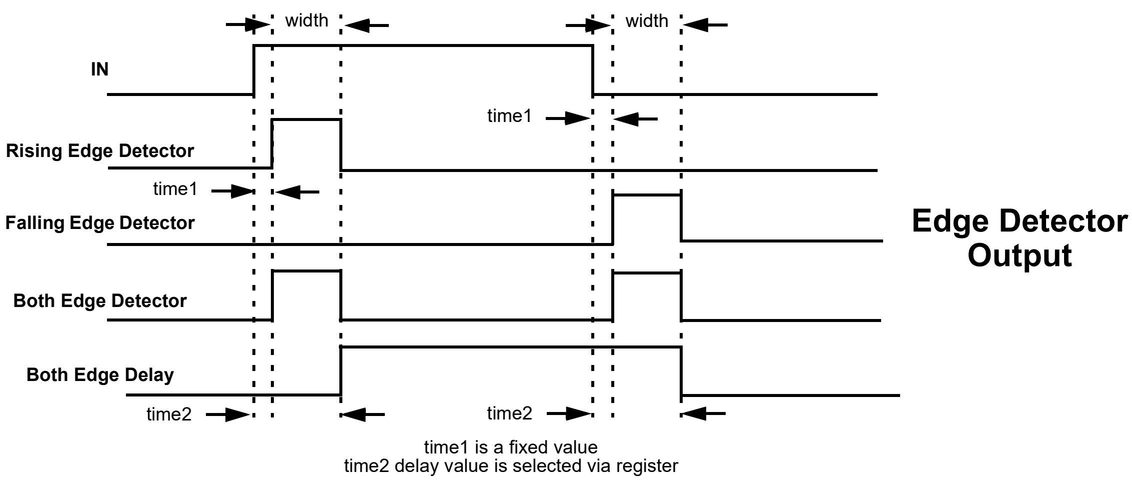


Figure 60: Edge Detector Output

Please refer to Table 11.

10 Additional Logic Function

The SLG46880/81 has one additional logic function that is connected directly to the Connection Matrix inputs and outputs. There is one deglitch filter, with edge detector function.

10.1 DEGLITCH FILTER/EDGE DETECTOR

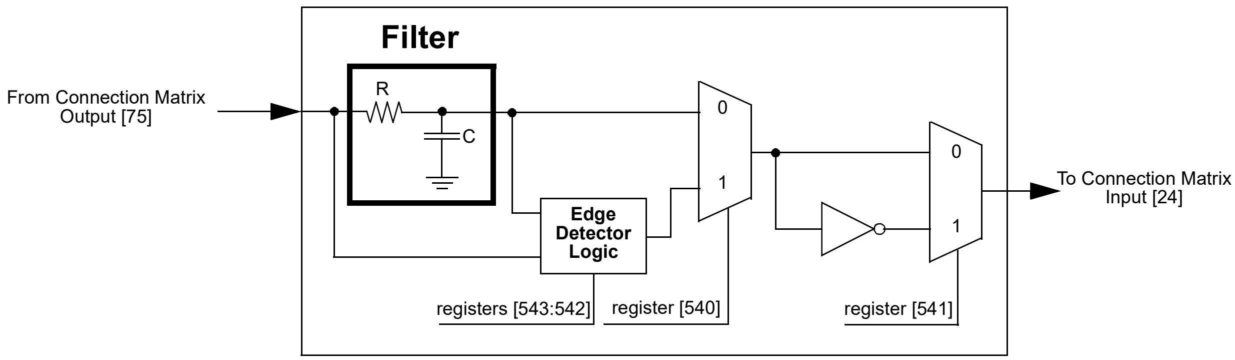


Figure 61: Deglitch Filter/Edge Detector

11 Voltage Reference

11.1 VOLTAGE REFERENCE OVERVIEW

The SLG46880/81 has a Voltage Reference (Vref) Macrocell to provide references to the four analog comparators. This macrocell can supply a user selection of fixed voltage references, or temperature sensor output. The macrocell also has the option to output reference voltages on GPIO2 and GPIO9. See Table 46 for the available selections for each analog comparator. Also see Figure 62, which shows the reference output structure.

11.2 VREF SELECTION TABLE

Table 46: Vref Selection Table

SEL[5:0]	Vref	SEL[5:0]	Vref
0	0.032	32	1.056
1	0.064	33	1.088
2	0.096	34	1.12
3	0.128	35	1.152
4	0.16	36	1.184
5	0.192	37	1.216
6	0.224	38	1.248
7	0.256	39	1.28
8	0.288	40	1.312
9	0.32	41	1.344
10	0.352	42	1.376
11	0.384	43	1.408
12	0.416	44	1.44
13	0.448	45	1.472
14	0.48	46	1.504
15	0.512	47	1.536
16	0.544	48	1.568
17	0.576	49	1.6
18	0.608	50	1.632
19	0.64	51	1.664
20	0.672	52	1.696
21	0.704	53	1.728
22	0.736	54	1.76
23	0.768	55	1.792
24	0.8	56	1.824
25	0.832	57	1.856
26	0.864	58	1.888
27	0.896	59	1.92
28	0.928	60	1.952
29	0.96	61	1.984
30	0.992	62	2.016
31	1.024	63	External

11.3 TRUTH TABLE FOR VREF0 BUFFER AND OUTPUT SWITCH CONTROL

Table 47: VrefO0 Truth Table

Function Enable	VrefO0 Source Selection register [655:654]	VrefO0 Buffer Selection register [623]	VrefO0 Buffer Enable register [653]	Matrix out78	TS PD Selection register [651]	TS PD Register Control register [650]	GPIO9 Analog Mode Enable register [856:855]= 11, means enable	Buffer state	Output switch	Note
None	00	0	0	0	0	0	Disable	Off	Off	VrefO0 is all off
ACMP0H_Vref	01	0	0	0	0	0	Disable	Off	Off	VrefO0 select ACMP0H; output has no buffer; pd comes from register [653]
	01	0	0	0	0	0	Enable	Off	On	
	01	0	1	0	0	0	Disable	On	Off	VrefO0 select ACMP0H; output has buffer; pd comes from register [653]
	01	0	1	0	0	0	Enable	On	On	
	01	1	0	0	0	0	Disable	Off	Off	VrefO0 select ACMP0H; output has no buffer; pd comes from matrix78
	01	1	0	0	0	0	Enable	Off	On	
	01	1	0	1	0	0	Disable	On	Off	VrefO0 select ACMP0H; output has buffer; pd comes from matrix78
	01	1	0	1	0	0	Enable	On	On	
ACMP1H_Vref	10	0	0	0	0	0	Disable	Off	Off	VrefO0 select ACMP1H; output has no buffer; pd comes from register [653]
	10	0	0	0	0	0	Enable	Off	On	
	10	0	1	0	0	0	Disable	On	Off	VrefO0 select ACMP1H; output has buffer; pd comes from register [653]
	10	0	1	0	0	0	Enable	On	On	
	10	1	0	0	0	0	Disable	Off	Off	VrefO0 select ACMP1H; output has no buffer; pd comes from matrix78
	10	1	0	0	0	0	Enable	Off	On	
	10	1	0	1	0	0	Disable	On	Off	VrefO0 select ACMP1H; output has buffer; pd comes from matrix78
	10	1	0	1	0	0	Enable	On	On	
TS function	11	0	0	0	0	0	Disable	Off	Off	TS enable comes from register [650]
	11	0	0	0	0	0	Enable	Off	Off	
	11	0	0	0	0	1	Disable	On	Off	
	11	0	0	0	0	1	Enable	On	On	
	11	0	0	0	0	0	Disable	Off	Off	TS enable comes from Matrix78
	11	0	0	0	0	0	Enable	Off	Off	
	11	0	0	1	0	0	Disable	On	Off	
	11	0	0	1	0	0	Enable	On	On	

11.4 TRUTH TABLE FOR VREF1 BUFFER AND OUTPUT SWITCH CONTROL

Table 48: VrefO1 Truth Table

Function Enable	VrefO1 Source Selection registers [658:657]	VrefO1 Buffer Selection register [656]	GPIO2 Analog Mode Enable registers [708:707]= 11, means enable	Buffer state	Output switch	Note
None	00	0	Disable	Off	Off	VrefO1 is all off
ACMP2L_Vref	01	0	Disable	Off	Off	VrefO1 select ACMP2L; output has no buffer; pd come from register [656]
	01	0	Enable	Off	On	
	01	1	Disable	On	Off	VrefO1 select ACMP2L; output has buffer; pd come from register [656]
	01	1	Enable	On	On	

Table 48: VrefO1 Truth Table(Continued)

Function Enable	VrefO1 Source Selection	VrefO1 Buffer Selection	GPIO2 Analog Mode Enable	Buffer state	Output switch	Note
	registers [658:657]	register [656]	registers [708:707]= 11, means enable			
ACMP3L_Vref	10	0	Disable	Off	Off	VrefO1 select ACMP2L; output has no buffer; pd come from register [656]
	10	0	Enable	Off	On	
	10	1	Disable	On	Off	VrefO1 select ACMP2L; output has buffer; pd come from register [656]
	10	1	Enable	On	On	

	valid output mode

11.5 VREF BLOCK DIAGRAM

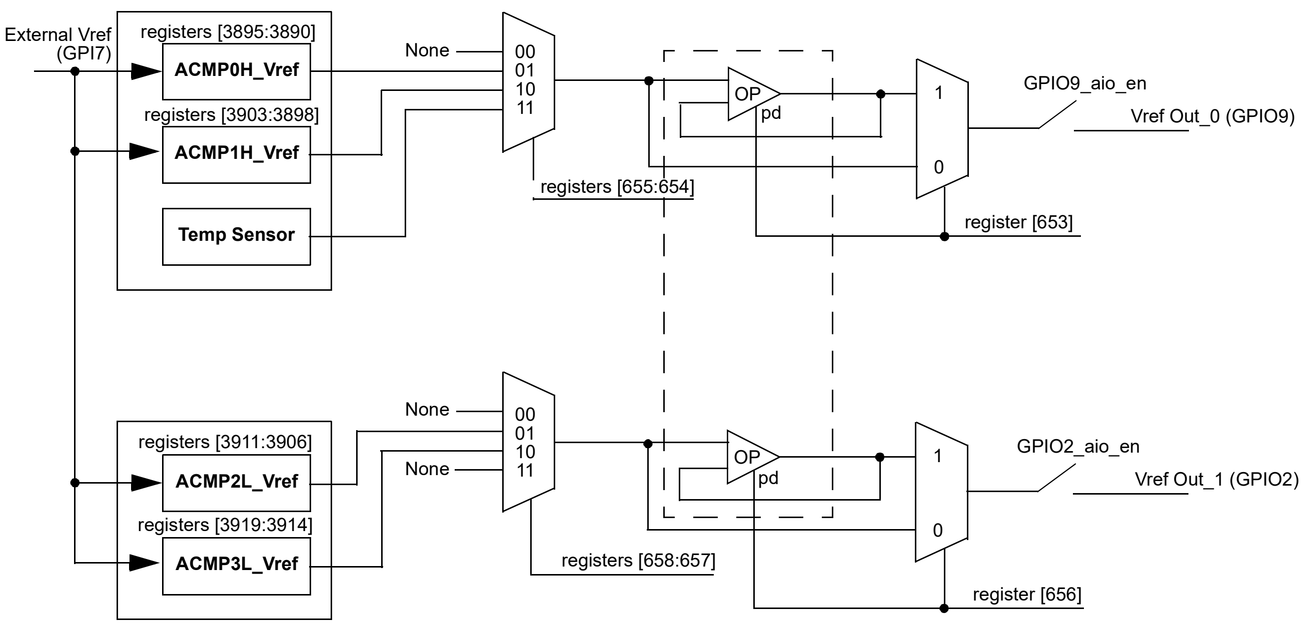


Figure 62: Voltage Reference Block Diagram

11.6 VREF LOAD REGULATION

Note 1 It is not recommended to use Vref connected to external pin without buffer.

Note 2 Vref buffer performance is not guaranteed at V_{DD} < 2.7 V.

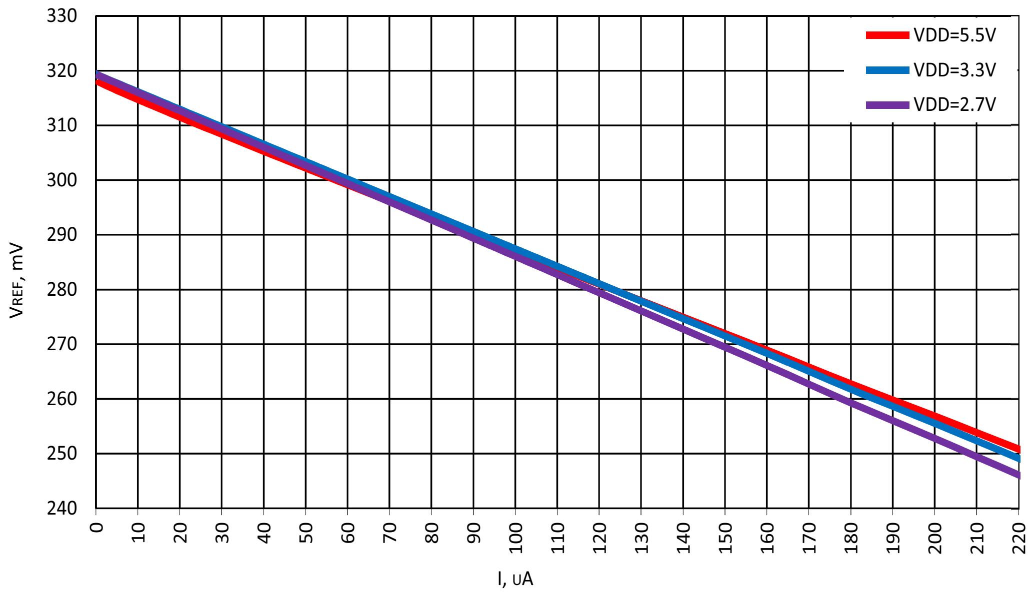


Figure 63: Typical Load Regulation, Vref = 320 mV, T = -40 °C to +85 °C, Buffer - Enable

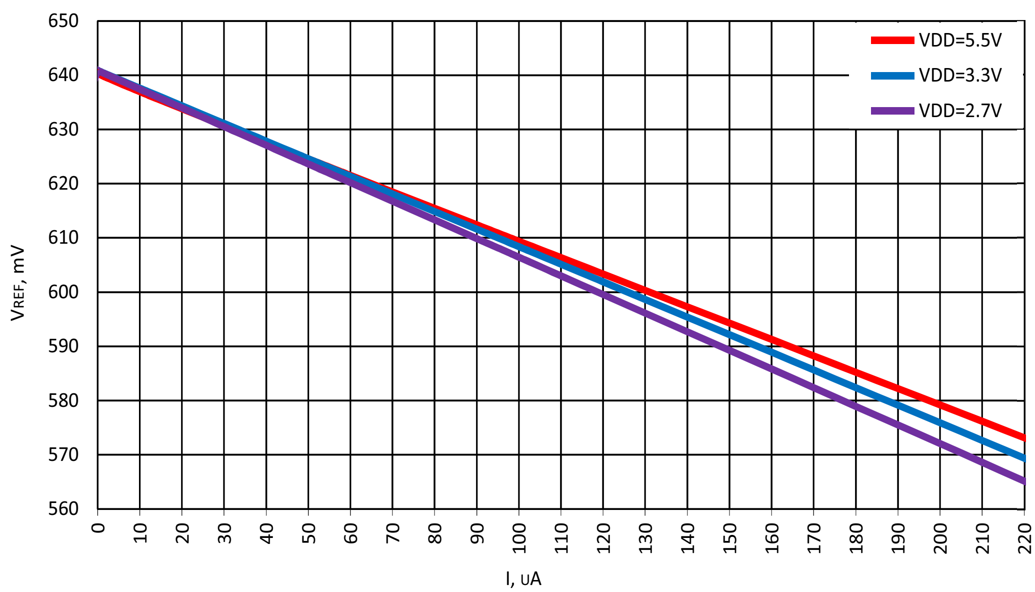


Figure 64: Typical Load Regulation, Vref = 640 mV, T = -40 °C to +85 °C, Buffer - Enable

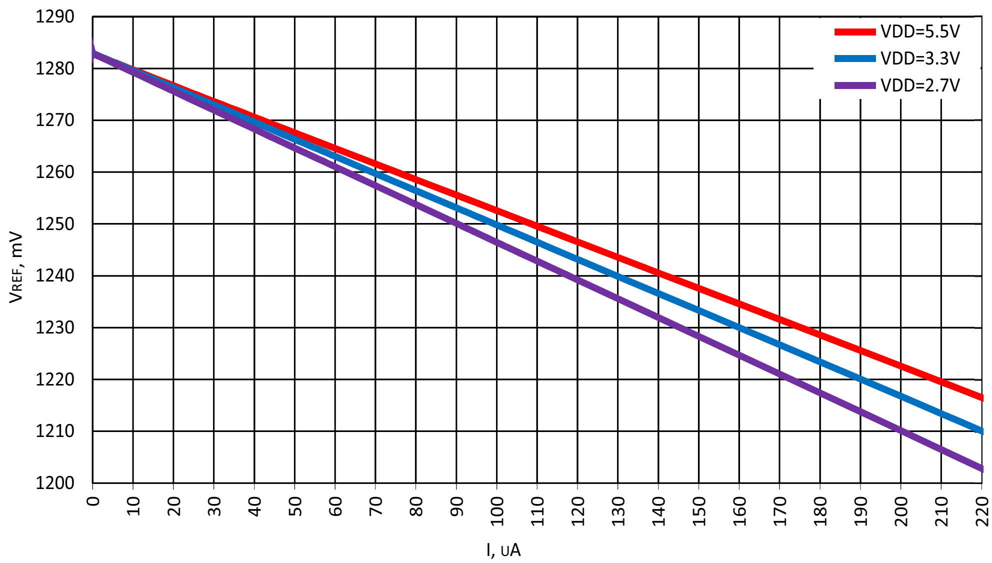


Figure 65: Typical Load Regulation, Vref = 1280 mV, T = -40 °C to +85 °C, Buffer - Enable

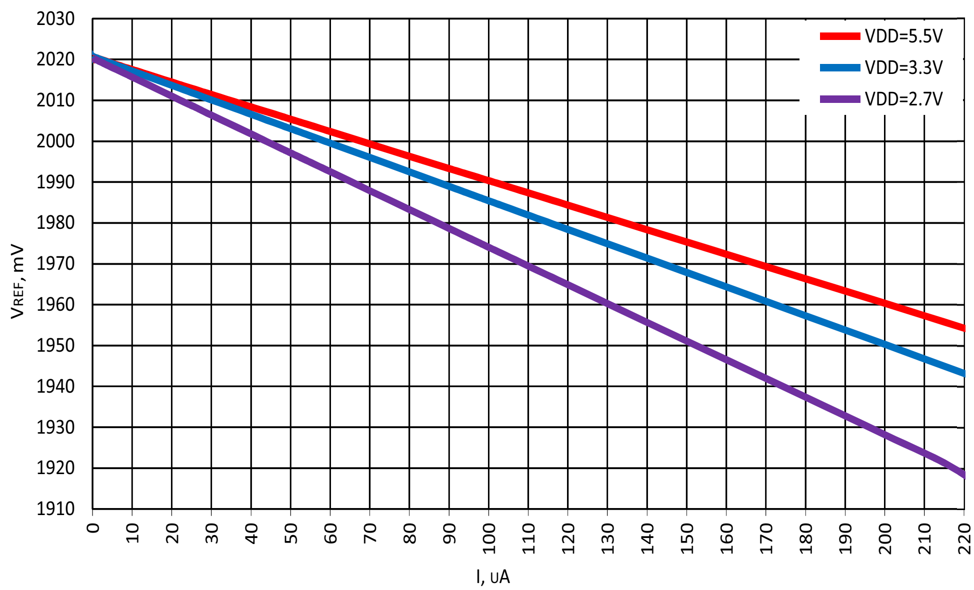


Figure 66: Typical Load Regulation, Vref = 2016 mV, T = -40 °C to +85 °C, Buffer - Enable

12 Clocking

12.1 GENERAL DESCRIPTION

The SLG46880/81 has three internal oscillators to support a variety of applications:

- Oscillator0 (2.048 kHz)
- Oscillator1 (2.048 MHz)
- Oscillator2 (25 MHz)

There are two divider stages for each oscillator that gives the user flexibility for introducing clock signals to connection matrix, as well as various other Macrocells. The pre-divider (first stage) for Oscillator allows the selection of /1, /2, /4 or /8 to divide down frequency from the fundamental. The second stage divider has an input of frequency from the pre-divider, and outputs one of eight different frequencies divided by /1, /2, /3, /4, /8, /12, /24 or /64 on Connection Matrix Input lines [27], [28] and [29]. Please see Figure 70, for more details on the SLG46880/81 clock scheme.

Oscillator2 (25 MHz) has an additional function of 100 ns delayed startup, which can be enabled/disabled by register [525]. This function is recommended to use when analog blocks are used along with the Oscillator.

The Matrix Power Down/Force On function allows switching off or force on the oscillator using an external pin. The Matrix Power Down/Force On (Connection Matrix Output [72], [73], [74]) signal has the highest priority. The OSC operates according to the Table 49.

Table 49: Oscillator Operation Mode Configuration Settings

POR	External Clock Selection	Signal From Connection Matrix	Register: Power Down or Force On by Matrix Input	Register: Auto Power-On or Force On	OSC Enable Signal from CNT/DLY Macrocells	OSC Operation Mode
0	X	X	X	X	X	OFF
1	1	X	X	X	X	Internal OSC is OFF, logic is ON
1	0	1	0	X	X	OFF
1	0	1	1	X	X	ON
1	0	0	X	1	X	ON
1	0	0	X	0	CNT/DLY requires OSC	ON
1	0	0	X	0	CNT/DLY does not require OSC	OFF
Note: The OSC will run only when any macrocell that uses OSC is powered on.						

12.2 OSCILLATOR0 (2.048 KHZ)

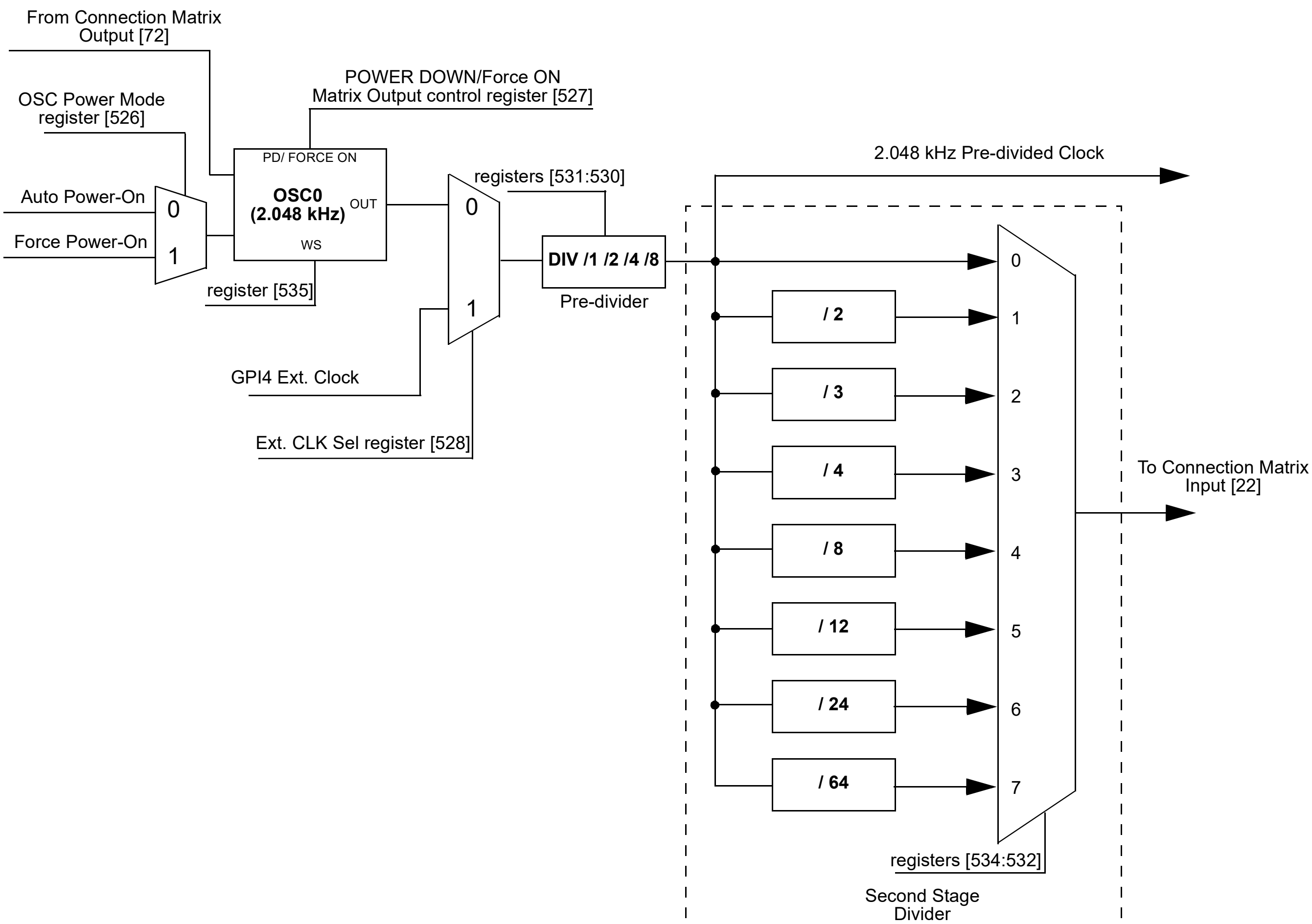


Figure 67: Oscillator0 Block Diagram

12.3 OSCILLATOR1 (2.048 MHZ)

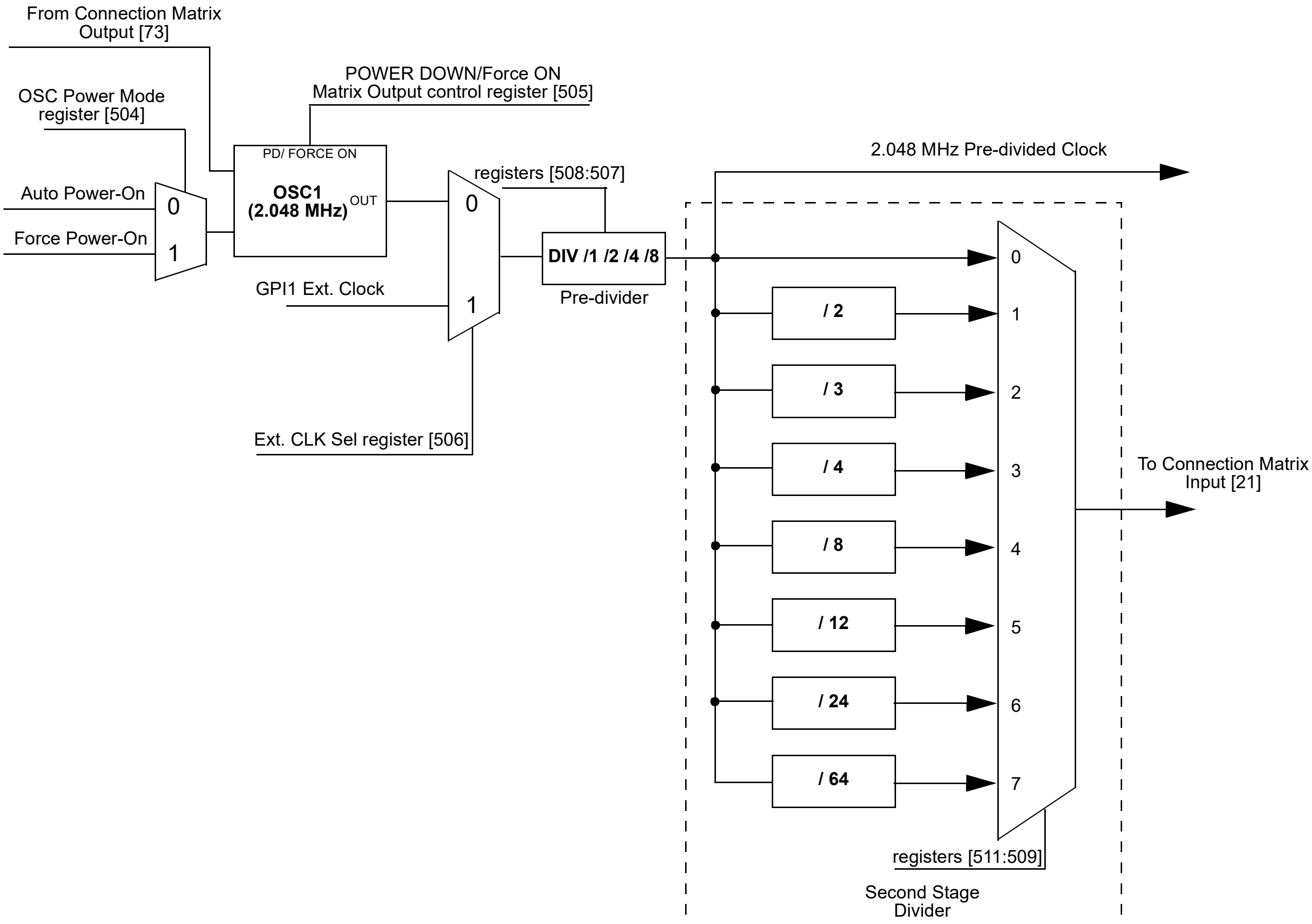


Figure 68: Oscillator1 Block Diagram

12.4 OSCILLATOR2 (25 MHZ)

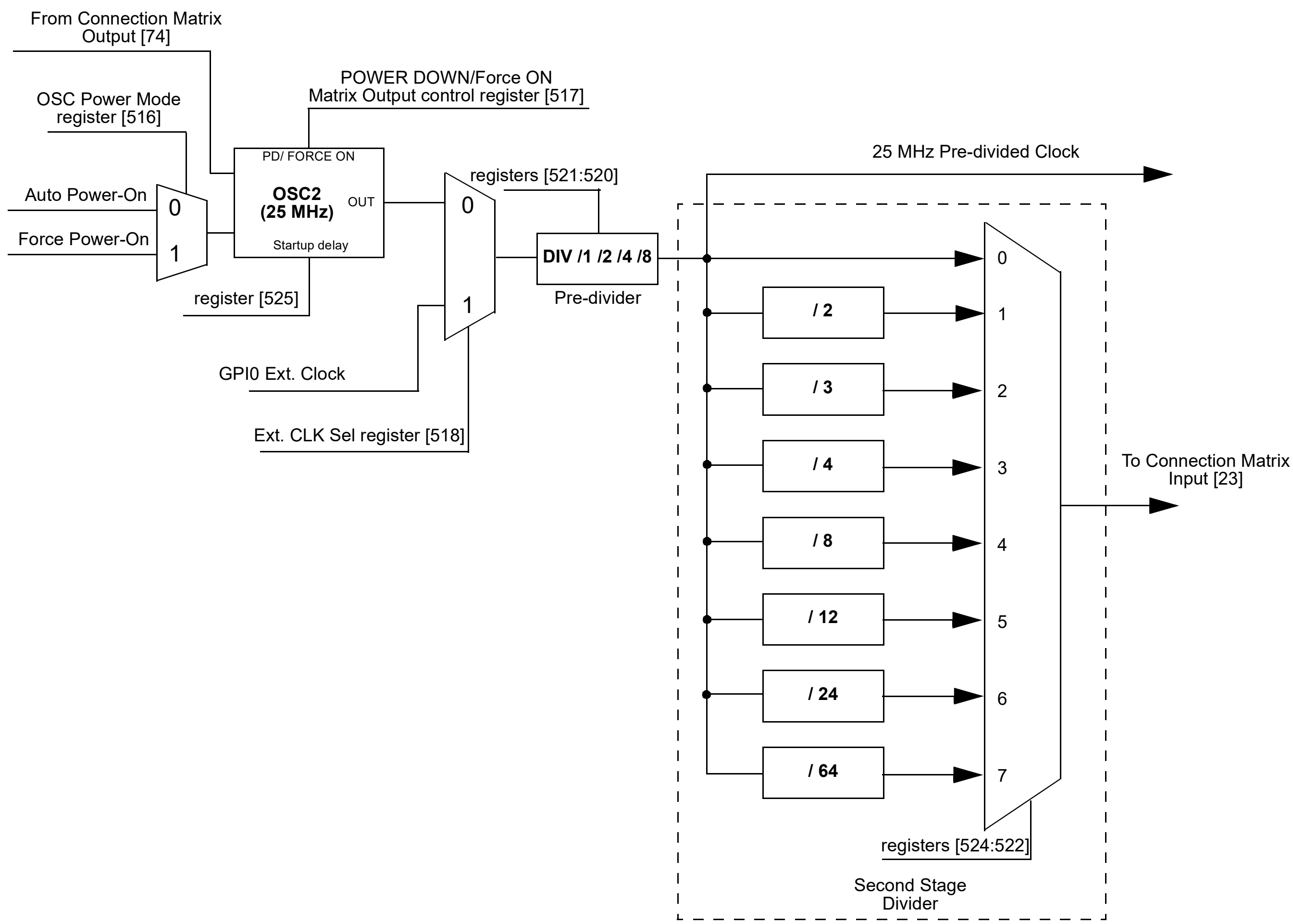


Figure 69: Oscillator2 Block Diagram

12.5 CLOCK SCHEME

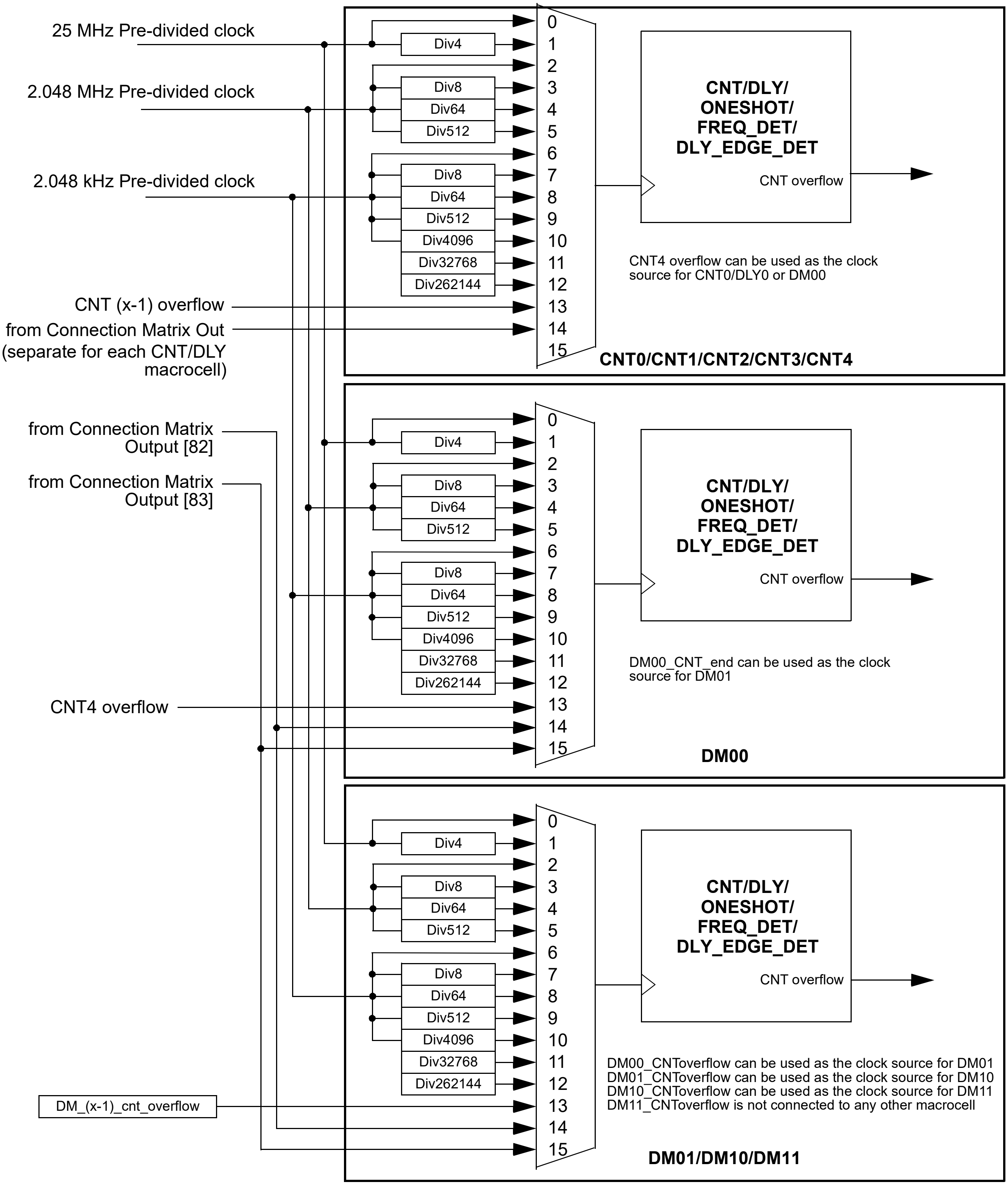


Figure 70: Clock Scheme

12.6 CRYSTAL OSCILLATOR

The Crystal OSC provides high precision and stability of the output frequency. GPI5 and GPI4 are input and output, respectively, of an inverting amplifier which is configured for use as an On-chip Oscillator, as shown in Figure 72. Either a quartz crystal or a ceramic resonator may be used. C1 and C2 should always be equal for both crystals and resonators. The optimal value of the capacitors depends on the crystal or resonator in use, the amount of stray capacitance, and the electromagnetic noise of the environment. Refer to Table 50. For the ceramic resonators, the capacitor values given by the manufacturer should be used. It is possible to use an external clock source, it must be connected to GPI4. In this case no external components are required.

The Power Down Mode is paired with temperature sensor, Section 20. If it is enabled for Crystal OSC, it is not available for Temp Sensor and vice versa. However, it is possible to enable Power Down Mode for Crystal OSC and Temp Sensor simultaneously.

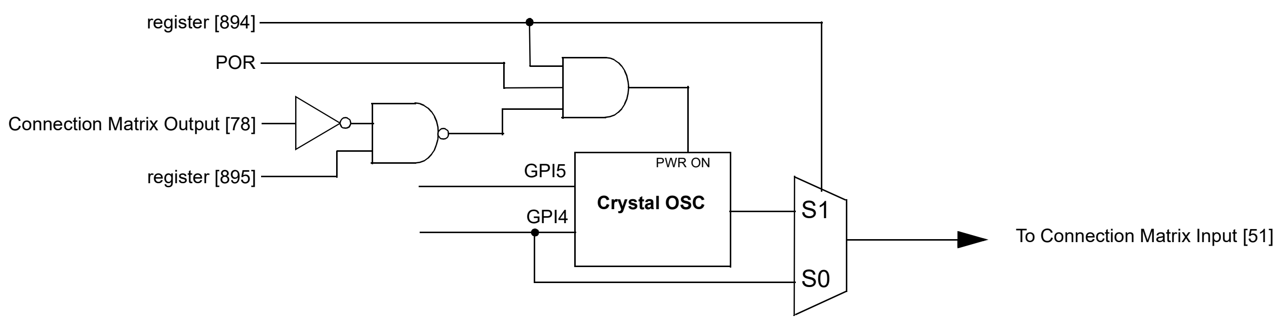


Figure 71: Crystal OSC Block Diagram

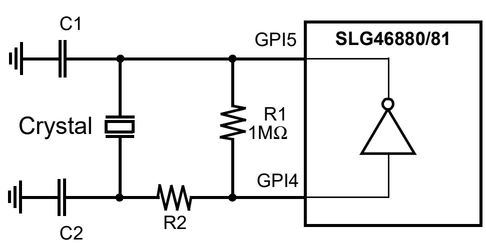


Figure 72: External Crystal Connection

Table 50: External Components Selection Table

f (MHz)	C1, C2	R2
5	33 pF	5 kΩ
10	22 pF	1 kΩ
15	15 pF	500 Ω
20	10 pF	270 Ω

12.7 EXTERNAL CLOCKING

The SLG46880/81 supports several ways to use an external, higher accuracy clock as a reference source for internal operations.

12.7.1 Crystal OSC Mode

When register [1136] is set to 1, an external crystal can be connected to GPI5 and GPI4 for supplying an accurate clock source. See Section 12.6. An external clocking signal on GPI4 can be used in place of the crystal. The high and low limits for crystal frequency that can be selected are 40 MHz and 32.75 kHz.

12.7.2 GPI4 Source for Oscillator0 (2.048 kHz)

When register [528] is set to 1, an external clocking signal on GPI4 will be routed in place of the internal oscillator derived 2.048 kHz clock source. See Figure 67 The high and low limits for external frequency are 0 MHz and 20 MHz.

12.7.3 GPI1 Source for Oscillator1 (2.048 kHz)

When register [506] is set to 1, an external clocking signal on GPI1 will be routed in place of the internal oscillator derived 2.048 MHz clock source. See Figure 68 The high and low limits for external frequency are 0 MHz and 70 MHz.

12.7.4 GPI0 Source for Oscillator2 (25 MHz)

When register [518] is set to 1, an external clocking signal on GPI0 will be routed in place of the internal oscillator derived 25 MHz clock source. See Figure 69 The high and low limits for external frequency are 0 MHz and 80 MHz.

13 Power-On Reset

The SLG46880/81 has a power-on reset (POR) macrocell to ensure correct device initialization and operation of all macrocells in the device. The purpose of the POR circuit is to have consistent behavior and predictable results when the V_{DD} power is first ramping to the device, and also while the V_{DD} is falling during power-down. To accomplish this goal, the POR drives a defined sequence of internal events that trigger changes to the states of different macrocells inside the device, and finally to the state of the IO pins.

13.1 GENERAL OPERATION

The SLG46880/81 is guaranteed to be powered down and non-operational when the V_{DD} voltage (voltage on V_{DD}) is less than Power Off Threshold (see in Table 3.3 and Table 5), but not less than -0.6 V. Another essential condition for the chip to be powered down is that no voltage higher (Note) than the V_{DD} voltage is applied to any other PIN. For example, if V_{DD} voltage is 0.3 V, applying a voltage higher than 0.3 V to any other PIN is incorrect, and can lead to incorrect or unexpected device behavior.

Note: There is a 0.6 V margin due to forward drop voltage of the ESD protection diodes.

To start the POR sequence in the SLG46880/81, the voltage applied on the V_{DD} should be higher than the Power-ON threshold (Note). The full operational V_{DD} range for the SLG46880/81 is 2.3 V to 5.5 V. This means that the V_{DD} voltage must ramp up to the operational voltage value, but the POR sequence will start earlier, as soon as the V_{DD} voltage rises to the Power-ON threshold. After the POR sequence has started, the SLG46880/81 will have a typical Startup Time (see in Table 4 and Table 5) to go through all the steps in the sequence, and will be ready and completely operational after the POR sequence is complete.

Note: The Power-ON threshold is defined in Table 3.3 and Table 5.

To power down the chip the, V_{DD} voltage should be lower than the operational and to guarantee that chip is powered down, it should be less than Power Off Threshold.

All PINs are in high impedance state when the chip is powered down and while the POR sequence is taking place. The last step in the POR sequence releases the IO structures from the high impedance state, at which time the device is operational. The pin configuration at this point in time is defined by the design programmed into the chip. Also as it was mentioned before, the voltage on PINs can’t be bigger than the V_{DD}, this rule also applies to the case when the chip is powered on.

13.2 POR SEQUENCE

The POR system generates a sequence of signals that enable certain macrocells. The sequence is shown in Figure 73.

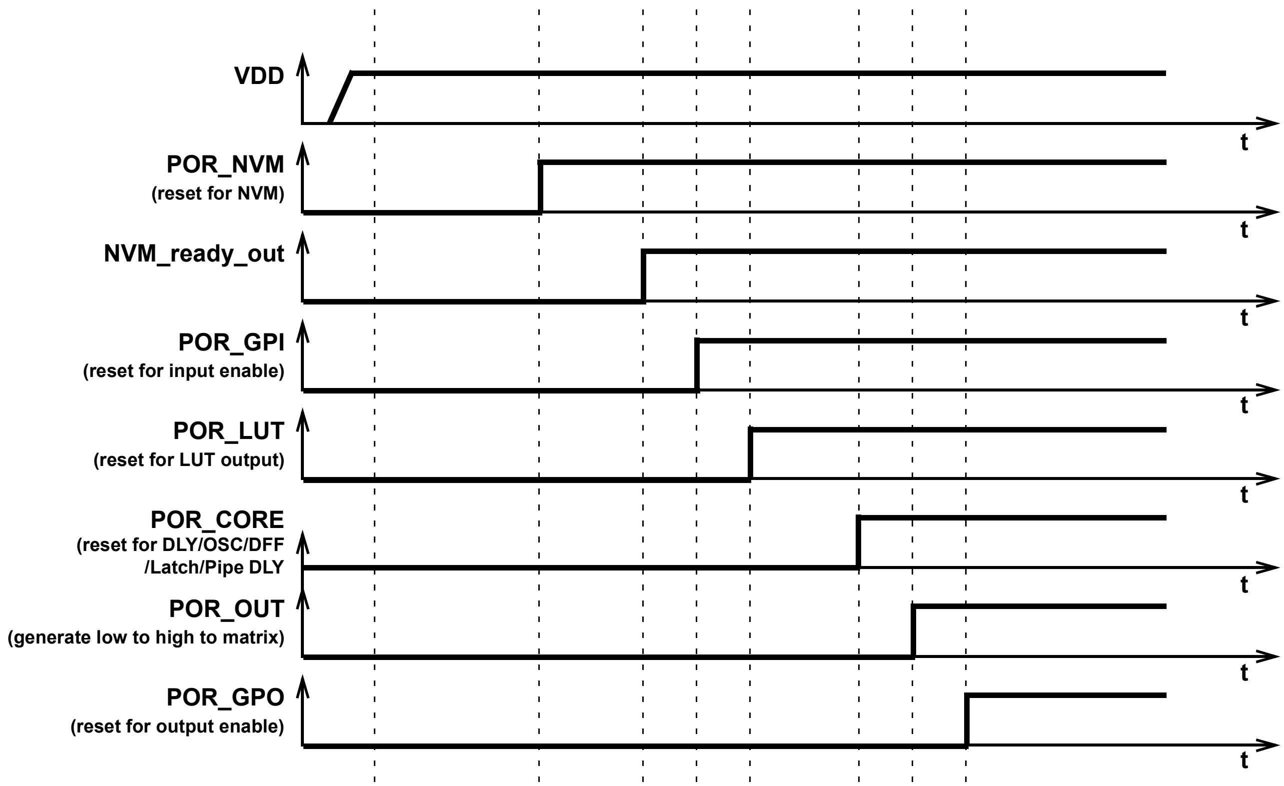


Figure 73: POR Sequence

As can be seen from Figure 73 after the V_{DD} has started ramping up and crossed the Power-ON threshold, first, the on-chip NVM memory is reset. Next the chip reads the data from NVM, and transfers this information to a CMOS Latch that serves to configure each macrocell, and the Connection Matrix which routes signals between macrocells. The third stage causes the reset of the input pins, and then to enable them. After that, the LUTs are reset and become active. After LUTs, the Delay cells, OSCs, DFFs, Latches and Pipe Delay are initialized. Only after all macrocells are initialized, internal POR signal (POR macrocell output) goes from LOW to HIGH (POR_OUT in Figure 73). The last portion of the device to be initialized is the output pins, which transition from high impedance to active at this point.

The typical time that takes to complete the POR sequence varies by device type in the GreenPAK family. It also depends on many environmental factors, such as: slew rate, V_{DD} value, temperature and even will vary from chip to chip (process influence).

13.3 MACROCELLS OUTPUT STATES DURING POR SEQUENCE

To have a full picture of SLG46880/81 operation during powering and POR sequence, refer to Figure 74 which describes the macrocell output states during the POR sequence.

First, before the NVM has been reset, all macrocells have their output set to logic LOW (except the output pins which are in high impedance state). On the next step, some of the macrocells start initialization: input pins output state becomes LOW; LUTs also output LOW. After that input pins are enabled. Next, only LUTs are configured. Then, all other macrocells are initialized. After macrocells are initialized, internal POR matrix signal switches from LOW to HIGH. The last are output pins that become active and determined by the input signals.

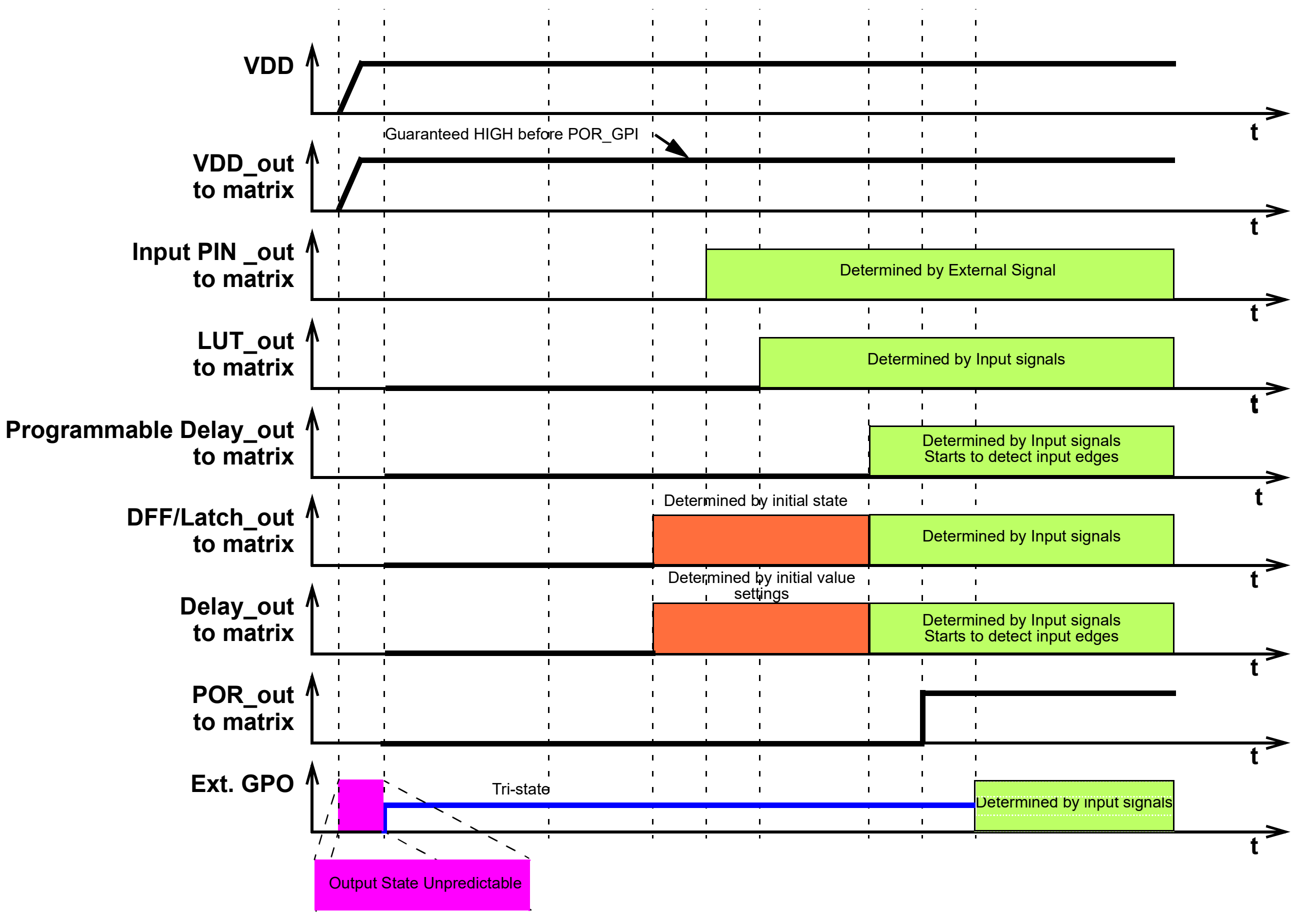


Figure 74: Internal Macrocell States during POR Sequence

13.3.1 Initialization

All internal macrocells by default have initial low level. Starting from indicated power-up time of 1.64 V to 2.11 V, macrocells in SLG46880/81 are powered on while forced to the reset state. All outputs are in Hi-Z and chip starts loading data from NVM. Then the reset signal is released for internal macrocells and they start to initialize according to the following sequence:

1. Input pins, pull up/down.
2. LUTs.
3. DFFs, Delays/Counters, Pipe Delay, OSCs, ACMPs.
4. POR output to matrix.
5. Output pin corresponds to the internal logic.

The Vref output pin driving signal can precede POR output signal going high by 3 µs to 5 µs. The POR signal going high indicates the mentioned power-up sequence is complete.

Note: The maximum voltage applied to any pin should not be higher than the V_{DD} level. There are ESD Diodes between pin –] V_{DD} and pin –> GND on each pin. Exceeding V_{DD} results in leakage current on the input pin, and V_{DD} will be pulled up, following the voltage on the input pin.

13.3.2 Power Down

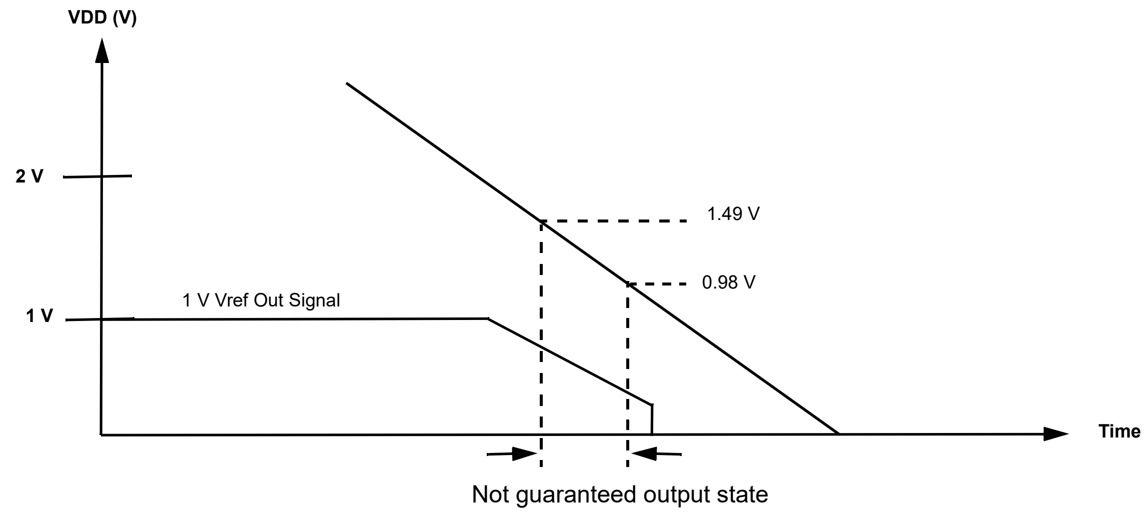


Figure 75: Power Down

During powerdown, macrocells in SLG46880/81 are powered off after V_{DD} falling down below Power Off Threshold. Please note that during a slow rampdown, outputs can possibly switch state.

14 Asynchronous State Machine Subsystem

14.1 ASM SUBSYSTEM OVERVIEW

The Asynchronous State Machine (ASM) Subsystem is designed to allow the user to create state machines with between 2 to 12 states. The user has flexibility to define the available states, the available state transitions, and the input signals (a, b, c …) that will cause transitions from one state to another state, as shown in Figure 76.

The ASM Sybsystem can persist in 1 of 12 states at any given time and the ASM Current State can be read via I^2C. See Section 19.4.6.4 for details.

The ASM Subsystem includes several discrete macrocells, including the ASM macrocell, four Dynamic Memory (DMx_x) macro-cells, three Matrix Interface (MIx) macrocells, and one f(1) Computation Macrocell. These macrocells are designed to work as a system for building user defined state machines. More information on each of these various macrocells can be found in the following chapters:

- ASM Macrocell – Section 15.
- Dynamic Memory (DM) Macrocells – Section 16.
- f(1) Computation Macrocell – Section 17.
- Matrix Interface (MI) Macrocells Section 18.

The ASM Subsystem has a total of 25 digital input signal lines, as shown in Figure 77, which all come from the Connection Matrix outputs. Of these 25 digital input signals, 3 are user selectable inputs going directly from the Connection Matrix to the three Matrix Interface (MI) macrocells. There are a total of 16 input signals that go to the DMx_x macrocell, four per macrocell. There is 1 ASM_nReset input that is for driving a state transition in both the ASM macrocell and the f(1) Computation Macrocell to an Initial/ Reset state. It is possible to use one macrocell only (MI or DM) for state to state transitions. There are 4 digital input signals coming from the Connection Matrix to the f(1) Computation Macrocell. There is also 1 dedicated Interrupt input signal to the f(1) Computation Macrocell that will halt any active operations and transfer control back to the ASM macrocell.

There are a total of 8 analog inputs coming from various pins which can be muxed into the positive input for the f(1) Analog Comparator inside the f(1) Computation Macrocell. The f(1) Analog Comparator can be re-programmed for analog input source and negative input reference settings. The user selections for both positive input signal and negative reference are included as part of the information stored in the f(1) Command Register Table. This allows the user to make different analog measurements that are state dependent in their analog sources and reference settings.

The ASM Subsystem has a total of 21 digital output signal lines, as shown in Figure 77, There are a total of 4 output signals which go to the Connections Matrix inputs, and from there can be routed to other internal macrocells or pins. The 4 outputs are user defined for each of the possible 12 states. There are a total of 8 output signals which go directly to the 8 GPOs. The 8 outputs are user defined for each of the possible 12 states. Each of the three macrocells, DM0_0, DM0_1 and f(1) have three output signals that go to the Connection Matrix.

In using this macrocell, the user must take into consideration the critical timing required on all input and output signals. The timing waveforms and timing specifications for this macrocell are all measured relative to the input signals (which come into the macrocell on the Connection Matrix outputs) and on the outputs from the macrocell (which are direct connections to Connection Matrix inputs). The user must consider any delays from other logic and internal chip connections, including IO delays, to insure that signals are properly processed, and state transitions are deterministic.

It is also important to note that the timing for the ASM Subsystem will change based on changes in temperature and system voltage. The user design that implements a state machine function must take into consideration, and be tolerant of, this variation

The GPAK Designer development tools support user designs for the ASM Subsystem at both the physical level and logic level. Figure 76 is a representation of the user design at the logical level, and Figure 77 shows the physical resources inside the various macrocells in the ASM Subsystem. To best utilize this subsystem, the user must develop a logical representation of their desired state machine, as well as a physical mapping of the input and outputs required for the desired functionality.

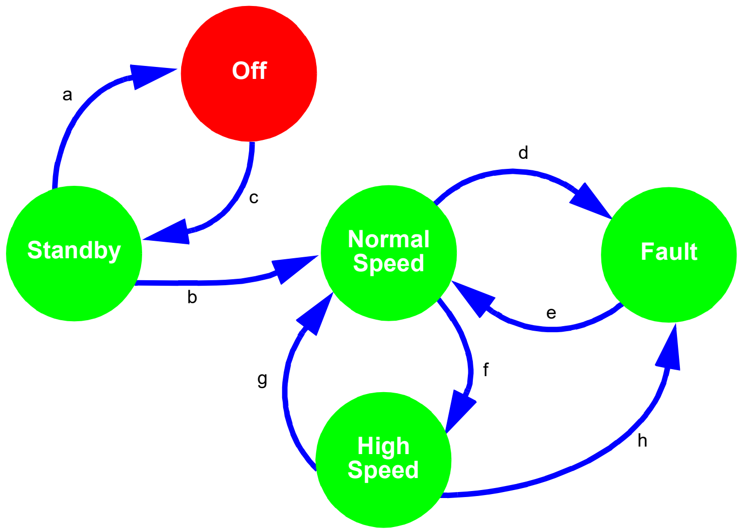


Figure 76: Asynchronous State Machine State Transitions

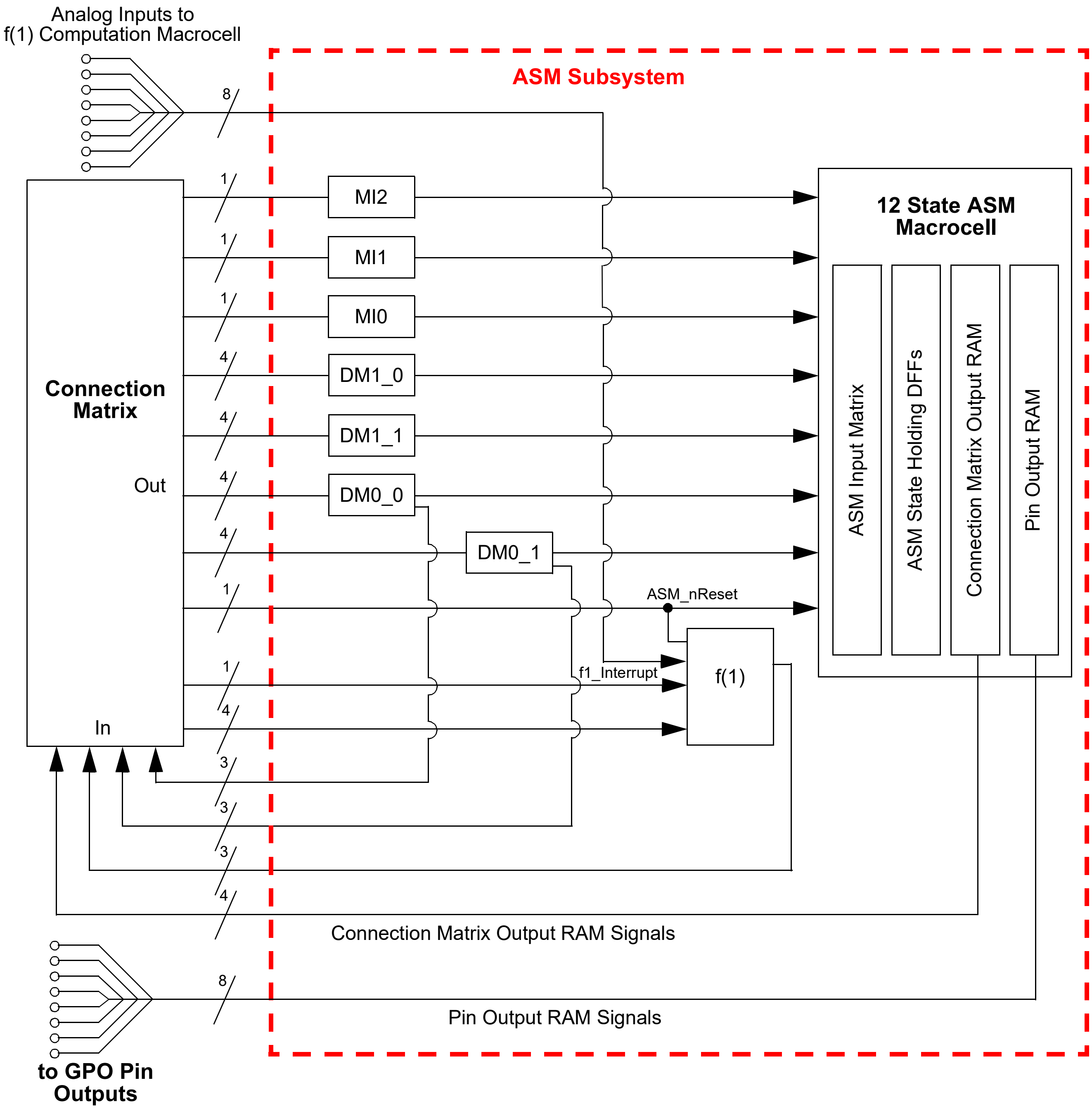


Figure 77: Connection Matrix to ASM Subsystem

14.2 ASM SUBSYSTEM INPUT SIGNALS

The ASM Subsystem has a total of 25 digital input signal lines, as shown in Figure 78, which all come from the Connection Matrix outputs. Of these 25 input signals, 3 are user selectable inputs going directly from the Connection Matrix to the three Matrix Interface (MI) macrocells. There are a total of 16 input signals that go to the DMx_x macrocell, four per macrocell. There is 1 ASM_nReset input that is for driving a state transition in both the ASM macrocell and the f(1) Computation Macrocell to an Initial/ Reset state. There are 4 digital input signals coming from the Connection Matrix to the f(1) Computation Macrocell. There is also 1 dedicated Interrupt input to the f(1) Computation Macrocell that will halt any active operations and transfer control back to the ASM macrocell. Each of the 25 input signals are level sensitive.

There are a total of 16 digital input signals to the ASM Subsystem which are inputs directly to the DM macrocells. These 16 signals are shown in Figure 78, highlighted in blue. While there are 4 input signals coming from the Connection Matrix and going to each DMx_ x macrocell, there is only 1 output signal from each of these macrocells, which goes directly to the ASM macrocell. There are also 3 signal lines that come directly from the Connection Matrix and go to the three Matrix Interface (MI) macrocells which can drive state transitions. These signals are shown in Figure 78, highlighted in green. This sets an upper bound on the number of transitions that the user can select going ***out of*** a particular state to be 7, shown in Figure 79. There is no limitation on the number of unique transitions that can be supported going into a particular state, the user can select to have transitions going from a state to all other states, shown in Figure 80 Each of these input signals to the ASM macrocell is level sensitive, and active high. A high level input will trigger a state transition.

There are a total of 8 analog inputs coming from various pins which can be muxed into the positive input for the f(1) Analog Comparator inside the f(1) Computation Macrocell. These 8 signals are shown in Figure 78, highlighted in pink. The f(1) Analog Comparator can be re-programmed for analog input source and negative input reference settings. The user selections for both positive input signal and negative reference are included as part of the information stored in the f(1) Command Register Table. This allows the user to make different analog measurements that are state dependent in their analog sources and reference settings.

Also there are 4 digital inputs that can be connected with any Connection Matrix output by the f(1) Computational Macrocell commands. These 4 signals are shown in highlighted in light blue.

The ASM macrocell also has a ASM_nReset input. This input to the ASM macrocell is level sensitive and active low. This signal is shown in Figure 78, highlighted in yellow. An active signal on this input will drive an immediate state transition to the user-defined Initial/Reset state. The user can choose which state within the ASM Editor inside GPAK Designer will be the reset state.

There is also 1 dedicated f1_Interrupt input to the f(1) Computation Macrocell that will halt any active operations and transfer control back to the ASM macrocell. This signal is shown in Figure 78 also highlighted in yellow.

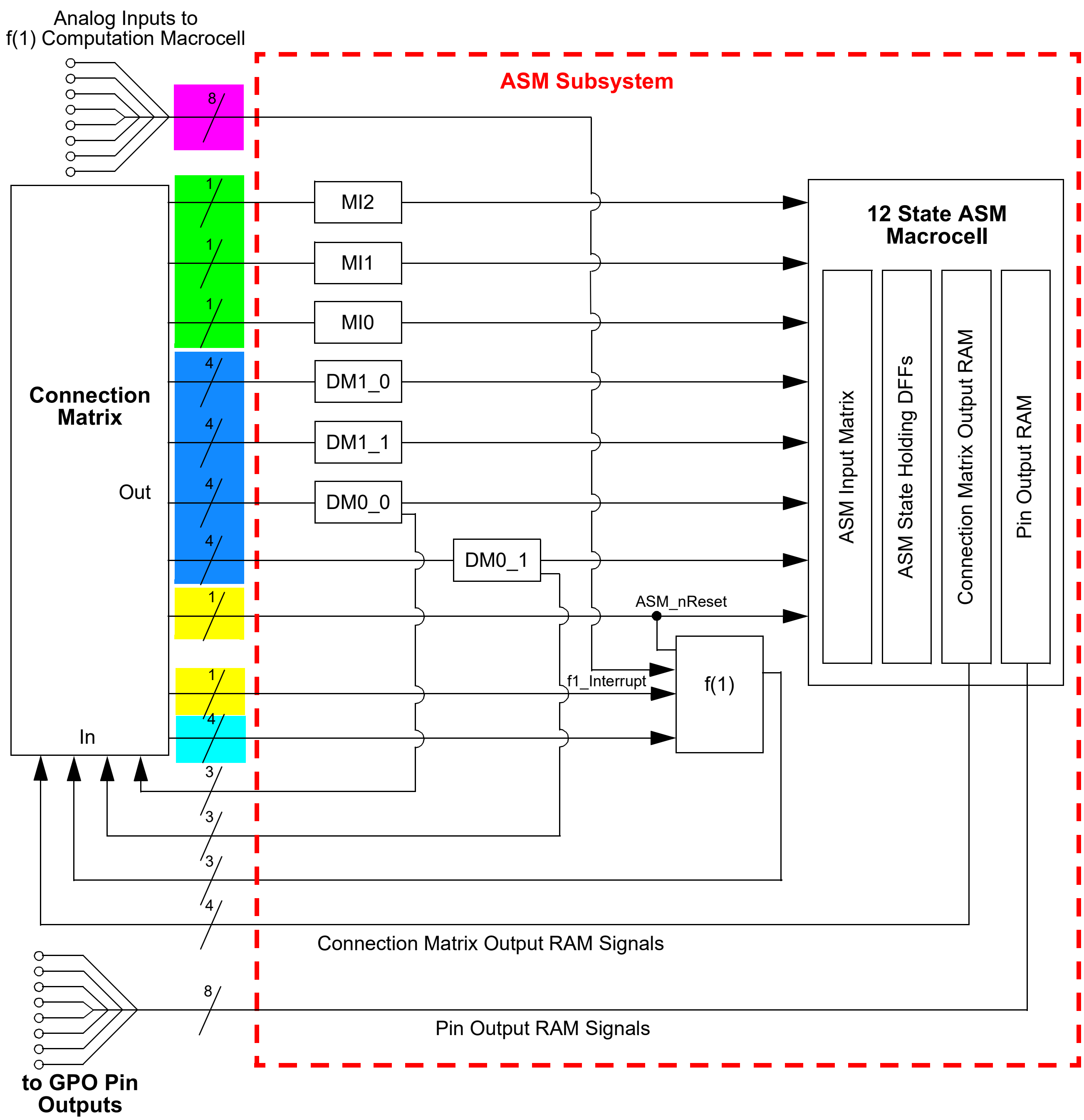


Figure 78: ASM Subsystem Input Signals

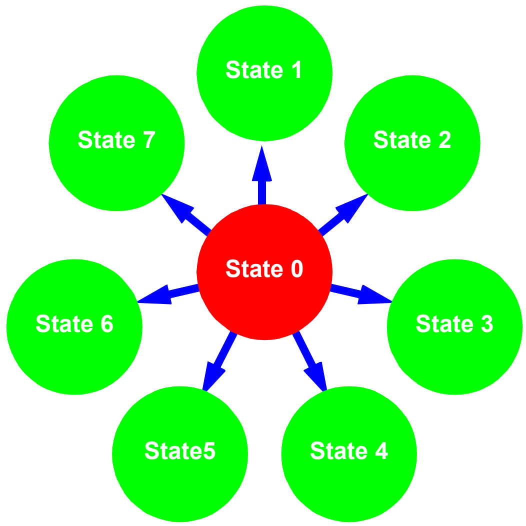


Figure 79: Maximum 7 State Transitions out of a Given State

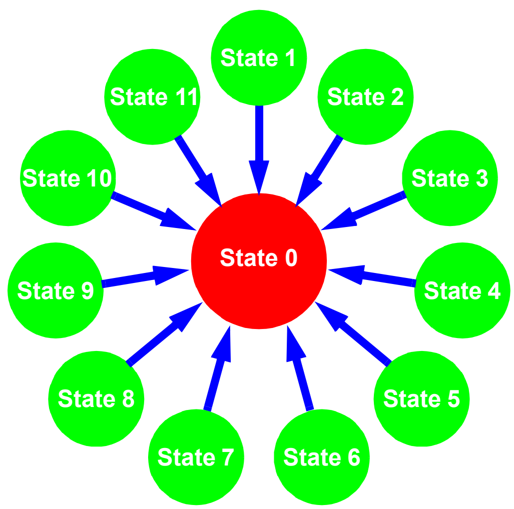


Figure 80: Maximum 11 State Transitions into Given State

14.3 ASM SUBSYSTEM OUTPUT SIGNALS

The ASM subsystem has a total of 21 output signal lines, as shown in Figure 81.

There are a total of 4 output signals from the ASM macrocell which go to the Connections Matrix inputs and from there can be routed to other internal macrocells or pins. These signals are shown in Figure 81, highlighted in green. The 4 outputs are user defined for each of the possible 12 states. The user selection for the output states is held in the Connection Matrix Output RAM.

There are a total of 8 output signals from the ASM macrocell which go directly to the 8 GPOs. These signals are shown in Figure 81, highlighted in blue. The 8 outputs are user defined for each of the possible 12 states. The user selection for the output states is held in the Pin Output RAM. Each of these GPOs has a single selection bit which defines the GPO input source as either the ASM Output RAM signal or the Connection Matrix signal.

Two of the Dynamic Memory macrocells, DM0_0 and DM0_1, can be used as either a resource for generating input signals for driving state transitions in the ASM macrocell, or to generate signals for use in other parts of the user design. When used to generate signals for purposes other than ASM state transitions, each of these macrocells has three output signals that go to the Connection Matrix, and from there can be routed to other internal macrocells or pins. Each of these macrocells has a total of 3 output signals of this type. These signals are shown in Figure 81, highlighted in yellow.

The f(1) Computation Macrocell has 3 output signals that go to the Connection Matrix, and from there can be routed to other internal macrocells or pins. These signals are shown in Figure 81, highlighted in pink.

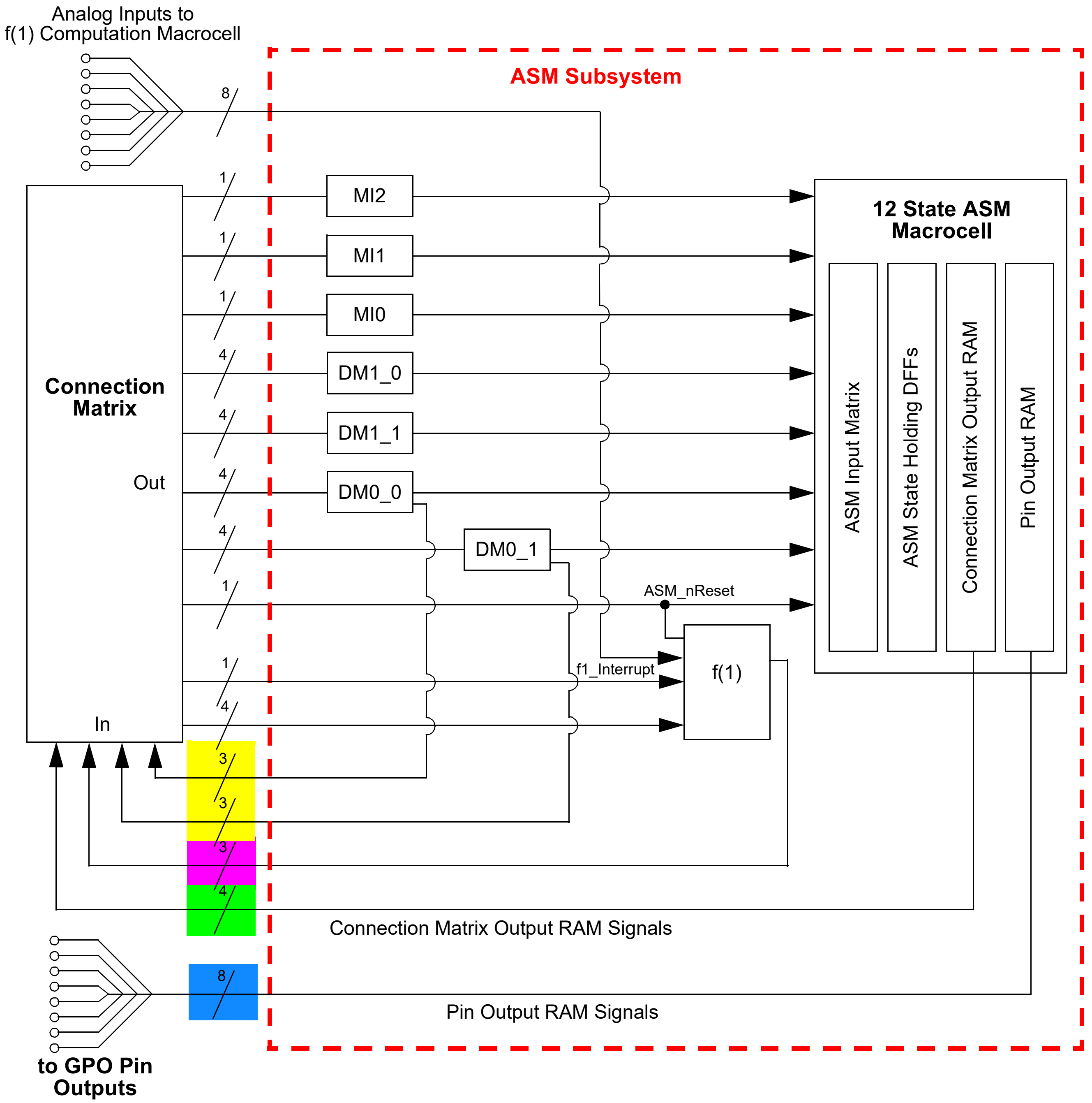


Figure 81: ASM Subsystem Input Signals

14.4 BASIC ASM_SUBSYSTEM TIMING

The basic state transition timing from input on one of 19 state transition input lines (4 going into each DMx_x and 3 from Connection Matrix going directly to the ASM macrocell) to the time when the 4 Connection Matrix Output RAM signals and 8 Pin Output RAM signals change is shown in Figure 82 and Figure 83. The time from a valid input signal to the time that there is a valid change of state, and valid signals on the 4 Connection Matrix Output RAM signals and 8 Pin Output RAM signals is State Machine Output Delay Time (Tst_out_delay).

At the point in time that the Connection Matrix Output RAM signals and Pin Output RAM signals are changing, the f(1) Computation Macrocell is prepared for executing commands coded for the new state, if the user has coded commands to execute. Based on the chosen commands, the f(1) Computation Macrocell outputs can change a number of times before the f(1) finishes for the new state. The ASM Subsystem will not be ready for the next state transition until the f(1) Computation Macrocell has completed the commands for the new state, or until it is reset by asserting the f1_Interrupt input from the Connection Matrix. The period of time between the input on one of the 7 inputs to the ASM macrocell and the ASM subsystem being ready for the next state transition input is State Machine Sequential Delay Time (Tst_sequential_delay).

From the input on one of 19 state transition input lines, there is a delay before the outputs are latched from the DM0_0 and DM0_1 macrocells, noted as DM Connection Matrix Output Delay Time (Tst_dmlatch_delay).

During state transitions, there will be no change in output levels on other states than the one state going active→inactive and the other state going inactive→active

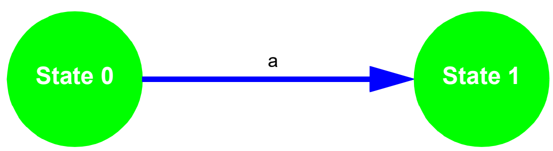


Figure 82: State Transition

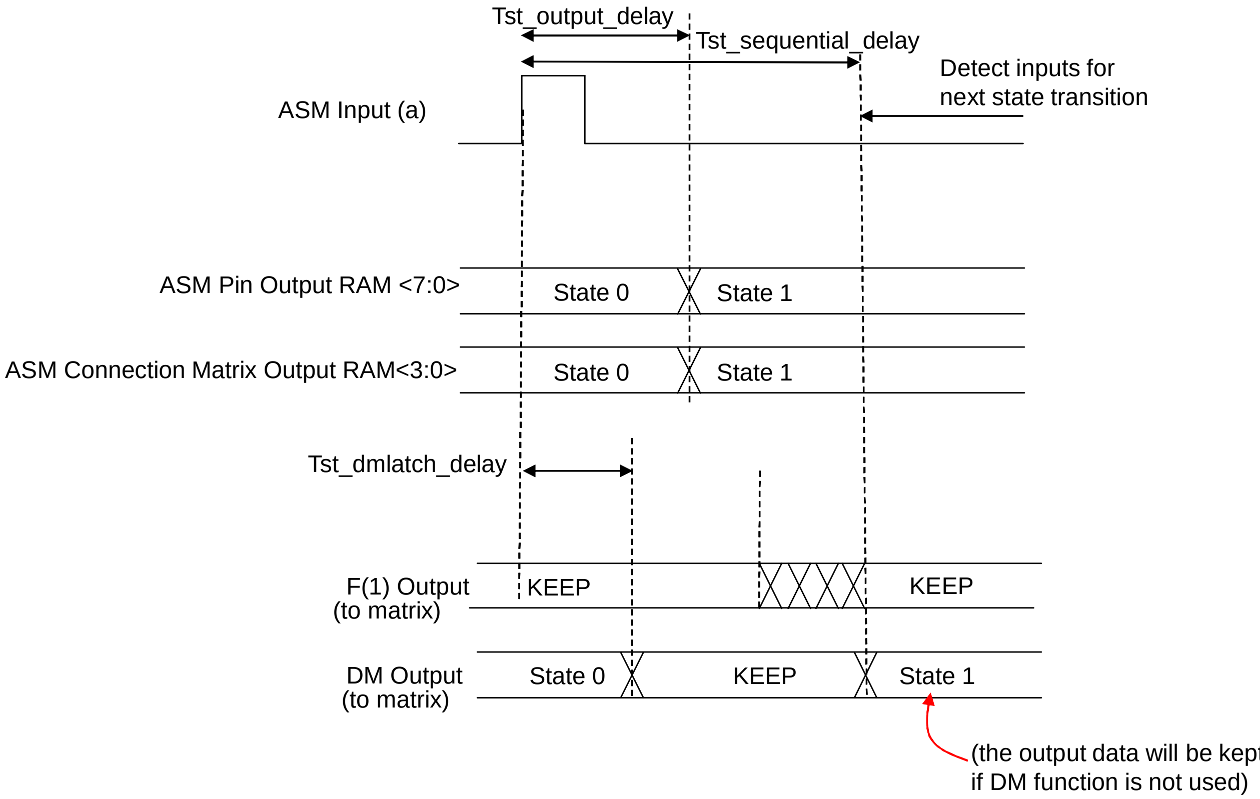


Figure 83: State Transition Timing

14.5 ASM POWER CONSIDERATIONS

A benefit of the asynchronous nature of this macrocell is that it will consume power only during state transitions. shown in Figure 84 and Figure 85, the current consumption of the macrocell will be a fraction of a μA between state transitions, and will rise only during state transitions. This is assuming that the DLY/CNT inside each DMx_x macrocells are also in-active. See table Table 8 to find average current during state transitions.

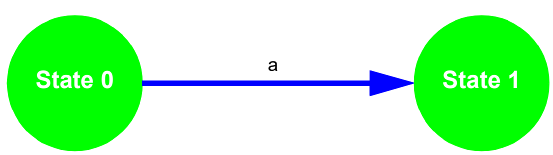


Figure 84: State Transition

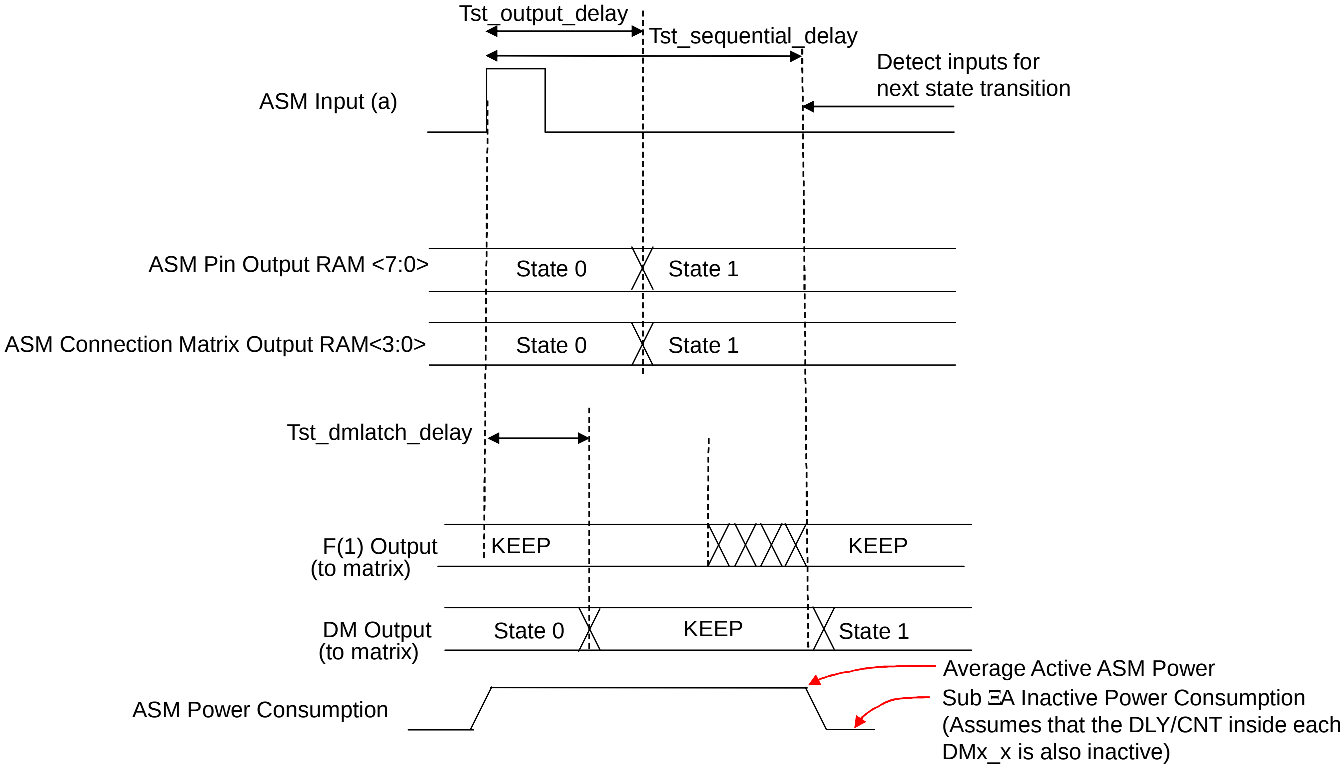


Figure 85: State Transition Timing and Power Consumption

14.6 ASYNCHRONOUS STATE MACHINES VS. SYNCHRONOUS STATE MACHINES

It is important to note that this macrocell is designed for asynchronous operation, which means the following:

1. No clock source is needed, it reacts only to input signals.
2. The input signals do not have to be synchronized to each other, the macrocell will react to the earliest valid signal for state transition.
3. This macrocell does not have traditional set-up and hold time specifications which are related to incoming clock, as this macrocell has no clock source.
4. The macrocell only consumes power while in state transition.

14.7 ASM SPECIAL CASE TIMING CONSIDERATIONS

14.7.1 State Transition Pulse Input Timing

All inputs to the ASM macrocell are level sensitive. If the input to the state machine macrocell for a state transition is a pulse, there is a minimum pulse width on the input to the state machine macrocell (as measured at the matrix input to the macrocell) which is guaranteed to result in a state transition shown in Figure 86 and Figure 87. This pulse width is defined by the State Machine Input Pulse Acceptance Time (Tst_pulse). If a pulse width that is shorter than Tst_pulse is input to the state machine macrocell, it is indeterminate whether the state transition will happen or not. If a pulse that is rejected (invalid due to the pulse width being narrower than the guaranteed minimum of Tst_pulse), this will not stop a valid pulse on another state transition input that does meet minimum pulse width.

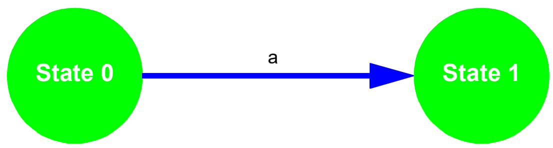


Figure 86: State Transition

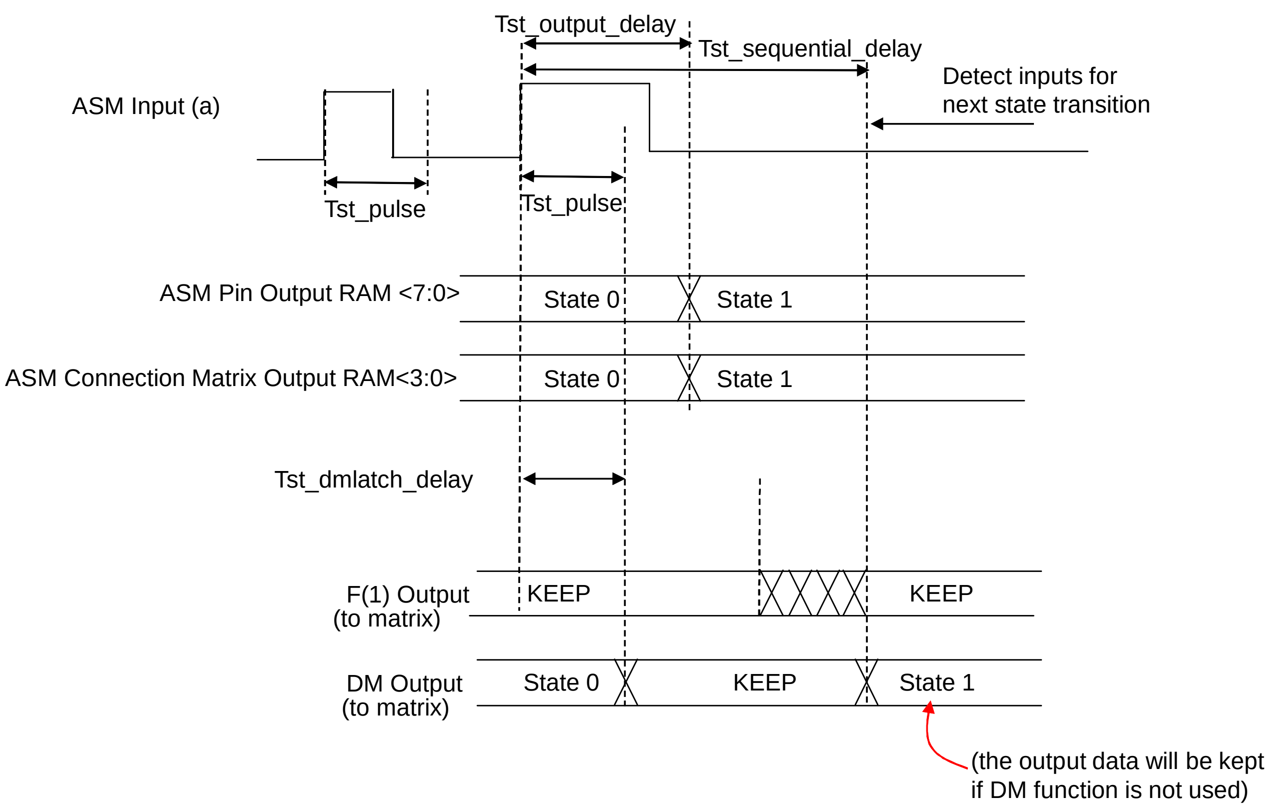


Figure 87: State Transition Pulse Input Timing

14.7.2 State Transition Competing Input Timing

There will be situations where two input signals can be valid inputs that will drive two different state transitions from a given state. In that sense, the two signals are "competing" (signals a and b in Figure 88), and the signal that arrives sooner should drive the state transition that will "win", or drive the state transition. If one signal arrives Tst_comp before the other one, it is guaranteed to win, and the state transition that it codes for will be taken, as shown in Figure 89. If the two signals arrive within Tst_comp of each other, it will be indeterminate which state transition will win, but one of the transitions will take place as long as the winning signal satisfies the pulse width criteria described in the paragraph above, as shown in Figure 90.

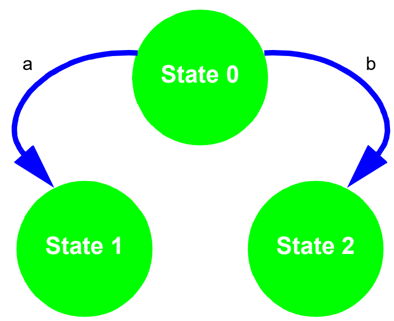


Figure 88: State Transition - Competing Inputs

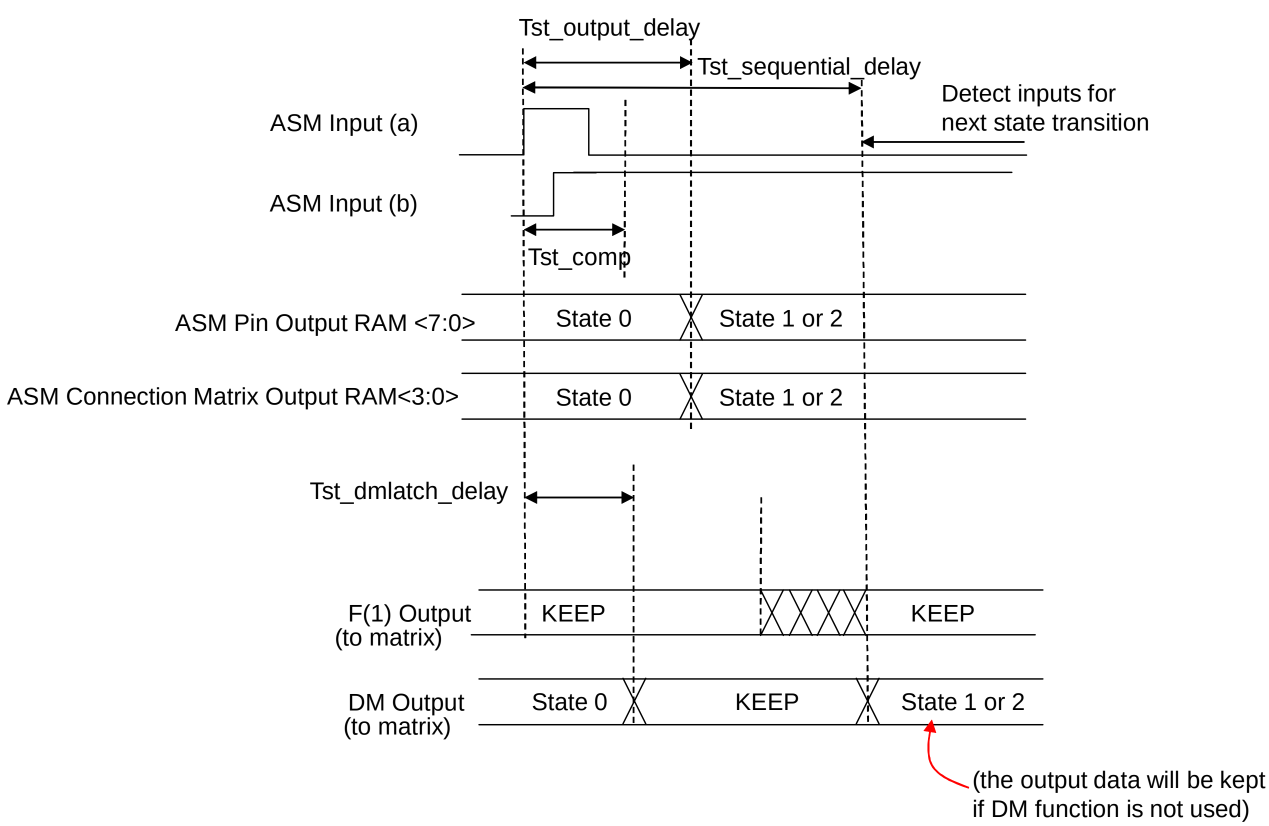


Figure 89: State Transition Timing - Competing Inputs Indeterminate

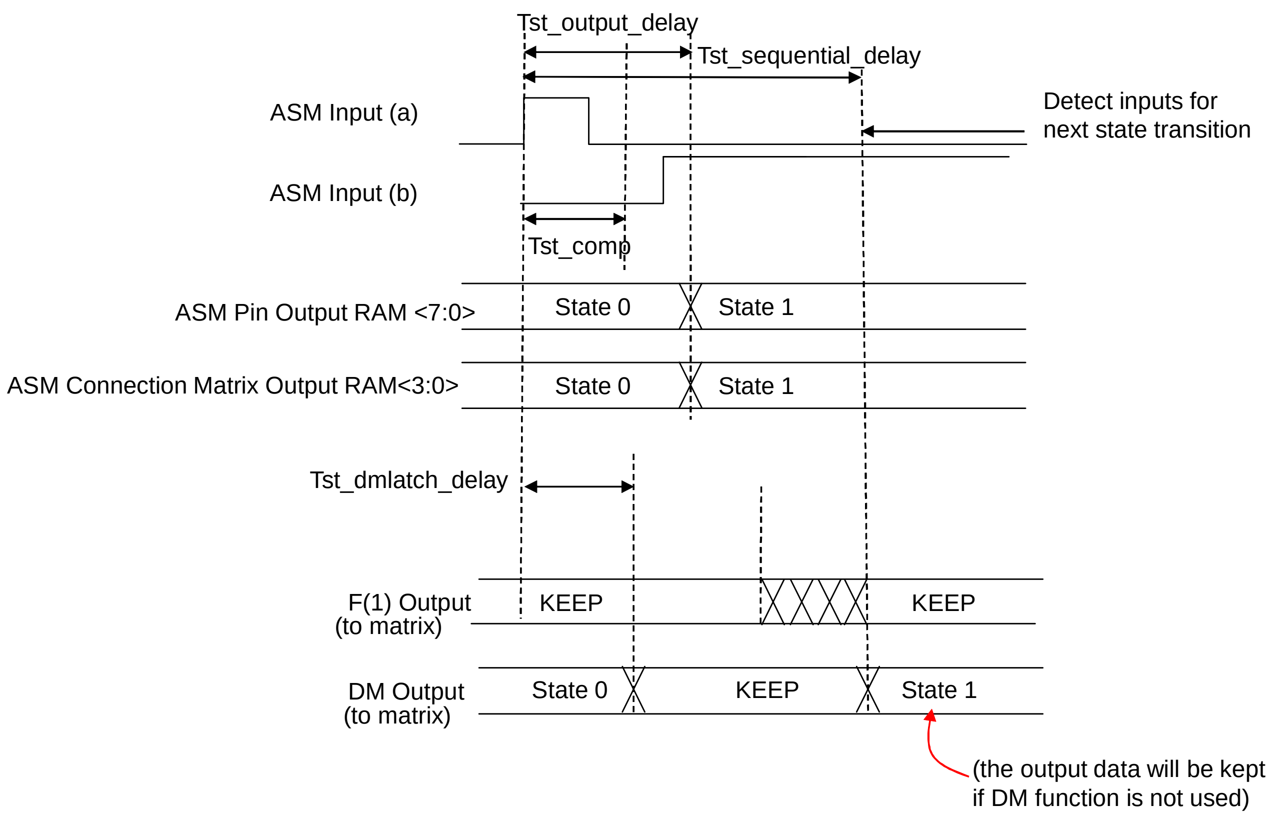


Figure 90: State Transition Timing - Competing Inputs Determinable

14.7.3 ASM State Transition Sequential Timing

It is possible to have a valid input signal for a transition out from a particular state be active before the state is active. If this is the case, the macrocell will only stay in that particular state for Tst_sequential_delay time before making the transition to the next state. An example of this sequential behavior is shown in Figure 91 and the associated timing is shown in Figure 92.

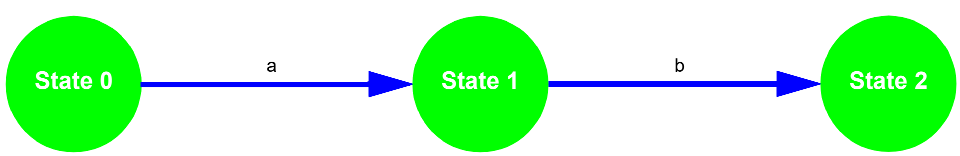


Figure 91: State Transition - Sequential

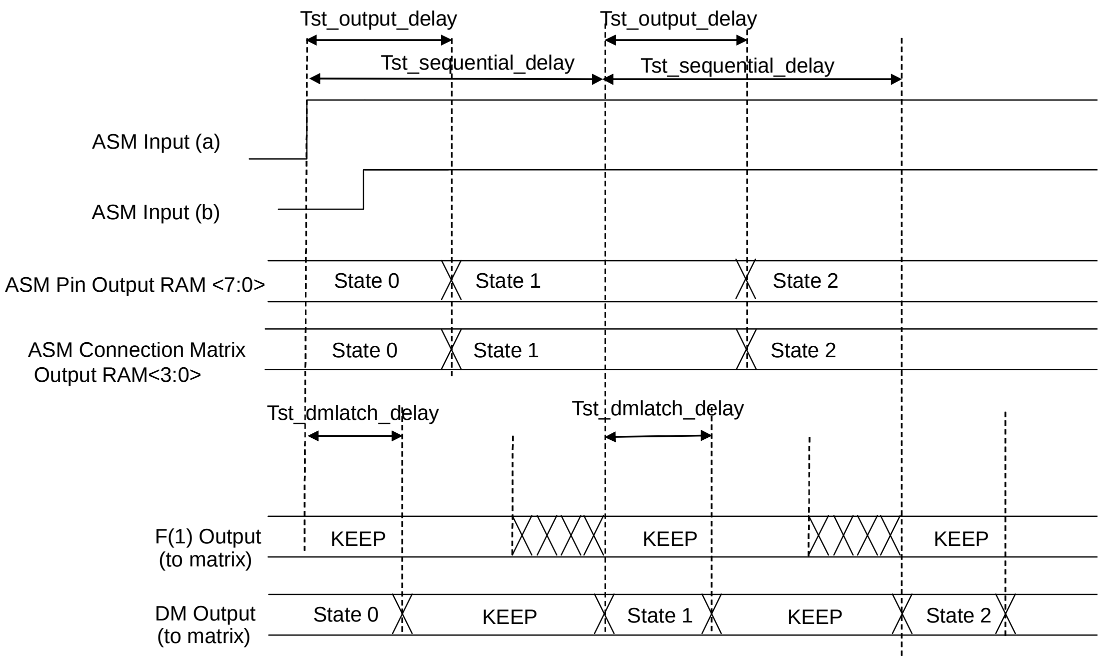


Figure 92: State Transition - Sequential Timing

14.7.4 State Transition Closed Cycling

It is possible to have a closed cycle of state transitions that will run continuously if there are valid inputs that are active at the same time. The rate at which the state transitions will take place is determined by Tst_sequential_delay, which determines the timing from one state transition signal that is accepted (and causes a state transition) to the ASM Subsystem being ready for the next input signal. The example shown in Figure 93 involves cycling between two states, but any number of two – twelve states can be included in state transition closed cycling of this nature. Figure 94 shows the associated timing for closed cycling.

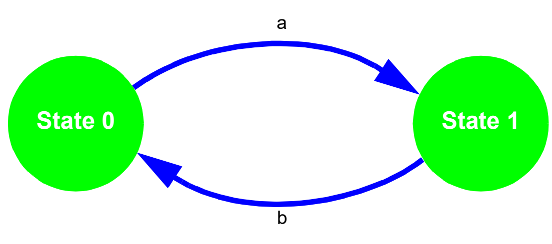


Figure 93: State Transition - Closed Cycling

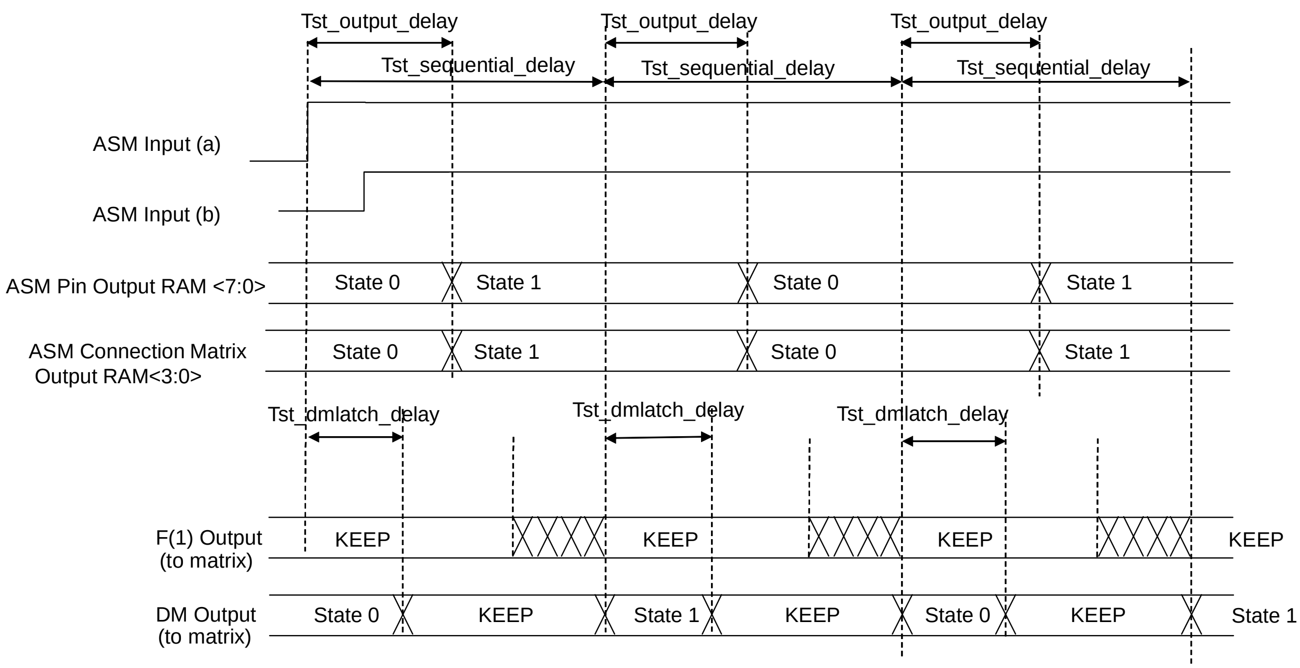


Figure 94: State Transition - Closed Cycling Timing

15 Asynchronous State Machine Macrocell

15.1 ASYNCHRONOUS STATE MACHINE OVERVIEW

The Asynchronous State Machine macrocell is one of several macrocells in the Asynchronous State Machine Subsystem, and it's specific role is to hold one active state at a time, and to facility user defined state transitions in a fast and power efficient manner. This macrocell is designed to allow the user to create state machines with between 2 to 12 states. When combined with the other macrocells in the ASM subsystem [four Dynamic Memory (DMx_x) macrocells, three Matrix Interface (MIx) macrocells, and one f(1) Computation Macrocell], the user has flexibility to define the available states, the available state transitions, and the input signals (a, b, c …) that will cause transitions from one state to another state, as shown in the example in Figure 95.

The ASM macrocell has a total of 8 input signal lines, as shown in Figure 96, which come from a combination of three Matrix Interface (MI) macrocell outputs and DM macrocell outputs. Of these 8 inputs, 3 are user selectable inputs coming from the three Matrix Interface (MI) macrocells (one per macrocell) to the ASM macrocell. There are also 4 inputs that come from the DMx_x macrocells (one per macrocell). There is 1 ASM_nReset input that is for driving a state transition in the ASM macrocell to a user defined Initial/Reset state.

The ASM macrocell has a total of 12 output signal lines, as shown in Figure 97, There are a total of 4 output signals which go to the Connections Matrix inputs, and from there can be routed to other internal macrocells or pins. The 4 output signals are user defined for each of the possible 12 states. There are a total of 8 output signals which go directly to the 8 GPOs. The 8 outputs are user defined for each of the possible 12 states.

In using this macrocell, the user must take into consideration the critical timing required on all input and output signals. The timing waveforms and timing specifications for this macrocell are all measured relative to the input signals (which come into the macrocell on the Connection Matrix outputs) and on the outputs from the macrocell (which are direct connections to Connection Matrix inputs). The user must consider any delays from other logic and internal chip connections, including IO delays, to insure that signals are properly processed, and state transitions are deterministic.

It is also important to note that the timing for the ASM Subsystem will change based on changes in temperature and system voltage. The user design that implements a state machine function must take into consideration, and be tolerant of this variation

The GPAK Designer development tools support user designs for the ASM macrocell at both the physical level and logic level. Figure 96 is a representation of the user design at the logical level, and Figure 96 shows the physical resources inside the various macrocells in the ASM Subsystem. To best utilize this subsystem, the user must develop a logical representation of their desired state machine, as well as a physical mapping of the input and outputs required for the desired functionality.

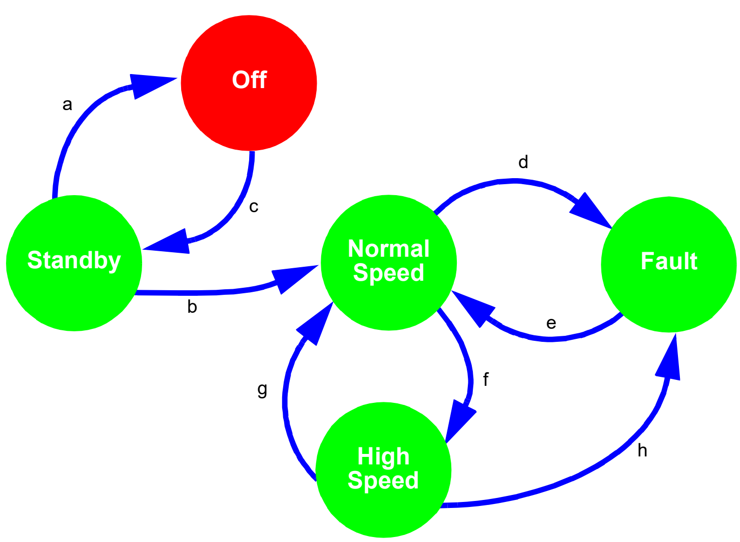


Figure 95: Asynchronous State Machine State Transitions

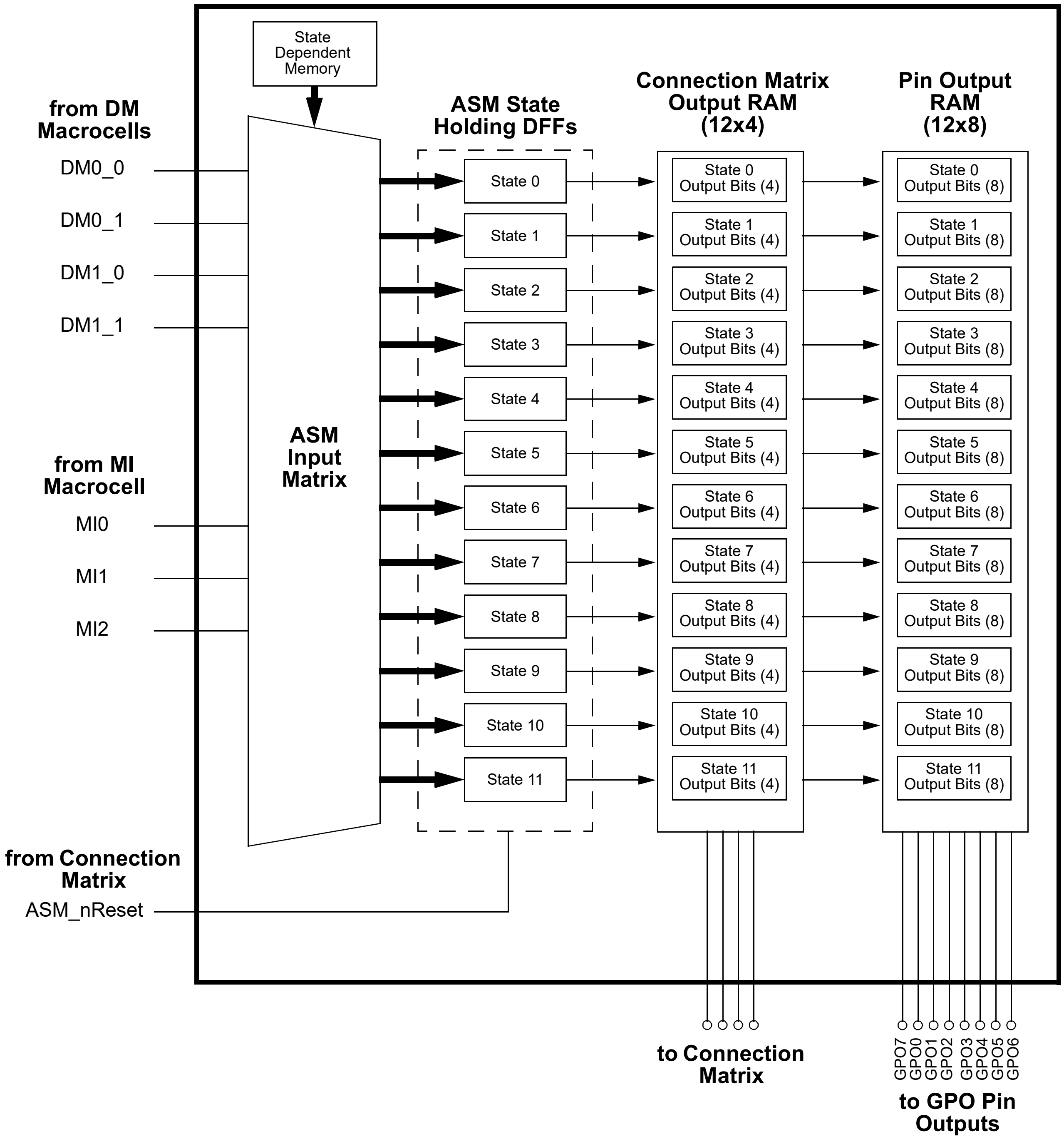


Figure 96: 12 State ASM Macrocell

15.2 ASM MACROCELL INPUT SIGNALS

The ASM macrocell has a total of 8 input signal lines, as shown in Figure 96, which come from a combination of Connection Matrix outputs and DM macrocell outputs.

There are 3 user selectable input signals that come from the MIx macrocells (one per macrocell) to the ASM macrocell. These signals are shown in Figure 98, highlighted in green. Each of these input signals are level sensitive and active high. A high level signal on any of these inputs can be enabled to drive a state transition, depending on the coding in the ASM Input Matrix.

There are 4 input signals that come from the DMx_x macrocells (one per macrocell). These signals are shown in Figure 98, highlighted in blue. Each of these input signals are level sensitive and active high. A high level signal on any of these inputs can be enabled to drive a state transition, depending on the coding in the ASM Input Matrix.

There is 1 ASM_nReset input that is for driving a state transition in the ASM macrocell to an user defined Initial/Reset state. This signal is shown in Figure 98, highlighted in yellow. This input signal is level sensitive and active low.

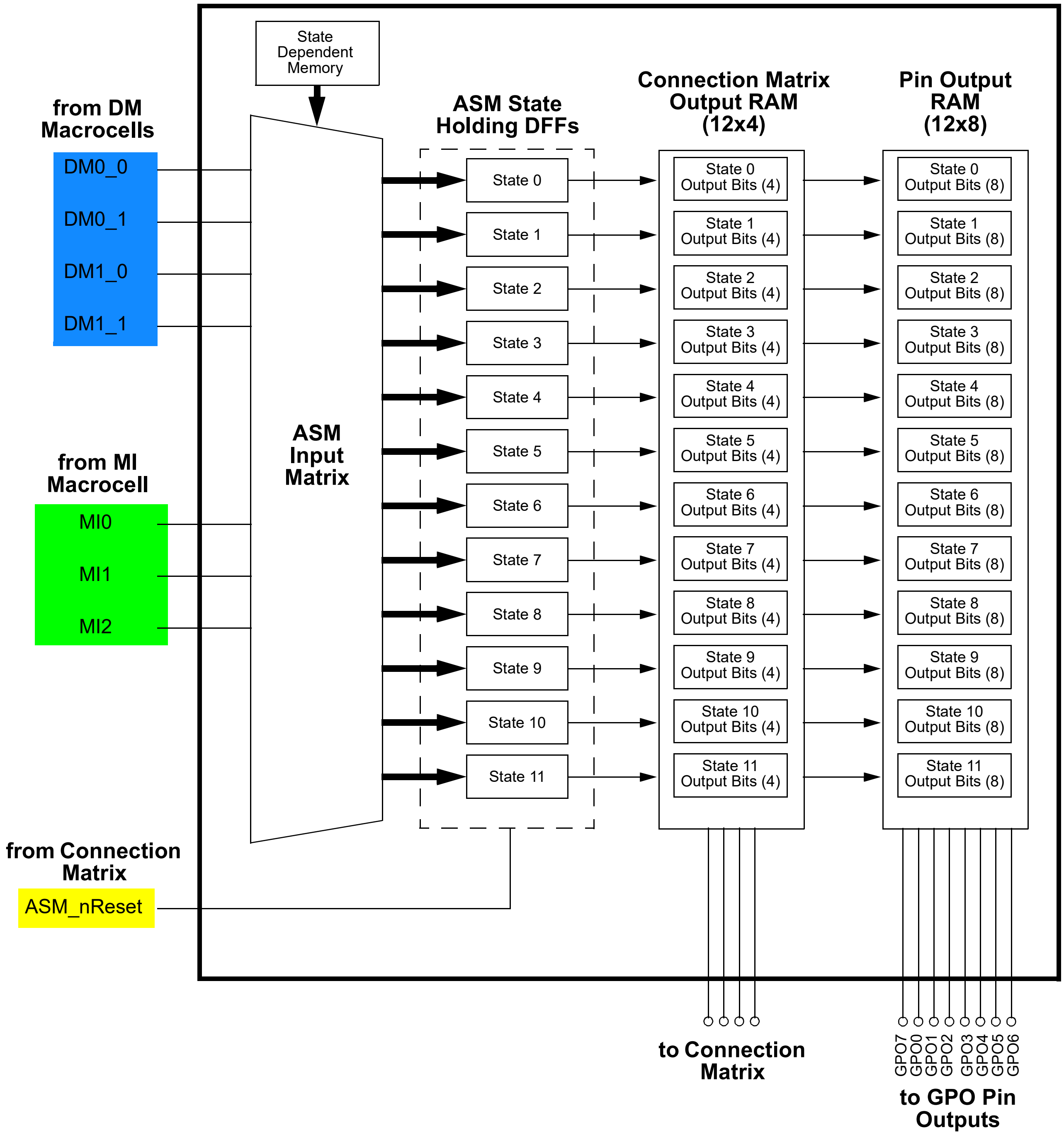


Figure 97: ASM Macrocell Input Signals

15.2.1 ASM Macrocell Output Signals

The ASM macrocell has a total of 12 output signal lines, as shown in Figure 98.

There are a total of 4 output signals which go to the Connections Matrix inputs, and from there can be routed to other internal macrocells or pins. These signals are shown in Figure 98, highlighted in green. The 4 outputs are user defined for each of the possible 12 states. The user defined values for these outputs is stored in the Connection Matrix Output RAM which is 12 x 4 in size (12 states x 4 outputs), for a total of 48 bits.

There are a total of 8 output signals which go directly to the 8 GPOs. These signals are shown in Figure 98, highlighted in blue. The 8 outputs are user defined for each of the possible 12 states. The user defined values for these outputs is stored in the Connection Matrix Output RAM which is 12 x 8 in size (12 states x 8 outputs), for a total of 96 bits. Each of the 8 GPOs has an internal mux that will either accept a signal from the outputs defined here, or directly from a Connection Matrix output. This mux in each GPO is under control of a register bit.

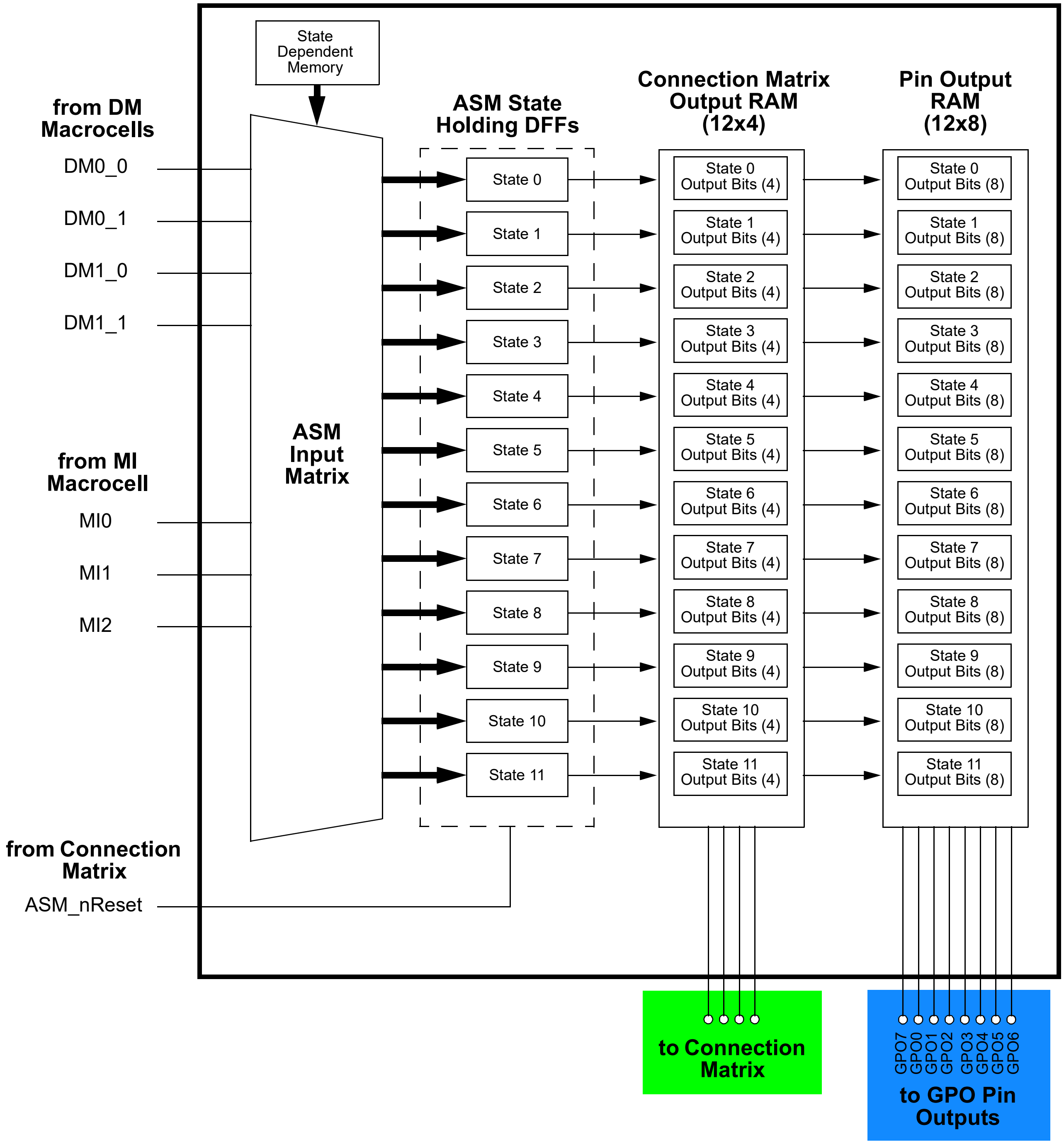


Figure 98: ASM Macrocell Output Signals

15.3 ASM LOGICAL VS. PHYSICAL DESIGN

A successful design with the ASM macrocell must include both the logic level design as well as the physical level design. The GPAK Designer development software support user designs for the ASM macrocell at both the logic level and physical level. The logic level design of the user defined state machine takes place inside the ASM Editor. In the ASM Editor, the user can select and name states, define and name allowed state transitions, define the Initial/Reset state and define the output values for the 8 outputs in the Pin Output RAM and 4 outputs in the Connection Matrix Output RAM. The physical level design takes place in the general GPAK Designer window, and here the user makes connections for the sources for ASM input signals, as well as making connections for destinations for ASM output signals.

16 Dynamic Memory Macrocell

16.1 DYNAMIC MEMORY MACROCELL OVERVIEW

The ASM Sub-System includes several discrete macrocells, including the ASM macrocell, four Dynamic Memory (DMx_x) macrocells, and one f(1) Computation Macrocell. These macrocells are designed to work as a system for building user defined state machines.

The Dynamic Memory (DM) macrocells have the characteristic that they can change internal configuration characteristics and their connections to the Connection Matrix based on the current state of the State Machine (SM) macrocell. This is accomplished by making different memory register bit settings contained within the macrocell active, based on the current active state of the SM. This allows the user to “repurpose” the resources inside these macrocells to match the circuit needs in various states.

There are two different types of DM macrocells, which vary slightly in the resources available inside the DM macrocell, as well as the connectivity to the Connection Matrix. The SLG46880/81 has a total of four DM macrocells. DM0_0 and DM0_1 have the same structure and resources as each other, and DM1_0 and DM1_1 also have the same structure and resources as each other. The DM0_x macrocells include all the functionality of the DM1_x macrocells, but they also have an output control capability, which is optimized for using the output of this macrocell to drive IO pin output states though the Connection Matrix. The DM CNT included in the DM0_x macrocells has more operating modes than the equivalent structure in the DM1_x macrocells.

Each DM macrocell has a DMx_x Configuration Register Table, which is a bank of 6 DMx_x Configuration Registers. The bits in these registers hold user selections which define all functional aspects of the behavior for the DM macrocell, including input connections from the Connection Matrix, DM LUT settings, DM CNT settings and settings of muxing internal to the DM macrocell. The fact that there are 6 Configuration Registers means that there can only be a total of six unique configurations for each DMx_x macrocell. There are a total of twelve states, which means that the user can either re-use the configuration coded in a particular DMx_x Operating Mode Register in more than one state, or not use some DMx_x macrocells in some states.

Each DM macrocell has a DMx_x Configuration Selection Table, which is a bank of 12 Configuration Selection Registers, one for each state of the State Machine macrocell. The bits in these registers hold the user’s selection of DM functional behavior, by mapping to a particular selection in the Configuration Register Table, based on the current state of the State Machine macrocell.

16.2 DM0_0 AND DM0_1 MACROCELL ARCHITECTURE

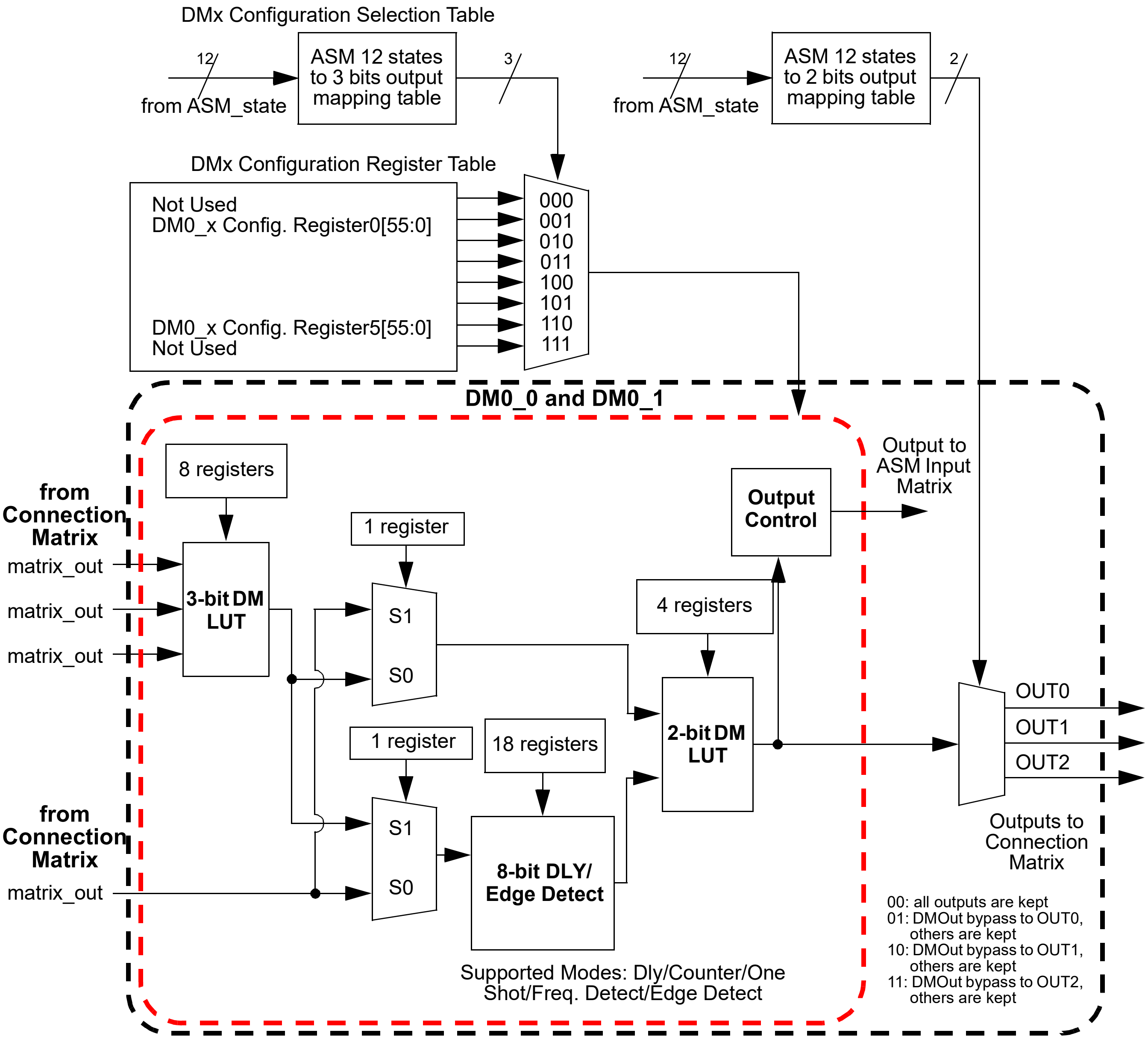


Figure 99: DM0_0/DM0_1

16.3 DM1_0 AND DM1_1 MACROCELL ARCHITECTURE

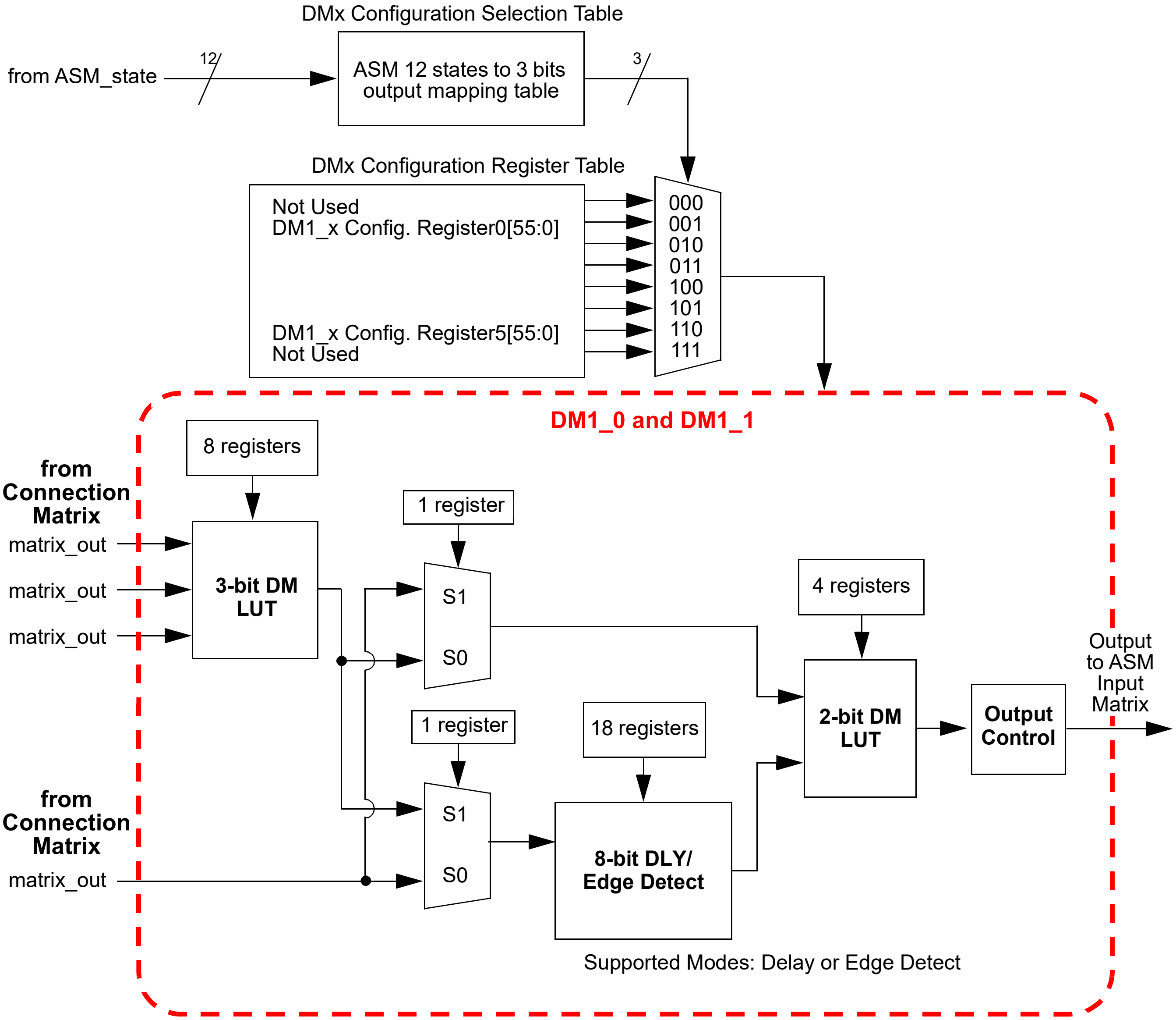


Figure 100: DM1_0/DM1_1

16.4 DMX_X MACROCELL INPUT SIGNALS

Each DMx_x macrocell has 4 digital input signals coming from the Connection Matrix and from there can be routed to other internal macrocells or pins. These 4 signals are shown in Figure 101 and Figure 102, highlighted in blue.

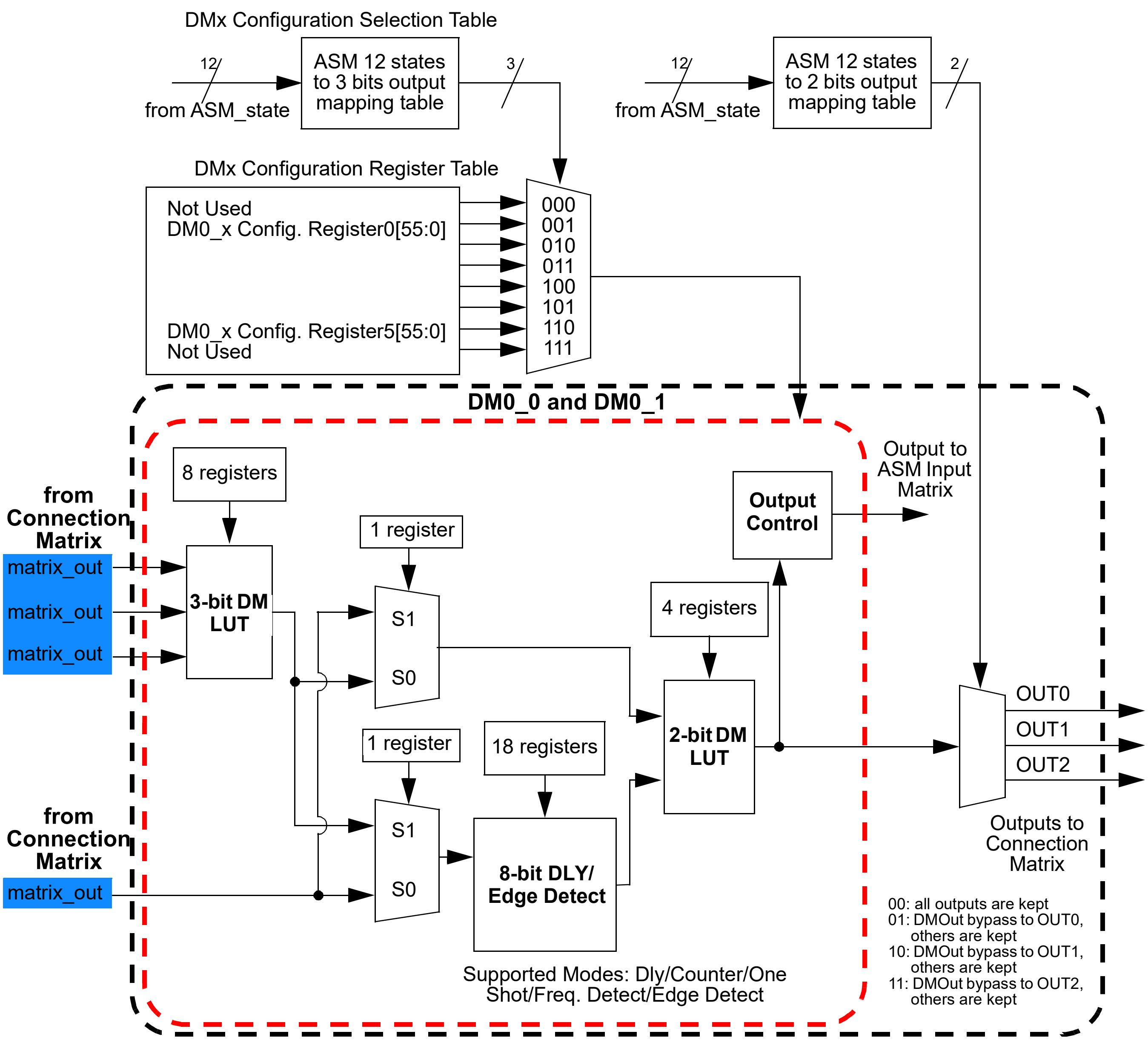


Figure 101: DM0_0/DM0_1 Inputs

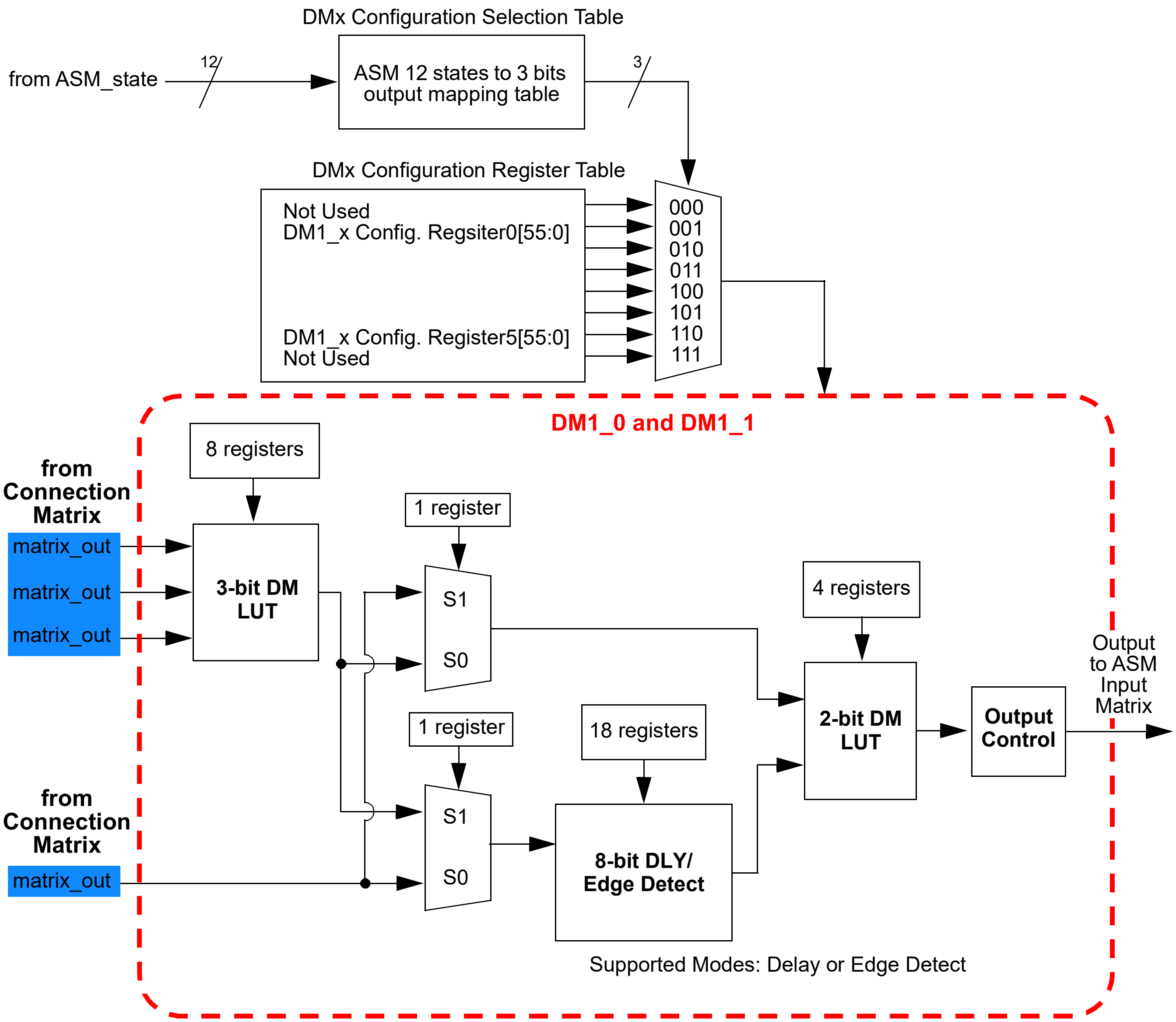


Figure 102: DM1_0/DM1_1 Inputs

16.5 DMX_X MACROCELL OUTPUT SIGNALS

Each DMx_ x macrocell has 1 digital output signal, which goes directly to the ASM Input Matrix inside the ASM Macrocell. This signal is shown in Figure 103 and Figure 104, highlighted in blue.

Additionally, the DM0_0 and DM0_1 Macrocells each have 3 digital output signals which go to the Connection Matrix and from there can be routed to other internal macrocells or pins. These 3 signals are shown in Figure 103, highlighted in green.

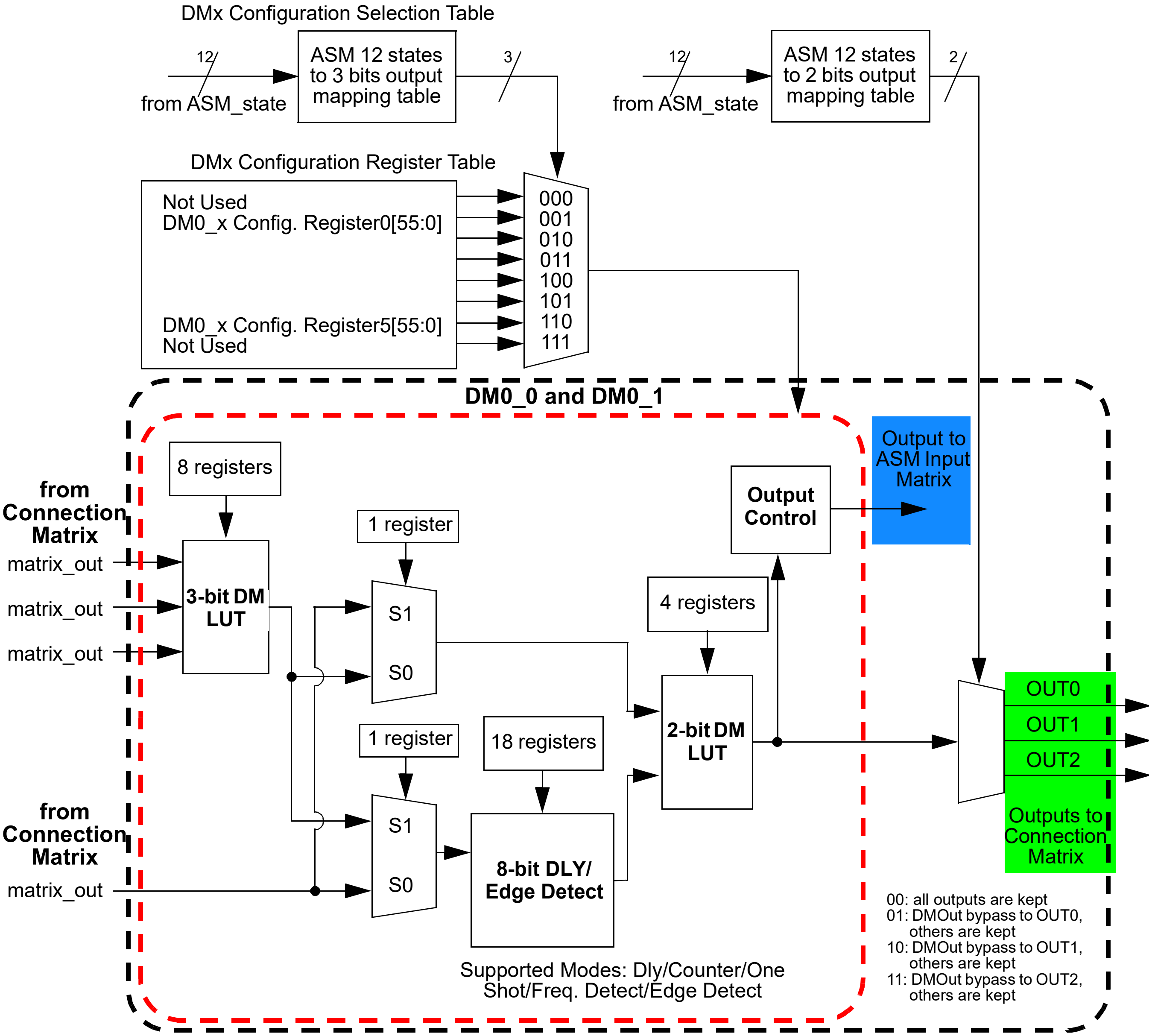


Figure 103: DM0_0/DM0_1 Outputs

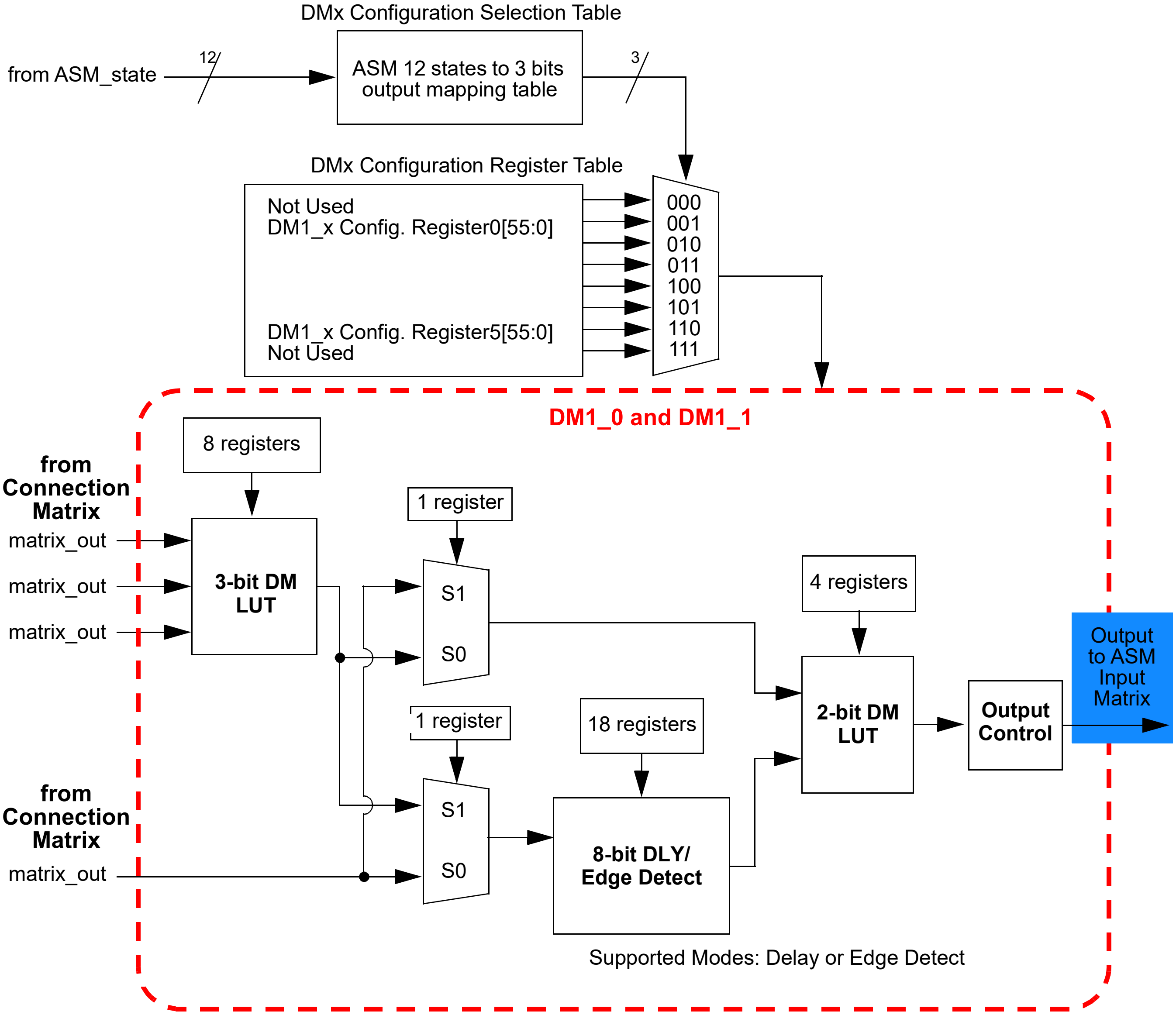


Figure 104: DM1_0/DM1_1 Outputs

17 f(1) Computation Macrocell

17.1 F(1) COMPUTATION MACROCELL OVERVIEW

The f(1) Computation Macrocell consists of a specialized state machine which is optimized for simple data manipulation activities on single data bit values. The operation of this macrocell can be initiated whenever the ASM Macrocell enters a new state, and can execute a string of up to 12 commands for loading and storing 1 bit data, as well as doing simple logical functions such as ANDs, ORs and XORs.

The only time the f(1) Computation Macrocell will begin to execute instructions is when the ASM Macrocell first enters a new state. At that point in time, the f(1) Computation Macrocell will execute the user selected commands, if any, that are associated with that particular ASM state. When the f(1) Computation Macrocell completes the commands, it will then relinquish control back to the ASM Macrocell. During the time that the f(1) Computation Macrocell is active, there can be no activity in the ASM microcell (i.e., the ASM Macrocell is prevented from any state transition during the time when the f(1) Macrocell is active).

The f(1) Computation Macrocell has two digital inputs, ASM_nReset and f1_Interupt. An active signal on either of these inputs will immediately halt any command execution for the f(1) Computation Macrocell, and will immediately relinquish control back to the ASM macrocell.

The f(1) Command Register Table has 4 registers, each of which holds a string of up to 12 commands to run when the f(1) Computation Macrocell is initiated. These 4 registers allow for 4 different command strings that the user can choose from. The f(1) Command Selection Table has 12 entries (one per ASM state), which allow the user to select which of the f(1) Command Registers will be used upon entry into each state. The user can also select that no commands are used in a particular state (one of the selection options for each entry in the f(1) Command Selection Table), in which case the f(1) Computation Macrocell is completely bypassed upon entry to that particular state.

There are a total of 8 analog inputs coming from various pins which can be muxed into the positive input for the f(1) Analog Comparator inside the f(1) Computation Macrocell. The f(1) Analog Comparator can be re-programmed for analog input source and negative input reference settings. The user selections for both positive input signal and negative reference are included as part of the information stored in the f(1) Command Register Table. This allows the user to make different analog measurements that are state dependent in their analog sources and reference settings.

This macrocell also includes a f(1) Memory Stack, which is 1 bit wide by 16 deep memory which is organized as a stack, and can serve as a data source or data destination for the commands running on the macrocell. LOADx commands will push data down into the stack. OUTx commands will pop data off the stack, and send to the contents of the Top-Of-Stack to one of three outputs of the f(1) macrocell to the Connection Matrix. The contents of this memory are not changed during ASM state transitions, and are only changed by the commands running inside the f(1) Computation Macrocell itself. The initial memory stack values are loaded from registers [3279:3264].

17.2 F(1) COMPUTATION MACROCELL ARCHITECTURE

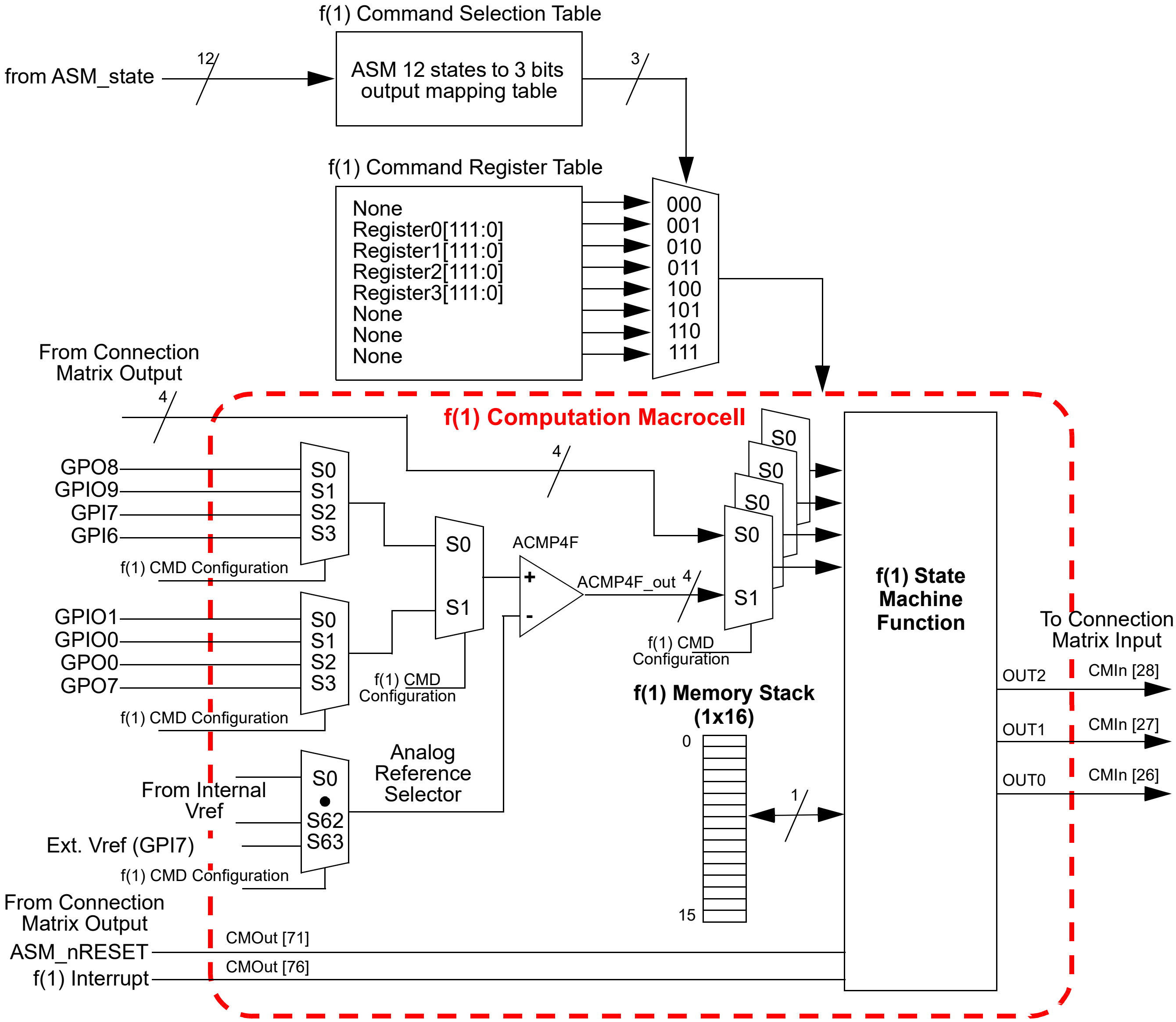


Figure 105: f(1) Computation Macrocell Architecture

17.3 F(1) COMPUTATION MACROCELL INPUT SIGNALS

The f(1) Computation Macrocell has 6 digital input signals, ASM_nReset, f1_Interupt, and four inputs from Connection Matrix outputs. An active signal on either of the first 2 inputs will immediately halt any command execution for the f(1) Computation Macrocell, and will immediately relinquish control back to the ASM macrocell. The ASM_nReset is a level sensitive signal, and active low. The f1_Interupt is a level sensitive signal, and active high. These signals are shown in Figure 106, highlighted in blue. Also there are 4 digital inputs from the Connection Matrix, which can be routed to any Connection Matrix outputs from the f(1) Commands. These signals are shown on Figure 106 highlighted in yellow.

There are a total of 8 analog inputs coming from various pins which can be muxed into the positive input for the f(1) Analog Comparator inside the f(1) Computation Macrocell. These signals are shown in Figure 82, highlighted in green. The f(1) Analog Comparator can be re-programmed for analog input source and negative input reference settings with settings inside the LOADx command. The user selections for both positive input signal and negative reference are included as part of the information stored in the f(1) Command Register Table. This allows the user to make different analog measurements that are state dependent in their analog sources and reference settings.

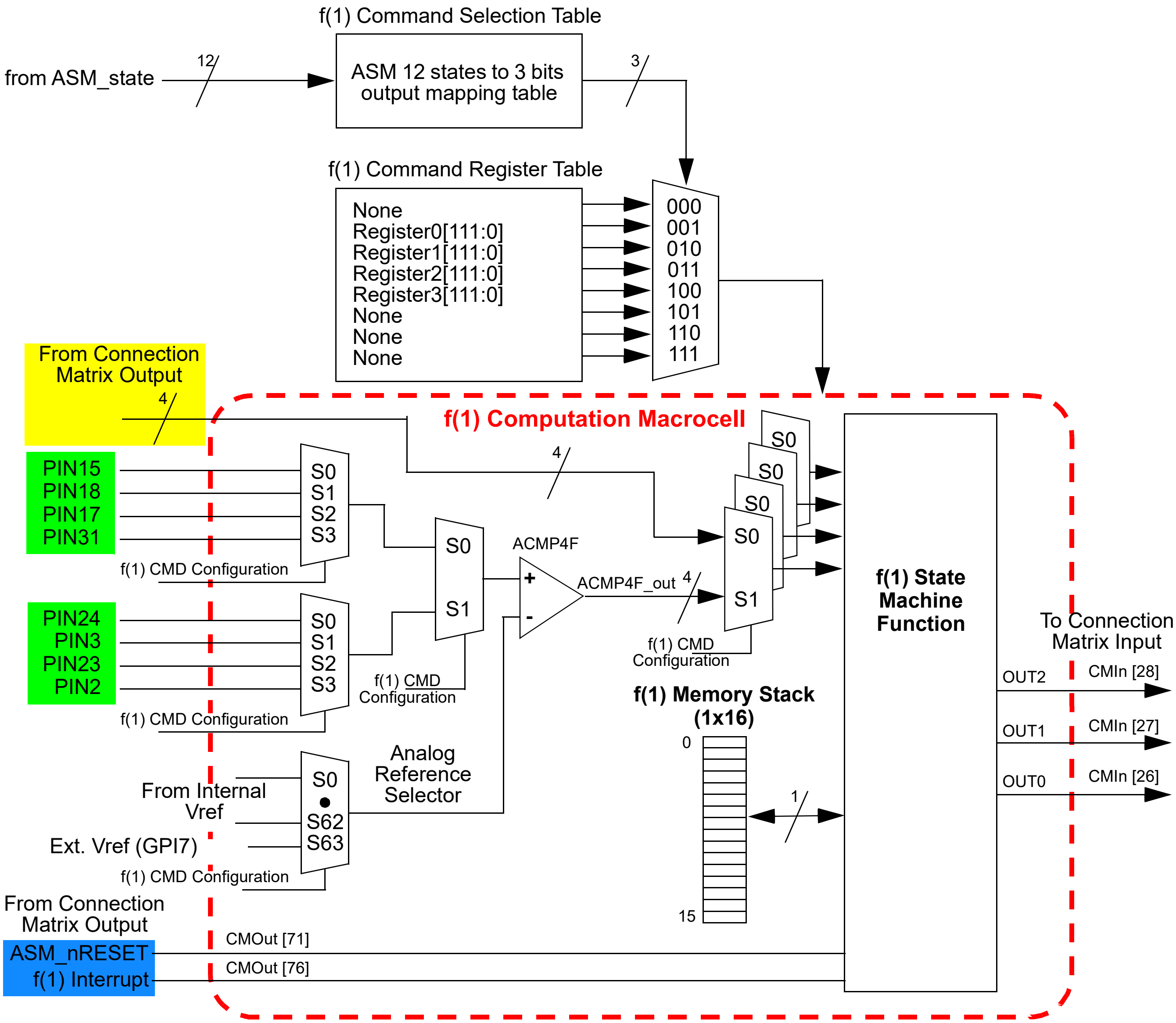


Figure 106: f(1) Computation Macrocell Input Signals

The f(1) interrupt signal comes from Connection Matrix Output. The high level f(1) interrupt signal forces the f(1) computation macrocell to immediately finish command execution and return control to the ASM similar to the END command. It is possible to load initial memory stack with the f(1) interrupt signal when register [3766] is high.

The ASM_nRESET low level signal forces the ASM macrocell and the f(1) computation macrocell to an initial state and an initial memory stack value.

17.4 F(1) COMPUTATION MACROCELL OUTPUT SIGNALS

The f(1) Computation Macrocell has 3 digital output signals that go to the Connection Matrix, and from there can be routed to other internal macrocells or pins. These signals are shown in Figure 107, highlighted in blue. The state of these output signals are under user control, and are changed based on the Output commands.

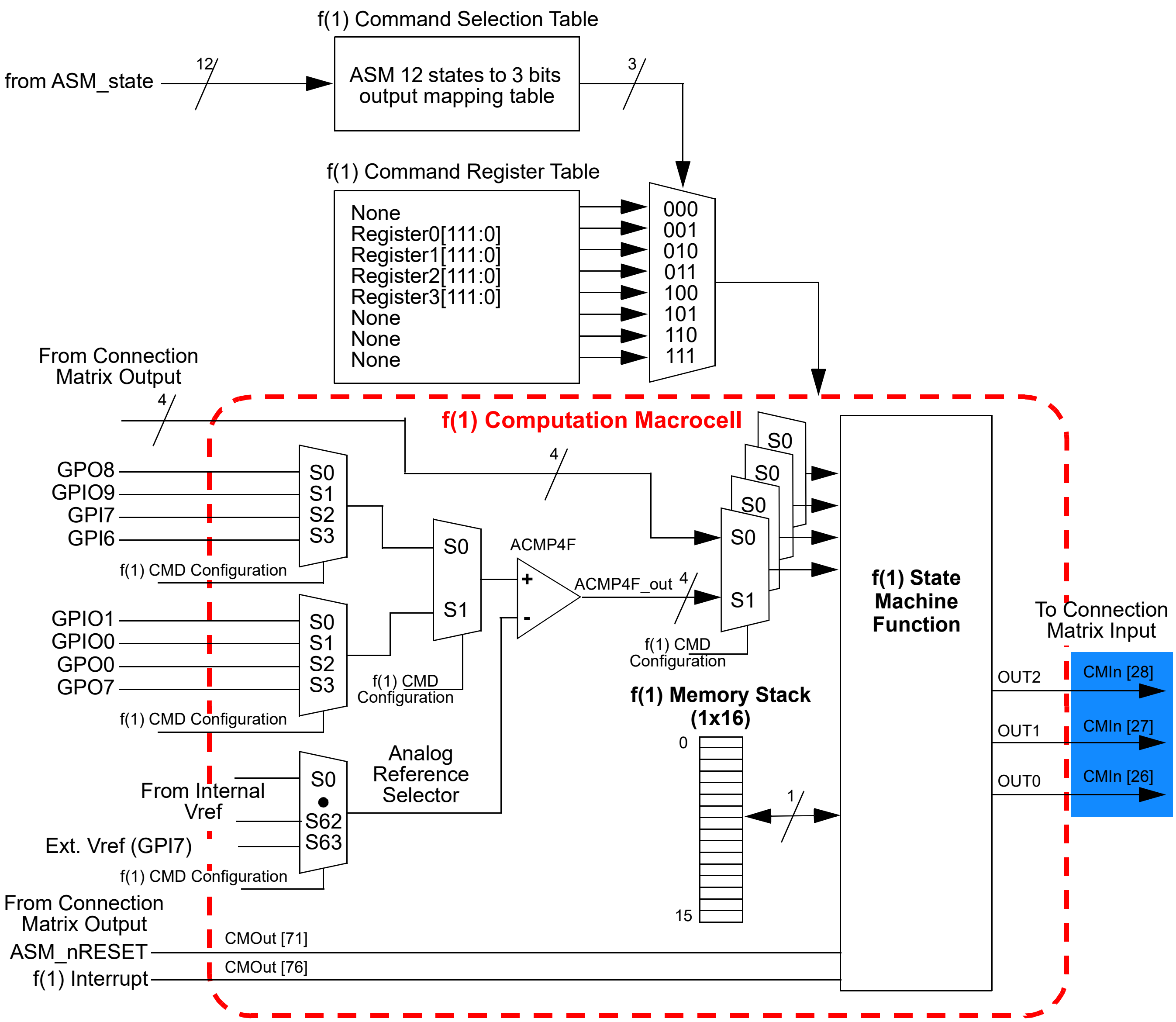


Figure 107: f(1) Computation Macrocell Output Signals

17.5 F(1) COMMAND REGISTERS

The f(1) Computation Macrocell consists of a specialized state machine which is optimized for simple data manipulation activities on single data bit values. The f(1) Computation Macrocell must be used for accessing the 8:1 analog multiplexer and associated analog comparator. The f(1) is also useful for storing state independent values, looping operations such as periodic signal checks, and for performing simple repetitive logic functions.

The operation of this macrocell can be initiated whenever the ASM Macrocell enters a new state, and can execute a string of up to 12 commands for loading and storing 1 bit data, as well as doing simple logical functions such as ANDs, ORs and XORs.

The f(1) Command Register Table has 4 registers, therefore 4 independent f(1) functions can be defined. Each state of the ASM can access one of the four f(1) configurable instances of the f(1).

Each of the four f(1) configurations may contain up to 12 commands which run when the f(1) Computation Macrocell is initiated. The list of available commands is as follows:

Command	Command Name	Command Description
0000	LOAD1	Loads a one bit value to the top of the memory stack (location 0). During the execution of this command, all other values are shifted down 1 location, and the value in location 15 is lost. The data loaded by Load 1 command is defined in the Load 1 register, which defines where the value is to be loaded from such as a pin, the f(1) comparator, etc.
0001	LOAD2	Loads a one bit value to the top of the memory stack (location 0). During the execution of this command, all other values are shifted down 1 location, and the value in location 15 is lost. The data loaded by Load 2 command is defined in the Load 2 register, which defines where the value is to be loaded from such as a pin, the f(1) comparator, etc.
0010	LOAD3	Loads a one bit value to the top of the memory stack (location 0). During the execution of this command, all other values are shifted down 1 location, and the value in location 15 is lost. The data loaded by Load 3 command is defined in the Load 3 register, which defines where the value is to be loaded from such as a pin, the f(1) comparator, etc.
0011	LOAD4	Loads a one bit value to the top of the memory stack (location 0). During the execution of this command, all other values are shifted down 1 location, and the value in location 15 is lost. The data loaded by Load 4 command is defined in the Load 4 register, which defines where the value is to be loaded from such as a pin, the f(1) comparator, etc
0100	AND	Performs a logical AND to the top two locations in the memory stack (location 0 and location 1). During execution of this command, the two values in the top two stack locations are deleted, and the logical AND result is pushed on the top of stack (location 0). In the process, all other values in the stack are shifted up 1 location, and a 0 is loaded in location 15.
0101	OR	Performs a logical OR to the top two locations in the memory stack (location 0 and location 1). During execution of this command, the two values in the top two stack locations are deleted, and the logical OR result is pushed on the top of stack (location 0). In the process, all other values in the stack are shifted up 1 location, and a 0 is loaded in location 15.
0110	XOR	Performs a logical XOR to the top two locations in the memory stack (location 0 and location 1). During execution of this command, the two values in the top two stack locations are deleted, and the logical XOR result is pushed on the top of stack (location 0). In the process, all other values in the stack are shifted up 1 location, and a 0 is loaded in location 15.
0111	INV	Performs a logical Invert (INV) to the top location in the memory stack (location 0). During execution of this command, the value in the top stack location is deleted, and the logical INV result is pushed on the top of stack. There is no effect on all other values in the stack.
1000	PUSH0	Pushes a 0 into the top location in the memory stack (location 0). During the execution of this command, all other values are shifted down 1 location, and the value in the location 15 is lost.
1001	POP	During execution of this command, values in the stack are shifted up 1 location, and a 0 is loaded in location 15.
1010	DELAY	The execution of commands by the f(1) Computation microcell is delayed by a period of time defined in the configuration of the delay function. Once this time period is completed, the next f(1) instruction will execute.
1011	LOOP with DELAY	If the top location in the memory stack (location 0) is equal to 0, the command execution in the f(1) Macrocell is delayed by a period of time defined in the configuration of the delay function and then executes the f(1) sequence at the specified jump location. If the top location in the memory stack (location 0) is equal to 1, the f(1) Macrocell proceeds with execution of the next command in sequence.
1100	OUT1	Outputs the top location in the memory stack (location 0) on matrix input OUT1
1101	OUT2	Outputs the top location in the memory stack (location 0) on matrix input OUT2
1110	OUT3	Outputs the top location in the memory stack (location 0) on matrix input OUT3
1111	END	Immediately ends execution of commands by f(1) Macrocell, and control is returned to ASM Macrocell

These commands form a machine level language that may be configured within GPAK Designer software using a simple GUI, as opposed to using a typical text editor. See application examples below:

Example #1: Sensor Application showing the command sequence for a potential use case of the f(1) Macrocell.

f(1) Command Sequence	Command	Description
1	INV	Change Top Memory location from 0 → 1
2	OUT1	Output a 1 to a pin defined by OUT1 register. This can be used to turn on or bias an external sensor
3	DELAY	Wait for a time defined by DELAY register. This can be used to allow sensor to settle.
4	LOAD1	Capture the output of f(1) ACMP from an analog pin connected to the sensor as defined by the LOAD1 register.
5	LOAD2	Capture the output of a pin as defined by the LOAD2 register. This can be used to check a power good signal
6	AND	Logically AND the top two values of the 1x16 memory that were just loaded with LOAD1 and LOAD2
7	OUT2	Output the result of sensor output AND power good signal for a control decision for the ASM
8	END	ASM can now act on OUT2 signal

Example #2: Power Good Application showing the command sequence for a potential use case of the f(1) Macrocell.

f(1) Command Sequence	Command	Description
1	LOAD1	Capture the output of f(1) ACMP from an analog pin connected to power rail 1 as defined by the LOAD1 register. A “1” means that power is good on power rail 1.
2	LOAD2	Capture the output of f(1) ACMP from an analog pin connected to power rail 2 as defined by the LOAD2 register. A “1” means that power is good on power rail 2.
3	LOAD3	Capture the output of f(1) ACMP from an analog pin connected to power rail 3 as defined by the LOAD3 register. A “1” means that power is good on power rail 3.
4	LOAD4	Capture the output of f(1) ACMP from an analog pin connected to power rail 4 as defined by the LOAD4 register. A “1” means that power is good on power rail 4.
5	AND	LOAD4 result ANDs with LOAD3 result (LOAD4 & LOAD3). This combines two of the Power Good signals.
6	AND	(LOAD4 & LOAD3) & LOAD2. This combines three of the Power Good signals.
7	AND	((LOAD4 & LOAD3) & LOAD2) & LOAD1. This combines four of the Power Good signals
8	OUT1	Output the Master Power Good signal to a location defined by the OUT1 register

The LOADx, OUTx, and DELAY/DELAY LOOP commands are required to be defined before using them.

17.5.1 Delay Command Configuration Bits

The Delay Command is defined by 12 bits. Each of the 4 instances of the f(1) command can configure a new value for the delays. However, the DELAY and DELAY LOOP use the same configuration data so these two delays must be identical.

Delay Configuration Bits

Configuration Bits	Description	
8 Bits	Delay Count (0 .. 255)	
3 Bits	Delay Clock	
	000	OSC2
	001	OSC2/4
	010	OSC1
	011	OSC1/8
	100	OSC1/64
	101	OSC0
	110	OSC0/8
	111	OSC0/64
1 Bit	ACMP Shutdown during Delay	ACMP is shutdown after data Load

17.5.2 LOADx Command Configuration Bits

There are two types of load configuration schemes. One method defines loading from one of eight analog pins via the f(1) ACMP. The other method defines loading from any of the matrix outputs connected to digital input pins, logic macrocells, ASM outputs, oscillators, etc. LOAD1 and LOAD2 can only be configured for 4 analog input pins. LOAD3 and LOAD 4 can be configured for the remaining 4 analog input pins.

LOAD1, 2, 3, 4 Command from f(1) ACMP or Matrix connection. A single bit determines if LOADx takes its value from the f(1) analog comparator or from a matrix output.

Configuration Bit	Description	
1 Bit	LOAD1 Connection	0: Matrix, 1: f(1) ACMP
1 Bit	LOAD2 Connection	0: Matrix, 1: f(1) ACMP
1 Bit	LOAD3 Connection	0: Matrix, 1: f(1) ACMP
1 Bit	LOAD4 Connection	0: Matrix, 1: f(1) ACMP

LOAD1 and LOAD2 Configuration Bits f(1) ACMP input

Configuration Bits	Description	
6 Bits	ACMP Voltage Reference value	000000 is 32 mV, 111111 is 2.048 V
2 Bits	One of four analog input pins	
	00	Analog pin 1
	01	Analog pin 2
	10	Analog pin 3
	11	Analog pin 4
1 Bit	Reserved	

LOAD3 and LOAD4 Configuration Bits f(1) ACMP input

Configuration Bits	Description	
6 Bits	ACMP Voltage Reference value	000000 is 32 mV, 111111 is 2.048 V
2 Bits	One of four analog input pins	
	00	Analog pin 5
	01	Analog pin 6
	10	Analog pin 7
	11	Analog pin 8
1 Bit	Reserved	

17.5.3 OUTx Command Configuration Bits

Each f(1) instance can be configured to output to up to three matrix inputs using the OUTx command. OUT1, 2, & 3's initial condition is two bit selectable. Each time the ASM changes state, the initial condition of the f(1) is re-loaded.

Configuration Bits	Description	
00	OUTx equals previous OUTx	
01	OUTx is 0	
10	OUTx is 1	
11	none (high Z)	

The only time the f(1) Computation Macrocell will run is when ASM macrocell first enters a new state. At that point in time, the f(1) Computation Macrocell will execute the user selected commands (based on user selection), and then relinquish control back to the ASM macrocell. During the time that the f(1) Computation Macrocell is active, there can be no activity in the ASM macrocell (i.e. no ASM macrocell state change).

The f(1) Computation Macrocell has two digital inputs, ASM_nReset and f1_Interupt. An active signal on either of these inputs will immediately halt any command execution for the f(1) Computation Macrocell, and will immediately relinquish control back to the ASM macrocell.

17.5.4 LOOP WITH DELAY Configuration Bits

There is one conditional command LOOP WITH DELAY in f(1) computation macrocell. The order of the f(1) command execution depends on the LOOP WITH DELAY usage and its configuration. If top value in 1 x 16 memory stack is 0, then the f(1) is delayed according to the configuration of the f(1) delay function and the f(1) command sequence starting from the location defined by 4-bit register is executed, otherwise f(1) continues to execute commands one by one.

Configuration Bits	Description	
4 bits	Next command location after LOOP WITH DELAY command	0000 is the first command in the f(1) sequence, 1011 is the twelfth last command in the f(1) sequence

Example #3: Rising Edge Deglitch Application showing the command sequence for a potential use case of the f(1) Macrocell.

f(1) Command Sequence	Command	Description
1	LOAD1	Capture the output of a pin or any macrocell output defined by the LOAD1 register.
2	DELAY	Delay for the time defined by configuration register.
3	LOAD1	Capture the output of a pin or any macrocell output defined by the LOAD1 register.
4	DELAY	Delay for time defined by configuration register.
5	LOAD1	Capture the output of a pin or any macrocell output defined by the LOAD1 register.
6	AND	Logically AND the top two values of the 1x16 memory stack, that was loaded before. (LOAD1 & LOAD1 after Delay).
7	AND	(LOAD1 & LOAD1 after Delay) & LOAD1 after double Delay.
8	LOOP WITH DELAY	If the calculated value is 0, then start to execute first command once again, which is defined by the configuration bits. Otherwise f(1) continues to execute next command (command 9).
9	OUT1	Output the result value, which is a high level.
10	END	ASM can act on any other signals.

The following flowchart shows the f(1) rising edge deglitch based on three samples application.

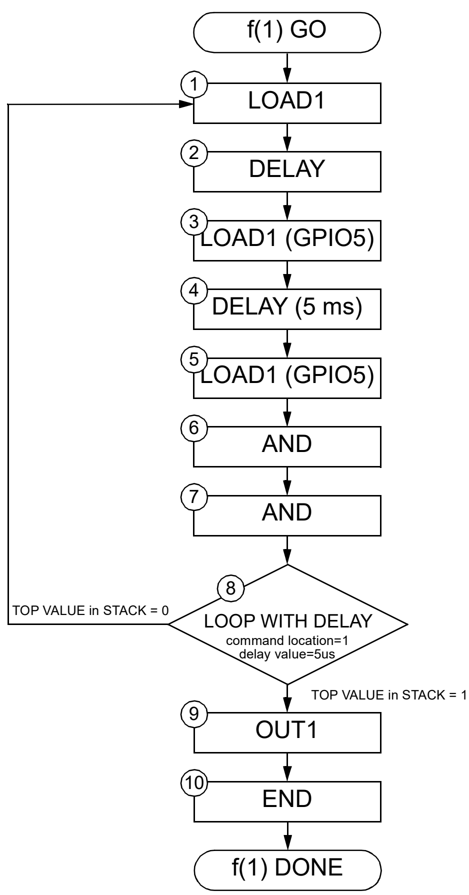


Figure 108: f(1) Flowchart for Rising Edge Deglitch

Example #4: Average Function for Captured Data, showing the command sequence for a potential use case of the f(1) Macrocell. This function requires two f(1) Macrocell command sequences to implement

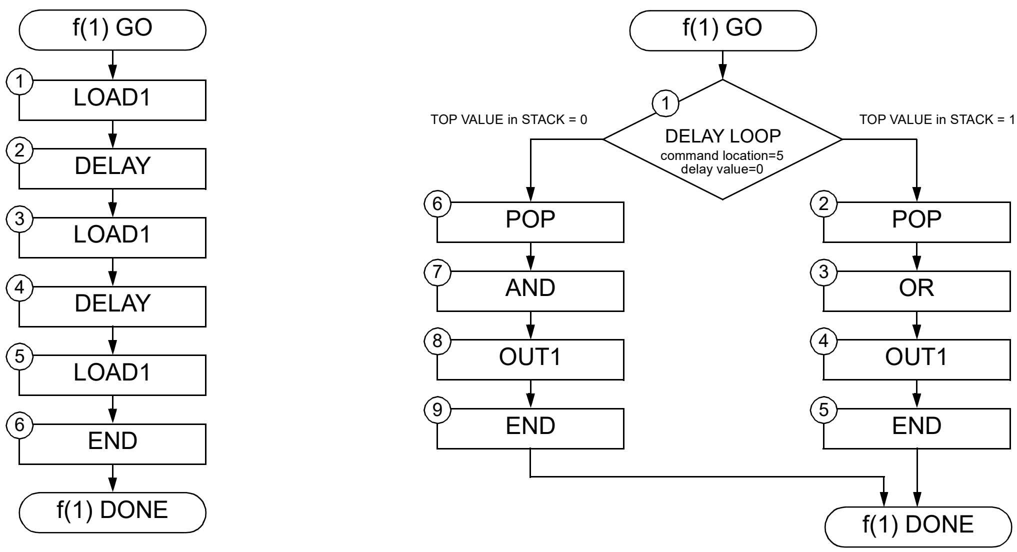


Figure 109: f(1) Flowchart for Average Function for Captured Data

18 Matrix Interface Macrocells

The ASM Sub-System includes several discrete macrocells, including the ASM macrocell, four Dynamic Memory (DMx_x) macrocells, three Matrix Interface (MI) Macrocells, and one f(1) Computation Macrocell. These macrocells are designed to work as a system for building user defined state machines.

The Matrix Interface macrocells have the characteristic that they can change internal configuration characteristics and their connections to the Connection Matrix based on the current state of the State Machine (SM) macrocell. This is accomplished by making different memory register bit settings contained within the macrocell active, based on the current active state of the SM. This allows the user to “repurpose” the resources inside these macrocells to match the circuit needs in various states.

The SLG46880/81 has a total of three MI macrocells, MI0, MI1 and MI2.

Each MI macrocell has a MIx Configuration Register Table, which is a bank of 4 MIx Configuration Registers. The bits in these registers hold user selections which define the input connections from the Connection Matrix. The fact that there are 4 Configuration Registers means that there can only be a total of four unique configurations for each MIx macrocell. There are a total of twelve states, which means that the user can either re-use the configuration coded in a particular MIx Operating Mode Register in more than one state, or not use some MIx macrocells in some states.

Each MI macrocell has a MIx Operating Mode Selection Table, which is a bank of 12 Configuration Selection Registers, one for each state of the State Machine macrocell. The bits in these registers hold the user’s selection of MI functional behavior (input selection from Connection Matrix), by mapping to a particular selection in the Configuration Register Table, based on the current state of the State Machine macrocell.

18.1 MI0, MI1, AND MI2 MACROCELL ARCHITECTURE

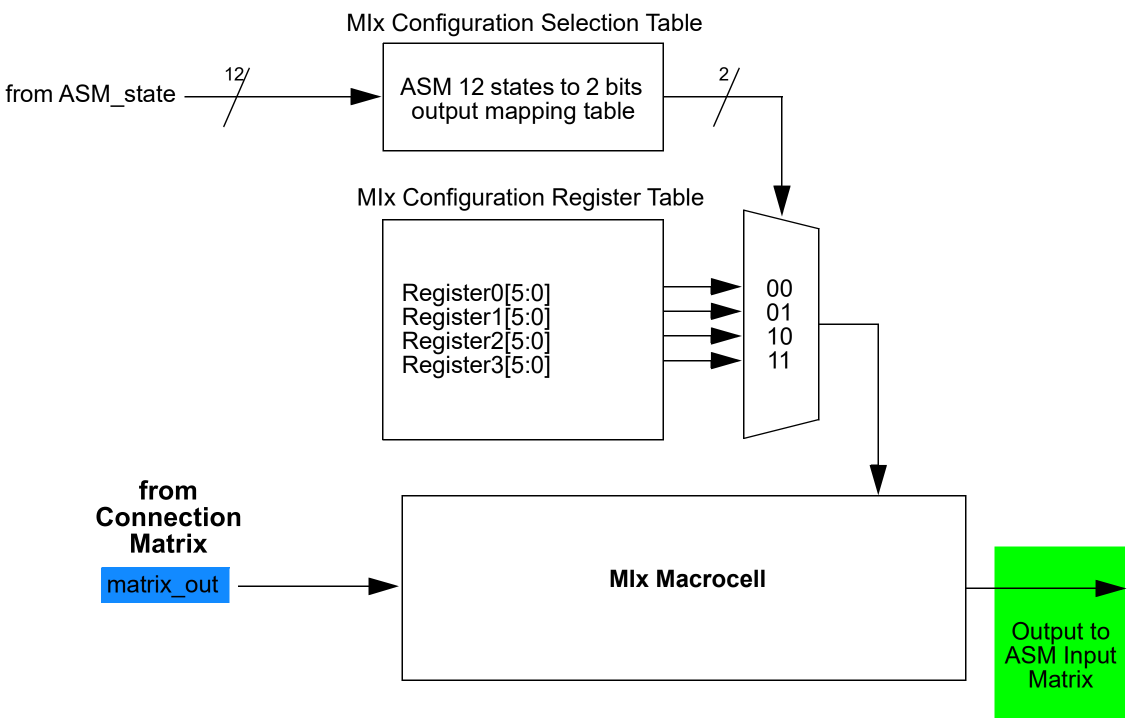


Figure 110: MIx Macrocell Architecture

18.2 MIX MACROCELL INPUT SIGNALS

Each MIx macrocell has a single digital input signal coming from the Connection Matrix and from there can be routed to other internal macrocells or pins. This signal is shown in Figure 110 highlighted in blue.

18.3 MIX MACROCELL OUTPUT SIGNALS

Each MIx macrocell has a single digital output signal, which goes directly to the ASM Input Matrix inside the ASM Macrocell. This signal is shown in Figure 110, highlighted in green.

19 I²C Serial Communications Macrocell

19.1 I²C SERIAL COMMUNICATIONS MACROCELL OVERVIEW

In the standard use case for the GreenPAK devices, the configuration choices made by the user are stored as bit settings in the Non-Volatile Memory (NVM), and this information is transferred at startup time to volatile RAM registers that enable the configuration of the macrocells. Other RAM registers in the device are responsible for setting the connections in the Connection Matrix to route signals in the manner most appropriate for the user's application.

The I²C Serial Communications Macrocell in this device allows an I²C bus Master to read and write this information via a serial channel directly to the RAM registers, allowing the remote re-configuration of macrocells, and remote changes to signal chains within the device.

An I²C bus Master is also able read and write other register bits that are not associated with NVM memory. As an example, the input lines to the Connection Matrix can be read as digital register bits. These are the signal outputs of each of the macrocells in the device, giving an I²C bus Master the capability to remotely read the current value of any macrocell.

The user has the flexibility to control read access and write access via registers bits registers [4071:4069]. See Section 19.4.6.1 for more details on I²C read/write memory protection.

19.2 I²C SERIAL COMMUNICATIONS DEVICE ADDRESSING

Each command to the I²C Serial Communications macrocell begins with a Control Byte. The bits inside this Control Byte are shown in Figure 111. After the Start bit, the first four bits are a control code, which can be set by the user in registers [4083:4080] or value defined externally by GPIs 4, 5, 6, and 7. The LSB of the control code is defined by the value of GPI4, while the MSB is defined by the value of GPI7. The address source is selected by register [4087]. This gives the user flexibility on the chip level addressing of this device and other devices on the same I²C bus. The Block Address is the next three bits (A10,A9, A8), which will define the most significant bits in the addressing of the data to be read or written by the command. The last bit in the Control Byte is the R/W bit, which selects whether a read command or write command is requested, with a "1" selecting for a Read command, and a "0" selecting for a Write command. This Control Byte will be followed by an Acknowledge bit (ACK), which is sent by this device to indicate successful communication of the Control Byte data.

In the read and write command address structure, there are a total of 11 bits of addressing, each pointing to a unique byte of information, resulting in a total address space of 2K bytes. Of this 2K byte address space, the valid addresses accessible to the I²C Macrocell on the SLG46880/81 are in the range from 0 (00H) to 511 (1FFH). The upper two address bits (A10 and A9) will be "0" for all commands to the SLG46880/81. The value of Address bit A8 will depend on whether the Bus Master is addressing the upper or lower half of the 4K bit address space.

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address.

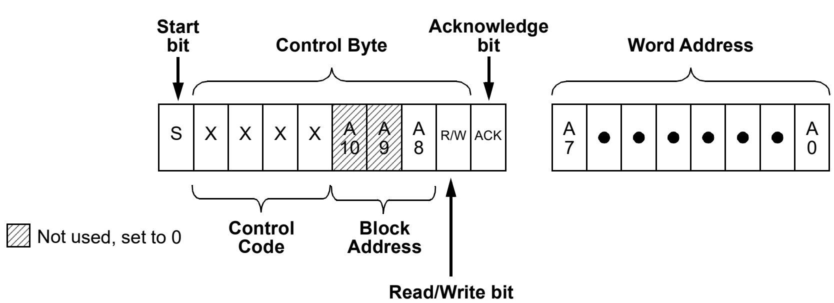


Figure 111: Basic Command Structure

19.3 I²C SERIAL GENERAL TIMING

General timing characteristics for the I²C Serial Communications macrocell are shown in Figure 112. Timing specifications can be found in the AC Characteristics section.

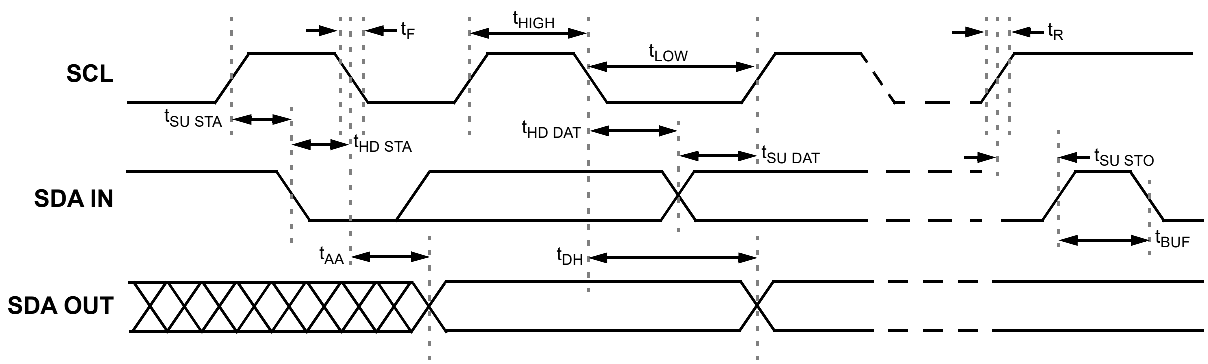


Figure 112: I²C General Timing Characteristics

19.4 I²C SERIAL COMMUNICATIONS COMMANDS

19.4.1 Byte Write Command

Following the Start condition from the Master, the Control Code [4 bits], the Block Address [3 bits] and the R/W bit (set to "0"), are placed onto the I²C bus by the Master. After the SLG46880/81 sends an Acknowledge bit (ACK), the next byte transmitted by the Master is the Word Address. The Block Address (A10, A9, A8), combined with the Word Address (A7 through A0), together set the internal address pointer in the SLG46880/81 where the data byte is to be written. After the SLG46880/81 sends another Acknowledge bit, the Master will transmit the data byte to be written into the addressed memory location. The SLG46880/81 again provides an Acknowledge bit and then the Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG46880/81 generates the Acknowledge bit.

It is possible to latch all IOs during I²C write command, register [4065]=1 - Enable. It means that IOs will remain their state until the write command is done.

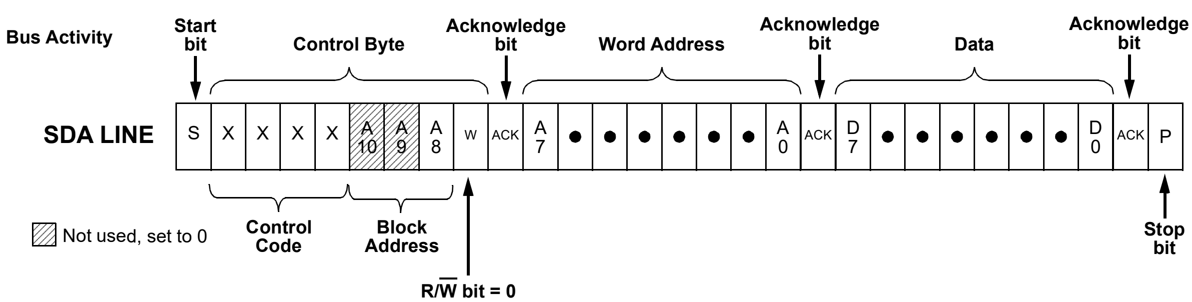


Figure 113: Byte Write Command, R/W = 0

19.4.2 Sequential Write Command

The write Control Byte, Word Address and the first data byte are transmitted to the SLG46880/81 in the same way as in a Byte Write command. However, instead of generating a Stop condition, the Bus Master continues to transmit data bytes to the SLG46880/81. Each subsequent data byte will increment the internal address counter, and will be written into the next higher byte in the command addressing. As in the case of the Byte Write command, the internal write cycle will take place at the time that the SLG46880/81 generates the Acknowledge bit.

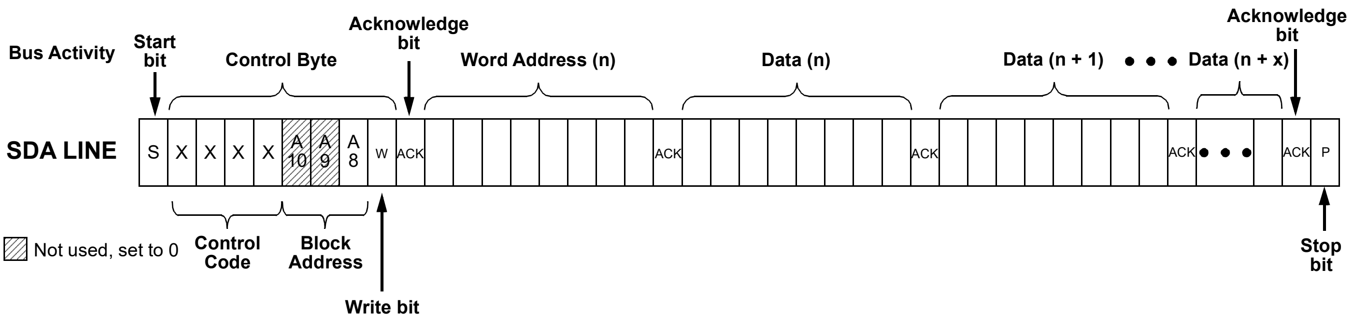


Figure 114: Sequential Write Command

19.4.3 Current Address Read Command

The Current Address Read Command reads from the current pointer address location. The address pointer is incremented at the first STOP bit following any write control byte. For example, if a Sequential Read command (which contains a write control byte) reads data up to address n, the address pointer would get incremented to n+1 upon the STOP of that command. Subsequently, a Current Address Read that follows would start reading data at n+1. The Current Address Read Command contains the Control Byte sent by the Master, with the R/$\overline{W}$ bit = "1". The SLG46880/81 will issue an Acknowledge bit, and then transmit eight data bits for the requested byte. The Master will not issue an Acknowledge bit, and follow immediately with a Stop condition.

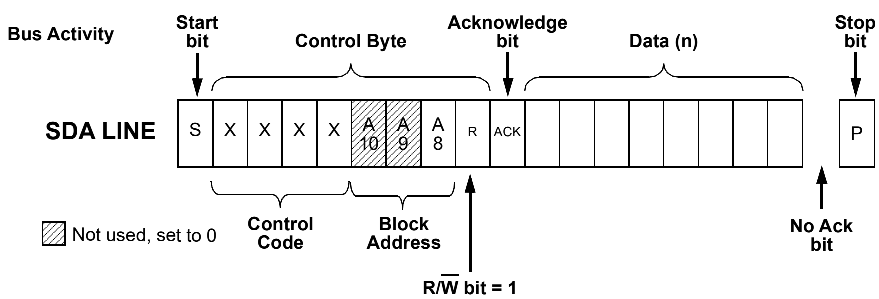


Figure 115: Current Address Read Command, R/$\overline{W}$ = 1

19.4.4 Random Read Command

The Random Read command starts with a Control Byte (with R/W bit set to "0", indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Master issues a second control byte with the R/W bit set to "1", after which the SLG46880/81 issues an Acknowledge bit, followed by the requested eight data bits.

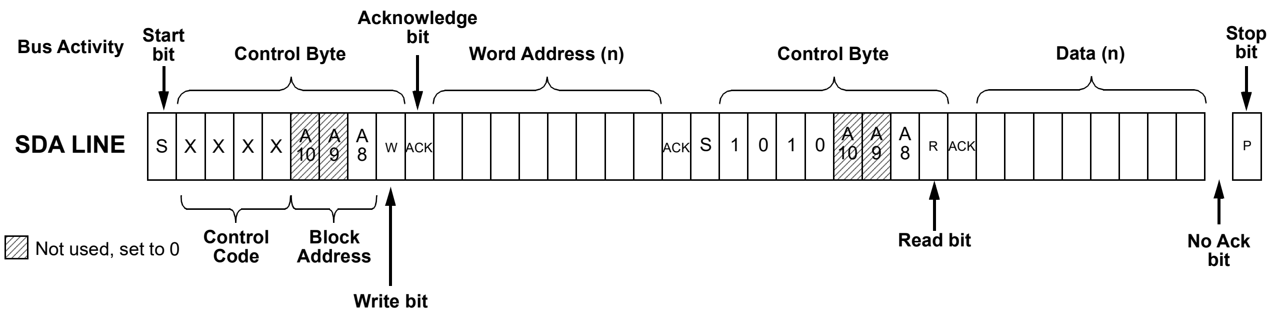


Figure 116: Random Read Command

19.4.5 Sequential Read Command

The Sequential Read command is initiated in the same way as a Random Read command, except that once the SLG46880/81 transmits the first data byte, the Bus Master issues an Acknowledge bit as opposed to a Stop condition in a random read. The Bus Master can continue reading sequential bytes of data, and will terminate the command with a Stop condition.

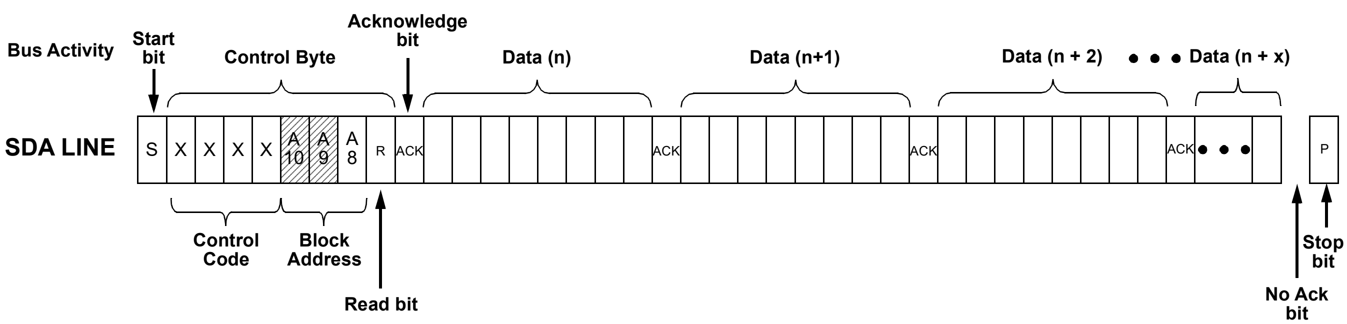


Figure 117: Sequential Read Command

19.4.6 I^{2}C SERIAL COMMAND REGISTER MAP

19.4.6.1 Register Read/Write Protection

There are seven read/write protect modes for the design sequence from being corrupted or copied. See Table 51 for details.

Table 51: Read/Write Protection Options

Configurations	Protection Modes Configuration							Data Output From	Register Address
	Unlocked	Partly Lock Read1	Partly Lock Read2	Partly Lock Read2/ Write	Lock Read	Lock Write	Lock Read/ Write		
	(Mode 0)	(Mode 1)	(Mode 2)	(Mode 3)	(Mode 4)	(Mode 5)	(Mode 6)		
I2C Byte Write Bit Masking (section 19.4.7)	R/W	R/W	R/W	R/W	W	R	-	Memory	1FD

Table 51: Read/Write Protection Options(Continued)

Configurations	Protection Modes Configuration							Data Output From	Register Address
	Unlocked (Mode 0)	Partly Lock Read1 (Mode 1)	Partly Lock Read2 (Mode 2)	Partly Lock Read2/ Write (Mode 3)	Lock Read (Mode 4)	Lock Write (Mode 5)	Lock Read/ Write (Mode 6)		
I2C Serial Reset Command (section 19.4.6.2)	R/W	R/W	R/W	R/W	W	R	-	Memory	1FC,b'0
Outputs Latching During I^2C Write	R/W	R/W	R/W	R/W	W	R	-	Memory	1FC,b'1
f(1) Computation Macrocell Stack	R/W	R/W	R/W	R/W	W	R	-	Macrocell	198~199
Connection Matrix Virtual Inputs (section 6.3)	R/W	R/W	R/W	R/W	W	R	-	Macrocell	1DB
Configuration Bits for All Macrocells (IO Pins, ACMPs, Combination Function Macrocells, ASM, etc.)	R/W	R/W	W	-	W	R	-	Memory	
Macrocells Inputs Configuration (Connection Matrix Outputs, section 6.2)	R/W	W	W	-	W	R	-	Memory	0~3E
Protection Mode Selection	R/W	R	R	R	R	R	R	Memory	1FC,b'7,6, 5
Macrocells Output Values (Connection Matrix Inputs, section 6.1)	R	R	R	R	-	R	-	Macrocell	1D7~1DA; 1DC~1DE
Counter Current Value	R	R	R	R	-	R	-	Macrocell	1DF,1E0,1 E1,1E2
ASM Current State	R	R	R	R	-	R	-	Macrocell	1E3,1E4
I^2C Control Code (section 19.4)	R	R	R	R	R	R	R	Memory	1FE,b'3~0
I^2C Disable/Enable	R	R	R	R	R	R	R	Memory	1FE,b'4

R/W	Allow Read and Write Data
W	Allow Write Data Only
R	Allow Read Data Only
-	The Data is protected for Read and Write

It is possible to read some data from macrocells, such as counter current value, ASM current state, connection matrix, f(1) computation macrocell stack and connection matrix virtual inputs. The I^2C write will do not have any impact on data in case data comes from macrocell output, except f(1) Computation Macrocell Stack and Connection Matrix Virtual Inputs. The silicon identification service bits allows identifying silicon family, its revision, etc.

See Section 21 for detailed information on all registers.

19.4.6.2 I^{2}C SERIAL RESET COMMAND

If I^{2}C serial communication is established with the device, it is possible to reset the device to initial power up conditions, including configuration of all macrocells, and all connections provided by the Connection Matrix. This is implemented by setting register [4064] I^{2}C reset bit to "1", which causes the device to re-enable the Power-On Reset (POR) sequence, including the reload of all register data from NVM. During the POR sequence, the outputs of the device will be in tri-state. After the reset has taken place, the contents of register [4064] will be set to "0" automatically. The timing diagram shown below illustrates the sequence of events for this reset function.

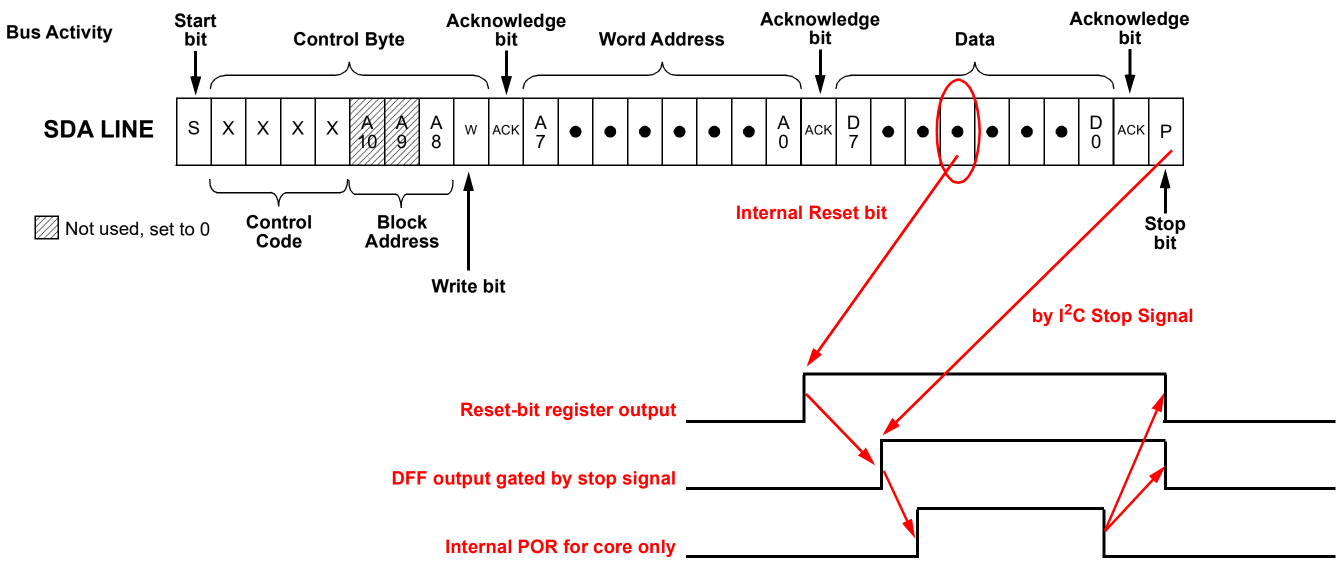


Figure 118: Reset Command Timing

19.4.6.3 Reading Counter Data via I^{2}C

The current count value in four counters in the device can be read via I^{2}C. The counters that have this additional functionality are 16-bit CNT0, and 8-bit counters CNT2 and CNT4.

19.4.6.4 Reading ASM Current State via I^{2}C

The Current State of the ASM can be read via I^{2}C. There are 12 memory bits located at registers [3875:3864]. Configuration for each Current State can be found in Table 52.

Table 52: ASM Current State Bits Configuration

I²C Address	Register Bit #	ASM State #	ASM Current State Bits Configuration											
			State 0	State 1	State 2	State 3	State 4	State 5	State 6	Stat e 7	State 8	State 9	State 10	State 11
1E3	3864	State 0	1	0	0	0	0	0	0	0	0	0	0	0
	3865	State 1	0	1	0	0	0	0	0	0	0	0	0	0
	3866	State 2	0	0	1	0	0	0	0	0	0	0	0	0
	3867	State 3	0	0	0	1	0	0	0	0	0	0	0	0
	3868	State 4	0	0	0	0	1	0	0	0	0	0	0	0
	3869	State 5	0	0	0	0	0	1	0	0	0	0	0	0
	3870	State 6	0	0	0	0	0	0	1	0	0	0	0	0
	3871	State 7	0	0	0	0	0	0	0	1	0	0	0	0
1E4	3872	State 8	0	0	0	0	0	0	0	0	1	0	0	0
	3873	State 9	0	0	0	0	0	0	0	0	0	1	0	0
	3874	State 10	0	0	0	0	0	0	0	0	0	0	1	0
	3875	State 11	0	0	0	0	0	0	0	0	0	0	0	1

19.4.6.5 I²C Expander

In addition to the eight Connection Matrix Virtual Inputs, the SLG46880/81 chip has four pins which can be used as an I²C Expander. These four pins are GPIO4, GPIO5, GPIO6, and GPIO7.

Each of these pins can be used as an I²C Expander output or used as a normal pin. Also each of these four expander outputs have initial state settings which are specified in registers [3880:3870].

19.4.7 I²C Byte Write Bit Masking

The I²C macrocell inside SLG46880/81 supports masking of individual bits within a byte that is written to the RAM memory space. This function is supported across the entire RAM memory space. To implement this function, the user performs a Byte Write Command (see Section 19.4.1 for details) on the I²C Byte Write Mask Register (address 0xxH) with the desired bit mask pattern. This sets a bit mask pattern for the target memory location that will take effect on the next Byte Write Command to this register byte. Any bit in the mask that is set to “1” in the I²C Byte Write Mask Register will mask the effect of changing that particular bit in the target register, during the next Byte Write Command. The contents of the I²C Byte Write Mask Register are reset (set to 00h) after the Byte Write Command. If the next command received by the device is not a Byte Write Command, the effect of the bit masking function will be aborted, and the I^2C Byte Write Mask Register will be reset with no effect. Figure 119 shows an example of this function.

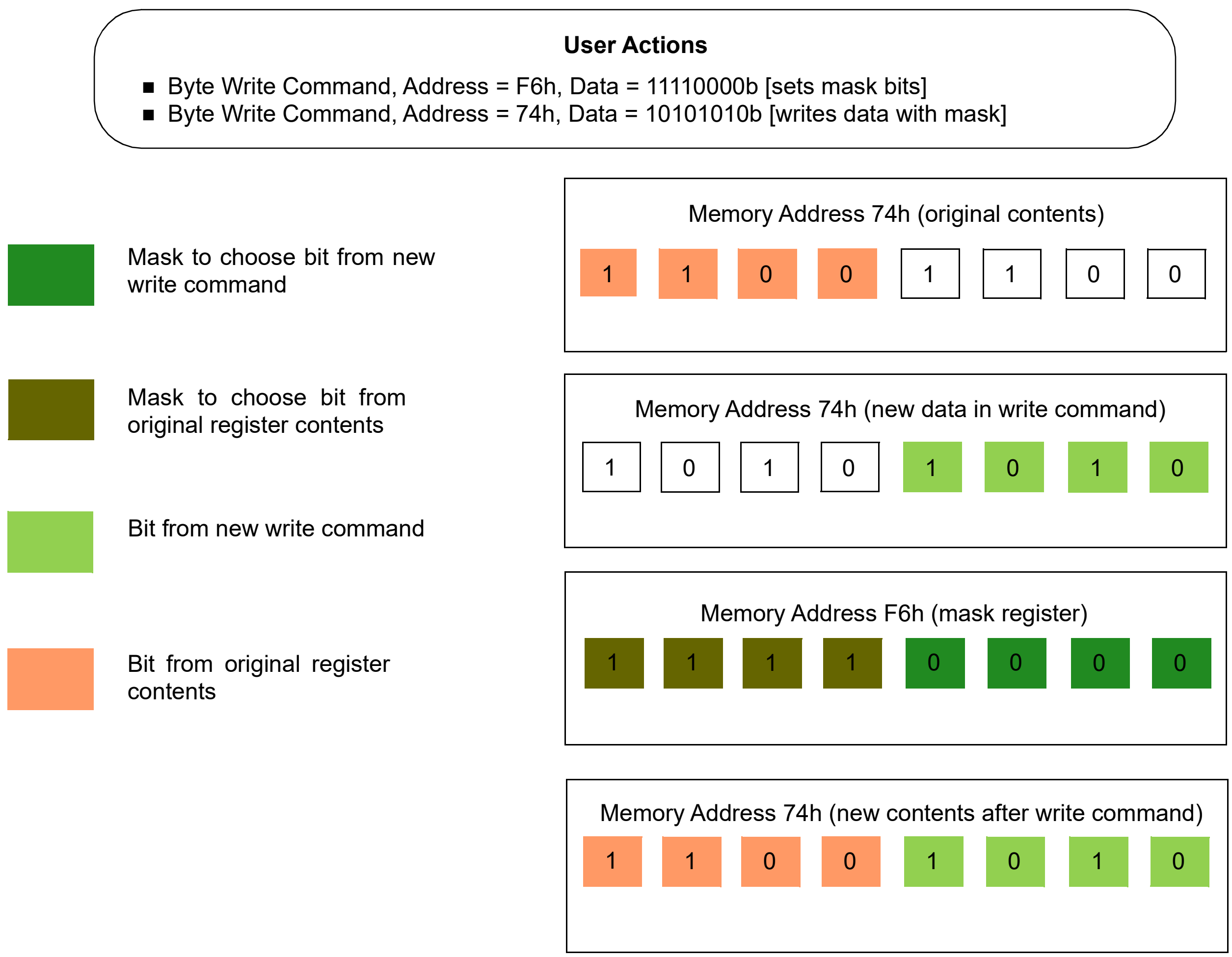


Figure 119: Example of I^2C Byte Write Bit Masking

20 Analog Temperature Sensor

The SLG46880 has an Analog Temperature sensor (TS) with an output voltage linearly-proportional to the Centigrade temperature. The TS cell shares buffer with Vref0, so it is impossible to use both cells simultaneously, its output can be connected directly to the GPIO9 or to the ACPM3_L positive input. Using buffer causes low-output impedance, linear output and makes interfacing to readout or control circuitry especially easy. The TS is rated to operate over a -40°C to 85°C temperature range. The error in the whole temperature range does not exceed ±3.6%. TS output voltage variation over V_{DD} at constant temperature is less than ±1%. For more detail refer to Section 3.

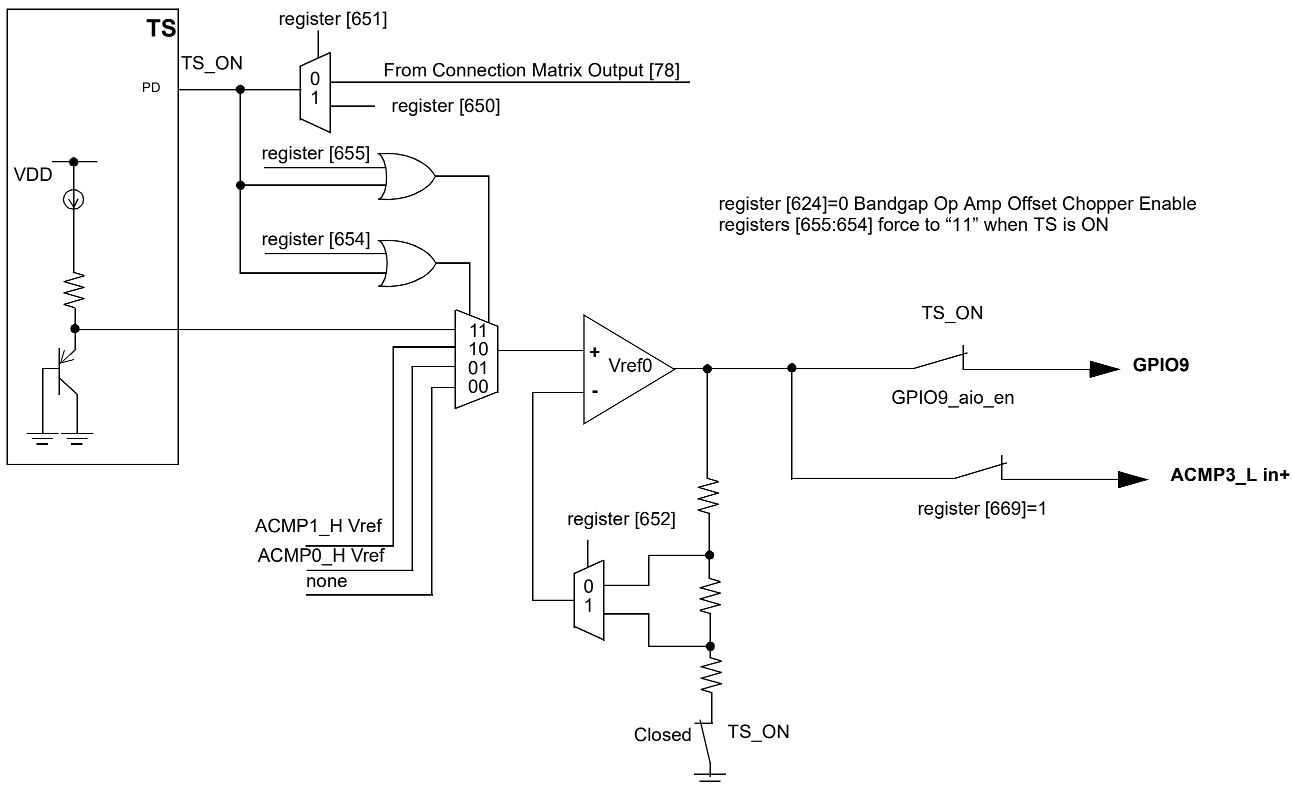


Figure 120: Analog Temperature Sensor Structure Diagram

Note that the Power-Down Mode is paired with Crystal OSC, see Section 12.6. If it is enabled for Temp Sensor, it is not available for Crystal OSC and vice versa. However, it is possible to enable Power-Down Mode for Crystal OSC and Temp Sensor simultaneously.

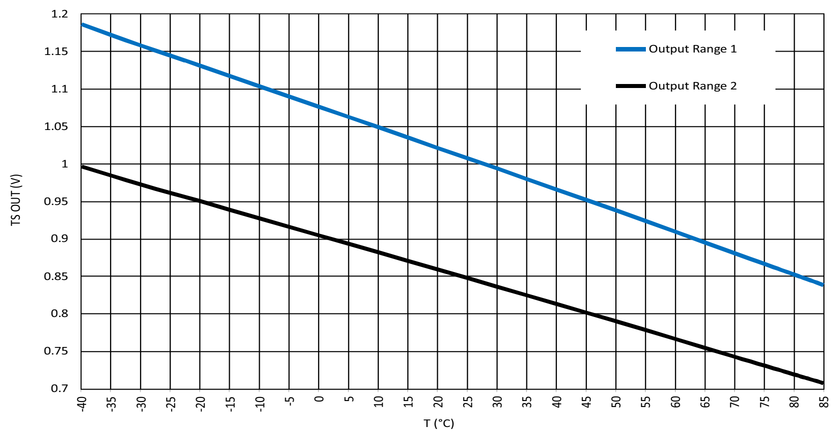


Figure 121: TS Output vs. Temperature, V_{DD} = 2.3 V to 5.5 V

21 Register Definitions

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
0	0	OUT0: IN0 of LUT2_0 or Clock Input of DFF0	
	1		
	2		
	3		
	4		
	5		
	6	OUT1: IN1 of LUT2_0 or Data Input of DFF0	
	7		
1	8		
	9		
	10		
	11		
	12	OUT2: IN0 of LUT2_1 or Clock Input of PGEN	
	13		
	14		
	15		
2	16		
	17		
	18	OUT3: IN1 of LUT2_1 or nRST of PGEN	
	19		
	20		
	21		
	22		
	23		
3	24	OUT4: IN0 of LUT3_0 or Clock Input of DFF1	
	25		
	26		
	27		
	28		
	29		
	30	OUT5: IN1 of LUT3_0 or Data Input of DFF1	
	31		
4	32		
	33		
	34		
	35		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
4	36	OUT6: IN2 of LUT3_0 or nRST (nSET) of DFF1	
	37		
	38		
	39		
5	40		
	41		
	42	OUT7:IN0 of LUT3_1 or Clock Input of DFF2	
	43		
	44		
	45		
	46		
	47		
6	48	OUT8:IN1 of LUT3_1 or Data Input of DFF2	
	49		
	50		
	51		
	52		
	53		
	54	OUT9:IN2 of LUT3_1 or nRST (nSET) of DFF2	
	55		
7	56		
	57		
	58		
	59		
	60	OUT10:IN0 of LUT3_2 or Clock Input of DFF3	
	61		
	62		
	63		
8	64		
	65		
	66	OUT11:IN1 of LUT3_2 or Data Input of DFF3	
	67		
	68		
	69		
	70		
	71		
9	72	OUT12:IN2 of LUT3_2 or nRST (nSET) of DFF3	
	73		
	74		
	75		
	76		
	77		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
9	78	OUT13:IN0 of LUT3_3 or Clock Input of DFF4	
	79		
A	80		
	81		
	82		
	83		
	84	OUT14:IN1 of LUT3_3 or Data Input of DFF4	
	85		
	86		
	87		
B	88		
	89		
	90	OUT15:IN2 of LUT3_3 or nRST (nSET) of DFF4	
	91		
	92		
	93		
	94		
	95		
C	96	OUT16:IN0 of LUT3_4 or Delay1 Input (or Counter1 nRST Input)	
	97		
	98		
	99		
	100		
	101		
	102	OUT17:IN1 of LUT3_4 or External Clock1 Input of Delay1 (or Counter1)	
	103		
D	104		
	105		
	106		
	107		
	108	OUT18:IN2 of LUT3_4	
	109		
	110		
	111		
E	112		
	113		
	114	OUT19:IN0 of LUT3_5 or Delay2 Input (or Counter2 nRST Input)	
	115		
	116		
	117		
	118		
	119		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
F	120	OUT20:IN1 of LUT3_5 or External Clock1 Input of Delay2 (or Counter2)	
	121		
	122		
	123		
	124		
	125		
	126	OUT21:IN2 of LUT3_5	
	127		
10	128		
	129		
	130		
	131		
	132	OUT22:IN0 of LUT3_6 or Delay3 Input (or Counter3 nRST Input)	
	133		
	134		
	135		
11	136		
	137		
	138	OUT23:IN1 of LUT3_6 or External Clock1 Input of Delay3 (or Counter3)	
	139		
	140		
	141		
	142		
	143		
12	144	OUT24:IN2 of LUT3_6	
	145		
	146		
	147		
	148		
	149		
	150	OUT25:IN0 of LUT3_7 or Delay4 Input (or Counter4 nRST Input)	
	151		
13	152		
	153		
	154		
	155		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
13	156	OUT26:IN1 of LUT3_7 or External Clock1 Input of Delay4 (or Counter4)	
	157		
	158		
	159		
14	160		
	161		
	162	OUT27:IN2 of LUT3_7	
	163		
	164		
	165		
	166		
	167		
15	168	OUT28:IN0 of LUT3_8 or Input of Pipe Delay or UP signal of Ripple CNT	
	169		
	170		
	171		
	172		
	173		
	174	OUT29:IN1 of LUT3_8 or nRST of Pipe Delay or STB of Ripple CNT	
	175		
16	176		
	177		
	178		
	179		
	180	OUT30:IN2 of LUT3_8 or Clock of Pipe Delay_Ripple CNT	
	181		
	182		
	183		
17	184		
	185		
	186	OUT31:IN0 of LUT4_0 or Delay0 Input (or Counter0 nRST Input)	
	187		
	188		
	189		
	190		
	191		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
18	192	OUT32:IN1 of LUT4_0 or External Clock Input of Delay0 (or Counter0)	
	193		
	194		
	195		
	196		
	197		
	198	OUT33:IN2 of LUT4_0 or UP Input of FSM0	
	199		
19	200		
	201		
	202		
	203		
	204	OUT34:IN3 of LUT4_0 or KEEP Input of FSM0	
	205		
	206		
	207		
1A	208		
	209		
	210	OUT35:pd of ACMP0_H	
	211		
	212		
	213		
	214		
	215		
1B	216	OUT36:pd of ACMP1_H	
	217		
	218		
	219		
	220		
	221		
	222	OUT37:pd of ACMP2_L	
	223		
1C	224		
	225		
	226		
	227		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
1C	228	OUT38:pd of ACMP3_L	
	229		
	230		
	231		
1D	232		
	233		
	234	OUT39: GPO7 DOUT	
	235		
	236		
	237		
	238		
	239		
1E	240	OUT40: GPO0 DOUT	
	241		
	242		
	243		
	244		
	245		
	246	OUT41: GPIO0 DOUT	
	247		
1F	248		
	249		
	250		
	251		
	252	OUT42: GPIO0 DOUT OE	
	253		
	254		
	255		
20	256		
	257		
	258	OUT43: GPIO1 DOUT	
	259		
	260		
	261		
	262		
	263		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
21	264	OUT44:GPIO1 DOUT OE	
	265		
	266		
	267		
	268		
	269		
	270	OUT45: GPIO2 DOUT	
	271		
22	272		
	273		
	274		
	275		
	276	OUT46: GPIO2 DOUT OE	
	277		
	278		
	279		
23	280		
	281		
	282	OUT47: GPIO3 DOUT	
	283		
	284		
	285		
	286		
	287		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
24	288	OUT48: GPIO3 DOUT OE	
	289		
	290		
	291		
	292		
	293		
	294	OUT49: GPIO4 DOUT	
	295		
25	296		
	297		
	298		
	299		
	300	OUT50: GPIO4 DOUT OE	
	301		
	302		
	303		
26	304		
	305		
	306	OUT51: GPIO5 DOUT	
	307		
	308		
	309		
	310		
	311		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
27	312	OUT52: GPIO5 DOUT OE	
	313		
	314		
	315		
	316		
	317		
	318	OUT53: GPO1 DOUT	
	319		
28	320		
	321		
	322		
	323		
	324	OUT54: GPO2 DOUT	
	325		
	326		
	327		
29	328		
	329		
	330	OUT55: GPO3 DOUT	
	331		
	332		
	333		
	334		
	335		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
2A	336	OUT56: GPO4 DOUT	
	337		
	338		
	339		
	340		
	341		
	342	OUT57: GPIO6 DOUT OE	
	343		
2B	344		
	345		
	346		
	347		
	348	OUT58: GPIO6 DOUT	
	349		
	350		
	351		
2C	352		
	353		
	354	OUT59: GPIO7 DOUT	
	355		
	356		
	357		
	358		
	359		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
2D	360	OUT60: GPIO7 DOUT OE	
	361		
	362		
	363		
	364		
	365		
	366	OUT61: GPIO8 DOUT OE	
	367		
2E	368		
	369		
	370		
	371		
	372	OUT62: GPIO8 DOUT	
	373		
	374		
	375		
2F	376		
	377		
	378	OUT63: GPIO9 DOUT OE	
	379		
	380		
	381		
	382		
	383		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
30	384	OUT64: GPIO9 DOUT	
	385		
	386		
	387		
	388		
	389		
	390	OUT65: GPIO10 DOUT OE	
	391		
31	392		
	393		
	394		
	395		
	396	OUT66: GPIO10 DOUT	
	397		
	398		
	399		
32	400		
	401		
	402	OUT67: GPIO11 DOUT OE	
	403		
	404		
	405		
	406		
	407		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
33	408	OUT68: GPIO11 DOUT	
	409		
	410		
	411		
	412		
	413		
	414	OUT69: GPO5 DOUT	
	415		
34	416		
	417		
	418		
	419		
	420	OUT70: GPO5 DOUT	
	421		
	422		
	423		
35	424		
	425		
	426	OUT71: ASM REnSET	
	427		
	428		
	429		
	430		
	431		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
36	432	OUT72: OSC0 ENABLE	
	433		
	434		
	435		
	436		
	437		
	438	OUT73: OSC1 ENABLE	
	439		
37	440		
	441		
	442		
	443		
	444	OUT74: OSC2 ENABLE	
	445		
	446		
	447		
38	448		
	449		
	450	OUT75: Filter/Edge detect input	
	451		
	452		
	453		
	454		
	455		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
39	456	OUT76: F1 interrupt	
	457		
	458		
	459		
	460		
	461		
	462	OUT77: Programmable delay/edge detect input	
	463		
3A	464		
	465		
	466		
	467		
	468	OUT78: Temp sensor/Crystal PD	
	469		
	470		
	471		
3B	472		
	473		
	474	OUT79: GPI Latch enable	
	475		
	476		
	477		
	478		
	479		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
3C	480	OUT80: GPIO Latch enable	
	481		
	482		
	483		
	484		
	485		
	486	OUT81: BG power-down	
	487		
3D	488		
	489		
	490		
	491		
	492	OUT82: DM EXT CLK0	
	493		
	494		
	495		
3E	496		
	497		
	498	OUT83: DM EXT CLK1	
	499		
	500		
	501		
	502		
	503		
3F	504	OSC1 turn on by register	when matrix output enable/pd control signal=0: 0: auto on by delay cells 1: always on
	505	OSC1 matrix power down or on select	0: matrix down, and register [504] should set to 1 1: matrix on, and register [504] should set to 0
	506	external clock source enable	0: internal OSC1 1: external clock from GPI1
	507	post divider ratio control	00: div 1 01: div 2 10: div 4 11: div 8
	508		
	509	matrix divider ratio control	000: /1 001: /2 010: /4 011: /3 100: /8 101: /12 110: /24 111: /64
	510		
	511		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
40	512	matrix out enable	0: disable 1: enable
	513	Reserved	
	514	Reserved	
	515	Reserved	
	516	OSC2 turn on by register	when matrix output enable/pd control signal=0: 0: auto on by delay cells 1: always on
	517	matrix power down or on select	0: matrix down 1: matrix on
	518	external clock source enable	0: internal OSC2 1: external clock from GPI0
	519	matrix out enable	0: disable 1: enable
41	520	post divider ratio control	00: div 1 01: div 2 10: div 4 11: div 8
	521		
	522	matrix divider ratio control	000: /1 001: /2 010: /4 011: /3 100: /8 101: /12 110: /24 111: /64
	523		
	524		
	525	100 ns Startup Delay	0: enable 1: disable
	526	OSC0 turn on by register	when matrix output enable/pd control signal=0: 0: auto on by delay cells 1: always on
	527	matrix power down or on select	0: matrix down 1: matrix on

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
42	528	external clock source enable	0: internal OSC0 1: external clock from PIN30
	529	matrix out enable	0: disable 1: enable
	530	post divider ratio control	00: div 1 01: div 2 10: div 4 11: div 8
	531		
	532	matrix divider ratio control	000: /1 001: /2 010: /4 011: /3 100: /8 101: /12 110: /24 111: /64
	533		
	534		
	535	enable OSC0 output gating by wake_sleep signal (note: the wake_sleep clock is seperated path, so it is not gated)	0: no gating 1: enable
43	536	GPI0 Digital Input 100 ns debounce enable	0: disable 1: enable
	537	GPI1 Digital Input 100 ns debounce enable	0: disable 1: enable
	538	GPI5 Digital Input 100 ns debounce enable	0: disable 1: enable
	539	GPI6 Digital Input 100 ns debounce enable	0: disable 1: enable
	540	Filter or Edge Detector selection	Filter or Edge Detector Select 0: filter 1: edge det
	541	Output Polarity Select	0: Filter/edge detect output 1: Filter/edge detect output inverted
	542	Select the edge mode	00: Rising Edges Det 01: Falling Edge Det 10: Both Edge Det 11: Both Edge dly
	543		
44	544	LUT value or pipe delay out sel or Nset/END value	[7:4]: LUT3_8 [7:4]/REG_S1[3:0] pipe delay out1 sel [3:0]: LUT3_8 [3:0]/REG_S0[3:0] pipe delay out0 sel at Ripple CNT mode: bit[546:544] is the nSET value. bit[549:547] is the END value bit [550] is the range control: 0: full cycle, 1: ranged cycle bit [551] Not used
	545		
	546		
	547		
	548		
	549		
	550		
	551		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
45	552	Pipe Delay OUT1 Polarity Select	0: Non-inverted 1: Inverted
	553	LUT3_8 or Pipe Delay Select	0: LUT3_8 1: Pipe Delay or Ripple CNT
	554	PIPE_Ripple_CNT_S	0: Pipe delay mode selection 1: Ripple Counter mode selection
	555	Reserved	
	556 557	Select the Edge Mode of Programmable Delay & Edge Detector	00: Rising Edge Detector 01: Falling Edge Detector 10: Both Edge Detector 11: Both Edge Delay
	558 559	Delay Value Select for Programmable Delay & Edge Detector	00: 125ns 01: 250ns 10: 375ns 11: 500ns
46	560 561 562 563	LUT2_0/DFF0 setting	[3]:LUT2_0 [3]/DFF0 or Latch Select 0: DFF function 1: Latch function [2]:LUT2_0 [2]/DFF0 Output Select 0: Q output 1: QB output [1]:LUT2_0 [1]/DFF0 Initial Polarity Select 0: Low 1: High [0]:LUT2_0 [0]
	564 565 566 567	LUT2_1_VAL or PGEN_data	LUT2_1[3:0] or PGEN 4bit counter data[3:0]
47	568 569 570 571 572 573 574 575	PGEN data	PGEN Data[15:0]
48	576 577 578 579 580 581 582 583		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
49	584 585 586 587 588 589 590 591	LUT3_0_DFF1 setting	[7]:LUT3_0 [7]/DFF1 or Latch Select 0: DFF function 1: Latch function [6]:LUT3_0 [6]/DFF1 Output Select 0: Q output 1: QB output [5]:LUT3_0 [5] /DFF1 0: nRST from Matrix Output 1: nSET from Matrix Output [4]:LUT3_0 [4]/DFF1 Initial Polarity Select 0: Low, 1: High [3:0]: LUT3_0 [3:0]
4A	592 593 594 595 596 597 598 599	LUT3_1_DFF2 setting	[7]:LUT3_1 [7]/DFF2 or Latch Select 0: DFF function 1: Latch function [6]:LUT3_1 [6]/DFF2 Output Select 0: Q output 1: QB output [5]:LUT3_1 [5] /DFF2 0: nRST from Matrix Output 1: nSET from Matrix Output [4]:LUT3_1 [4]/DFF2 Initial Polarity Select 0: Low 1: High [3:0]: LUT3_1 [3:0]
4B	600 601 602 603 604 605 606 607	LUT3_2_DFF3 setting	[7]:LUT3_2 [7]/DFF3 or Latch Select 0: DFF function, 1: Latch function [6]:LUT3_2 [6]/DFF3 Output Select 0: Q output 1: QB output [5]:LUT3_2 [5] /DFF3 0: nRST from Matrix Output 1: nSET from Matrix Output [4]:LUT3_2 [4]/DFF3 Initial Polarity Select 0: Low 1: High [3:0]: LUT3_2 [3:0]
4C	608 609 610 611 612 613 614 615	LUT3_3_DFF4 setting	[7]:LUT3_3 [7]/DFF4 or Latch Select 0: DFF function 1: Latch function [6]:LUT3_3 [6]/DFF4 Output Select 0: Q output 1: QB output [5]:LUT3_3 [5] /DFF4 0: nRST from Matrix Output 1: nSET from Matrix Output [4]:LUT3_3 [4]/DFF4 Initial Polarity Select 0: Low 1: High [3:0]: LUT3_3 [3:0]

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
4D	616	LUT2_0 or DFF0 Select	0: LUT2_0 1: DFF0
	617	LUT2_1 or PGEN Select	0: LUT2_1 1: PGEN
	618	LUT3_0 or DFF1 Select	0: LUT3_0 1: DFF1
	619	DFF1_SECONDQ_Sel	0: Q of first DFF 1 Q of second DFF
	620	LUT3_1 or DFF2 Select	0: LUT3_1 1: DFF2
	621	LUT3_2 or DFF3 Select	0: LUT3_2 1: DFF3
	622	LUT3_3 or DFF4 Select	0: LUT3_3 1: DFF4
	623	Reserved	
4E	624	BG CHOP OFF	0: CHOP enable 1: chopper off
	625	BG Chopper clock test enable	1: enable
	626	Bandgap internal voltage output to Pin enable	1: enable
	627	ACMP0_H hysteresis	00: 0mV 01: 32mV 10: 64mv 11: 196mV
	628		
	629	Reserved	
	630	ACMP0_H input buffer enable	1: enable
	631	Reserved	
4F	632	ACMP0_H input tie to V_{DD} enable	1: enable
	633	ACMP1_H positive input come from ACMP0_H's input mux output enable	1: enable
	634	Reserved	
	635	ACMP1_H hysteresis	00: 0mV 01: 32mV 10: 64mv 11: 196mV
	636		
	637	ACMP1_H input buffer enable	0: disable 1: enable
	638	Reserved	
	639	ACMP2_L positive input come from ACMP0_H's input mux output enable	1: enable

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
50	640	ACMP2_L positive input come from ACMP1_H's input mux output enable	1: enable
50	641	ACMP2_L hysteresis	00: 0 mV 01: 32 mV 10: 64 mv 11: 196 mV
50	642		
50	643	Reserved	
50	644	Reserved	
50	645	ACMP3_L hysteresis	00: 0mV 01: 32mV 10: 64mv 11: 196mV
50	646		
50	647	Reserved	
51	648	Reserved	
51	649	ACMP3_L positive input come from ACMP2_L's input mux output enable	1: enable
51	650	Temp sensor register pd control	0: power-down 1: power-on
51	651	Temp sensor register pd select	0: come from register 1: come matrix
51	652	Temp sensor range select	0: 0.62V ~ 0.99V (TYP) 1: 0.75V ~ 1.2V (TYP)
51	653	Vref0 output OP	0: disable 1: enable
51	654	Vref0 input selection	00: None 01: ACMP0_H Vref 10: ACMP1_H Vref 11: temp sensor
51	655		
52	656	Vref1 output OP	0: disable 1: enable
52	657	Vref1 input selection	00: None 01: ACMP2_L Vref 10: ACMP3_L Vref
52	658		
52	659	Reserved	
52	660		
52	661		
52	662		
52	663	ACMP0_H Wake/sleep enable	1: enable

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
53	664	ACMP1_H Wake/sleep enable	1: enable
	665	ACMP wake/sleep time selection,	0: short time 1: normal w/s
	666	ACMP0_H 100uA current source enable	1: enable
	667	Reserved for ACMP	
	668	BG Trimming source select	0: VBG 1: Vref normal 2.048 output
	669	ACMP3_L input come from Temp sensor output enable	1: enable
	670	IO fast pull up/down enable	0: disable 1: enable
	671	8 GPO outputs skew enable	0: disable 1: enable

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
54	672	GPO7output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain
	673		
	674	GPO7pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	675		
	676	GPO7pull up/down selection	0: pull down 1: pull up
	677	GPO7digital output source selection	0: from matrix 1: from ASM (ASM output to GPO bit[0])
	678	GPO7output enable	0: disable 1: enable.
	679	GPO0output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain
55	680		
	681	GPO0pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	682		
	683	GPO0pull up/down selection	0: pull down 1: pull up
	684	GPO0digital output source selection	0: from matrix 1: from ASM (ASM output to GPO bit[1])
	685	GPO0output enable	0: disable 1: enable
	686	GPIO0 ultra-low power digital in enable (only used in SLG46881)	0: disable 1: enable
	687	GPIO0input mode configuration	00: digital without schmitt trigger 01: digital with schmitt trigger 10: low voltage digital in 11: analog IO
56	688		
	689	GPIO0output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain
	690		
	691	GPIO0pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	692		
	693	GPIO0pull up/down selection	0: pull down 1: pull up
	694	Reserved	
	695	GPIO1 ultra-low power digital in enable (only used in SLG46881)	0: disable 1: enable

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
57	696	GPIO1input mode configuration	00: digital without schmitt trigger 01: digital with schmitt trigger 10: low voltage digital in 11: analog IO
	697		
	698	GPIO1output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain
	699		
	700	GPIO1pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	701		
	702	GPIO1pull up/down selection	0: pull down 1: pull up
	703	Reserved	
58	704	GPIO2 ultra-low power digital in enable (only used in SLG46881)	0: disable 1: enable
	705	GPIO2digital input latch configuration	00: without latch 01: normal latch 10: input data 0 latch (when latch_en is high) 11: input data 1 latch (when latch_en is high)
	706		
	707	GPIO2input mode configuration	00: digital without schmitt trigger 01: digital with schmitt trigger 10: low voltage digital in 11: analog IO
	708		
	709	GPIO2output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain
	710		
	711	GPIO2pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
59	712		
	713	GPIO2pull up/down selection	0: pull down 1: pull up
	714	GPI0digital input latch configuration	00: without latch 01: normal latch 10: input data 0 latch (when latch_en is high) 11: input data 1 latch (when latch_en is high)
	715		
	716	GPI0input mode configuration	00: digital without schmitt trigger 01: digital with schmitt trigger 10: low voltage digital in 11: analog IO
	717		
	718	GPI0pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	719		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
5A	720	GPI0pull up/down selection	0: pull down 1: pull up
	721	GPI1 ultra-low power digital in enable (only used in SLG46881)	0: disable 1: enable
	722 723	GPI1digital input latch configuration	00: without latch 01: normal latch 10: input data 0 latch (when latch_en is high) 11: input data 1 latch (when latch_en is high)
	724 725	GPI1input mode configuration	00: digital without schmitt trigger 01: digital with schmitt trigger 10: low voltage digital in 11: analog IO
	726 727	GPI1pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
5B	728	GPI1pull up/down selection	0: pull down 1: pull up
	729	GPI2 ultra-low power digital in enable (only used in SLG46881)	0: disable 1: enable
	730 731	GPI2/SDA input mode configuration	00: digital without schmitt trigger 01: digital with schmitt trigger 10: low voltage digital in 11: analog IO
	732 733	GPI2/SDA pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	734	GPI2/SDApull up/down selection	0: pull down 1: pull up
	735	GPI3 ultra-low power digital in enable (only used in SLG46881)	0: disable 1: enable
5C	736 737	GPI3/SCL input mode configuration	00: digital without schmitt trigger 01: digital with schmitt trigger 10: low voltage digital in 11: analog IO
	738 739	GPI3/SCLpull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	740	GPI3/SCLpull up/down selection	0: pull down 1: pull up
	741	GPIO3 ultra-low power digital in enable (only used in SLG46881)	0: disable 1: enable
	742 743	GPIO3digital input latch configuration	00: without latch 01: normal latch 10: input data 0 latch (when latch_en is high) 11: input data 1 latch (when latch_en is high)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
5D	744	GPIO3input mode configuration	00: digital without schmitt trigger 01: digital with schmitt trigger 10: low voltage digital in 11: analog IO.
	745		
	746	GPIO3output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain
	747		
	748	GPIO3pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	749		
	750	GPIO3pull up/down selection	0: pull down 1: pull up
	751	Reserved	
5E	752	Reserved	
	753	GPIO4input mode configuration	00: digital without schmitt trigger 01: digital with schmitt trigger 10: low voltage digital in 11: analog IO
	754		
	755	GPIO4output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain
	756		
	757	GPIO4pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	758		
	759	GPIO4pull up/down selection	0: pull down 1: pull up
5F	760	Reserved	
	761	GPIO5input mode configuration	00: digital without schmitt trigger 01: digital with schmitt trigger 10: low voltage digital in 11: analog IO
	762		
	763	GPIO5output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain
	764		
	765	GPIO5pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	766		
	767	GPIO5pull up/down selection	0: pull down 1: pull up

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
60	768	GPO1output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain
	769		
	770	GPO1pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	771		
	772	GPO1pull up/down selection	0: pull down 1: pull up
	773	GPO1digital output source selection	0: from matrix 1: from ASM (ASM output to GPO bit[2])
	774	GPO1output enable	0: disable 1: enable.
	775	GPO2output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain
61	776		
	777	GPO2pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	778		
	779	GPO2pull up/down selection	0: pull down 1: pull up
	780	GPO2digital output source selection	0: from matrix 1: from ASM (ASM output to GPO bit[3]).
	781	GPO2output enable	0: disable 1: enable.
	782	GPO3output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain
	783		
62	784	GPO3pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	785		
	786	GPO3pull up/down selection	0: pull down 1: pull up
	787	GPO3digital output source selection	0: from matrix 1: from ASM (ASM output to GPO bit[4]).
	788	GPO3output enable	0: disable 1: enable.
	789	GPO4output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain
	790		
	791	GPO4pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
63	792		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
63	793	GPO4pull up/down selection	0: pull down 1: pull up
	794	GPO4digital output source selection	0: from matrix 1: from ASM (ASM output to GPO bit[5]).
	795	GPO4output enable	0: disable 1: enable.
	796	Reserved	
	797	GPIO6digital input latch configuration	00: without latch 01: normal latch 10: input data 0 latch (when latch_en is high) 11: input data 1 latch (when latch_en is high)
	798		
	799	GPIO6input mode configuration	00: digital without schmitt trigger 01: digital with schmitt trigger 10: low voltage digital in 11: analog IO.
64	800		
	801	GPIO6output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain
	802		
	803	GPIO6pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M.
	804		
	805	GPIO6pull up/down selection	0: pull down 1: pull up
	806	Reserved	
	807	Reserved	
65	808	GPIO7digital input latch configuration	00: without latch 01: normal latch 10: input data 0 latch (when latch_en is high) 11: input data 1 latch (when latch_en is high)
	809		
	810	GPIO7input mode configuration	00: digital without schmitt trigger 01: digital with schmitt trigger 10: low voltage digital in 11: analog IO
	811		
	812	GPIO7output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain
	813		
	814	GPIO7pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	815		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
66	816	GPIO7pull up/down selection	0: pull down 1: pull up
66	817	Reserved	
66	818	GPIO8 ultra-low power digital in enable (only used in SLG46881)	0: disable 1: enable
66	819 820	GPIO8input mode configuration	00: digital without schmitt trigger 01: digital with schmitt trigger 10: low voltage digital in 11: analog IO
66	821 822	GPIO8output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain
66 / 67	823 824	GPIO8pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
67	825	GPIO8pull up/down selection	0: pull down 1: pull up
67	826	GPI4 ultra-low power digital in enable (only used in SLG46881)	0: disable 1: enable
67	827 828	GPI4digital input latch configuration	00: without latch 01: normal latch 10: input data 0 latch (when latch_en is high) 11: input data 1 latch (when latch_en is high)
67	829 830	GPI4input mode configuration	00: digital without schmitt trigger 01: digital with schmitt trigger 10: low voltage digital in 11: analog IO
67 / 68	831 832	GPI4pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
68	833	GPI4pull up/down selection	0: pull down 1: pull up
68	834	GPI5 ultra-low power digital in enable (only used in SLG46881)	0: disable 1: enable
68	835 836	GPI5digital input latch configuration	00: without latch 01: normal latch 10: input data 0 latch (when latch_en is high) 11: input data 1 latch (when latch_en is high)
68	837 838	GPI5input mode configuration	00: digital without schmitt trigger 01: digital with schmitt trigger 10: low voltage digital in 11: analog IO

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
68	839	GPI5pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
69	840		
69	841	GPI5pull up/down selection	0: pull down 1: pull up
69	842	GPI6 ultra-low power digital in enable (only used in SLG46881)	0: disable 1: enable
69	843	GPI6input mode configuration	00: digital without schmitt trigger 01: digital with schmitt trigger 10: low voltage digital in 11: analog IO
69	844		
69	845	GPI6pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
69	846		
69	847	GPI6pull up/down selection	0: pull down 1: pull up

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
6A	848	GPI7 ultra-low power digital in enable (only used in SLG46881)	0: disable 1: enable
6A	849 850	GPI7input mode configuration	00: digital without schmitt trigger 01: digital with schmitt trigger 10: low voltage digital in 11: analog IO
6A	851 852	GPI7pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
6A	853	GPI7pull up/down selection	0: pull down 1: pull up
6A	854	GPIO9 ultra-low power digital in enable (only used in SLG46881)	0: disable 1: enable
6A / 6B	855 856	GPIO9input mode configuration	00: digital without schmitt trigger 01: digital with schmitt trigger 10: low voltage digital in 11: analog IO
6B	857 858	GPIO9output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain
6B	859 860	GPIO9pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
6B	861	GPIO9pull up/down selection	0: pull down 1: pull up
6B	862	GPIO10 ultra-low power digital in enable (only used in SLG46881)	0: disable 1: enable
6B / 6C	863 864	GPIO10input mode configuration	00: digital without schmitt trigger 01: digital with schmitt trigger 10: low voltage digital in 11: analog IO
6C	865 866	GPIO10output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain
6C	867 868	GPIO10pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M.
6C	869	GPIO10pull up/down selection	0: pull down 1: pull up
6C	870	GPIO11 ultra-low power digital in enable (only used in SLG46881)	0: disable 1: enable

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
6C	871	GPIO11input mode configuration	00: digital without schmitt trigger 01: digital with schmitt trigger 10: low voltage digital in 11: analog IO
6D	872		
6D	873	GPIO11output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain
6D	874		
6D	875	GPIO11pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
6D	876		
6D	877	GPIO11pull up/down selection	0: pull down 1: pull up
6D	878	Reserved	
6D	879	GPO5output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain
6E	880		
6E	881	GPO5pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
6E	882		
6E	883	GPO5pull up/down selection	0: pull down 1: pull up
6E	884	GPO5digital output source selection	0: from matrix 1: from ASM (ASM output to GPO bit[6])
6E	885	GPO5output enable	0: disable 1: enable
6E	886	GPO6output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain
6E	887		
6F	888	GPO6pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
6F	889		
6F	890	GPO6pull up/down selection	0: pull down 1: pull up
6F	891	GPO6digital output source selection	0: from matrix 1: from ASM (ASM output to GPO bit[7]).
6F	892	GPO6output enable	0: disable 1: enable
6F	893	I^2C mode selection.	0: I^2C fast mode + 1: I^2C standard/fast mode
6F	894	XTAL enable and matrix in51 source mux select	1: xtal enable is controlled by matrix out78 and matrix in51 source is from Xtal OSC 0: xtal is powered down and matrix in51 source is from GPI4

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
6F	895	XTAL matrix enable signal gating	0: matrix enable signal (matrix out78) is gated and xtal is controlled be register [894] 1: matrix enable signal is effective if register [894] = 1 (matrix out78 = 0 -] off, matrix out78 = 1 -] on)
70	896	DLY/CNT0 Mode Selection	00:DLY 01: one shot 10: frequency det 11: cnt register [913]=0
	897		
	898	DLY/CNT0 edge Mode Selection	00:both edge 01: falling edge 10: rising edge 11: High Level Reset (only in CNT mode)
	899		
	900	DLY/CNT0 Clock Source Select	Clock source sel[3:0] 0000: 25M; 0001: 25M/4; 0010: 2.048M 0011: 2.048M/8; 0100: 2.048M/64; 0101: 2.048M/512; 0110: 2.048K; 0111: 2.048K/8; 1000: 2.048K/64; 1001: 2.048K/512; 1010: 2.048K/4096 1011: 2.048K/32768; 1100: 2.048K/262144; 1101: CNT4_END; 1110: External; 1111: No-used
	901		
	902		
	903		
71	904	FSM0 SET/RST Selection	0: Reset to 0 1: Set to data
	905	CNT0 output pol selection	0: Default Output 1: Inverted Output
	906	CNT0 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	907		
	908	lut4_0 or DLY/CNT0 selection	0: LUT4_0 1: DLY/CNT0(16bits)
	909	Wake sleep power down state selection	0: (low) 1: (high)
	910	wake sleep mode selection	0: Default Mode 1: Wake Sleep Mode (registers [897:896]=11)
	911	Keep signal sync selection	0: bypass 1: after two DFFs
72	912	UP signal sync selection	0: bypass 1: after two DFFs
	913	CNT0 DLY EDET FUNCTION Selection	0: normal 1: DLY function edge detection (registers [897:896]=00)
	914	CNT0 CNT mode SYNC selection	0: bypass 1: after two DFFs
	915	CNT1 CNT mode SYNC selection	0: bypass 1: after two DFFs

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
72	916	DLY/CNT1 Clock Source Select	Clock source sel[3:0] 0000: 25M; 0001: 25M/4; 0010: 2.048M 0011: 2.048M/8; 0100: 2.048M/64; 0101: 2.048M/512; 0110: 2.048K; 0111: 2.048K/8; 1000: 2.048K/64; 1001: 2.048K/512; 1010: 2.048K/4096 1011: 2.048K/32768; 1100: 2.048K/262144; 1101: CNT0_END; 1110: External; 1111: No-used
	917		
	918		
	919		
73	920	CNT1 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	921		
	922	CNT1 function and edge mode selection	0000: Both Edge Delay 0001: Falling Edge Delay 0010: Rising Edge Delay 0011: Both Edge One Shot 0100: Falling Edge One Shot 0101: Rising Edge One Shot 0110: Both Edge Freq Detect 0111: Falling Edge Freq Detect 1000: Rising Edge Freq Detect 1001: Both Edge Detect 1010: Falling Edge Detect 1011: Rising Edge Detect 1100: Both Edge Reset CNT 1101: Falling Edge Reset CNT 1110: Rising Edge Reset CNT 1111: High Level Reset CNT
	923		
	924		
	925		
	926	CNT1 output pol selection	0: Default Output 1: Inverted Output
	927	LUT3_4 or CNT_1 selection	0: LUT3_4 1: DLY/CNT1(8bits)
74	928	CNT2 CNT mode SYNC selection	0: bypass; 1: after two DFFs

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
74	929	DLY/CNT2 Clock Source Select	Clock source sel[3:0] 0000: 25M; 0001: 25M/4; 0010: 2.048M 0011: 2.048M/8; 0100: 2.048M/64; 0101: 2.048M/512; 0110: 2.048K; 0111: 2.048K/8; 1000: 2.048K/64; 1001: 2.048K/512; 1010: 2.048K/4096 1011: 2.048K/32768; 1100: 2.048K/262144; 1101: CNT1_END; 1110: External; 1111: No-used
	930		
	931		
	932		
	933	CNT2 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	934		
	935	CNT2 function and edge mode selection	0000: Both Edge Delay 0001: Falling Edge Delay 0010: Rising Edge Delay 0011: Both Edge One Shot 0100: Falling Edge One Shot 0101: Rising Edge One Shot 0110: Both Edge Freq Detect 0111: Falling Edge Freq Detect 1000: Rising Edge Freq Detect 1001: Both Edge Detect 1010: Falling Edge Detect 1011: Rising Edge Detect 1100: Both Edge Reset CNT 1101: Falling Edge Reset CNT 1110: Rising Edge Reset CNT 1111: High Level Reset CNT register [941]=0
75	936		
	937		
	938		
	939	CNT2 output pol selection	0: Default Output 1: Inverted Output
	940	LUT3_5 or CNT_2 selection	0: LUT3_5 1: DLY/CNT2(8bits)
	941	CNT2 DLY EDET FUNCTION Selection	0: normal 1: DLY function edge detection (registers [938:935]=0000/0001/0010)
	942	CNT3 CNT mode SYNC selection	0: bypass 1: after two DFFs

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
75	943	DLY/CNT3 Clock Source Select	Clock source sel[3:0] 0000: 25M; 0001: 25M/4; 0010: 2.048M 0011: 2.048M/8; 0100: 2.048M/64; 0101: 2.048M/512; 0110: 2.048K; 0111: 2.048K/8; 1000: 2.048K/64; 1001: 2.048K/512; 1010: 2.048K/4096 1011: 2.048K/32768; 1100: 2.048K/262144; 1101: CNT2_END; 1110: External; 1111: No-used
76	944		
	945		
	946		
	947	CNT3 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	948		
	949	CNT3 function and edge mode selection	0000: Both Edge Delay 0001: Falling Edge Delay 0010: Rising Edge Delay 0011: Both Edge One Shot 0100: Falling Edge One Shot 0101: Rising Edge One Shot 0110: Both Edge Freq Detect 0111: Falling Edge Freq Detect 1000: Rising Edge Freq Detect 1001: Both Edge Detect 1010: Falling Edge Detect 1011: Rising Edge Detect 1100: Both Edge Reset CNT 1101: Falling Edge Reset CNT 1110: Rising Edge Reset CNT 1111: High Level Reset CNT
	950		
	951		
77	952		
	953	CNT3 output pol selection	0: Default Output 1: Inverted Output
	954	LUT3_6 or CNT_3 selection	0: LUT3_6 1: DLY/CNT3(8bits)
	955	CNT4 CNT mode SYNC selection	0: bypass 1: after two DFFs

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
77	956	DLY/CNT4 Clock Source Select	Clock source sel[3:0] 0000: 25M; 0001: 25M/4; 0010: 2.048M 0011: 2.048M/8; 0100: 2.048M/64; 0101: 2.048M/512; 0110: 2.048K; 0111: 2.048K/8; 1000: 2.048K/64; 1001: 2.048K/512; 1010: 2.048K/4096 1011: 2.048K/32768; 1100: 2.048K/262144; 1101: CNT3_END; 1110: External; 1111: No-used
	957		
	958		
	959		
78	960	CNT3 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	961		
	962	CNT4 function and edge mode selection	0000: Both Edge Delay 0001: Falling Edge Delay 0010: Rising Edge Delay 0011: Both Edge One Shot 0100: Falling Edge One Shot 0101: Rising Edge One Shot 0110: Both Edge Freq Detect 0111: Falling Edge Freq Detect 1000: Rising Edge Freq Detect 1001: Both Edge Detect 1010: Falling Edge Detect 1011: Rising Edge Detect 1100: Both Edge Reset CNT 1101: Falling Edge Reset CNT 1110: Rising Edge Reset CNT 1111: High Level Reset CNT
	963		
	964		
	965		
	966	CNT4 output pol selection	0: Default Output 1: Inverted Output
	967	LUT3_7 or CNT_4 selection	0: LUT3_7 1: DLY/CNT4(8bits)
79	968	REG_TEST_EN	

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
79	969	TOP test path select	Digital test mux selection: 0000: GPO6 normal output, 0001: CNT_GOOD 0010: BG CHOP CK 0011: Data compare result 0100:ASM error flag 0101:F1_GO 0110: F1_GOOD 0111: DM_DONE 1000: BG_OK no delay 1001: BGOK_DLY 1010: 100ns delay test 1011: 1uS delay test 1100: sig_F1ACMP_OUT 1101: normal speed ACMP VrefOK 1110: low speed ACMP VrefOK 1111: ACMP_H0_OK signal
	970		
	971		
	972		
	973	Control DFT Test enable	0: matrix work at normal function 1: test matrix by DFT
	974	Signal of DFT selection (AOUT[83])	Select DFT test matrix or test DFT itself function 0: bypass mode (normal DFT test) 1:tied high or low (test DFT itself function)
	975	Signal of DFT tied low or high	Set input signal high or low to test DFT itself function 0: tied low 1: tied high
7A	976	ASM State 0 Output Memory for 8 GPOs	Memory for GPO 0
	977		Memory for GPO 1
	978		Memory for GPO 2
	979		Memory for GPO 3
	980		Memory for GPO 4
	981		Memory for GPO 5
	982		Memory for GPO 6
	983		Memory for GPO 7
7B	984	ASM State 1 Output Memory for 8 GPOs	Memory for GPO 0
	985		Memory for GPO 1
	986		Memory for GPO 2
	987		Memory for GPO 3
	988		Memory for GPO 4
	989		Memory for GPO 5
	990		Memory for GPO 6
	991		Memory for GPO 7

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
7C	992	ASM State 2 Output Memory for 8 GPOs	Memory for GPO 0
	993		Memory for GPO 1
	994		Memory for GPO 2
	995		Memory for GPO 3
	996		Memory for GPO 4
	997		Memory for GPO 5
	998		Memory for GPO 6
	999		Memory for GPO 7
7D	1000	ASM State 3 Output Memory for 8 GPOs	Memory for GPO 0
	1001		Memory for GPO 1
	1002		Memory for GPO 2
	1003		Memory for GPO 3
	1004		Memory for GPO 4
	1005		Memory for GPO 5
	1006		Memory for GPO 6
	1007		Memory for GPO 7
7E	1008	ASM State 4 Output Memory for 8 GPOs	Memory for GPO 0
	1009		Memory for GPO 1
	1010		Memory for GPO 2
	1011		Memory for GPO 3
	1012		Memory for GPO 4
	1013		Memory for GPO 5
	1014		Memory for GPO 6
	1015		Memory for GPO 7
7F	1016	ASM State 5 Output Memory for 8 GPOs	Memory for GPO 0
	1017		Memory for GPO 1
	1018		Memory for GPO 2
	1019		Memory for GPO 3
	1020		Memory for GPO 4
	1021		Memory for GPO 5
	1022		Memory for GPO 6
	1023		Memory for GPO 7
80	1024	ASM State 6 Output Memory for 8 GPOs	Memory for GPO 0
	1025		Memory for GPO 1
	1026		Memory for GPO 2
	1027		Memory for GPO 3
	1028		Memory for GPO 4
	1029		Memory for GPO 5
	1030		Memory for GPO 6
	1031		Memory for GPO 7

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
81	1032	ASM State 7 Output Memory for 8 GPOs	Memory for GPO 0
	1033		Memory for GPO 1
	1034		Memory for GPO 2
	1035		Memory for GPO 3
	1036		Memory for GPO 4
	1037		Memory for GPO 5
	1038		Memory for GPO 6
	1039		Memory for GPO 7
82	1040	ASM State 8 Output Memory for 8 GPOs	Memory for GPO 0
	1041		Memory for GPO 1
	1042		Memory for GPO 2
	1043		Memory for GPO 3
	1044		Memory for GPO 4
	1045		Memory for GPO 5
	1046		Memory for GPO 6
	1047		Memory for GPO 7
83	1048	ASM State 9 Output Memory for 8 GPOs	Memory for GPO 0
	1049		Memory for GPO 1
	1050		Memory for GPO 2
	1051		Memory for GPO 3
	1052		Memory for GPO 4
	1053		Memory for GPO 5
	1054		Memory for GPO 6
	1055		Memory for GPO 7
84	1056	ASM State 10 Output Memory for 8 GPOs	Memory for GPO 0
	1057		Memory for GPO 1
	1058		Memory for GPO 2
	1059		Memory for GPO 3
	1060		Memory for GPO 4
	1061		Memory for GPO 5
	1062		Memory for GPO 6
	1063		Memory for GPO 7
85	1064	ASM State 11 Output Memory for 8 GPOs	Memory for GPO 0
	1065		Memory for GPO 1
	1066		Memory for GPO 2
	1067		Memory for GPO 3
	1068		Memory for GPO 4
	1069		Memory for GPO 5
	1070		Memory for GPO 6
	1071		Memory for GPO 7

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
86	1072	ASM State 0 Output Memory for Matrix Input	Memory for Matrix input 0
	1073		Memory for Matrix input 1
	1074		Memory for Matrix input 2
	1075		Memory for Matrix input 3
	1076	ASM State 1 Output Memory for Matrix Input	Memory for Matrix input 0
	1077		Memory for Matrix input 1
	1078		Memory for Matrix input 2
	1079		Memory for Matrix input 3
87	1080	ASM State 2 Output Memory for Matrix Input	Memory for Matrix input 0
	1081		Memory for Matrix input 1
	1082		Memory for Matrix input 2
	1083		Memory for Matrix input 3
	1084	ASM State 3 Output Memory for Matrix Input	Memory for Matrix input 0
	1085		Memory for Matrix input 1
	1086		Memory for Matrix input 2
	1087		Memory for Matrix input 3
88	1088	ASM State 4 Output Memory for Matrix Input	Memory for Matrix input 0
	1089		Memory for Matrix input 1
	1090		Memory for Matrix input 2
	1091		Memory for Matrix input 3
	1092	ASM State 5 Output Memory for Matrix Input	Memory for Matrix input 0
	1093		Memory for Matrix input 1
	1094		Memory for Matrix input 2
	1095		Memory for Matrix input 3
89	1096	ASM State 6 Output Memory for Matrix Input	Memory for Matrix input 0
	1097		Memory for Matrix input 1
	1098		Memory for Matrix input 2
	1099		Memory for Matrix input 3
	1100	ASM State 7 Output Memory for Matrix Input	Memory for Matrix input 0
	1101		Memory for Matrix input 1
	1102		Memory for Matrix input 2
	1103		Memory for Matrix input 3
8A	1104	ASM State 8 Output Memory for Matrix Input	Memory for Matrix input 0
	1105		Memory for Matrix input 1
	1106		Memory for Matrix input 2
	1107		Memory for Matrix input 3
	1108	ASM State 9 Output Memory for Matrix Input	Memory for Matrix input 0
	1109		Memory for Matrix input 1
	1110		Memory for Matrix input 2
	1111		Memory for Matrix input 3

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
8B	1112	ASM State 10 Output Memory for Matrix Input	Memory for Matrix input 0
	1113		Memory for Matrix input 1
	1114		Memory for Matrix input 2
	1115		Memory for Matrix input 3
	1116	ASM State 11 Output Memory for Matrix Input	Memory for Matrix input 0
	1117		Memory for Matrix input 1
	1118		Memory for Matrix input 2
	1119		Memory for Matrix input 3
8C	1120	ASM Initial State Selection	0000 --] 1011: State 0 --] State 11
	1121		
	1122		
	1123		
	1124	Reserved registers for ASM	
	1125		
	1126		
	1127		
8D	1128	6Bit MATRIX_IN_Setting0	OUT0_Setting0: REG_MATRIX_IN_SEL[5:0]
	1129		
	1130		
	1131		
	1132		
	1133		
	1134	6Bit MATRIX_IN_Setting1	OUT0_Setting0: REG_MATRIX_IN_SEL[11:6]
	1135		
8E	1136		
	1137		
	1138		
	1139		
	1140	6Bit MATRIX_IN_Setting2	OUT0_Setting0: REG_MATRIX_IN_SEL[17:12]
	1141		
	1142		
	1143		
8F	1144		
	1145		
	1146	6Bit MATRIX_IN_Setting3	OUT0_Setting0: REG_MATRIX_IN_SEL[23:18]
	1147		
	1148		
	1149		
	1150		
	1151		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
90	1152	6Bit MATRIX_IN_Setting0	OUT1_Setting0: REG_MATRIX_IN_SEL[5:0]
	1153		
	1154		
	1155		
	1156		
	1157		
	1158	6Bit MATRIX_IN_Setting1	OUT1_Setting0: REG_MATRIX_IN_SEL[11:6]
	1159		
91	1160		
	1161		
	1162		
	1163		
	1164	6Bit MATRIX_IN_Setting2	OUT1_Setting0: REG_MATRIX_IN_SEL[17:12]
	1165		
	1166		
	1167		
92	1168		
	1169		
	1170	6Bit MATRIX_IN_Setting3	OUT1_Setting0: REG_MATRIX_IN_SEL[23:18]
	1171		
	1172		
	1173		
	1174		
	1175		
93	1176	6Bit MATRIX_IN_Setting0	OUT2_Setting0: REG_MATRIX_IN_SEL[5:0]
	1177		
	1178		
	1179		
	1180		
	1181		
	1182	6Bit MATRIX_IN_Setting1	OUT2_Setting0: REG_MATRIX_IN_SEL[11:6]
	1183		
94	1184		
	1185		
	1186		
	1187		
	1188	6Bit MATRIX_IN_Setting2	OUT2_Setting0: REG_MATRIX_IN_SEL[17:12]
	1189		
	1190		
	1191		
95	1192		
	1193		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
95	1194	6Bit MATRIX_IN_Setting3	OUT2_Setting0: REG_MATRIX_IN_SEL[23:18]
	1195		
	1196		
	1197		
	1198		
	1199		
96	1200	State0_6BitMatrix_OUT0 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
	1201		
	1202	State0_6BitMatrix_OUT1 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
	1203		
	1204	State0_6BitMatrix_OUT2 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
	1205		
	1206	State1_6BitMatrix_OUT0 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
	1207		
97	1208	State1_6BitMatrix_OUT1 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
	1209		
	1210	State1_6BitMatrix_OUT2 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
	1211		
	1212	State2_6BitMatrix_OUT0 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
	1213		
	1214	State2_6BitMatrix_OUT1 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
	1215		
98	1216	State2_6BitMatrix_OUT2 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
	1217		
	1218	State3_6BitMatrix_OUT0 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
	1219		
	1220	State3_6BitMatrix_OUT1 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
	1221		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
98	1222 1223	State3_6BitMatrix_OUT2 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
99	1224 1225	State4_6BitMatrix_OUT0 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
99	1226 1227	State4_6BitMatrix_OUT1 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
99	1228 1229	State4_6BitMatrix_OUT2 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
99	1230 1231	State5_6BitMatrix_OUT0 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
9A	1232 1233	State5_6BitMatrix_OUT1 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
9A	1234 1235	State5_6BitMatrix_OUT2 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
9A	1236 1237	State6_6BitMatrix_OUT0 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
9A	1238 1239	State6_6BitMatrix_OUT1 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
9B	1240 1241	State6_6BitMatrix_OUT2 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
9B	1242 1243	State7_6BitMatrix_OUT0 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
9B	1244 1245	State7_6BitMatrix_OUT1 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
9B	1246 1247	State7_6BitMatrix_OUT2 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
9C	1248	State8_6BitMatrix_OUT0 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
	1249		
	1250	State8_6BitMatrix_OUT1 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
	1251		
	1252	State8_6BitMatrix_OUT2 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
	1253		
	1254	State9_6BitMatrix_OUT0 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
	1255		
9D	1256	State9_6BitMatrix_OUT1 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
	1257		
	1258	State9_6BitMatrix_OUT2 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
	1259		
	1260	State10_6BitMatrix_OUT0 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
	1261		
	1262	State10_6BitMatrix_OUT1 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
	1263		
9E	1264	State10_6BitMatrix_OUT2 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
	1265		
	1266	State11_6BitMatrix_OUT0 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
	1267		
	1268	State11_6BitMatrix_OUT1 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
	1269		
	1270	State11_6BitMatrix_OUT2 4 Settings selection	00: Settings 0 01: Settings 1 10: Settings 2 11: Settings 3
	1271		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
9F	1272	ASM Input Matrix (Signal Source for State 0 →State 0 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1273		
	1274		
	1275	ASM Input Matrix (Signal Source for State 0 →State 1 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1276		
	1277		
	1278	ASM Input Matrix (Signal Source for State 0 →State 2 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1279		
A0	1280		
	1281	ASM Input Matrix (Signal Source for State 0 →State 3 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1282		
	1283		
	1284	ASM Input Matrix (Signal Source for State 0 →State 4 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1285		
	1286		
	1287	ASM Input Matrix (Signal Source for State 0 →State 5 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
A1	1288		
	1289		
	1290	ASM Input Matrix (Signal Source for State 0 →State 6 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1291		
	1292		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
A1	1293	ASM Input Matrix (Signal Source for State 0 →State 7 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1294		
	1295		
A2	1296	ASM Input Matrix (Signal Source for State 0 →State 8 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1297		
	1298		
	1299	ASM Input Matrix (Signal Source for State 0 →State 9 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1300		
	1301		
	1302	ASM Input Matrix (Signal Source for State 0 →State 10 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1303		
A3	1304		
	1305	ASM Input Matrix (Signal Source for State 0 →State 11 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1306		
	1307		
	1308	ASM Input Matrix (Signal Source for State 1 →State 10 Transition), bit [2] Note: This bit, along with registers [1343:1342], select the signal source for State 1 to State 10 Transition	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1309	ASM Input Matrix (Signal Source for State 1 →State 11 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1310		
	1311		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
A4	1312 1313 1314	ASM Input Matrix (Signal Source for State 1 →State 0 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
A4	1315 1316 1317	ASM Input Matrix (Signal Source for State 1 →State 1 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
A4	1318 1319	ASM Input Matrix (Signal Source for State 1 →State 2 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
A5	1320		
A5	1321 1322 1323	ASM Input Matrix (Signal Source for State 1 →State 3 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
A5	1324 1325 1326	ASM Input Matrix (Signal Source for State 1 →State 4 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
A5	1327	ASM Input Matrix (Signal Source for State 1 →State 5 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
A6	1328 1329		
A6	1330 1331 1332	ASM Input Matrix (Signal Source for State 1 →State 6 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
A6	1333	ASM Input Matrix (Signal Source for State 1 →State 7 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1334		
	1335		
A7	1336	ASM Input Matrix (Signal Source for State 1 →State 8 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1337		
	1338		
	1339	ASM Input Matrix (Signal Source for State 1 →State 9 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1340		
	1341		
	1342	ASM Input Matrix (Signal Source for State 1 →State 10 Transition), bits [1:0] Note: These bits, along with register [1308], select the signal source for State 1 to State 10 Transition	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1343		
A8	1344	ASM Input Matrix (Signal Source for State 2 →State 0 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1345		
	1346		
	1347	ASM Input Matrix (Signal Source for State 2 →State 1 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1348		
	1349		
	1350	ASM Input Matrix (Signal Source for State 2 →State 2 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1351		
A9	1352		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
A9	1353 1354 1355	ASM Input Matrix (Signal Source for State 2 →State 3 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
A9	1356 1357 1358	ASM Input Matrix (Signal Source for State 2 →State 4 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
A9 / AA	1359 1360 1361	ASM Input Matrix (Signal Source for State 2 →State 5 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
AA	1362 1363 1364	ASM Input Matrix (Signal Source for State 2 →State 6 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
AA	1365 1366 1367	ASM Input Matrix (Signal Source for State 2 →State 7 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
AB	1368 1369 1370	ASM Input Matrix (Signal Source for State 2 →State 8 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
AB	1371 1372 1373	ASM Input Matrix (Signal Source for State 2 →State 9 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1

Address Byte	Register Bit	Signal Function	Register Bit Definition
AB	1374	ASM Input Matrix (Signal Source for State 2 →State 10 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
AB	1375		
AC	1376		
AC	1377	ASM Input Matrix (Signal Source for State 2 →State 11 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
AC	1378		
AC	1379		
AC	1380	ASM Input Matrix (Signal Source for State 3 →State 10 Transition), bit [2] Note: This bit, along with registers [1415:1414], select the signal source for State 3 to State 10 Transition	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
AC	1381	ASM Input Matrix (Signal Source for State 3 →State 11 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
AC	1382		
AC	1383		
AD	1384	ASM Input Matrix (Signal Source for State 3 →State 0 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
AD	1385		
AD	1386		
AD	1387	ASM Input Matrix (Signal Source for State 3 →State 1 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
AD	1388		
AD	1389		
AD	1390	ASM Input Matrix (Signal Source for State 3 →State 2 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
AD	1391		
AE	1392		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
AE	1393	ASM Input Matrix (Signal Source for State 3 →State 3 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1394		
	1395		
	1396	ASM Input Matrix (Signal Source for State 3 →State 4 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1397		
	1398		
	1399	ASM Input Matrix (Signal Source for State 3 →State 5 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
AF	1400		
	1401		
	1402	ASM Input Matrix (Signal Source for State 3 →State 6 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1403		
	1404		
	1405	ASM Input Matrix (Signal Source for State 3 →State 7 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1406		
	1407		
BO	1408	ASM Input Matrix (Signal Source for State 3 →State 8 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1409		
	1410		
	1411	ASM Input Matrix (Signal Source for State 3 →State 9 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1412		
	1413		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
BO	1414	ASM Input Matrix (Signal Source for State 3 →State 10 Transition), bits [1:0] Note: These bits, along with registers [1380], select the signal source for State 3 to State 10 Transition	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
BO	1415		
B1	1416	ASM Input Matrix (Signal Source for State 4 →State 0 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
B1	1417		
B1	1418		
B1	1419	ASM Input Matrix (Signal Source for State 4 →State 1 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
B1	1420		
B1	1421		
B1	1422	ASM Input Matrix (Signal Source for State 4 →State 2 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
B1	1423		
B2	1424		
B2	1425	ASM Input Matrix (Signal Source for State 4 →State 3 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
B2	1426		
B2	1427		
B2	1428	ASM Input Matrix (Signal Source for State 4 →State 4 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
B2	1429		
B2	1430		
B2	1431	ASM Input Matrix (Signal Source for State 4 →State 5 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
B3	1432		
B3	1433		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
B3	1434	ASM Input Matrix (Signal Source for State 4 →State 6 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1435		
	1436		
	1437	ASM Input Matrix (Signal Source for State 4 →State 7 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1438		
	1439		
B4	1440	ASM Input Matrix (Signal Source for State 4 →State 8 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1441		
	1442		
	1443	ASM Input Matrix (Signal Source for State 4 →State 9 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1444		
	1445		
	1446	ASM Input Matrix (Signal Source for State 4 →State 10 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1447		
B5	1448		
	1449	ASM Input Matrix (Signal Source for State 4 →State 11 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1450		
	1451		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
B5	1452	ASM Input Matrix (Signal Source for State 5 →State 10 Transition), bit [2] Note: This bit, along with registers [1487:1486], select the signal source for State 5 to State 10 Transition	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
B5	1453 1454 1455	ASM Input Matrix (Signal Source for State 5 →State 11 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
B6	1456 1457 1458	ASM Input Matrix (Signal Source for State 5 →State 0 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
B6	1459 1460 1461	ASM Input Matrix (Signal Source for State 5 →State 1 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
B6 B7	1462 1463 1464	ASM Input Matrix (Signal Source for State 5 →State 2 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
B7	1465 1466 1467	ASM Input Matrix (Signal Source for State 5 →State 3 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
B7	1468	ASM Input Matrix (Signal Source for State 5 →State 4 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1469		
	1470		
	1471	ASM Input Matrix (Signal Source for State 5 →State 5 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
B8	1472		
	1473		
	1474	ASM Input Matrix (Signal Source for State 5 →State 6 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1475		
	1476		
	1477	ASM Input Matrix (Signal Source for State 5 →State 7 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1478		
	1479		
B9	1480	ASM Input Matrix (Signal Source for State 5 →State 8 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1481		
	1482		
	1483	ASM Input Matrix (Signal Source for State 5 →State 9 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1484		
	1485		
	1486	ASM Input Matrix (Signal Source for State 5 →State 10 Transition), bits [1:0] Note: These bits, along with register [1452], select the signal source for State 5 to State 10 Transition	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1487		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
BA	1488	ASM Input Matrix (Signal Source for State 6 →State 0 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1489		
	1490		
	1491	ASM Input Matrix (Signal Source for State 6 →State 1 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1492		
	1493		
	1494	ASM Input Matrix (Signal Source for State 6 →State 2 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1495		
BB	1496		
	1497	ASM Input Matrix (Signal Source for State 6 →State 3 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1498		
	1499		
	1500	ASM Input Matrix (Signal Source for State 6 →State 4 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1501		
	1502		
	1503	ASM Input Matrix (Signal Source for State 6 →State 5 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
BC	1504		
	1505		
	1506	ASM Input Matrix (Signal Source for State 6 →State 6 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1507		
	1508		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
BC	1509	ASM Input Matrix (Signal Source for State 6 →State 7 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
BC	1510		
BC	1511		
BD	1512	ASM Input Matrix (Signal Source for State 6 →State 8 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
BD	1513		
BD	1514		
BD	1515	ASM Input Matrix (Signal Source for State 6 →State 9 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
BD	1516		
BD	1517		
BD	1518	ASM Input Matrix (Signal Source for State 6 →State 10 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
BD	1519		
BE	1520		
BE	1521	ASM Input Matrix (Signal Source for State 6 →State 11 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
BE	1522		
BE	1523		
BE	1524	ASM Input Matrix (Signal Source for State 7 →State 10 Transition), bit [2] Note: This bit, along with registers [1559:1558], select the signal source for State 7 to State 10 Transition	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
BE	1525	ASM Input Matrix (Signal Source for State 7 →State 11 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
BE	1526		
BE	1527		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
BF	1528	ASM Input Matrix (Signal Source for State 7 →State 0 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1529		
	1530		
	1531	ASM Input Matrix (Signal Source for State 7 →State 1 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1532		
	1533		
	1534	ASM Input Matrix (Signal Source for State 7 →State 2 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1535		
C0	1536		
	1537	ASM Input Matrix (Signal Source for State 7 →State 3 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1538		
	1539		
	1540	ASM Input Matrix (Signal Source for State 7 →State 4 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1541		
	1542		
	1543	ASM Input Matrix (Signal Source for State 7 →State 5 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
C1	1544		
	1545		
	1546	ASM Input Matrix (Signal Source for State 7 →State 6 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1547		
	1548		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
C1	1549	ASM Input Matrix (Signal Source for State 7 →State 7 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1550		
	1551		
C2	1552	ASM Input Matrix (Signal Source for State 7 →State 8 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1553		
	1554		
	1555	ASM Input Matrix (Signal Source for State 7 →State 9 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1556		
	1557		
	1558	ASM Input Matrix (Signal Source for State 7 →State 10 Transition), bits [1:0] Note: These bits, along with register [1524], select the signal source for State 7 to State 10 Transition	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1559		
C3	1560	ASM Input Matrix (Signal Source for State 8 →State 0 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1561		
	1562		
	1563	ASM Input Matrix (Signal Source for State 8 →State 1 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1564		
	1565		
	1566	ASM Input Matrix (Signal Source for State 8 →State 2 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1567		
C4	1568		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
C4	1569	ASM Input Matrix (Signal Source for State 8 →State 3 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
C4	1570		
C4	1571		
C4	1572	ASM Input Matrix (Signal Source for State 8 →State 4 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
C4	1573		
C4	1574		
C4	1575	ASM Input Matrix (Signal Source for State 8 →State 5 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
C5	1576		
C5	1577		
C5	1578	ASM Input Matrix (Signal Source for State 8 →State 6 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
C5	1579		
C5	1580		
C5	1581	ASM Input Matrix (Signal Source for State 8 →State 7 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
C5	1582		
C5	1583		
C6	1584	ASM Input Matrix (Signal Source for State 8 →State 8Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
C6	1585		
C6	1586		
C6	1587	ASM Input Matrix (Signal Source for State 8 →State 9 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
C6	1588		
C6	1589		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
C6	1590	ASM Input Matrix (Signal Source for State 8 →State 10 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1591		
C7	1592		
	1593	ASM Input Matrix (Signal Source for State 8 →State 11 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1594		
	1595		
	1596	ASM Input Matrix (Signal Source for State 9 →State 10 Transition), bit [2] Note: This bit, along with registers [1631:1630], select the signal source for State 9 to State 10 Transition	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1597	ASM Input Matrix (Signal Source for State 9 →State 11 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1598		
	1599		
C8	1600	ASM Input Matrix (Signal Source for State 9 →State 0 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1601		
	1602		
	1603	ASM Input Matrix (Signal Source for State 9 →State 1 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1604		
	1605		
	1606	ASM Input Matrix (Signal Source for State 9 →State 2 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1607		
C9	1608		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
C9	1609	ASM Input Matrix (Signal Source for State 9 →State 3 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1610		
	1611		
	1612	ASM Input Matrix (Signal Source for State 9 →State 4 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1613		
	1614		
	1615	ASM Input Matrix (Signal Source for State 9 →State 5 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
CA	1616		
	1617		
	1618	ASM Input Matrix (Signal Source for State 9 →State 6 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1619		
	1620		
	1621	ASM Input Matrix (Signal Source for State 9 →State 7 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1622		
	1623		
CB	1624	ASM Input Matrix (Signal Source for State 9 →State 8 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1625		
	1626		
	1627	ASM Input Matrix (Signal Source for State 9 →State 9 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1628		
	1629		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
CB	1630	ASM Input Matrix (Signal Source for State 9 →State 10 Transition), bits [1:0] Note: These bits, along with register [1596], select the signal source for State 9 to State 10 Transition	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1631		
CC	1632	ASM Input Matrix (Signal Source for State 10 →State 0 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1633		
	1634		
	1635	ASM Input Matrix (Signal Source for State 10 →State 1 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1636		
	1637		
	1638	ASM Input Matrix (Signal Source for State 10 →State 2 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1639		
CD	1640		
	1641	ASM Input Matrix (Signal Source for State 10 →State 3 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1642		
	1643		
	1644	ASM Input Matrix (Signal Source for State 10 →State 4 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1645		
	1646		
	1647	ASM Input Matrix (Signal Source for State 10 →State 5 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
CE	1648		
	1649		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
CE	1650 1651 1652	ASM Input Matrix (Signal Source for State 10 →State 6 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
CE	1653 1654 1655	ASM Input Matrix (Signal Source for State 10 →State 7 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
CF	1656 1657 1658	ASM Input Matrix (Signal Source for State 10 →State 8 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
CF	1659 1660 1661	ASM Input Matrix (Signal Source for State 10 →State 9 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
CF / D0	1662 1663 1664	ASM Input Matrix (Signal Source for State 10 →State 10 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
D0	1665 1666 1667	ASM Input Matrix (Signal Source for State 10 →State 11 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
D0	1668	ASM Input Matrix (Signal Source for State 11 →State 10 Transition), bit [2] Note: This bit, along with registers [1703:1702], select the signal source for State 11 to State 10 Transition	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
D0	1669	ASM Input Matrix (Signal Source for State 11 →State 11 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1670		
	1671		
D1	1672	ASM Input Matrix (Signal Source for State 11 →State 0 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1673		
	1674		
	1675	ASM Input Matrix (Signal Source for State 11 →State 1 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1676		
	1677		
	1678	ASM Input Matrix (Signal Source for State 11 →State 2 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1679		
D2	1680		
	1681	ASM Input Matrix (Signal Source for State 11 →State 3 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1682		
	1683		
	1684	ASM Input Matrix (Signal Source for State 11 →State 4 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1685		
	1686		
	1687	ASM Input Matrix (Signal Source for State 11 →State 5 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
D3	1688		
	1689		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
D3	1690	ASM Input Matrix (Signal Source for State 11 →State 6 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1691		
	1692		
	1693	ASM Input Matrix (Signal Source for State 11 →State 7 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1694		
	1695		
D4	1696	ASM Input Matrix (Signal Source for State 11 →State 8Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1697		
	1698		
	1699	ASM Input Matrix (Signal Source for State 11 →State 9 Transition)	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1700		
	1701		
	1702	ASM Input Matrix (Signal Source for State 11 →State 10 Transition), bits [1:0] Note: These bits, along with register [1668], select the signal source for State 11 to State 10 Transition	000: VSS; 001: 6Bit_Matrix_OUT0; 010: 6Bit_Matrix_OUT1; 011: 6Bit_Matrix_OUT2; 100: DM0_0; 101: DM0_1; 110: DM1_0; 111: DM1_1
	1703		
D5	1704	DM0_0 Configuration Register 0 IN0 of LUT3	REG_MATRIX_LUT3_IN0_SEL[5:0]
	1705		
	1706		
	1707		
	1708		
	1709		
	1710	DM0_0 Configuration Register 0 IN1 of LUT3	REG_MATRIX_LUT3_IN1_SEL[5:0]
	1711		
D6	1712		
	1713		
	1714		
	1715		

Address Byte	Address Register Bit	Signal Function	Register Bit Definition
D6	1716	DM0_0 Configuration Register 0 IN2 of LUT3	REG_MATRIX_LUT3_IN2_SEL[5:0]
	1717		
	1718		
	1719		
D7	1720		
	1721		
	1722	DM0_0 Configuration Register 0 DLY input from matrix	DM Delay input
	1723		
	1724		
	1725		
	1726		
	1727		
D8	1728	DM0_0 Configuration Register 0 Data of LUT3	REG_VAL_LUT3[0]
	1729		REG_VAL_LUT3[1]
	1730		REG_VAL_LUT3[2]
	1731		REG_VAL_LUT3[3]
	1732		REG_VAL_LUT3[4]
	1733		REG_VAL_LUT3[5]
	1734		REG_VAL_LUT3[6]
	1735		REG_VAL_LUT3[7]
D9	1736	DM0_0 Configuration Register 0 Data of LUT2	REG_VAL_LUT2[0]
	1737		REG_VAL_LUT2[1]
	1738		REG_VAL_LUT2[2]
	1739		REG_VAL_LUT2[3]
	1740	DM0_0 Configuration Register 0 Clock source selection	Clock source sel[3:0] 0000: 25M; 0001: 25M/4; 0010: 2.048M 0011: 2.048M/8; 0100: 2.048M/64; 0101: 2.048M/512; 0110: 2.048K; 0111: 2.048K/8; 1000: 2.048K/64; 1001: 2.048K/512; 1010: 2.048K/4096 1011: 2.048K/32768; 1100: 2.048K/262144; 1101: CNT_END; 1110: External; 1111: External
	1741		
	1742		
	1743		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
DA	1744	DM0_0 Configuration Register 0 Data of Delay	Data[7:0]
	1745		
	1746		
	1747		
	1748		
	1749		
	1750		
	1751		
DB	1752	DM0_0 Configuration Register 0 DLY input initial selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1753		
	1754	DM0_0 Configuration Register 0 DLY/CNT Function selection	0000: Both Edge Delay 0001: Falling Edge Delay 0010: Rising Edge Delay 0011: Both Edge One Shot 0100: Falling Edge One Shot 0101: Rising Edge One Shot 0110: Both Edge Freq Detect 0111: Falling Edge Freq Detect 1000: Rising Edge Freq Detect 1001: Both Edge Detect 1010: Falling Edge Detect 1011: Rising Edge Detect 1100: Both Edge Reset CNT 1101: Falling Edge Reset CNT 1110: Rising Edge Reset CNT 1111: High Level Reset CNT
	1755		
	1756		
	1757		
	1758	DM0_0 Configuration Register 0 MUX1 selection for LUT2	0: from LUT3 1: from matrix (DLY IN)
	1759	DM0_0 Configuration Register 0 MUX2 selection for DLY input	0: from matrix (DLY IN) 1: from LUT3
DC	1760	DM0_0 Configuration Register 1 IN0 of LUT3	REG_MATRIX_LUT3_IN0_SEL[5:0]
	1761		
	1762		
	1763		
	1764		
	1765		
	1766	DM0_0 Configuration Register 1 IN1 of LUT3	REG_MATRIX_LUT3_IN1_SEL[5:0]
	1767		
DD	1768		
	1769		
	1770		
	1771		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
DD	1772	DM0_0 Configuration Register 1 IN2 of LUT3	REG_MATRIX_LUT3_IN2_SEL[5:0]
	1773		
	1774		
	1775		
DE	1776		
	1777		
	1778	DM0_0 Configuration Register 1 DLY input from matrix	DM Delay input
	1779		
	1780		
	1781		
	1782		
	1783		
DF	1784	DM0_0 Configuration Register 1 Data of LUT3	REG_VAL_LUT3[0]
	1785		REG_VAL_LUT3[1]
	1786		REG_VAL_LUT3[2]
	1787		REG_VAL_LUT3[3]
	1788		REG_VAL_LUT3[4]
	1789		REG_VAL_LUT3[5]
	1790		REG_VAL_LUT3[6]
	1791		REG_VAL_LUT3[7]
E0	1792	DM0_0 Configuration Register 1 Data of LUT2	REG_VAL_LUT2[0]
	1793		REG_VAL_LUT2[1]
	1794		REG_VAL_LUT2[2]
	1795		REG_VAL_LUT2[3]
	1796	DM0_0 Configuration Register 1 Clock source selection	Clock source sel[3:0] 0000: 25M; 0001: 25M/4; 0010: 2.048M 0011: 2.048M/8; 0100: 2.048M/64; 0101: 2.048M/512; 0110: 2.048K; 0111: 2.048K/8; 1000: 2.048K/64; 1001: 2.048K/512; 1010: 2.048K/4096 1011: 2.048K/32768; 1100: 2.048K/262144; 1101: CNT_END; 1110: External; 1111: External
	1797		
	1798		
	1799		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
E1	1800	DM0_0 Configuration Register 1 Data of Delay	Data[7:0]
	1801		
	1802		
	1803		
	1804		
	1805		
	1806		
	1807		
E2	1808	DM0_0 Configuration Register 1 DLY input initial selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1809		
	1810	DM0_0 Configuration Register 1 DLY/CNT Function selection	0000: Both Edge Delay 0001: Falling Edge Delay 0010: Rising Edge Delay 0011: Both Edge One Shot 0100: Falling Edge One Shot 0101: Rising Edge One Shot 0110: Both Edge Freq Detect 0111: Falling Edge Freq Detect 1000: Rising Edge Freq Detect 1001: Both Edge Detect 1010: Falling Edge Detect 1011: Rising Edge Detect 1100: Both Edge Reset CNT 1101: Falling Edge Reset CNT 1110: Rising Edge Reset CNT 1111: High Level Reset CNT
	1811		
	1812		
	1813		
	1814	DM0_0 Configuration Register 1 MUX1 selection for LUT2	0: from LUT3 1: from matrix (DLY IN)
	1815	DM0_0 Configuration Register 1 MUX2 selection for DLY input	0: from matrix (DLY IN) 1: from LUT3
E3	1816	DM0_0 Configuration Register 2 IN0 of LUT3	REG_MATRIX_LUT3_IN0_SEL[5:0]
	1817		
	1818		
	1819		
	1820		
	1821		
	1822	DM0_0 Configuration Register 2 IN1 of LUT3	REG_MATRIX_LUT3_IN1_SEL[5:0]
	1823		
E4	1824		
	1825		
	1826		
	1827		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
E4	1828	DM0_0 Configuration Register 2 IN2 of LUT3	REG_MATRIX_LUT3_IN2_SEL[5:0]
	1829		
	1830		
	1831		
E5	1832		
	1833		
	1834	DM0_0 Configuration Register 2 DLY input from matrix	DM Delay input
	1835		
	1836		
	1837		
	1838		
	1839		
E6	1840	DM0_0 Configuration Register 2 Data of LUT3	REG_VAL_LUT3[0]
	1841		REG_VAL_LUT3[1]
	1842		REG_VAL_LUT3[2]
	1843		REG_VAL_LUT3[3]
	1844		REG_VAL_LUT3[4]
	1845		REG_VAL_LUT3[5]
	1846		REG_VAL_LUT3[6]
	1847		REG_VAL_LUT3[7]
E7	1848	DM0_0 Configuration Register 2 Data of LUT2	REG_VAL_LUT2[0]
	1849		REG_VAL_LUT2[1]
	1850		REG_VAL_LUT2[2]
	1851		REG_VAL_LUT2[3]
	1852	DM0_0 Configuration Register 2 Clock source selection	Clock source sel[3:0] 0000: 25M; 0001: 25M/4; 0010: 2.048M 0011: 2.048M/8; 0100: 2.048M/64; 0101: 2.048M/512; 0110: 2.048K; 0111: 2.048K/8; 1000: 2.048K/64; 1001: 2.048K/512; 1010: 2.048K/4096 1011: 2.048K/32768; 1100: 2.048K/262144; 1101: CNT_END; 1110: External; 1111: External
	1853		
	1854		
	1855		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
E8	1856	DM0_0 Configuration Register 2 Data of Delay	Data[7:0]
	1857		
	1858		
	1859		
	1860		
	1861		
	1862		
	1863		
E9	1864	DM0_0 Configuration Register 2 DLY input initial selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1865		
	1866	DM0_0 Configuration Register 2 DLY/CNT Function selection	0000: Both Edge Delay 0001: Falling Edge Delay 0010: Rising Edge Delay 0011: Both Edge One Shot 0100: Falling Edge One Shot 0101: Rising Edge One Shot 0110: Both Edge Freq Detect 0111: Falling Edge Freq Detect 1000: Rising Edge Freq Detect 1001: Both Edge Detect 1010: Falling Edge Detect 1011: Rising Edge Detect 1100: Both Edge Reset CNT 1101: Falling Edge Reset CNT 1110: Rising Edge Reset CNT 1111: High Level Reset CNT
	1867		
	1868		
	1869		
	1870	DM0_0 Configuration Register 2 MUX1 selection for LUT2	0: from LUT3 1: from matrix (DLY IN)
	1871	DM0_0 Configuration Register 2 MUX2 selection for DLY input	0: from matrix (DLY IN) 1: from LUT3
EA	1872	DM0_0 Configuration Register 3 IN0 of LUT3	REG_MATRIX_LUT3_IN0_SEL[5:0]
	1873		
	1874		
	1875		
	1876		
	1877		
	1878	DM0_0 Configuration Register 3 IN1 of LUT3	REG_MATRIX_LUT3_IN1_SEL[5:0]
	1879		
EB	1880		
	1881		
	1882		
	1883		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
EB	1884	DM0_0 Configuration Register 3 IN2 of LUT3	REG_MATRIX_LUT3_IN2_SEL[5:0]
	1885		
	1886		
	1887		
EC	1888		
	1889		
	1890	DM0_0 Configuration Register 3 DLY input from matrix	DM Delay input
	1891		
	1892		
	1893		
	1894		
	1895		
ED	1896	DM0_0 Configuration Register 3 Data of LUT3	REG_VAL_LUT3[0]
	1897		REG_VAL_LUT3[1]
	1898		REG_VAL_LUT3[2]
	1899		REG_VAL_LUT3[3]
	1900		REG_VAL_LUT3[4]
	1901		REG_VAL_LUT3[5]
	1902		REG_VAL_LUT3[6]
	1903		REG_VAL_LUT3[7]
EE	1904	DM0_0 Configuration Register 3 Data of LUT2	REG_VAL_LUT2[0]
	1905		REG_VAL_LUT2[1]
	1906		REG_VAL_LUT2[2]
	1907		REG_VAL_LUT2[3]
	1908	DM0_0 Configuration Register 3 Clock source selection	Clock source sel[3:0] 0000: 25M; 0001: 25M/4; 0010: 2.048M 0011: 2.048M/8; 0100: 2.048M/64; 0101: 2.048M/512; 0110: 2.048K; 0111: 2.048K/8; 1000: 2.048K/64; 1001: 2.048K/512; 1010: 2.048K/4096 1011: 2.048K/32768; 1100: 2.048K/262144; 1101: CNT_END; 1110: External; 1111: External
	1909		
	1910		
	1911		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
EF	1912	DM0_0 Configuration Register 3 Data of Delay	Data[7:0]
	1913		
	1914		
	1915		
	1916		
	1917		
	1918		
	1919		
F0	1920	DM0_0 Configuration Register 3 DLY input initial selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1921		
	1922	DM0_0 Configuration Register 3 DLY/CNT Function selection	0000: Both Edge Delay 0001: Falling Edge Delay 0010: Rising Edge Delay 0011: Both Edge One Shot 0100: Falling Edge One Shot 0101: Rising Edge One Shot 0110: Both Edge Freq Detect 0111: Falling Edge Freq Detect 1000: Rising Edge Freq Detect 1001: Both Edge Detect 1010: Falling Edge Detect 1011: Rising Edge Detect 1100: Both Edge Reset CNT 1101: Falling Edge Reset CNT 1110: Rising Edge Reset CNT 1111: High Level Reset CNT
	1923		
	1924		
	1925		
	1926	DM0_0 Configuration Register 3 MUX1 selection for LUT2	0: from LUT3 1: from matrix (DLY IN)
	1927	DM0_0 Configuration Register 3 MUX2 selection for DLY input	0: from matrix (DLY IN) 1: from LUT3
F1	1928	DM0_0 Configuration Register 4 IN0 of LUT3	REG_MATRIX_LUT3_IN0_SEL[5:0]
	1929		
	1930		
	1931		
	1932		
	1933		
	1934	DM0_0 Configuration Register 4 IN1 of LUT3	REG_MATRIX_LUT3_IN1_SEL[5:0]
	1935		
F2	1936		
	1937		
	1938		
	1939		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
F2	1940	DM0_0 Configuration Register 4 IN2 of LUT3	REG_MATRIX_LUT3_IN2_SEL[5:0]
	1941		
	1942		
	1943		
F3	1944		
	1945		
	1946	DM0_0 Configuration Register 4 DLY input from matrix	DM Delay input
	1947		
	1948		
	1949		
	1950		
	1951		
F4	1952	DM0_0 Configuration Register 4 Data of LUT3	REG_VAL_LUT3[0]
	1953		REG_VAL_LUT3[1]
	1954		REG_VAL_LUT3[2]
	1955		REG_VAL_LUT3[3]
	1956		REG_VAL_LUT3[4]
	1957		REG_VAL_LUT3[5]
	1958		REG_VAL_LUT3[6]
	1959		REG_VAL_LUT3[7]
F5	1960	DM0_0 Configuration Register 4 Data of LUT2	REG_VAL_LUT2[0]
	1961		REG_VAL_LUT2[1]
	1962		REG_VAL_LUT2[2]
	1963		REG_VAL_LUT2[3]
	1964	DM0_0 Configuration Register 4 Clock source selection	Clock source sel[3:0] 0000: 25M; 0001: 25M/4; 0010: 2.048M 0011: 2.048M/8; 0100: 2.048M/64; 0101: 2.048M/512; 0110: 2.048K; 0111: 2.048K/8; 1000: 2.048K/64; 1001: 2.048K/512; 1010: 2.048K/4096 1011: 2.048K/32768; 1100: 2.048K/262144; 1101: CNT_END; 1110: External; 1111: External
	1965		
	1966		
	1967		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
F6	1968	DM0_0 Configuration Register 4 Data of Delay	Data[7:0]
	1969		
	1970		
	1971		
	1972		
	1973		
	1974		
	1975		
F7	1976	DM0_0 Configuration Register 4 DLY input initial selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1977		
	1978	DM0_0 Configuration Register 4 DLY/CNT Function selection	0000: Both Edge Delay 0001: Falling Edge Delay 0010: Rising Edge Delay 0011: Both Edge One Shot 0100: Falling Edge One Shot 0101: Rising Edge One Shot 0110: Both Edge Freq Detect 0111: Falling Edge Freq Detect 1000: Rising Edge Freq Detect 1001: Both Edge Detect 1010: Falling Edge Detect 1011: Rising Edge Detect 1100: Both Edge Reset CNT 1101: Falling Edge Reset CNT 1110: Rising Edge Reset CNT 1111: High Level Reset CNT
	1979		
	1980		
	1981		
	1982	DM0_0 Configuration Register 4 MUX1 selection for LUT2	0: from LUT3 1: from matrix (DLY IN)
	1983	DM0_0 Configuration Register 4 MUX2 selection for DLY input	0: from matrix (DLY IN) 1: from LUT3
F8	1984	DM0_0 Configuration Register 5 IN0 of LUT3	REG_MATRIX_LUT3_IN0_SEL[5:0]
	1985		
	1986		
	1987		
	1988		
	1989		
	1990	DM0_0 Configuration Register 5 IN1 of LUT3	REG_MATRIX_LUT3_IN1_SEL[5:0]
	1991		
F9	1992		
	1993		
	1994		
	1995		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
F9	1996	DM0_0 Configuration Register 5 IN2 of LUT3	REG_MATRIX_LUT3_IN2_SEL[5:0]
F9	1997		
F9	1998		
F9	1999		
FA	2000		
FA	2001		
FA	2002	DM0_0 Configuration Register 5 DLY input from matrix	DM Delay input
FA	2003		
FA	2004		
FA	2005		
FA	2006		
FA	2007		
FB	2008	DM0_0 Configuration Register 5 Data of LUT3	REG_VAL_LUT3[0]
FB	2009		REG_VAL_LUT3[1]
FB	2010		REG_VAL_LUT3[2]
FB	2011		REG_VAL_LUT3[3]
FB	2012		REG_VAL_LUT3[4]
FB	2013		REG_VAL_LUT3[5]
FB	2014		REG_VAL_LUT3[6]
FB	2015		REG_VAL_LUT3[7]
FC	2016	DM0_0 Configuration Register 5 Data of LUT2	REG_VAL_LUT2[0]
FC	2017		REG_VAL_LUT2[1]
FC	2018		REG_VAL_LUT2[2]
FC	2019		REG_VAL_LUT2[3]
FC	2020	DM0_0 Configuration Register 5 Clock source selection	Clock source sel[3:0] 0000: 25M; 0001: 25M/4; 0010: 2.048M 0011: 2.048M/8; 0100: 2.048M/64; 0101: 2.048M/512; 0110: 2.048K; 0111: 2.048K/8; 1000: 2.048K/64; 1001: 2.048K/512; 1010: 2.048K/4096 1011: 2.048K/32768; 1100: 2.048K/262144; 1101: CNT_END; 1110: External; 1111: External
FC	2021		
FC	2022		
FC	2023		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
FD	2024	DM0_0 Configuration Register 5 Data of Delay	Data[7:0]
	2025		
	2026		
	2027		
	2028		
	2029		
	2030		
	2031		
FE	2032	DM0_0 Configuration Register 5 DLY input initial selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	2033		
	2034	DM0_0 Configuration Register 5 DLY/CNT Function selection	0000: Both Edge Delay 0001: Falling Edge Delay 0010: Rising Edge Delay 0011: Both Edge One Shot 0100: Falling Edge One Shot 0101: Rising Edge One Shot 0110: Both Edge Freq Detect 0111: Falling Edge Freq Detect 1000: Rising Edge Freq Detect 1001: Both Edge Detect 1010: Falling Edge Detect 1011: Rising Edge Detect 1100: Both Edge Reset CNT 1101: Falling Edge Reset CNT 1110: Rising Edge Reset CNT 1111: High Level Reset CNT
	2035		
	2036		
	2037		
	2038	DM0_0 Configuration Register 5 MUX1 selection for LUT2	0: from LUT3 1: from matrix (DLY IN)
	2039	DM0_0 Configuration Register 5 MUX2 selection for DLY input	0: from matrix (DLY IN) 1: from LUT3
FF	2040	power sequency byte 5A	5A fixed
	2041		
	2042		
	2043		
	2044		
	2045		
	2046		
	2047		
100	2048	DM0_1 Configuration Register 0 IN0 of LUT3	REG_MATRIX_LUT3_IN0_SEL[5:0]
	2049		
	2050		
	2051		
	2052		
	2053		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
100	2054	DM0_1 Configuration Register 0 IN1 of LUT3	REG_MATRIX_LUT3_IN1_SEL[5:0]
	2055		
101	2056		
	2057		
	2058		
	2059		
	2060	DM0_1 Configuration Register 0 IN2 of LUT3	REG_MATRIX_LUT3_IN2_SEL[5:0]
	2061		
	2062		
	2063		
102	2064		
	2065		
	2066	DM0_1 Configuration Register 0 DLY input from matrix	DM Delay input
	2067		
	2068		
	2069		
	2070		
	2071		
103	2072	DM0_1 Configuration Register 0 Data of LUT3	REG_VAL_LUT3[0]
	2073		REG_VAL_LUT3[1]
	2074		REG_VAL_LUT3[2]
	2075		REG_VAL_LUT3[3]
	2076		REG_VAL_LUT3[4]
	2077		REG_VAL_LUT3[5]
	2078		REG_VAL_LUT3[6]
	2079		REG_VAL_LUT3[7]
104	2080	DM0_1 Configuration Register 0 Data of LUT2	REG_VAL_LUT2[0]
	2081		REG_VAL_LUT2[1]
	2082		REG_VAL_LUT2[2]
	2083		REG_VAL_LUT2[3]

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
104	2084	DM0_1 Configuration Register 0 Clock source selection	Clock source sel[3:0] 0000: 25M; 0001: 25M/4; 0010: 2.048M 0011: 2.048M/8; 0100: 2.048M/64; 0101: 2.048M/512; 0110: 2.048K; 0111: 2.048K/8; 1000: 2.048K/64; 1001: 2.048K/512; 1010: 2.048K/4096 1011: 2.048K/32768; 1100: 2.048K/262144; 1101: CNT_END; 1110: External; 1111: External
	2085		
	2086		
	2087		
105	2088	DM0_1 Configuration Register 0 Data of Delay	Data[7:0]
	2089		
	2090		
	2091		
	2092		
	2093		
	2094		
	2095		
106	2096	DM0_1 Configuration Register 0 DLY input initial selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	2097		
	2098	DM0_1 Configuration Register 0 DLY/CNT Function selection	0000: Both Edge Delay 0001: Falling Edge Delay 0010: Rising Edge Delay 0011: Both Edge One Shot 0100: Falling Edge One Shot 0101: Rising Edge One Shot 0110: Both Edge Freq Detect 0111: Falling Edge Freq Detect 1000: Rising Edge Freq Detect 1001: Both Edge Detect 1010: Falling Edge Detect 1011: Rising Edge Detect 1100: Both Edge Reset CNT 1101: Falling Edge Reset CNT 1110: Rising Edge Reset CNT 1111: High Level Reset CNT
	2099		
	2100		
	2101		
	2102	DM0_1 Configuration Register 0 MUX1 selection for LUT2	0: from LUT3 1: from matrix (DLY IN)
	2103	DM0_1 Configuration Register 0 MUX2 selection for DLY input	0: from matrix (DLY IN) 1: from LUT3

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
107	2104	DM0_1 Configuration Register 1 IN0 of LUT3	REG_MATRIX_LUT3_IN0_SEL[5:0]
	2105		
	2106		
	2107		
	2108		
	2109		
	2110	DM0_1 Configuration Register 1 IN1 of LUT3	REG_MATRIX_LUT3_IN1_SEL[5:0]
	2111		
108	2112		
	2113		
	2114		
	2115		
	2116	DM0_1 Configuration Register 1 IN2 of LUT3	REG_MATRIX_LUT3_IN2_SEL[5:0]
	2117		
	2118		
	2119		
109	2120		
	2121		
	2122	DM0_1 Configuration Register 1 DLY input from matrix	DM Delay input
	2123		
	2124		
	2125		
	2126		
	2127		
10A	2128	DM0_1 Configuration Register 1 Data of LUT3	REG_VAL_LUT3[0]
	2129		REG_VAL_LUT3[1]
	2130		REG_VAL_LUT3[2]
	2131		REG_VAL_LUT3[3]
	2132		REG_VAL_LUT3[4]
	2133		REG_VAL_LUT3[5]
	2134		REG_VAL_LUT3[6]
	2135		REG_VAL_LUT3[7]
10B	2136	DM0_1 Configuration Register 1 Data of LUT2	REG_VAL_LUT2[0]
	2137		REG_VAL_LUT2[1]
	2138		REG_VAL_LUT2[2]
	2139		REG_VAL_LUT2[3]

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
10B	2140	DM0_1 Configuration Register 1 Clock source selection	Clock source sel[3:0] 0000: 25M; 0001: 25M/4; 0010: 2.048M 0011: 2.048M/8; 0100: 2.048M/64; 0101: 2.048M/512; 0110: 2.048K; 0111: 2.048K/8; 1000: 2.048K/64; 1001: 2.048K/512; 1010: 2.048K/4096 1011: 2.048K/32768; 1100: 2.048K/262144; 1101: CNT_END; 1110: External; 1111: External
	2141		
	2142		
	2143		
10C	2144	DM0_1 Configuration Register 1 Data of Delay	Data[7:0]
	2145		
	2146		
	2147		
	2148		
	2149		
	2150		
	2151		
10D	2152	DM0_1 Configuration Register 1 DLY input initial selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	2153		
	2154	DM0_1 Configuration Register 1 DLY/CNT Function selection	0000: Both Edge Delay 0001: Falling Edge Delay 0010: Rising Edge Delay 0011: Both Edge One Shot 0100: Falling Edge One Shot 0101: Rising Edge One Shot 0110: Both Edge Freq Detect 0111: Falling Edge Freq Detect 1000: Rising Edge Freq Detect 1001: Both Edge Detect 1010: Falling Edge Detect 1011: Rising Edge Detect 1100: Both Edge Reset CNT 1101: Falling Edge Reset CNT 1110: Rising Edge Reset CNT 1111: High Level Reset CNT
	2155		
	2156		
	2157		
	2158	DM0_1 Configuration Register 1 MUX1 selection for LUT2	0: from LUT3 1: from matrix (DLY IN)
	2159	DM0_1 Configuration Register 1 MUX2 selection for DLY input	0: from matrix (DLY IN) 1: from LUT3

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
10E	2160	DM0_1 Configuration Register 2 IN0 of LUT3	REG_MATRIX_LUT3_IN0_SEL[5:0]
	2161		
	2162		
	2163		
	2164		
	2165		
	2166	DM0_1 Configuration Register 2 IN1 of LUT3	REG_MATRIX_LUT3_IN1_SEL[5:0]
	2167		
10F	2168		
	2169		
	2170		
	2171		
	2172	DM0_1 Configuration Register 2 IN2 of LUT3	REG_MATRIX_LUT3_IN2_SEL[5:0]
	2173		
	2174		
	2175		
110	2176		
	2177		
	2178	DM0_1 Configuration Register 2 DLY input from matrix	DM Delay input
	2179		
	2180		
	2181		
	2182		
	2183		
111	2184	DM0_1 Configuration Register 2 Data of LUT3	REG_VAL_LUT3[0]
	2185		REG_VAL_LUT3[1]
	2186		REG_VAL_LUT3[2]
	2187		REG_VAL_LUT3[3]
	2188		REG_VAL_LUT3[4]
	2189		REG_VAL_LUT3[5]
	2190		REG_VAL_LUT3[6]
	2191		REG_VAL_LUT3[7]
112	2192	DM0_1 Configuration Register 2 Data of LUT2	REG_VAL_LUT2[0]
	2193		REG_VAL_LUT2[1]
	2194		REG_VAL_LUT2[2]
	2195		REG_VAL_LUT2[3]

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
112	2196	DM0_1 Configuration Register 2 Clock source selection	Clock source sel[3:0] 0000: 25M; 0001: 25M/4; 0010: 2.048M 0011: 2.048M/8; 0100: 2.048M/64; 0101: 2.048M/512; 0110: 2.048K; 0111: 2.048K/8; 1000: 2.048K/64; 1001: 2.048K/512; 1010: 2.048K/4096 1011: 2.048K/32768; 1100: 2.048K/262144; 1101: CNT_END; 1110: External; 1111: External
	2197		
	2198		
	2199		
113	2200	DM0_1 Configuration Register 2 Data of Delay	Data[7:0]
	2201		
	2202		
	2203		
	2204		
	2205		
	2206		
	2207		
114	2208	DM0_1 Configuration Register 2 DLY input initial selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	2209		
	2210	DM0_1 Configuration Register 2 DLY/CNT Function selection	0000: Both Edge Delay 0001: Falling Edge Delay 0010: Rising Edge Delay 0011: Both Edge One Shot 0100: Falling Edge One Shot 0101: Rising Edge One Shot 0110: Both Edge Freq Detect 0111: Falling Edge Freq Detect 1000: Rising Edge Freq Detect 1001: Both Edge Detect 1010: Falling Edge Detect 1011: Rising Edge Detect 1100: Both Edge Reset CNT 1101: Falling Edge Reset CNT 1110: Rising Edge Reset CNT 1111: High Level Reset CNT
	2211		
	2212		
	2213		
	2214	DM0_1 Configuration Register 2 MUX1 selection for LUT2	0: from LUT3 1: from matrix (DLY IN)
	2215	DM0_1 Configuration Register 2 MUX2 selection for DLY input	0: from matrix (DLY IN) 1: from LUT3

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
115	2216	DM0_1 Configuration Register 3 IN0 of LUT3	REG_MATRIX_LUT3_IN0_SEL[5:0]
	2217		
	2218		
	2219		
	2220		
	2221		
	2222	DM0_1 Configuration Register 3 IN1 of LUT3	REG_MATRIX_LUT3_IN1_SEL[5:0]
	2223		
116	2224		
	2225		
	2226		
	2227		
	2228	DM0_1 Configuration Register 3 IN2 of LUT3	REG_MATRIX_LUT3_IN2_SEL[5:0]
	2229		
	2230		
	2231		
117	2232		
	2233		
	2234	DM0_1 Configuration Register 3 DLY input from matrix	DM Delay input
	2235		
	2236		
	2237		
	2238		
	2239		
118	2240	DM0_1 Configuration Register 3 Data of LUT3	REG_VAL_LUT3[0]
	2241		REG_VAL_LUT3[1]
	2242		REG_VAL_LUT3[2]
	2243		REG_VAL_LUT3[3]
	2244		REG_VAL_LUT3[4]
	2245		REG_VAL_LUT3[5]
	2246		REG_VAL_LUT3[6]
	2247		REG_VAL_LUT3[7]
119	2248	DM0_1 Configuration Register 3 Data of LUT2	REG_VAL_LUT2[0]
	2249		REG_VAL_LUT2[1]
	2250		REG_VAL_LUT2[2]
	2251		REG_VAL_LUT2[3]

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
119	2252	DM0_1 Configuration Register 3 Clock source selection	Clock source sel[3:0] 0000: 25M; 0001: 25M/4; 0010: 2.048M 0011: 2.048M/8; 0100: 2.048M/64; 0101: 2.048M/512; 0110: 2.048K; 0111: 2.048K/8; 1000: 2.048K/64; 1001: 2.048K/512; 1010: 2.048K/4096 1011: 2.048K/32768; 1100: 2.048K/262144; 1101: CNT_END; 1110: External; 1111: External
	2253		
	2254		
	2255		
11A	2256	DM0_1 Configuration Register 3 Data of Delay	Data[7:0]
	2257		
	2258		
	2259		
	2260		
	2261		
	2262		
	2263		
11B	2264	DM0_1 Configuration Register 3 DLY input initial selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	2265		
	2266	DM0_1 Configuration Register 3 DLY/CNT Function selection	0000: Both Edge Delay 0001: Falling Edge Delay 0010: Rising Edge Delay 0011: Both Edge One Shot 0100: Falling Edge One Shot 0101: Rising Edge One Shot 0110: Both Edge Freq Detect 0111: Falling Edge Freq Detect 1000: Rising Edge Freq Detect 1001: Both Edge Detect 1010: Falling Edge Detect 1011: Rising Edge Detect 1100: Both Edge Reset CNT 1101: Falling Edge Reset CNT 1110: Rising Edge Reset CNT 1111: High Level Reset CNT
	2267		
	2268		
	2269		
	2270	DM0_1 Configuration Register 3 MUX1 selection for LUT2	0: from LUT3 1: from matrix (DLY IN)
	2271	DM0_1 Configuration Register 3 MUX2 selection for DLY input	0: from matrix (DLY IN) 1: from LUT3

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
11C	2272	DM0_1 Configuration Register 4 IN0 of LUT3	REG_MATRIX_LUT3_IN0_SEL[5:0]
	2273		
	2274		
	2275		
	2276		
	2277		
	2278	DM0_1 Configuration Register 4 IN1 of LUT3	REG_MATRIX_LUT3_IN1_SEL[5:0]
	2279		
11D	2280		
	2281		
	2282		
	2283		
	2284	DM0_1 Configuration Register 4 IN2 of LUT3	REG_MATRIX_LUT3_IN2_SEL[5:0]
	2285		
	2286		
	2287		
11E	2288		
	2289		
	2290	DM0_1 Configuration Register 4 DLY input from matrix	DM Delay input
	2291		
	2292		
	2293		
	2294		
	2295		
11F	2296	DM0_1 Configuration Register 4 Data of LUT3	REG_VAL_LUT3[0]
	2297		REG_VAL_LUT3[1]
	2298		REG_VAL_LUT3[2]
	2299		REG_VAL_LUT3[3]
	2300		REG_VAL_LUT3[4]
	2301		REG_VAL_LUT3[5]
	2302		REG_VAL_LUT3[6]
	2303		REG_VAL_LUT3[7]
120	2304	DM0_1 Configuration Register 4 Data of LUT2	REG_VAL_LUT2[0]
	2305		REG_VAL_LUT2[1]
	2306		REG_VAL_LUT2[2]
	2307		REG_VAL_LUT2[3]

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
120	2308	DM0_1 Configuration Register 4 Clock source selection	Clock source sel[3:0] 0000: 25M; 0001: 25M/4; 0010: 2.048M 0011: 2.048M/8; 0100: 2.048M/64; 0101: 2.048M/512; 0110: 2.048K; 0111: 2.048K/8; 1000: 2.048K/64; 1001: 2.048K/512; 1010: 2.048K/4096 1011: 2.048K/32768; 1100: 2.048K/262144; 1101: CNT_END; 1110: External; 1111: External
	2309		
	2310		
	2311		
121	2312	DM0_1 Configuration Register 4 Data of Delay	Data[7:0]
	2313		
	2314		
	2315		
	2316		
	2317		
	2318		
	2319		
122	2320	DM0_1 Configuration Register 4 DLY input initial selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	2321		
	2322	DM0_1 Configuration Register 4 DLY/CNT Function selection	0000: Both Edge Delay 0001: Falling Edge Delay 0010: Rising Edge Delay 0011: Both Edge One Shot 0100: Falling Edge One Shot 0101: Rising Edge One Shot 0110: Both Edge Freq Detect 0111: Falling Edge Freq Detect 1000: Rising Edge Freq Detect 1001: Both Edge Detect 1010: Falling Edge Detect 1011: Rising Edge Detect 1100: Both Edge Reset CNT 1101: Falling Edge Reset CNT 1110: Rising Edge Reset CNT 1111: High Level Reset CNT
	2323		
	2324		
	2325		
	2326	DM0_1 Configuration Register 4 MUX1 selection for LUT2	0: from LUT3 1: from matrix (DLY IN)
	2327	DM0_1 Configuration Register 4 MUX2 selection for DLY input	0: from matrix (DLY IN) 1: from LUT3

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
123	2328	DM0_1 Configuration Register 5 IN0 of LUT3	REG_MATRIX_LUT3_IN0_SEL[5:0]
	2329		
	2330		
	2331		
	2332		
	2333		
	2334	DM0_1 Configuration Register 5 IN1 of LUT3	REG_MATRIX_LUT3_IN1_SEL[5:0]
	2335		
124	2336		
	2337		
	2338		
	2339		
	2340	DM0_1 Configuration Register 5 IN2 of LUT3	REG_MATRIX_LUT3_IN2_SEL[5:0]
	2341		
	2342		
	2343		
125	2344		
	2345		
	2346	DM0_1 Configuration Register 5 DLY input from matrix	DM Delay input
	2347		
	2348		
	2349		
	2350		
	2351		
126	2352	DM0_1 Configuration Register 5 Data of LUT3	REG_VAL_LUT3[0]
	2353		REG_VAL_LUT3[1]
	2354		REG_VAL_LUT3[2]
	2355		REG_VAL_LUT3[3]
	2356		REG_VAL_LUT3[4]
	2357		REG_VAL_LUT3[5]
	2358		REG_VAL_LUT3[6]
	2359		REG_VAL_LUT3[7]

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
127	2360	DM0_1 Configuration Register 5 Data of LUT2	REG_VAL_LUT2[0]
	2361		REG_VAL_LUT2[1]
	2362		REG_VAL_LUT2[2]
	2363		REG_VAL_LUT2[3]
	2364 2365 2366 2367	DM0_1 Configuration Register 5 Clock source selection	Clock source sel[3:0] 0000: 25M; 0001: 25M/4; 0010: 2.048M 0011: 2.048M/8; 0100: 2.048M/64; 0101: 2.048M/512; 0110: 2.048K; 0111: 2.048K/8; 1000: 2.048K/64; 1001: 2.048K/512; 1010: 2.048K/4096 1011: 2.048K/32768; 1100: 2.048K/262144; 1101: CNT_END; 1110: External; 1111: External
128	2368 2369 2370 2371 2372 2373 2374 2375	DM0_1 Configuration Register 5 Data of Delay	Data[7:0]
129	2376 2377	DM0_1 Configuration Register 5 DLY input initial selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	2378 2379 2380 2381	DM0_1 Configuration Register 5 DLY/CNT Function selection	0000: Both Edge Delay 0001: Falling Edge Delay 0010: Rising Edge Delay 0011: Both Edge One Shot 0100: Falling Edge One Shot 0101: Rising Edge One Shot 0110: Both Edge Freq Detect 0111: Falling Edge Freq Detect 1000: Rising Edge Freq Detect 1001: Both Edge Detect 1010: Falling Edge Detect 1011: Rising Edge Detect 1100: Both Edge Reset CNT 1101: Falling Edge Reset CNT 1110: Rising Edge Reset CNT 1111: High Level Reset CNT
	2382	DM0_1 Configuration Register 5 MUX1 selection for LUT2	0: from LUT3 1: from matrix (DLY IN)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
129	2383	DM0_1 Configuration Register 5 MUX2 selection for DLY input	0: from matrix (DLY IN) 1: from LUT3
12A	2384	DM1_0 Configuration Register 0 IN0 of LUT3	REG_MATRIX_LUT3_IN0_SEL[5:0]
	2385		
	2386		
	2387		
	2388		
	2389		
	2390	DM1_0 Configuration Register 0 IN1 of LUT3	REG_MATRIX_LUT3_IN1_SEL[5:0]
	2391		
12B	2392		
	2393		
	2394		
	2395		
	2396	DM1_0 Configuration Register 0 IN2 of LUT3	REG_MATRIX_LUT3_IN2_SEL[5:0]
	2397		
	2398		
	2399		
12C	2400		
	2401		
	2402	DM1_0 Configuration Register 0 DLY input from matrix	DM Delay input
	2403		
	2404		
	2405		
	2406		
	2407		
12D	2408	DM1_0 Configuration Register 0 Data of LUT3	REG_VAL_LUT3[0]
	2409		REG_VAL_LUT3[1]
	2410		REG_VAL_LUT3[2]
	2411		REG_VAL_LUT3[3]
	2412		REG_VAL_LUT3[4]
	2413		REG_VAL_LUT3[5]
	2414		REG_VAL_LUT3[6]
	2415		REG_VAL_LUT3[7]
12E	2416	DM1_0 Configuration Register 0 Data of LUT2	REG_VAL_LUT2[0]
	2417		REG_VAL_LUT2[1]
	2418		REG_VAL_LUT2[2]
	2419		REG_VAL_LUT2[3]

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
12E	2420	DM1_0 Configuration Register 0 Clock source selection	Clock source sel[3:0] 0000: 25M; 0001: 25M/4; 0010: 2.048M 0011: 2.048M/8; 0100: 2.048M/64; 0101: 2.048M/512; 0110: 2.048K; 0111: 2.048K/8; 1000: 2.048K/64; 1001: 2.048K/512; 1010: 2.048K/4096 1011: 2.048K/32768; 1100: 2.048K/262144; 1101: CNT_END; 1110: External; 1111: External
	2421		
	2422		
	2423		
12F	2424	DM1_0 Configuration Register 0 Data of Delay	Data[7:0]
	2425		
	2426		
	2427		
	2428		
	2429		
	2430		
	2431		
130	2432	DM1_0 Configuration Register 0 DLY input initial selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	2433		
	2434	DM1_0 Configuration Register 0 DLY/CNT Function selection	0000: Both Edge Delay 0001: Falling Edge Delay 0010: Rising Edge Delay 0011: Both Edge One Shot 0100: Falling Edge One Shot 0101: Rising Edge One Shot 0110: Both Edge Freq Detect 0111: Falling Edge Freq Detect 1000: Rising Edge Freq Detect 1001: Both Edge Detect 1010: Falling Edge Detect 1011: Rising Edge Detect 1100: Both Edge Reset CNT 1101: Falling Edge Reset CNT 1110: Rising Edge Reset CNT 1111: High Level Reset CNT
	2435		
	2436		
	2437		
	2438	DM1_0 Configuration Register 0 MUX1 selection for LUT2	0: from LUT3 1: from matrix (DLY IN)
	2439	DM1_0 Configuration Register 0 MUX2 selection for DLY input	0: from matrix (DLY IN) 1: from LUT3

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
131	2440	DM1_0 Configuration Register 1 IN0 of LUT3	REG_MATRIX_LUT3_IN0_SEL[5:0]
	2441		
	2442		
	2443		
	2444		
	2445		
	2446	DM1_0 Configuration Register 1 IN1 of LUT3	REG_MATRIX_LUT3_IN1_SEL[5:0]
	2447		
132	2448		
	2449		
	2450		
	2451		
	2452	DM1_0 Configuration Register 1 IN2 of LUT3	REG_MATRIX_LUT3_IN2_SEL[5:0]
	2453		
	2454		
	2455		
133	2456		
	2457		
	2458	DM1_0 Configuration Register 1 DLY input from matrix	DM Delay input
	2459		
	2460		
	2461		
	2462		
	2463		
134	2464	DM1_0 Configuration Register 1 Data of LUT3	REG_VAL_LUT3[0]
	2465		REG_VAL_LUT3[1]
	2466		REG_VAL_LUT3[2]
	2467		REG_VAL_LUT3[3]
	2468		REG_VAL_LUT3[4]
	2469		REG_VAL_LUT3[5]
	2470		REG_VAL_LUT3[6]
	2471		REG_VAL_LUT3[7]
135	2472	DM1_0 Configuration Register 1 Data of LUT2	REG_VAL_LUT2[0]
	2473		REG_VAL_LUT2[1]
	2474		REG_VAL_LUT2[2]
	2475		REG_VAL_LUT2[3]

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
135	2476	DM1_0 Configuration Register 1 Clock source selection	Clock source sel[3:0] 0000: 25M; 0001: 25M/4; 0010: 2.048M 0011: 2.048M/8; 0100: 2.048M/64; 0101: 2.048M/512; 0110: 2.048K; 0111: 2.048K/8; 1000: 2.048K/64; 1001: 2.048K/512; 1010: 2.048K/4096 1011: 2.048K/32768; 1100: 2.048K/262144; 1101: CNT_END; 1110: External; 1111: External
	2477		
	2478		
	2479		
136	2480	DM1_0 Configuration Register 1 Data of Delay	Data[7:0]
	2481		
	2482		
	2483		
	2484		
	2485		
	2486		
	2487		
137	2488	DM1_0 Configuration Register 1 DLY input initial selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	2489		
	2490	DM1_0 Configuration Register 1 DLY/CNT Function selection	0000: Both Edge Delay 0001: Falling Edge Delay 0010: Rising Edge Delay 0011: Both Edge One Shot 0100: Falling Edge One Shot 0101: Rising Edge One Shot 0110: Both Edge Freq Detect 0111: Falling Edge Freq Detect 1000: Rising Edge Freq Detect 1001: Both Edge Detect 1010: Falling Edge Detect 1011: Rising Edge Detect 1100: Both Edge Reset CNT 1101: Falling Edge Reset CNT 1110: Rising Edge Reset CNT 1111: High Level Reset CNT
	2491		
	2492		
	2493		
	2494	DM1_0 Configuration Register 1 MUX1 selection for LUT2	0: from LUT3 1: from matrix (DLY IN)
	2495	DM1_0 Configuration Register 1 MUX2 selection for DLY input	0: from matrix (DLY IN) 1: from LUT3

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
138	2496	DM1_0 Configuration Register 2 IN0 of LUT3	REG_MATRIX_LUT3_IN0_SEL[5:0]
	2497		
	2498		
	2499		
	2500		
	2501		
	2502	DM1_0 Configuration Register 2 IN1 of LUT3	REG_MATRIX_LUT3_IN1_SEL[5:0]
	2503		
139	2504		
	2505		
	2506		
	2507		
	2508	DM1_0 Configuration Register 2 IN2 of LUT3	REG_MATRIX_LUT3_IN2_SEL[5:0]
	2509		
	2510		
	2511		
13A	2512		
	2513		
	2514	DM1_0 Configuration Register 2 DLY input from matrix	DM Delay input
	2515		
	2516		
	2517		
	2518		
	2519		
13B	2520	DM1_0 Configuration Register 2 Data of LUT3	REG_VAL_LUT3[0]
	2521		REG_VAL_LUT3[1]
	2522		REG_VAL_LUT3[2]
	2523		REG_VAL_LUT3[3]
	2524		REG_VAL_LUT3[4]
	2525		REG_VAL_LUT3[5]
	2526		REG_VAL_LUT3[6]
	2527		REG_VAL_LUT3[7]
13C	2528	DM1_0 Configuration Register 2 Data of LUT2	REG_VAL_LUT2[0]
	2529		REG_VAL_LUT2[1]
	2530		REG_VAL_LUT2[2]
	2531		REG_VAL_LUT2[3]

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
13C	2532	DM1_0 Configuration Register 2 Clock source selection	Clock source sel[3:0] 0000: 25M; 0001: 25M/4; 0010: 2.048M 0011: 2.048M/8; 0100: 2.048M/64; 0101: 2.048M/512; 0110: 2.048K; 0111: 2.048K/8; 1000: 2.048K/64; 1001: 2.048K/512; 1010: 2.048K/4096 1011: 2.048K/32768; 1100: 2.048K/262144; 1101: CNT_END; 1110: External; 1111: External
	2533		
	2534		
	2535		
13D	2536	DM1_0 Configuration Register 2 Data of Delay	Data[7:0]
	2537		
	2538		
	2539		
	2540		
	2541		
	2542		
	2543		
13E	2544	DM1_0 Configuration Register 2 DLY input initial selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	2545		
	2546	DM1_0 Configuration Register 2 DLY/CNT Function selection	0000: Both Edge Delay 0001: Falling Edge Delay 0010: Rising Edge Delay 0011: Both Edge One Shot 0100: Falling Edge One Shot 0101: Rising Edge One Shot 0110: Both Edge Freq Detect 0111: Falling Edge Freq Detect 1000: Rising Edge Freq Detect 1001: Both Edge Detect 1010: Falling Edge Detect 1011: Rising Edge Detect 1100: Both Edge Reset CNT 1101: Falling Edge Reset CNT 1110: Rising Edge Reset CNT 1111: High Level Reset CNT
	2547		
	2548		
	2549		
	2550	DM1_0 Configuration Register 2 MUX1 selection for LUT2	0: from LUT3 1: from matrix (DLY IN)
	2551	DM1_0 Configuration Register 2 MUX2 selection for DLY input	0: from matrix (DLY IN) 1: from LUT3

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
13F	2552	DM1_0 Configuration Register 3 IN0 of LUT3	REG_MATRIX_LUT3_IN0_SEL[5:0]
	2553		
	2554		
	2555		
	2556		
	2557		
	2558	DM1_0 Configuration Register 3 IN1 of LUT3	REG_MATRIX_LUT3_IN1_SEL[5:0]
	2559		
140	2560		
	2561		
	2562		
	2563		
	2564	DM1_0 Configuration Register 3 IN2 of LUT3	REG_MATRIX_LUT3_IN2_SEL[5:0]
	2565		
	2566		
	2567		
141	2568		
	2569		
	2570	DM1_0 Configuration Register 3 DLY input from matrix	DM Delay input
	2571		
	2572		
	2573		
	2574		
	2575		
142	2576	DM1_0 Configuration Register 3 Data of LUT3	REG_VAL_LUT3[0]
	2577		REG_VAL_LUT3[1]
	2578		REG_VAL_LUT3[2]
	2579		REG_VAL_LUT3[3]
	2580		REG_VAL_LUT3[4]
	2581		REG_VAL_LUT3[5]
	2582		REG_VAL_LUT3[6]
	2583		REG_VAL_LUT3[7]
143	2584	DM1_0 Configuration Register 3 Data of LUT2	REG_VAL_LUT2[0]
	2585		REG_VAL_LUT2[1]
	2586		REG_VAL_LUT2[2]
	2587		REG_VAL_LUT2[3]

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
143	2588	DM1_0 Configuration Register 3 Clock source selection	Clock source sel[3:0] 0000: 25M; 0001: 25M/4; 0010: 2.048M 0011: 2.048M/8; 0100: 2.048M/64; 0101: 2.048M/512; 0110: 2.048K; 0111: 2.048K/8; 1000: 2.048K/64; 1001: 2.048K/512; 1010: 2.048K/4096 1011: 2.048K/32768; 1100: 2.048K/262144; 1101: CNT_END; 1110: External; 1111: External
	2589		
	2590		
	2591		
144	2592	DM1_0 Configuration Register 3 Data of Delay	Data[7:0]
	2593		
	2594		
	2595		
	2596		
	2597		
	2598		
	2599		
145	2600	DM1_0 Configuration Register 3 DLY input initial selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	2601		
	2602	DM1_0 Configuration Register 3 DLY/CNT Function selection	0000: Both Edge Delay 0001: Falling Edge Delay 0010: Rising Edge Delay 0011: Both Edge One Shot 0100: Falling Edge One Shot 0101: Rising Edge One Shot 0110: Both Edge Freq Detect 0111: Falling Edge Freq Detect 1000: Rising Edge Freq Detect 1001: Both Edge Detect 1010: Falling Edge Detect 1011: Rising Edge Detect 1100: Both Edge Reset CNT 1101: Falling Edge Reset CNT 1110: Rising Edge Reset CNT 1111: High Level Reset CNT
	2603		
	2604		
	2605		
	2606	DM1_0 Configuration Register 3 MUX1 selection for LUT2	0: from LUT3 1: from matrix (DLY IN)
	2607	DM1_0 Configuration Register 3 MUX2 selection for DLY input	0: from matrix (DLY IN) 1: from LUT3

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
146	2608	DM1_0 Configuration Register 4 IN0 of LUT3	REG_MATRIX_LUT3_IN0_SEL[5:0]
	2609		
	2610		
	2611		
	2612		
	2613		
	2614	DM1_0 Configuration Register 4 IN1 of LUT3	REG_MATRIX_LUT3_IN1_SEL[5:0]
	2615		
147	2616		
	2617		
	2618		
	2619		
	2620	DM1_0 Configuration Register 4 IN2 of LUT3	REG_MATRIX_LUT3_IN2_SEL[5:0]
	2621		
	2622		
	2623		
148	2624		
	2625		
	2626	DM1_0 Configuration Register 4 DLY input from matrix	DM Delay input
	2627		
	2628		
	2629		
	2630		
	2631		
149	2632	DM1_0 Configuration Register 4 Data of LUT3	REG_VAL_LUT3[0]
	2633		REG_VAL_LUT3[1]
	2634		REG_VAL_LUT3[2]
	2635		REG_VAL_LUT3[3]
	2636		REG_VAL_LUT3[4]
	2637		REG_VAL_LUT3[5]
	2638		REG_VAL_LUT3[6]
	2639		REG_VAL_LUT3[7]
14A	2640	DM1_0 Configuration Register 4 Data of LUT2	REG_VAL_LUT2[0]
	2641		REG_VAL_LUT2[1]
	2642		REG_VAL_LUT2[2]
	2643		REG_VAL_LUT2[3]

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
14A	2644	DM1_0 Configuration Register 4 Clock source selection	Clock source sel[3:0] 0000: 25M; 0001: 25M/4; 0010: 2.048M 0011: 2.048M/8; 0100: 2.048M/64; 0101: 2.048M/512; 0110: 2.048K; 0111: 2.048K/8; 1000: 2.048K/64; 1001: 2.048K/512; 1010: 2.048K/4096 1011: 2.048K/32768; 1100: 2.048K/262144; 1101: CNT_END; 1110: External; 1111: External
	2645		
	2646		
	2647		
14B	2648	DM1_0 Configuration Register 4 Data of Delay	Data[7:0]
	2649		
	2650		
	2651		
	2652		
	2653		
	2654		
	2655		
14C	2656	DM1_0 Configuration Register 4 DLY input initial selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	2657		
	2658	DM1_0 Configuration Register 4 DLY/CNT Function selection	0000: Both Edge Delay 0001: Falling Edge Delay 0010: Rising Edge Delay 0011: Both Edge One Shot 0100: Falling Edge One Shot 0101: Rising Edge One Shot 0110: Both Edge Freq Detect 0111: Falling Edge Freq Detect 1000: Rising Edge Freq Detect 1001: Both Edge Detect 1010: Falling Edge Detect 1011: Rising Edge Detect 1100: Both Edge Reset CNT 1101: Falling Edge Reset CNT 1110: Rising Edge Reset CNT 1111: High Level Reset CNT
	2659		
	2660		
	2661		
	2662	DM1_0 Configuration Register 4 MUX1 selection for LUT2	0: from LUT3 1: from matrix (DLY IN)
	2663	DM1_0 Configuration Register 4 MUX2 selection for DLY input	0: from matrix (DLY IN) 1: from LUT3

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
14D	2664	DM1_0 Configuration Register 5 IN0 of LUT3	REG_MATRIX_LUT3_IN0_SEL[5:0]
	2665		
	2666		
	2667		
	2668		
	2669		
	2670	DM1_0 Configuration Register 5 IN1 of LUT3	REG_MATRIX_LUT3_IN1_SEL[5:0]
	2671		
14E	2672		
	2673		
	2674		
	2675		
	2676	DM1_0 Configuration Register 5 IN2 of LUT3	REG_MATRIX_LUT3_IN2_SEL[5:0]
	2677		
	2678		
	2679		
14F	2680		
	2681		
	2682	DM1_0 Configuration Register 5 DLY input from matrix	DM Delay input
	2683		
	2684		
	2685		
	2686		
	2687		
150	2688	DM1_0 Configuration Register 5 Data of LUT3	REG_VAL_LUT3[0]
	2689		REG_VAL_LUT3[1]
	2690		REG_VAL_LUT3[2]
	2691		REG_VAL_LUT3[3]
	2692		REG_VAL_LUT3[4]
	2693		REG_VAL_LUT3[5]
	2694		REG_VAL_LUT3[6]
	2695		REG_VAL_LUT3[7]
151	2696	DM1_0 Configuration Register 5 Data of LUT2	REG_VAL_LUT2[0]
	2697		REG_VAL_LUT2[1]
	2698		REG_VAL_LUT2[2]
	2699		REG_VAL_LUT2[3]

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
151	2700	DM1_0 Configuration Register 5 Clock source selection	Clock source sel[3:0] 0000: 25M; 0001: 25M/4; 0010: 2.048M 0011: 2.048M/8; 0100: 2.048M/64; 0101: 2.048M/512; 0110: 2.048K; 0111: 2.048K/8; 1000: 2.048K/64; 1001: 2.048K/512; 1010: 2.048K/4096 1011: 2.048K/32768; 1100: 2.048K/262144; 1101: CNT_END; 1110: External; 1111: External
	2701		
	2702		
	2703		
152	2704	DM1_0 Configuration Register 5 Data of Delay	Data[7:0]
	2705		
	2706		
	2707		
	2708		
	2709		
	2710		
	2711		
153	2712	DM1_0 Configuration Register 5 DLY input initial selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	2713		
	2714	DM1_0 Configuration Register 5 DLY/CNT Function selection	0000: Both Edge Delay 0001: Falling Edge Delay 0010: Rising Edge Delay 0011: Both Edge One Shot 0100: Falling Edge One Shot 0101: Rising Edge One Shot 0110: Both Edge Freq Detect 0111: Falling Edge Freq Detect 1000: Rising Edge Freq Detect 1001: Both Edge Detect 1010: Falling Edge Detect 1011: Rising Edge Detect 1100: Both Edge Reset CNT 1101: Falling Edge Reset CNT 1110: Rising Edge Reset CNT 1111: High Level Reset CNT
	2715		
	2716		
	2717		
	2718	DM1_0 Configuration Register 5 MUX1 selection for LUT2	0: from LUT3 1: from matrix (DLY IN)
	2719	DM1_0 Configuration Register 5 MUX2 selection for DLY input	0: from matrix (DLY IN) 1: from LUT3

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
154	2720	DM1_1 Configuration Register 0 IN0 of LUT3	REG_MATRIX_LUT3_IN0_SEL[5:0]
	2721		
	2722		
	2723		
	2724		
	2725		
	2726	DM1_1 Configuration Register 0 IN1 of LUT3	REG_MATRIX_LUT3_IN1_SEL[5:0]
	2727		
155	2728		
	2729		
	2730		
	2731		
	2732	DM1_1 Configuration Register 0 IN2 of LUT3	REG_MATRIX_LUT3_IN2_SEL[5:0]
	2733		
	2734		
	2735		
156	2736		
	2737		
	2738	DM1_1 Configuration Register 0 DLY input from matrix	DM Delay input
	2739		
	2740		
	2741		
	2742		
	2743		
157	2744	DM1_1 Configuration Register 0 Data of LUT3	REG_VAL_LUT3[0]
	2745		REG_VAL_LUT3[1]
	2746		REG_VAL_LUT3[2]
	2747		REG_VAL_LUT3[3]
	2748		REG_VAL_LUT3[4]
	2749		REG_VAL_LUT3[5]
	2750		REG_VAL_LUT3[6]
	2751		REG_VAL_LUT3[7]
158	2752	DM1_1 Configuration Register 0 Data of LUT2	REG_VAL_LUT2[0]
	2753		REG_VAL_LUT2[1]
	2754		REG_VAL_LUT2[2]
	2755		REG_VAL_LUT2[3]

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
158	2756	DM1_1 Configuration Register 0 Clock source selection	Clock source sel[3:0] 0000: 25M; 0001: 25M/4; 0010: 2.048M 0011: 2.048M/8; 0100: 2.048M/64; 0101: 2.048M/512; 0110: 2.048K; 0111: 2.048K/8; 1000: 2.048K/64; 1001: 2.048K/512; 1010: 2.048K/4096 1011: 2.048K/32768; 1100: 2.048K/262144; 1101: CNT_END; 1110: External; 1111: External
	2757		
	2758		
	2759		
159	2760	DM1_1 Configuration Register 0 Data of Delay	Data[7:0]
	2761		
	2762		
	2763		
	2764		
	2765		
	2766		
	2767		
15A	2768	DM1_1 Configuration Register 0 DLY input initial selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	2769		
	2770	DM1_1 Configuration Register 0 DLY/CNT Function selection	0000: Both Edge Delay 0001: Falling Edge Delay 0010: Rising Edge Delay 0011: Both Edge One Shot 0100: Falling Edge One Shot 0101: Rising Edge One Shot 0110: Both Edge Freq Detect 0111: Falling Edge Freq Detect 1000: Rising Edge Freq Detect 1001: Both Edge Detect 1010: Falling Edge Detect 1011: Rising Edge Detect 1100: Both Edge Reset CNT 1101: Falling Edge Reset CNT 1110: Rising Edge Reset CNT 1111: High Level Reset CNT
	2771		
	2772		
	2773		
	2774	DM1_1 Configuration Register 0 MUX1 selection for LUT2	0: from LUT3 1: from matrix (DLY IN)
	2775	DM1_1 Configuration Register 0 MUX2 selection for DLY input	0: from matrix (DLY IN) 1: from LUT3

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
15B	2776	DM1_1 Configuration Register 1 IN0 of LUT3	REG_MATRIX_LUT3_IN0_SEL[5:0]
	2777		
	2778		
	2779		
	2780		
	2781		
	2782	DM1_1 Configuration Register 1 IN1 of LUT3	REG_MATRIX_LUT3_IN1_SEL[5:0]
	2783		
15C	2784		
	2785		
	2786		
	2787		
	2788	DM1_1 Configuration Register 1 IN2 of LUT3	REG_MATRIX_LUT3_IN2_SEL[5:0]
	2789		
	2790		
	2791		
15D	2792		
	2793		
	2794	DM1_1 Configuration Register 1 DLY input from matrix	DM Delay input
	2795		
	2796		
	2797		
	2798		
	2799		
15E	2800	DM1_1 Configuration Register 1 Data of LUT3	REG_VAL_LUT3[0]
	2801		REG_VAL_LUT3[1]
	2802		REG_VAL_LUT3[2]
	2803		REG_VAL_LUT3[3]
	2804		REG_VAL_LUT3[4]
	2805		REG_VAL_LUT3[5]
	2806		REG_VAL_LUT3[6]
	2807		REG_VAL_LUT3[7]
15F	2808	DM1_1 Configuration Register 1 Data of LUT2	REG_VAL_LUT2[0]
	2809		REG_VAL_LUT2[1]
	2810		REG_VAL_LUT2[2]
	2811		REG_VAL_LUT2[3]

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
15F	2812	DM1_1 Configuration Register 1 Clock source selection	Clock source sel[3:0] 0000: 25M; 0001: 25M/4; 0010: 2.048M 0011: 2.048M/8; 0100: 2.048M/64; 0101: 2.048M/512; 0110: 2.048K; 0111: 2.048K/8; 1000: 2.048K/64; 1001: 2.048K/512; 1010: 2.048K/4096 1011: 2.048K/32768; 1100: 2.048K/262144; 1101: CNT_END; 1110: External; 1111: External
	2813		
	2814		
	2815		
160	2816	DM1_1 Configuration Register 1 Data of Delay	Data[7:0]
	2817		
	2818		
	2819		
	2820		
	2821		
	2822		
	2823		
161	2824	DM1_1 Configuration Register 1 DLY input initial selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	2825		
	2826	DM1_1 Configuration Register 1 DLY/CNT Function selection	0000: Both Edge Delay 0001: Falling Edge Delay 0010: Rising Edge Delay 0011: Both Edge One Shot 0100: Falling Edge One Shot 0101: Rising Edge One Shot 0110: Both Edge Freq Detect 0111: Falling Edge Freq Detect 1000: Rising Edge Freq Detect 1001: Both Edge Detect 1010: Falling Edge Detect 1011: Rising Edge Detect 1100: Both Edge Reset CNT 1101: Falling Edge Reset CNT 1110: Rising Edge Reset CNT 1111: High Level Reset CNT
	2827		
	2828		
	2829		
	2830	DM1_1 Configuration Register 1 MUX1 selection for LUT2	0: from LUT3 1: from matrix (DLY IN)
	2831	DM1_1 Configuration Register 1 MUX2 selection for DLY input	0: from matrix (DLY IN) 1: from LUT3

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
162	2832	DM1_1 Configuration Register 2 IN0 of LUT3	REG_MATRIX_LUT3_IN0_SEL[5:0]
	2833		
	2834		
	2835		
	2836		
	2837		
	2838	DM1_1 Configuration Register 2 IN1 of LUT3	REG_MATRIX_LUT3_IN1_SEL[5:0]
	2839		
163	2840		
	2841		
	2842		
	2843		
	2844	DM1_1 Configuration Register 2 IN2 of LUT3	REG_MATRIX_LUT3_IN2_SEL[5:0]
	2845		
	2846		
	2847		
164	2848		
	2849		
	2850	DM1_1 Configuration Register 2 DLY input from matrix	DM Delay input
	2851		
	2852		
	2853		
	2854		
	2855		
165	2856	DM1_1 Configuration Register 2 Data of LUT3	REG_VAL_LUT3[0]
	2857		REG_VAL_LUT3[1]
	2858		REG_VAL_LUT3[2]
	2859		REG_VAL_LUT3[3]
	2860		REG_VAL_LUT3[4]
	2861		REG_VAL_LUT3[5]
	2862		REG_VAL_LUT3[6]
	2863		REG_VAL_LUT3[7]
166	2864	DM1_1 Configuration Register 2 Data of LUT2	REG_VAL_LUT2[0]
	2865		REG_VAL_LUT2[1]
	2866		REG_VAL_LUT2[2]
	2867		REG_VAL_LUT2[3]

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
166	2868	DM1_1 Configuration Register 2 Clock source selection	Clock source sel[3:0] 0000: 25M; 0001: 25M/4; 0010: 2.048M 0011: 2.048M/8; 0100: 2.048M/64; 0101: 2.048M/512; 0110: 2.048K; 0111: 2.048K/8; 1000: 2.048K/64; 1001: 2.048K/512; 1010: 2.048K/4096 1011: 2.048K/32768; 1100: 2.048K/262144; 1101: CNT_END; 1110: External; 1111: External
	2869		
	2870		
	2871		
167	2872	DM1_1 Configuration Register 2 Data of Delay	Data[7:0]
	2873		
	2874		
	2875		
	2876		
	2877		
	2878		
	2879		
168	2880	DM1_1 Configuration Register 2 DLY input initial selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	2881		
	2882	DM1_1 Configuration Register 2 DLY/CNT Function selection	0000: Both Edge Delay 0001: Falling Edge Delay 0010: Rising Edge Delay 0011: Both Edge One Shot 0100: Falling Edge One Shot 0101: Rising Edge One Shot 0110: Both Edge Freq Detect 0111: Falling Edge Freq Detect 1000: Rising Edge Freq Detect 1001: Both Edge Detect 1010: Falling Edge Detect 1011: Rising Edge Detect 1100: Both Edge Reset CNT 1101: Falling Edge Reset CNT 1110: Rising Edge Reset CNT 1111: High Level Reset CNT
	2883		
	2884		
	2885		
	2886	DM1_1 Configuration Register 2 MUX1 selection for LUT2	0: from LUT3 1: from matrix (DLY IN)
	2887	DM1_1 Configuration Register 2 MUX2 selection for DLY input	0: from matrix (DLY IN) 1: from LUT3

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
169	2888	DM1_1 Configuration Register 3 IN0 of LUT3	REG_MATRIX_LUT3_IN0_SEL[5:0]
	2889		
	2890		
	2891		
	2892		
	2893		
	2894	DM1_1 Configuration Register 3 IN1 of LUT3	REG_MATRIX_LUT3_IN1_SEL[5:0]
	2895		
16A	2896		
	2897		
	2898		
	2899		
	2900	DM1_1 Configuration Register 3 IN2 of LUT3	REG_MATRIX_LUT3_IN2_SEL[5:0]
	2901		
	2902		
	2903		
16B	2904		
	2905		
	2906	DM1_1 Configuration Register 3 DLY input from matrix	DM Delay input
	2907		
	2908		
	2909		
	2910		
	2911		
16C	2912	DM1_1 Configuration Register 3 Data of LUT3	REG_VAL_LUT3[0]
	2913		REG_VAL_LUT3[1]
	2914		REG_VAL_LUT3[2]
	2915		REG_VAL_LUT3[3]
	2916		REG_VAL_LUT3[4]
	2917		REG_VAL_LUT3[5]
	2918		REG_VAL_LUT3[6]
	2919		REG_VAL_LUT3[7]
16D	2920	DM1_1 Configuration Register 3 Data of LUT2	REG_VAL_LUT2[0]
	2921		REG_VAL_LUT2[1]
	2922		REG_VAL_LUT2[2]
	2923		REG_VAL_LUT2[3]

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
16D	2924	DM1_1 Configuration Register 3 Clock source selection	Clock source sel[3:0] 0000: 25M; 0001: 25M/4; 0010: 2.048M 0011: 2.048M/8; 0100: 2.048M/64; 0101: 2.048M/512; 0110: 2.048K; 0111: 2.048K/8; 1000: 2.048K/64; 1001: 2.048K/512; 1010: 2.048K/4096 1011: 2.048K/32768; 1100: 2.048K/262144; 1101: CNT_END; 1110: External; 1111: External
	2925		
	2926		
	2927		
16E	2928	DM1_1 Configuration Register 3 Data of Delay	Data[7:0]
	2929		
	2930		
	2931		
	2932		
	2933		
	2934		
	2935		
16F	2936	DM1_1 Configuration Register 3 DLY input initial selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	2937		
	2938	DM1_1 Configuration Register 3 DLY/CNT Function selection	0000: Both Edge Delay 0001: Falling Edge Delay 0010: Rising Edge Delay 0011: Both Edge One Shot 0100: Falling Edge One Shot 0101: Rising Edge One Shot 0110: Both Edge Freq Detect 0111: Falling Edge Freq Detect 1000: Rising Edge Freq Detect 1001: Both Edge Detect 1010: Falling Edge Detect 1011: Rising Edge Detect 1100: Both Edge Reset CNT 1101: Falling Edge Reset CNT 1110: Rising Edge Reset CNT 1111: High Level Reset CNT
	2939		
	2940		
	2941		
	2942	DM1_1 Configuration Register 3 MUX1 selection for LUT2	0: from LUT3 1: from matrix (DLY IN)
	2943	DM1_1 Configuration Register 3 MUX2 selection for DLY input	0: from matrix (DLY IN) 1: from LUT3

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
170	2944	DM1_1 Configuration Register 4 IN0 of LUT3	REG_MATRIX_LUT3_IN0_SEL[5:0]
	2945		
	2946		
	2947		
	2948		
	2949		
	2950	DM1_1 Configuration Register 4 IN1 of LUT3	REG_MATRIX_LUT3_IN1_SEL[5:0]
	2951		
171	2952		
	2953		
	2954		
	2955		
	2956	DM1_1 Configuration Register 4 IN2 of LUT3	REG_MATRIX_LUT3_IN2_SEL[5:0]
	2957		
	2958		
	2959		
172	2960		
	2961		
	2962	DM1_1 Configuration Register 4 DLY input from matrix	DM Delay input
	2963		
	2964		
	2965		
	2966		
	2967		
173	2968	DM1_1 Configuration Register 4 Data of LUT3	REG_VAL_LUT3[0]
	2969		REG_VAL_LUT3[1]
	2970		REG_VAL_LUT3[2]
	2971		REG_VAL_LUT3[3]
	2972		REG_VAL_LUT3[4]
	2973		REG_VAL_LUT3[5]
	2974		REG_VAL_LUT3[6]
	2975		REG_VAL_LUT3[7]
174	2976	DM1_1 Configuration Register 4 Data of LUT2	REG_VAL_LUT2[0]
	2977		REG_VAL_LUT2[1]
	2978		REG_VAL_LUT2[2]
	2979		REG_VAL_LUT2[3]

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
174	2980	DM1_1 Configuration Register 4 Clock source selection	Clock source sel[3:0] 0000: 25M; 0001: 25M/4; 0010: 2.048M 0011: 2.048M/8; 0100: 2.048M/64; 0101: 2.048M/512; 0110: 2.048K; 0111: 2.048K/8; 1000: 2.048K/64; 1001: 2.048K/512; 1010: 2.048K/4096 1011: 2.048K/32768; 1100: 2.048K/262144; 1101: CNT_END; 1110: External; 1111: External
	2981		
	2982		
	2983		
175	2984	DM1_1 Configuration Register 4 Data of Delay	Data[7:0]
	2985		
	2986		
	2987		
	2988		
	2989		
	2990		
	2991		
176	2992	DM1_1 Configuration Register 4 DLY input initial selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	2993		
	2994	DM1_1 Configuration Register 4 DLY/CNT Function selection	0000: Both Edge Delay 0001: Falling Edge Delay 0010: Rising Edge Delay 0011: Both Edge One Shot 0100: Falling Edge One Shot 0101: Rising Edge One Shot 0110: Both Edge Freq Detect 0111: Falling Edge Freq Detect 1000: Rising Edge Freq Detect 1001: Both Edge Detect 1010: Falling Edge Detect 1011: Rising Edge Detect 1100: Both Edge Reset CNT 1101: Falling Edge Reset CNT 1110: Rising Edge Reset CNT 1111: High Level Reset CNT
	2995		
	2996		
	2997		
	2998	DM1_1 Configuration Register 4 MUX1 selection for LUT2	0: from LUT3 1: from matrix (DLY IN)
	2999	DM1_1 Configuration Register 4 MUX2 selection for DLY input	0: from matrix (DLY IN) 1: from LUT3

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
177	3000	DM1_1 Configuration Register 5 IN0 of LUT3	REG_MATRIX_LUT3_IN0_SEL[5:0]
	3001		
	3002		
	3003		
	3004		
	3005		
	3006	DM1_1 Configuration Register 5 IN1 of LUT3	REG_MATRIX_LUT3_IN1_SEL[5:0]
	3007		
178	3008		
	3009		
	3010		
	3011		
	3012	DM1_1 Configuration Register 5 IN2 of LUT3	REG_MATRIX_LUT3_IN2_SEL[5:0]
	3013		
	3014		
	3015		
179	3016		
	3017		
	3018	DM1_1 Configuration Register 5 DLY input from matrix	DM Delay input
	3019		
	3020		
	3021		
	3022		
	3023		
17A	3024	DM1_1 Configuration Register 5 Data of LUT3	REG_VAL_LUT3[0]
	3025		REG_VAL_LUT3[1]
	3026		REG_VAL_LUT3[2]
	3027		REG_VAL_LUT3[3]
	3028		REG_VAL_LUT3[4]
	3029		REG_VAL_LUT3[5]
	3030		REG_VAL_LUT3[6]
	3031		REG_VAL_LUT3[7]
17B	3032	DM1_1 Configuration Register 5 Data of LUT2	REG_VAL_LUT2[0]
	3033		REG_VAL_LUT2[1]
	3034		REG_VAL_LUT2[2]
	3035		REG_VAL_LUT2[3]

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
17B	3036	DM1_1 Configuration Register 5 Clock source selection	Clock source sel[3:0] 0000: 25M; 0001: 25M/4; 0010: 2.048M 0011: 2.048M/8; 0100: 2.048M/64; 0101: 2.048M/512; 0110: 2.048K; 0111: 2.048K/8; 1000: 2.048K/64; 1001: 2.048K/512; 1010: 2.048K/4096 1011: 2.048K/32768; 1100: 2.048K/262144; 1101: CNT_END; 1110: External; 1111: External
	3037		
	3038		
	3039		
17C	3040	DM1_1 Configuration Register 5 Data of Delay	Data[7:0]
	3041		
	3042		
	3043		
	3044		
	3045		
	3046		
	3047		
17D	3048	DM1_1 Configuration Register 5 DLY input initial selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	3049		
	3050	DM1_1 Configuration Register 5 DLY/CNT Function selection	0000: Both Edge Delay 0001: Falling Edge Delay 0010: Rising Edge Delay 0011: Both Edge One Shot 0100: Falling Edge One Shot 0101: Rising Edge One Shot 0110: Both Edge Freq Detect 0111: Falling Edge Freq Detect 1000: Rising Edge Freq Detect 1001: Both Edge Detect 1010: Falling Edge Detect 1011: Rising Edge Detect 1100: Both Edge Reset CNT 1101: Falling Edge Reset CNT 1110: Rising Edge Reset CNT 1111: High Level Reset CNT
	3051		
	3052		
	3053		
	3054	DM1_1 Configuration Register 5 MUX1 selection for LUT2	0: from LUT3 1: from matrix (DLY IN)
	3055	DM1_1 Configuration Register 5 MUX2 selection for DLY input	0: from matrix (DLY IN) 1: from LUT3

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
17E	3056	DM0_0 Selection Register State 0, bit [0]	selection bit[2:0]: 000: Not Used 001: DM0_0 Configuration Register 0 010: DM0_0 Conflagration Register 1 011: DM0_0 Configuration Register 2 100: DM0_0 Configuration Register 3 101: DM0_0 Configuration Register 4 110: DM0_0 Configuration Register 5 111: Not Used
	3057	DM0_0 Selection Register State 1, bit [0]	
	3058	DM0_0 Selection Register State 2, bit [0]	
	3059	DM0_0 Selection Register State 3, bit [0]	
	3060	DM0_0 Selection Register State 4, bit [0]	
	3061	DM0_0 Selection Register State 5, bit [0]	
	3062	DM0_0 Selection Register State 6, bit [0]	
	3063	DM0_0 Selection Register State 7, bit [0]	
17F	3064	DM0_0 Selection Register State 8, bit [0]	
	3065	DM0_0 Selection Register State 9, bit [0]	
	3066	DM0_0 Selection Register State 10, bit [0]	
	3067	DM0_0 Selection Register State 11, bit [0]	
	3068	DM0_0 Selection Register State 0, bit [1]	selection bit[2:0]: 000: Not Used 001: DM0_0 Configuration Register 0 010: DM0_0 Conflagration Register 1 011: DM0_0 Configuration Register 2 100: DM0_0 Configuration Register 3 101: DM0_0 Configuration Register 4 110: DM0_0 Configuration Register 5 111: Not Used
	3069	DM0_0 Selection Register State 1, bit [1]	
	3070	DM0_0 Selection Register State 2, bit [1]	
	3071	DM0_0 Selection Register State 3, bit [1]	
180	3072	DM0_0 Selection Register State 4, bit [1]	
	3073	DM0_0 Selection Register State 5, bit [1]	
	3074	DM0_0 Selection Register State 6, bit [1]	
	3075	DM0_0 Selection Register State 7, bit [1]	
	3076	DM0_0 Selection Register State 8, bit [1]	
	3077	DM0_0 Selection Register State 9, bit [1]	
	3078	DM0_0 Selection Register State 10, bit [1]	
	3079	DM0_0 Selection Register State 11, bit [1]	
181	3080	DM0_0 Selection Register State 0, bit [2]	selection bit[2:0]: 000: Not Used 001: DM0_0 Configuration Register 0 010: DM0_0 Conflagration Register 1 011: DM0_0 Configuration Register 2 100: DM0_0 Configuration Register 3 101: DM0_0 Configuration Register 4 110: DM0_0 Configuration Register 5 111: Not Used
	3081	DM0_0 Selection Register State 1, bit [2]	
	3082	DM0_0 Selection Register State 2, bit [2]	
	3083	DM0_0 Selection Register State 3, bit [2]	
	3084	DM0_0 Selection Register State 4, bit [2]	
	3085	DM0_0 Selection Register State 5, bit [2]	
	3086	DM0_0 Selection Register State 6, bit [2]	
	3087	DM0_0 Selection Register State 7, bit [2]	
182	3088	DM0_0 Selection Register State 8, bit [2]	
	3089	DM0_0 Selection Register State 9, bit [2]	
	3090	DM0_0 Selection Register State 10, bit [2]	
	3091	DM0_0 Selection Register State 11, bit [2]	

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
182	3092	DM0_0 Output Configuration Selection Register State 0, bit [0]	control bit[1:0]: 00:DM out0/1/2 keep 01:DM out bypass to out0, out1/2 keep 10: DM out bypass to out1, out0/2 keep 11: DM out bypass to out2, out0/1 keep
	3093	DM0_0 Output Configuration Selection Register State 1, bit [0]	
	3094	DM0_0 Output Configuration Selection Register State 2, bit [0]	
	3095	DM0_0 Output Configuration Selection Register State 3, bit [0]	
183	3096	DM0_0 Output Configuration Selection Register State 4, bit [0]	
	3097	DM0_0 Output Configuration Selection Register State 5, bit [0]	
	3098	DM0_0 Output Configuration Selection Register State 6, bit [0]	
	3099	DM0_0 Output Configuration Selection Register State 7, bit [0]	
	3100	DM0_0 Output Configuration Selection Register State 8, bit [0]	
	3101	DM0_0 Output Configuration Selection Register State 9, bit [0]	
	3102	DM0_0 Output Configuration Selection Register State 10, bit [0]	
	3103	DM0_0 Output Configuration Selection Register State 11, bit [0]	
184	3104	DM0_0 Output Configuration Selection Register State 0, bit [1]	control bit[1:0]: 00:DM out0/1/2 keep 01:DM out bypass to out0, out1/2 keep 10: DM out bypass to out1, out0/2 keep 11: DM out bypass to out2, out0/1 keep
	3105	DM0_0 Output Configuration Selection Register State 1, bit [1]	
	3106	DM0_0 Output Configuration Selection Register State 2, bit [1]	
	3107	DM0_0 Output Configuration Selection Register State 3, bit [1]	
	3108	DM0_0 Output Configuration Selection Register State 4, bit [1]	
	3109	DM0_0 Output Configuration Selection Register State 5, bit [1]	
	3110	DM0_0 Output Configuration Selection Register State 6, bit [1]	
	3111	DM0_0 Output Configuration Selection Register State 7, bit [1]	
185	3112	DM0_0 Output Configuration Selection Register State 8, bit [1]	
	3113	DM0_0 Output Configuration Selection Register State 9, bit [1]	
	3114	DM0_0 Output Configuration Selection Register State 10, bit [1]	
	3115	DM0_0 Output Configuration Selection Register State 11, bit [1]	

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
185	3116	DM1_0 Selection Register State 0, bit [0]	selection bit[2:0]: 000: Not Used 001: DM1_0 Configuration Register 0 010: DM1_0 Conflagration Register 1 011: DM1_0 Configuration Register 2 100: DM1_0 Configuration Register 3 101: DM1_0 Configuration Register 4 110: DM1_0 Configuration Register 5 111: Not Used
	3117	DM1_0 Selection Register State 1, bit [0]	
	3118	DM1_0 Selection Register State 2, bit [0]	
	3119	DM1_0 Selection Register State 3, bit [0]	
186	3120	DM1_0 Selection Register State 4, bit [0]	
	3121	DM1_0 Selection Register State 5, bit [0]	
	3122	DM1_0 Selection Register State 6, bit [0]	
	3123	DM1_0 Selection Register State 7, bit [0]	
	3124	DM1_0 Selection Register State 8, bit [0]	
	3125	DM1_0 Selection Register State 9, bit [0]	
	3126	DM1_0 Selection Register State 10, bit [0]	
	3127	DM1_0 Selection Register State 11, bit [0]	
187	3128	DM1_0 Selection Register State 0, bit [1]	selection bit[2:0]: 000: Not Used 001: DM1_0 Configuration Register 0 010: DM1_0 Conflagration Register 1 011: DM1_0 Configuration Register 2 100: DM1_0 Configuration Register 3 101: DM1_0 Configuration Register 4 110: DM1_0 Configuration Register 5 111: Not Used
	3129	DM1_0 Selection Register State 1, bit [1]	
	3130	DM1_0 Selection Register State 2, bit [1]	
	3131	DM1_0 Selection Register State 3, bit [1]	
	3132	DM1_0 Selection Register State 4, bit [1]	
	3133	DM1_0 Selection Register State 5, bit [1]	
	3134	DM1_0 Selection Register State 6, bit [1]	
	3135	DM1_0 Selection Register State 7, bit [1]	
188	3136	DM1_0 Selection Register State 8, bit [1]	
	3137	DM1_0 Selection Register State 9, bit [1]	
	3138	DM1_0 Selection Register State 10, bit [1]	
	3139	DM1_0 Selection Register State 11, bit [1]	
	3140	DM1_0 Selection Register State 0, bit [2]	selection bit[2:0]: 000: Not Used 001: DM1_0 Configuration Register 0 010: DM1_0 Conflagration Register 1 011: DM1_0 Configuration Register 2 100: DM1_0 Configuration Register 3 101: DM1_0 Configuration Register 4 110: DM1_0 Configuration Register 5 111: Not Used
	3141	DM1_0 Selection Register State 1, bit [2]	
	3142	DM1_0 Selection Register State 2, bit [2]	
	3143	DM1_0 Selection Register State 3, bit [2]	
189	3144	DM1_0 Selection Register State 4, bit [2]	
	3145	DM1_0 Selection Register State 5, bit [2]	
	3146	DM1_0 Selection Register State 6, bit [2]	
	3147	DM1_0 Selection Register State 7, bit [2]	
	3148	DM1_0 Selection Register State 8, bit [2]	
	3149	DM1_0 Selection Register State 9, bit [2]	
	3150	DM1_0 Selection Register State 10, bit [2]	
	3151	DM1_0 Selection Register State 11, bit [2]	

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
18A	3152	DM0_1 Selection Register State 0, bit [0]	selection bit[2:0]: 000: Not Used 001: DM0_1 Configuration Register 0 010: DM0_1 Conflagration Register 1 011: DM0_1 Configuration Register 2 100: DM0_1 Configuration Register 3 101: DM0_1 Configuration Register 4 110: DM0_1 Configuration Register 5 111: Not Used
	3153	DM0_1 Selection Register State 1, bit [0]	
	3154	DM0_1 Selection Register State 2, bit [0]	
	3155	DM0_1 Selection Register State 3, bit [0]	
	3156	DM0_1 Selection Register State 4, bit [0]	
	3157	DM0_1 Selection Register State 5, bit [0]	
	3158	DM0_1 Selection Register State 6, bit [0]	
	3159	DM0_1 Selection Register State 7, bit [0]	
18B	3160	DM0_1 Selection Register State 8, bit [0]	
	3161	DM0_1 Selection Register State 9, bit [0]	
	3162	DM0_1 Selection Register State 10, bit [0]	
	3163	DM0_1 Selection Register State 11, bit [0]	
	3164	DM0_1 Selection Register State 0, bit [1]	selection bit[2:0]: 000: Not Used 001: DM0_1 Configuration Register 0 010: DM0_1 Conflagration Register 1 011: DM0_1 Configuration Register 2 100: DM0_1 Configuration Register 3 101: DM0_1 Configuration Register 4 110: DM0_1 Configuration Register 5 111: Not Used
	3165	DM0_1 Selection Register State 1, bit [1]	
	3166	DM0_1 Selection Register State 2, bit [1]	
	3167	DM0_1 Selection Register State 3, bit [1]	
18C	3168	DM0_1 Selection Register State 4, bit [1]	
	3169	DM0_1 Selection Register State 5, bit [1]	
	3170	DM0_1 Selection Register State 6, bit [1]	
	3171	DM0_1 Selection Register State 7, bit [1]	
	3172	DM0_1 Selection Register State 8, bit [1]	
	3173	DM0_1 Selection Register State 9, bit [1]	
	3174	DM0_1 Selection Register State 10, bit [1]	
	3175	DM0_1 Selection Register State 11, bit [1]	
18D	3176	DM0_1 Selection Register State 0, bit [2]	selection bit[2:0]: 000: Not Used 001: DM0_1 Configuration Register 0 010: DM0_1 Conflagration Register 1 011: DM0_1 Configuration Register 2 100: DM0_1 Configuration Register 3 101: DM0_1 Configuration Register 4 110: DM0_1 Configuration Register 5 111: Not Used
	3177	DM0_1 Selection Register State 1, bit [2]	
	3178	DM0_1 Selection Register State 2, bit [2]	
	3179	DM0_1 Selection Register State 3, bit [2]	
	3180	DM0_1 Selection Register State 4, bit [2]	
	3181	DM0_1 Selection Register State 5, bit [2]	
	3182	DM0_1 Selection Register State 6, bit [2]	
	3183	DM0_1 Selection Register State 7, bit [2]	
18E	3184	DM0_1 Selection Register State 8, bit [2]	
	3185	DM0_1 Selection Register State 9, bit [2]	
	3186	DM0_1 Selection Register State 10, bit [2]	
	3187	DM0_1 Selection Register State 11, bit [2]	

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
18E	3188	DM0_1 Output Configuration Selection Register State 0, bit [0]	control bit[1:0]: 00:DM out0/1/2 keep 01:DM out bypass to out0, out1/2 keep 10: DM out bypass to out1, out0/2 keep 11: DM out bypass to out2, out0/1 keep
	3189	DM0_1 Output Configuration Selection Register State 1, bit [0]	
	3190	DM0_1 Output Configuration Selection Register State 2, bit [0]	
	3191	DM0_1 Output Configuration Selection Register State 3, bit [0]	
18F	3192	DM0_1 Output Configuration Selection Register State 4, bit [0]	
	3193	DM0_1 Output Configuration Selection Register State 5, bit [0]	
	3194	DM0_1 Output Configuration Selection Register State 6, bit [0]	
	3195	DM0_1 Output Configuration Selection Register State 7, bit [0]	
	3196	DM0_1 Output Configuration Selection Register State 8, bit [0]	
	3197	DM0_1 Output Configuration Selection Register State 9, bit [0]	
	3198	DM0_1 Output Configuration Selection Register State 10, bit [0]	
	3199	DM0_1 Output Configuration Selection Register State 11, bit [0]	

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
190	3200	DM0_1 Output Configuration Selection Register State 0, bit [1]	control bit[1:0]: 00:DM out0/1/2 keep 01:DM out bypass to out0, out1/2 keep 10: DM out bypass to out1, out0/2 keep 11: DM out bypass to out2, out0/1 keep
	3201	DM0_1 Output Configuration Selection Register State 1, bit [1]	
	3202	DM0_1 Output Configuration Selection Register State 2, bit [1]	
	3203	DM0_1 Output Configuration Selection Register State 3, bit [1]	
	3204	DM0_1 Output Configuration Selection Register State 4, bit [1]	
	3205	DM0_1 Output Configuration Selection Register State 5, bit [1]	
	3206	DM0_1 Output Configuration Selection Register State 6, bit [1]	
	3207	DM0_1 Output Configuration Selection Register State 7, bit [1]	
191	3208	DM0_1 Output Configuration Selection Register State 8, bit [1]	
	3209	DM0_1 Output Configuration Selection Register State 9, bit [1]	
	3210	DM0_1 Output Configuration Selection Register State 10, bit [1]	
	3211	DM0_1 Output Configuration Selection Register State 11, bit [1]	
	3212	DM1_1 Selection Register State 0, bit [0]	selection bit[2:0]: 000: Not Used 001: DM1_1 Configuration Register 0 010: DM1_1 Conflagration Register 1 011: DM1_1 Configuration Register 2 100: DM1_1 Configuration Register 3 101: DM1_1 Configuration Register 4 110: DM1_1 Configuration Register 5 111: Not Used
	3213	DM1_1 Selection Register State 1, bit [0]	
	3214	DM1_1 Selection Register State 2, bit [0]	
	3215	DM1_1 Selection Register State 3, bit [0]	
192	3216	DM1_1 Selection Register State 4, bit [0]	
	3217	DM1_1 Selection Register State 5, bit [0]	
	3218	DM1_1 Selection Register State 6, bit [0]	
	3219	DM1_1 Selection Register State 7, bit [0]	
	3220	DM1_1 Selection Register State 8, bit [0]	
	3221	DM1_1 Selection Register State 9, bit [0]	
	3222	DM1_1 Selection Register State 10, bit [0]	
	3223	DM1_1 Selection Register State 11, bit [0]	

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
193	3224	DM1_1 Selection Register State 0, bit [1]	selection bit[2:0]: 000: Not Used 001: DM1_1 Configuration Register 0 010: DM1_1 Conflagration Register 1 011: DM1_1 Configuration Register 2 100: DM1_1 Configuration Register 3 101: DM1_1 Configuration Register 4 110: DM1_1 Configuration Register 5 111: Not Used
	3225	DM1_1 Selection Register State 1, bit [1]	
	3226	DM1_1 Selection Register State 2, bit [1]	
	3227	DM1_1 Selection Register State 3, bit [1]	
	3228	DM1_1 Selection Register State 4, bit [1]	
	3229	DM1_1 Selection Register State 5, bit [1]	
	3230	DM1_1 Selection Register State 6, bit [1]	
	3231	DM1_1 Selection Register State 7, bit [1]	
194	3232	DM1_1 Selection Register State 8, bit [1]	
	3233	DM1_1 Selection Register State 9, bit [1]	
	3234	DM1_1 Selection Register State 10, bit [1]	
	3235	DM1_1 Selection Register State 11, bit [1]	
	3236	DM1_1 Selection Register State 0, bit [2]	selection bit[2:0]: 000: Not Used 001: DM1_1 Configuration Register 0 010: DM1_1 Conflagration Register 1 011: DM1_1 Configuration Register 2 100: DM1_1 Configuration Register 3 101: DM1_1 Configuration Register 4 110: DM1_1 Configuration Register 5 111: Not Used
	3237	DM1_1 Selection Register State 1, bit [2]	
	3238	DM1_1 Selection Register State 2, bit [2]	
	3239	DM1_1 Selection Register State 3, bit [2]	
195	3240	DM1_1 Selection Register State 4, bit [2]	
	3241	DM1_1 Selection Register State 5, bit [2]	
	3242	DM1_1 Selection Register State 6, bit [2]	
	3243	DM1_1 Selection Register State 7, bit [2]	
	3244	DM1_1 Selection Register State 8, bit [2]	
	3245	DM1_1 Selection Register State 9, bit [2]	
	3246	DM1_1 Selection Register State 10, bit [2]	
	3247	DM1_1 Selection Register State 11, bit [2]	
196	3248	DM0_0 function 4 outputs initial value	0: initial 0 1: initial 1
	3249	DM0_1 function 4 outputs initial value	0: initial 0 1: initial 1
	3250	Reserved	
	3251	Reserved	
	3252	Reserved	
	3253	Reserved	
	3254	Reserved	
	3255	Reserved	
197	3256	Reserved	
	3257	Reserved	
	3258	Reserved	
	3259	Reserved	
	3260	VrefO0 register PD control	Vrefo0 register power down signal 0: power-down, 1: power-on
	3261	VrefO0 PD control select	Vrefo0 pd selection 0: come from reg[3260], 1: come from matrix out78

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
197	3262	VrefO1 register PD control	Vrefo1 register power down signal 0: power-down, 1: power-on
	3263	VrefO1 PD control select	Vrefo1 pd selection 0: come from reg[3260], 1: come from matrix out78
198	3264	F1 stack memory, lower byte	Bit0 (top memory)
	3265		Bit1
	3266		Bit2
	3267		Bit3
	3268		Bit4
	3269		Bit5
	3270		Bit6
	3271		Bit7
199	3272	F1 stack memory, higher byte	Bit8
	3273		Bit9
	3274		Bit10
	3275		Bit11
	3276		Bit12
	3277		Bit13
	3278		Bit14
	3279		Bit15
19A	3280	aio0-3 input selection load 1	00: aio0 01: aio1 10: aio2 11: aio3
	3281		
	3282	ACMP4_F Vref selection load 1	"F1 input selection load 1" bit=0: Matrix input select: 000000: Matrix in0; ~ 111111: Matrix in63 "F1 input selection load 1" bit=1: ACMP Vref select: 000000: 32mV ~ 111110: 2.016V/ step=32mV; 111111: External Vref
	3283		
	3284		
	3285		
	3286		
	3287		
19B	3288	aio0-3 input selection load 2	00: aio0 01: aio1 10: aio2 11: aio3
	3289		
	3290	ACMP4_F Vref selection load 2	"F1 input selection load 1" bit=0: Matrix input select: 000000: Matrix in0; ~ 111111: Matrix in63 "F1 input selection load 1" bit=1: ACMP Vref select: 000000: 32mV ~ 111110: 2.016V/ step=32mV; 111111: External Vref
	3291		
	3292		
	3293		
	3294		
	3295		
19C	3296	aio4-7 input selection load 3	00: aio4 01: aio5 10: aio6 11: aio7
	3297		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
19C	3298	ACMP4_F Vref selection load 3	"F1 input selection load 1" bit=0: Matrix input select: 000000: Matrix in0; ~ 111111: Matrix in63 "F1 input selection load 1" bit=1: ACMP Vref select: 000000: 32mV ~ 111110: 2.016V/ step=32mV; 111111: External Vref
	3299		
	3300		
	3301		
	3302		
	3303		
19D	3304	aio4-7 input selection load 4	00: aio4 01: aio5 10: aio6 11: aio7
	3305		
	3306	ACMP4_F Vref selection load 4	"F1 input selection load 1" bit=0: Matrix input select: 000000: Matrix in0; ~ 111111: Matrix in63 "F1 input selection load 1" bit=1: ACMP Vref select: 000000: 32mV ~ 111110: 2.016V/ step=32mV; 111111: External Vref
	3307		
	3308		
	3309		
	3310		
	3311		
19E	3312	F1 input selection load 1	0: from matrix 1: from ACMP4_F
	3313	F1 input selection load 2	0: from matrix 1: from ACMP4_F
	3314	F1 input selection load 3	0: from matrix 1: from ACMP4_F
	3315	F1 input selection load 4	0: from matrix 1: from ACMP4_F
	3316	Reserved	
	3317	delay clock source selection	000: RING; 001: RING/4 010: RC 011: RC/8 100: RC/64 101: LF 110: LF/8 111: LF/64
	3318		
	3319		
19F	3320	F1 delay data	Data[7:0]
	3321		
	3322		
	3323		
	3324		
	3325		
	3326		
	3327		
1A0	3328	F1 CMD1 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3329		
	3330		
	3331		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
1A0	3332	F1 CMD2 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3333		
	3334		
	3335		
1A1	3336	F1 CMD3 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3337		
	3338		
	3339		
	3340	F1 CMD4 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3341		
	3342		
	3343		
1A2	3344	F1 CMD5 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3345		
	3346		
	3347		
	3348	F1 CMD6 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3349		
	3350		
	3351		
1A3	3352	F1 CMD7 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3353		
	3354		
	3355		
	3356	F1 CMD8 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3357		
	3358		
	3359		
1A4	3360	F1 CMD9 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3361		
	3362		
	3363		
	3364	F1 CMD10 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3365		
	3366		
	3367		
1A5	3368	F1 CMD11 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3369		
	3370		
	3371		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
1A5	3372	F1 CMD12 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3373		
	3374		
	3375		
1A6	3376	delay loop to location selection	0000:CMD1;0001:CMD2;0010:CMD3;0011:CMD4;0100:CMD5;0101:CMD6:or;0110:CMD7;0111:CMD8;1000:CMD9;1001:CMD10;1010:CMD11;1011:CMD12
	3377		
	3378		
	3379		
	3380	output mux1 initial state setting	00: keep 01: 0 10: 1 11: none
	3381		
	3382	output mux2 initial state setting	00: keep 01: 0 10: 1 11: none
	3383		
1A7	3384	output mux3 initial state setting	00: keep 01: 0 10: 1 11: none
	3385		
	3386	interrupt reset stack memory enable	0: no reset stack memory 1: reset stack memory
	3387	Reserved	
	3388	Reserved	
	3389	Reserved	
	3390	Reserved	
	3391	Reserved	
1A8	3392	aio0-3 input selection load 1	00: aio0 01: aio1 10: aio2 11: aio3
	3393		
	3394	ACMP4_F Vref selection load 1	"F1 input selection load 1" bit=0: Matrix input select: 000000: Matrix in0; ~ 111111: Matrix in63 "F1 input selection load 1" bit=1: ACMP Vref select: 000000: 32mV ~ 111110: 2.016V/ step=32mV; 111111: External Vref
	3395		
	3396		
	3397		
	3398		
	3399		
1A9	3400	aio0-3 input selection load 2	00: aio0 01: aio1 10: aio2 11: aio3
	3401		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
1A9	3402	ACMP4_F Vref selection load 2	"F1 input selection load 1" bit=0: Matrix input select: 000000: Matrix in0; ~ 111111: Matrix in63 "F1 input selection load 1" bit=1: ACMP Vref select: 000000: 32mV ~ 111110: 2.016V/ step=32mV; 111111: External Vref
	3403		
	3404		
	3405		
	3406		
	3407		
1AA	3408	aio4-7 input selection load 3	00: aio4 01: aio5 10: aio6 11: aio7
	3409		
	3410	ACMP4_F Vref selection load 3	"F1 input selection load 1" bit=0: Matrix input select: 000000: Matrix in0; ~ 111111: Matrix in63 "F1 input selection load 1" bit=1: ACMP Vref select: 000000: 32mV ~ 111110: 2.016V/ step=32mV; 111111: External Vref
	3411		
	3412		
	3413		
	3414		
	3415		
1AB	3416	aio4-7 input selection load 4	00: aio4 01: aio5 10: aio6 11: aio7
	3417		
	3418	ACMP4_F Vref selection load 4	"F1 input selection load 1" bit=0: Matrix input select: 000000: Matrix in0; ~ 111111: Matrix in63 "F1 input selection load 1" bit=1: ACMP Vref select: 000000: 32mV ~ 111110: 2.016V/ step=32mV; 111111: External Vref
	3419		
	3420		
	3421		
	3422		
	3423		
1AC	3424	F1 input selection load 1	0: from matrix 1: from ACMP4_F
	3425	F1 input selection load 2	0: from matrix 1: from ACMP4_F
	3426	F1 input selection load 3	0: from matrix 1: from ACMP4_F
	3427	F1 input selection load 4	0: from matrix 1: from ACMP4_F
	3428	Reserved	
	3429	delay clock source selection	000: RING; 001: RING/4 010: RC 011: RC/8 100: RC/64 101: LF 110: LF/8 111: LF/64
	3430		
	3431		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
1AD	3432	F1 delay data	Data[7:0]
	3433		
	3434		
	3435		
	3436		
	3437		
	3438		
	3439		
1AE	3440	F1 CMD1 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3441		
	3442		
	3443		
	3444	F1 CMD2 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3445		
	3446		
	3447		
1AF	3448	F1 CMD3 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3449		
	3450		
	3451		
	3452	F1 CMD4 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3453		
	3454		
	3455		
1B0	3456	F1 CMD5 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3457		
	3458		
	3459		
	3460	F1 CMD6 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3461		
	3462		
	3463		
1B1	3464	F1 CMD7 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3465		
	3466		
	3467		
	3468	F1 CMD8 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3469		
	3470		
	3471		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
1B2	3472	F1 CMD9 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3473		
	3474		
	3475		
	3476	F1 CMD10 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3477		
	3478		
	3479		
1B3	3480	F1 CMD11 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3481		
	3482		
	3483		
	3484	F1 CMD12 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3485		
	3486		
	3487		
1B4	3488	delay loop to location selection	0000:CMD1;0001:CMD2;0010:CMD3;0011:CMD4;0100:CMD5;0101:CMD6:or;0110:CMD7;0111:CMD8;1000:CMD9;1001:CMD10;1010:CMD11;1011:CMD12
	3489		
	3490		
	3491		
	3492	output mux1 initial state setting	00: keep 01: 0 10: 1 11: none
	3493		
	3494	output mux2 initial state setting	00: keep 01: 0 10: 1 11: none
	3495		
1B5	3496	output mux3 initial state setting	00: keep 01: 0 10: 1 11: none
	3497		
	3498	interrupt reset stack memory enable	0: no reset stack memory 1: reset stack memory.
	3499	Reserved	
	3500	Reserved	
	3501	Reserved	
	3502	Reserved	
	3503	Reserved	
1B6	3504	aio0-3 input selection load 1	00: aio0 01: aio1 10: aio2 11: aio3
	3505		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
1B6	3506	ACMP4_F Vref selection load 1	"F1 input selection load 1" bit=0: Matrix input select: 000000: Matrix in0; ~ 111111: Matrix in63 "F1 input selection load 1" bit=1: ACMP Vref select: 000000: 32mV ~ 111110: 2.016V/ step=32mV; 111111: External Vref
	3507		
	3508		
	3509		
	3510		
	3511		
1B7	3512	aio0-3 input selection load 2	00: aio0 01: aio1 10: aio2 11: aio3
	3513		
	3514	ACMP4_F Vref selection load 2	"F1 input selection load 1" bit=0: Matrix input select: 000000: Matrix in0; ~ 111111: Matrix in63 "F1 input selection load 1" bit=1: ACMP Vref select: 000000: 32mV ~ 111110: 2.016V/ step=32mV; 111111: External Vref
	3515		
	3516		
	3517		
	3518		
	3519		
1B8	3520	aio4-7 input selection load 3	00: aio4 01: aio5 10: aio6 11: aio7
	3521		
	3522	ACMP4_F Vref selection load 3	"F1 input selection load 1" bit=0: Matrix input select: 000000: Matrix in0; ~ 111111: Matrix in63 "F1 input selection load 1" bit=1: ACMP Vref select: 000000: 32mV ~ 111110: 2.016V/ step=32mV; 111111: External Vref
	3523		
	3524		
	3525		
	3526		
	3527		
1B9	3528	aio4-7 input selection load 4	00: aio4 01: aio5 10: aio6 11: aio7
	3529		
	3530	ACMP4_F Vref selection load 4	"F1 input selection load 1" bit=0: Matrix input select: 000000: Matrix in0; ~ 111111: Matrix in63 "F1 input selection load 1" bit=1: ACMP Vref select: 000000: 32mV ~ 111110: 2.016V/ step=32mV; 111111: External VRE
	3531		
	3532		
	3533		
	3534		
	3535		
1BA	3536	F1 input selection load 1	0: from matrix 1: from ACMP4_F
	3537	F1 input selection load 2	0: from matrix 1: from ACMP4_F
	3538	F1 input selection load 3	0: from matrix 1: from ACMP4_F
	3539	F1 input selection load 4	0: from matrix 1: from ACMP4_F
	3540	Reserved	

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
1BA	3541	delay clock source selection	000: RING; 001: RING/4 010: RC 011: RC/8 100: RC/64 101: LF 110: LF/8 111: LF/64
	3542		
	3543		
1BB	3544	F1 delay data	Data[7:0]
	3545		
	3546		
	3547		
	3548		
	3549		
	3550		
	3551		
1BC	3552	F1 CMD1 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3553		
	3554		
	3555		
	3556	F1 CMD2 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3557		
	3558		
	3559		
1BD	3560	F1 CMD3 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3561		
	3562		
	3563		
	3564	F1 CMD4 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3565		
	3566		
	3567		
1BE	3568	F1 CMD5 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3569		
	3570		
	3571		
	3572	F1 CMD6 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3573		
	3574		
	3575		
1BF	3576	F1 CMD7 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3577		
	3578		
	3579		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
1BF	3580	F1 CMD8 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3581		
	3582		
	3583		
1C0	3584	F1 CMD9 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3585		
	3586		
	3587		
	3588	F1 CMD10 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3589		
	3590		
	3591		
1C1	3592	F1 CMD11 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3593		
	3594		
	3595		
	3596	F1 CMD12 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3597		
	3598		
	3599		
1C2	3600	delay loop to location selection	0000:CMD1;0001:CMD2;0010:CMD3;0011:CMD4;0100:CMD5;0101:CMD6:or;0110:CMD7;0111:CMD8;1000:CMD9;1001:CMD10;1010:CMD11;1011:CMD12
	3601		
	3602		
	3603		
	3604	output mux1 initial state setting	00: keep 01: 0 10: 1 11: none
	3605		
	3606	output mux2 initial state setting	00: keep 01: 0 10: 1 11: none
	3607		
1C3	3608	output mux3 initial state setting	00: keep 01: 0 10: 1 11: none
	3609		
	3610	interrupt reset stack memory enable	0: no reset stack memory 1: reset stack memory
	3611	Reserved	
	3612	Reserved	
	3613	Reserved	
	3614	Reserved	
1C3	3615	Reserved	

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
1C4	3616	aio0-3 input selection load 1	00: aio0 01: aio1 10: aio2 11: aio3
	3617		
	3618	ACMP4_F Vref selection load 1	"F1 input selection load 1" bit=0: Matrix input select: 000000: Matrix in0; ~ 111111: Matrix in63 "F1 input selection load 1" bit=1: ACMP Vref select: 000000: 32mV ~ 111110: 2.016V/ step=32mV; 111111: External Vref
	3619		
	3620		
	3621		
	3622		
	3623		
1C5	3624	aio0-3 input selection load 2	00: aio0 01: aio1 10: aio2 11: aio3
	3625		
	3626	ACMP4_F Vref selection load 2	"F1 input selection load 1" bit=0: Matrix input select: 000000: Matrix in0; ~ 111111: Matrix in63 "F1 input selection load 1" bit=1: ACMP Vref select: 000000: 32mV ~ 111110: 2.016V/ step=32mV; 111111: External Vref
	3627		
	3628		
	3629		
	3630		
	3631		
1C6	3632	aio4-7 input selection load 3	00: aio4 01: aio5 10: aio6 11: aio7
	3633		
	3634	ACMP4_F Vref selection load 3	"F1 input selection load 1" bit=0: Matrix input select: 000000: Matrix in0; ~ 111111: Matrix in63 "F1 input selection load 1" bit=1: ACMP Vref select: 000000: 32mV ~ 111110: 2.016V/ step=32mV; 111111: External Vref
	3635		
	3636		
	3637		
	3638		
	3639		
1C7	3640	aio4-7 input selection load 4	00: aio4 01: aio5 10: aio6 11: aio7
	3641		
	3642	ACMP4_F Vref selection load 4	"F1 input selection load 1" bit=0: Matrix input select: 000000: Matrix in0; ~ 111111: Matrix in63 "F1 input selection load 1" bit=1: ACMP Vref select: 000000: 32mV ~ 111110: 2.016V/ step=32mV; 111111: External Vref
	3643		
	3644		
	3645		
	3646		
	3647		
1C8	3648	F1 input selection load 1	0: from matrix 1: from ACMP4_F
	3649	F1 input selection load 2	0: from matrix 1: from ACMP4_F

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
1C8	3650	F1 input selection load 3	0: from matrix 1: from ACMP4_F
	3651	F1 input selection load 4	0: from matrix 1: from ACMP4_F
	3652	Reserved	
	3653	delay clock source selection	000: RING; 001: RING/4 010: RC 011: RC/8 100: RC/64 101: LF 110: LF/8 111: LF/64
	3654		
	3655		
1C9	3656	F1 delay data	Data[7:0]
	3657		
	3658		
	3659		
	3660		
	3661		
	3662		
	3663		
1CA	3664	F1 CMD1 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3665		
	3666		
	3667		
	3668	F1 CMD2 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3669		
	3670		
	3671		
1CB	3672	F1 CMD3 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3673		
	3674		
	3675		
	3676	F1 CMD4 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3677		
	3678		
	3679		
1CC	3680	F1 CMD5 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3681		
	3682		
	3683		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
1CC	3684	F1 CMD6 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3685		
	3686		
	3687		
1CD	3688	F1 CMD7 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3689		
	3690		
	3691		
	3692	F1 CMD8 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3693		
	3694		
	3695		
1CE	3696	F1 CMD9 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3697		
	3698		
	3699		
	3700	F1 CMD10 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3701		
	3702		
	3703		
1CF	3704	F1 CMD11 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3705		
	3706		
	3707		
	3708	F1 CMD12 selection	0000:load1;0001:load2;0010:load3;0011:load4;0100:and;0101:or;0110:xor;0111:inv;1000:push0;1001:pop;1010:delay;1011:delay with loop;1100:out1;1101:out2;1110:out3; 1111:end.
	3709		
	3710		
	3711		
1D0	3712	delay loop to location selection	0000: CMD1; 0001: CMD2; 0010: CMD3; 0011: CMD4; 0100: CMD5; 0101: CMD6 or; 0110: CMD7; 0111: CMD8; 1000: CMD9; 1001: CMD10; 1010: CMD11; 1011: CMD12
	3713		
	3714		
	3715		
	3716	output mux1 initial state setting	00: keep 01: 0 10: 1 11: none
	3717		
	3718	output mux2 initial state setting	00: keep 01: 0 10: 1 11: none
	3719		
1D1	3720	output mux3 initial state setting	00: keep 01: 0 10: 1 11: none
	3721		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
1D1	3722	interrupt reset stack memory enable	0: no reset stack memory 1: reset stack memory
	3723	Reserved	
	3724	Reserved	
	3725	Reserved	
	3726	Reserved	
	3727	Reserved	
1D2	3728 3729 3730	F1 state0 setting selection	000: none 001: setting 0 010: setting 1 011: setting 2 100: setting 3 101: none 110: none 111: none
	3731 3732 3733	F1 state 1 setting selection	000: none 001: setting 0 010: setting 1 011: setting 2 100: setting 3 101: none 110: none 111: none
	3734 3735	F1 state 2 setting selection	000: none 001: setting 0 010: setting 1 011: setting 2 100: setting 3 101: none 110: none 111: none
1D3	3736		
	3737 3738 3739	F1 state 3 setting selection	000: none 001: setting 0 010: setting 1 011: setting 2 100: setting 3 101: none 110: none 111: none
	3740 3741 3742	F1 state 4 setting selection	000: none 001: setting 0 010: setting 1 011: setting 2 100: setting 3 101: none 110: none 111: none

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
1D3	3743	F1 state 5 setting selection	000: none 001: setting 0 010: setting 1 011: setting 2 100: setting 3 101: none 110: none 111: none
1D4	3744		
1D4	3745		
1D4	3746	F1 state 6 setting selection	000: none 001: setting 0 010: setting 1 011: setting 2 100: setting 3 101: none 110: none 111: none
1D4	3747		
1D4	3748		
1D4	3749	F1 state 7 setting selection	000: none 001: setting 0 010: setting 1 011: setting 2 100: setting 3 101: none 110: none 111: none
1D4	3750		
1D4	3751		
1D5	3752	F1 state 8 setting selection	000: none 001: setting 0 010: setting 1 011: setting 2 100: setting 3 101: none 110: none 111: none
1D5	3753		
1D5	3754		
1D5	3755	F1 state 9 setting selection	000: none 001: setting 0 010: setting 1 011: setting 2 100: setting 3 101: none 110: none 111: none
1D5	3756		
1D5	3757		
1D5	3758	F1 state 10 setting selection	000: none 001: setting 0 010: setting 1 011: setting 2 100: setting 3 101: none 110: none 111: none
1D5	3759		
1D6	3760		
1D6	3761	F1 state 11 setting selection	000: none 001: setting 0 010: setting 1 011: setting 2 100: setting 3 101: none 110: none 111: none.
1D6	3762		
1D6	3763		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
1D6	3764	F1 ACMP4_F input LPF enable	0: input no LPF 1: input with LPF
	3765	F1 ACMP4_F output LPF enable	0: output no LPF 1: output with LPF
	3766	register interrupt	1: interrupt active
	3767	Reserved	
1D7	3768	Matrix Input 0	
	3769	Matrix Input 1	
	3770	Matrix Input 2	
	3771	Matrix Input 3	
	3772	Matrix Input 4	
	3773	Matrix Input 5	
	3774	Matrix Input 6	
	3775	Matrix Input 7	
1D8	3776	Matrix Input 8	
	3777	Matrix Input 9	
	3778	Matrix Input 10	
	3779	Matrix Input 11	
	3780	Matrix Input 12	
	3781	Matrix Input 13	
	3782	Matrix Input 14	
	3783	Matrix Input 15	
1D9	3784	Matrix Input 16	
	3785	Matrix Input 17	
	3786	Matrix Input 18	
	3787	Matrix Input 19	
	3788	Matrix Input 20	
	3789	Matrix Input 21	
	3790	Matrix Input 22	
	3791	Matrix Input 23	
1DA	3792	Matrix Input 24	
	3793	Matrix Input 25	
	3794	Matrix Input 26	
	3795	Matrix Input 27	
	3796	Matrix Input 28	
	3797	Matrix Input 29	
	3798	Matrix Input 30	
	3799	Matrix Input 31	
1DB	3800	Matrix Input 32	Virtual Input [0]
	3801	Matrix Input 33	Virtual Input [1]
	3802	Matrix Input 34	Virtual Input [2]
	3803	Matrix Input 35	Virtual Input [3]

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
1DB	3804	Matrix Input 36	Virtual Input [4]
	3805	Matrix Input 37	Virtual Input [5]
	3806	Matrix Input 38	Virtual Input [6]
	3807	Matrix Input 39	Virtual Input [7]
1DC	3808	Matrix Input 40	
	3809	Matrix Input 41	
	3810	Matrix Input 42	
	3811	Matrix Input 43	
	3812	Matrix Input 44	
	3813	Matrix Input 45	
	3814	Matrix Input 46	
	3815	Matrix Input 47	
1DD	3816	Matrix Input 48	
	3817	Matrix Input 49	
	3818	Matrix Input 50	
	3819	Matrix Input 51	
	3820	Matrix Input 52	
	3821	Matrix Input 53	
	3822	Matrix Input 54	
	3823	Matrix Input 55	
1DE	3824	Matrix Input 56	
	3825	Matrix Input 57	
	3826	Matrix Input 58	
	3827	Matrix Input 59	
	3828	Matrix Input 60	
	3829	Matrix Input 61	
	3830	Matrix Input 62	
	3831	Matrix Input 63	

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
1DF	3832	CNT0 (16bits) Counted Value	
	3833		
	3834		
	3835		
	3836		
	3837		
	3838		
	3839		
1E0	3840		
	3841		
	3842		
	3843		
	3844		
	3845		
	3846		
	3847		
1E1	3848	CNT2 (8bits) Counted Value	
	3849		
	3850		
	3851		
	3852		
	3853		
	3854		
	3855		
1E2	3856	CNT4 (8bits) Counted Value	
	3857		
	3858		
	3859		
	3860		
	3861		
	3862		
	3863		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
1E3	3864	ASM state read back	
	3865		
	3866		
	3867		
	3868		
	3869		
	3870		
	3871		
1E4	3872		
	3873		
	3874		
	3875		
	3876		
	3877		
	3878		
	3879		
1E5	3880	GPIO4 I^2C output expender data	
	3881	GPIO4 I^2C output expender select	0: GPIO4 output come from matrix 1: GPIO4 output is register
	3882	GPIO5 I^2C output expender data	
	3883	GPIO5 I^2C output expender select	0: GPIO5 output come from matrix 1: GPIO5 output is register
	3884	GPIO6 I^2C output expender data	
	3885	GPIO6 I^2C output expender select	0: GPIO6 output come from matrix 1: GPIO6 output is register
	3886	GPIO7 I^2C output expender data	
	3887	GPIO7 I^2C output expender select	0: GPIO7 output come from matrix 1: GPIO7 output is register
1E6	3888	ACMP0_H Gain divider	ACMP gain divider select: 00: 1X 01: 0.5X 10: 0.33X 11: Reserved
	3889		
	3890	ACMP0_H Vref	ACMP Vref select: 000000: 32mV ~ 111110: 2.016V/ step=32mV 111111: External Vref
	3891		
	3892		
	3893		
	3894		
	3895		
1E7	3896	ACMP1_H Gain divider	ACMP gain divider select: 00: 1X 01: 0.5X 10: 0.33X 11: Reserved
	3897		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
1E7	3898	ACMP1_H Vref	ACMP Vref select: 000000: 32mV ~ 111110: 2.016V/ step=32mV 111111: External Vref
	3899		
	3900		
	3901		
	3902		
	3903		
1E8	3904	ACMP2_L Gain divider	ACMP gain divider select: 00: 1X 01: 0.5X 10: 0.33X 11: Reserved
	3905		
	3906	ACMP2_L Vref	ACMP Vref select: 000000: 32mV ~ 111110: 2.016V/ step=32mV 111111: External Vref
	3907		
	3908		
	3909		
	3910		
	3911		
1E9	3912	ACMP3_L Gain divider	ACMP gain divider select: 00: 1X 01: 0.5X 10: 0.33X 11: Reserved
	3913		
	3914	ACMP3_L Vref	ACMP Vref select: 000000: 32mV ~ 111110: 2.016V/ step=32mV 111111: External Vref
	3915		
	3916		
	3917		
	3918		
	3919		
1EA	3920	REG_LUT4_0_D0[15:0]	Data[15:0]
	3921		
	3922		
	3923		
	3924		
	3925		
	3926		
	3927		
1EB	3928		
	3929		
	3930		
	3931		
	3932		
	3933		
	3934		
	3935		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
1EC	3936	REG_LUT3_4_D1[7:0]	Data[7:0]
	3937		
	3938		
	3939		
	3940		
	3941		
	3942		
	3943		
1ED	3944	REG_LUT3_5_D2[7:0]	Data[7:0]
	3945		
	3946		
	3947		
	3948		
	3949		
	3950		
	3951		
1EE	3952	REG_LUT3_6_D3[7:0]	Data[7:0]
	3953		
	3954		
	3955		
	3956		
	3957		
	3958		
	3959		
1EF	3960	REG_LUT3_7_D4[7:0]	Data[7:0]
	3961		
	3962		
	3963		
	3964		
	3965		
	3966		
	3967		
1F0	3968	band gap trim bit0	
	3969	band gap trim bit1	
	3970	band gap trim bit2	
	3971	band gap trim bit3	
	3972	band gap trim bit4	
	3973	band gap trim bit5	
	3974	band gap trim bits6	
	3975	band gap trim bits program protect; CK&CKB function enable	1: program protect; CK&CKB function disable

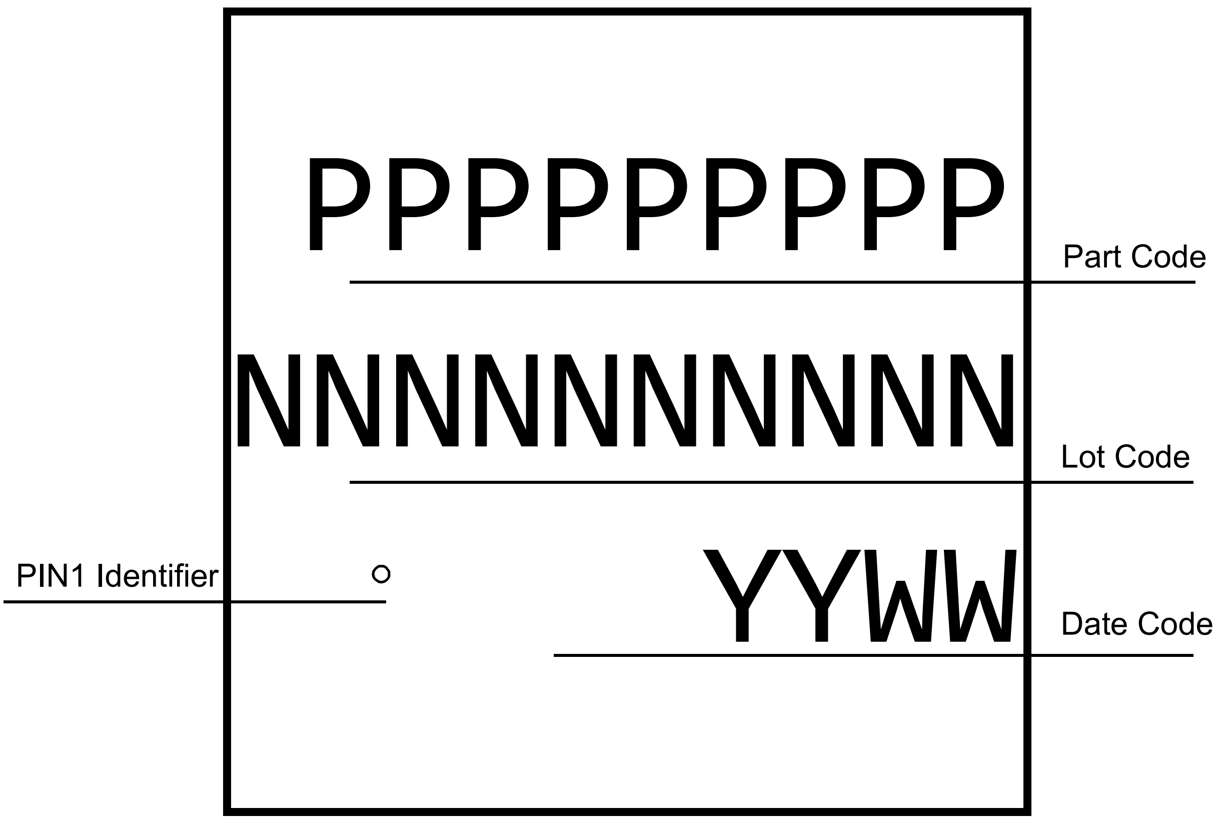
Address		Signal Function	Register Bit Definition
Byte	Register Bit		
1F1	3976	F1 Vref trim bit0	
	3977	F1 Vref trim bit1	
	3978	F1 Vref trim bit2	
	3979	F1 Vref trim bit3	
	3980	Reserved	
	3981	Reserved	
	3982	F1 ACMP test enable	1: enable
	3983	F1 Vref trim bits program protect	1: program protect
1F2	3984	Temperature sensor trim bit0	
	3985	Temperature sensor trim bit1	
	3986	Temperature sensor trim bit2	
	3987	Temperature sensor trim bit3	
	3988	Reserved	
	3989	Reserved	
	3990	Reserved	
	3991	Temperature sensor trim bits program protect	1: program protect
1F3	3992	LPVref trim bit0	
	3993	LPVref trim bit1	
	3994	LPVref trim bit2	
	3995	LPVref trim bit3	
	3996	LPVref trim bit4	
	3997	Reserved	
	3998	F1 ACMP test enable	1: enable
	3999	LPVref trim bits program protect	1: program protect
1F4	4000	OSC0 trim bit0	
	4001	OSC0 trim bit1	
	4002	OSC0 trim bit2	
	4003	OSC0 trim bit3	
	4004	OSC0 trim bit4	
	4005	OSC0 trim bit5	
	4006	Reserved	
	4007	OSC0 trim bits program protect	1: program protect
1F5	4008	OSC1 trim bit0	
	4009	OSC1 trim bit1	
	4010	OSC1 trim bit2	
	4011	OSC1 trim bit3	
	4012	OSC1 trim bit4	
	4013	OSC1 trim bit5	
	4014	Reserved	
	4015	OSC1 trim bits program protect	1: program protect

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
1F6	4016	OSC2 trim bit0	
	4017	OSC2 trim bit1	
	4018	OSC2 trim bit2	
	4019	OSC2 trim bit3	
	4020	OSC2 trim bit4	
	4021	OSC2 trim bit5	
	4022	Reserved	
	4023	OSC2 trim bits program protect	1: program protect
1F7	4024	Reserved	
	4025		
	4026		
	4027		
	4028		
	4029		
	4030		
	4031		
1F8	4032	NVM blank check result (From check circuit): ID[24]	
	4033	NVM Power-Up Check Pattern Status (From Flag): ID[25] (Reg[2047:2040]=0xA5, Reg[2015:2008]=0x5A)	0: Incorrect 1: Correct
	4034	Reserved for ID (From Metal Hard Code): ID[27:26]	00: Reserved
	4035		
	4036	Product Family ID (From Metal Hard Code): ID[31:28]	0000: 46880 0001: 46881
	4037		
	4038		
	4039		
1F9	4040	8-bit Pattern ID Byte 0 (From NVM): ID[23:16]	
	4041		
	4042		
	4043		
	4044		
	4045		
	4046		
	4047		

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
1FA	4048	Metal Revision ID (From Metal Hard Code): ID[15:8]	Hard Code 0x00
	4049		
	4050		
	4051		
	4052		
	4053		
	4054		
	4055		
1FB	4056	Base Die ID (From Metal Hard Code): ID[7:0]	Hard Code 0x58
	4057		
	4058		
	4059		
	4060		
	4061		
	4062		
	4063		
1FC	4064	I^2C reset bit with reloading NVM into Data register (soft reset)	0: Keep existing condition 1: Reset execution
	4065	IO Latching Enable During I^2C Write Interface	0: Disable 1: Enable
	4066	Reserved	
	4067	protect mode enable	0: Disable 1: Enable
	4068	trim enable	0: Disable 1: Enable
	4069	register protection mode bit 0	000: all open read/write (mode 0); 001: partly lock read (mode 1); 010: partly lock read2 (mode 2);011: partly lock read2/write (mode 3);100: all lock read (mode 4); 101: all lock write (mode 5); 110: all lock read/write (mode 6).
	4070	register protection mode bit 1	
	4071	register protection mode bit 2	
1FD	4072	I^2C write mask bits	1: mask 0: overwrite
	4073		
	4074		
	4075		
	4076		
	4077		
	4078		
	4079		

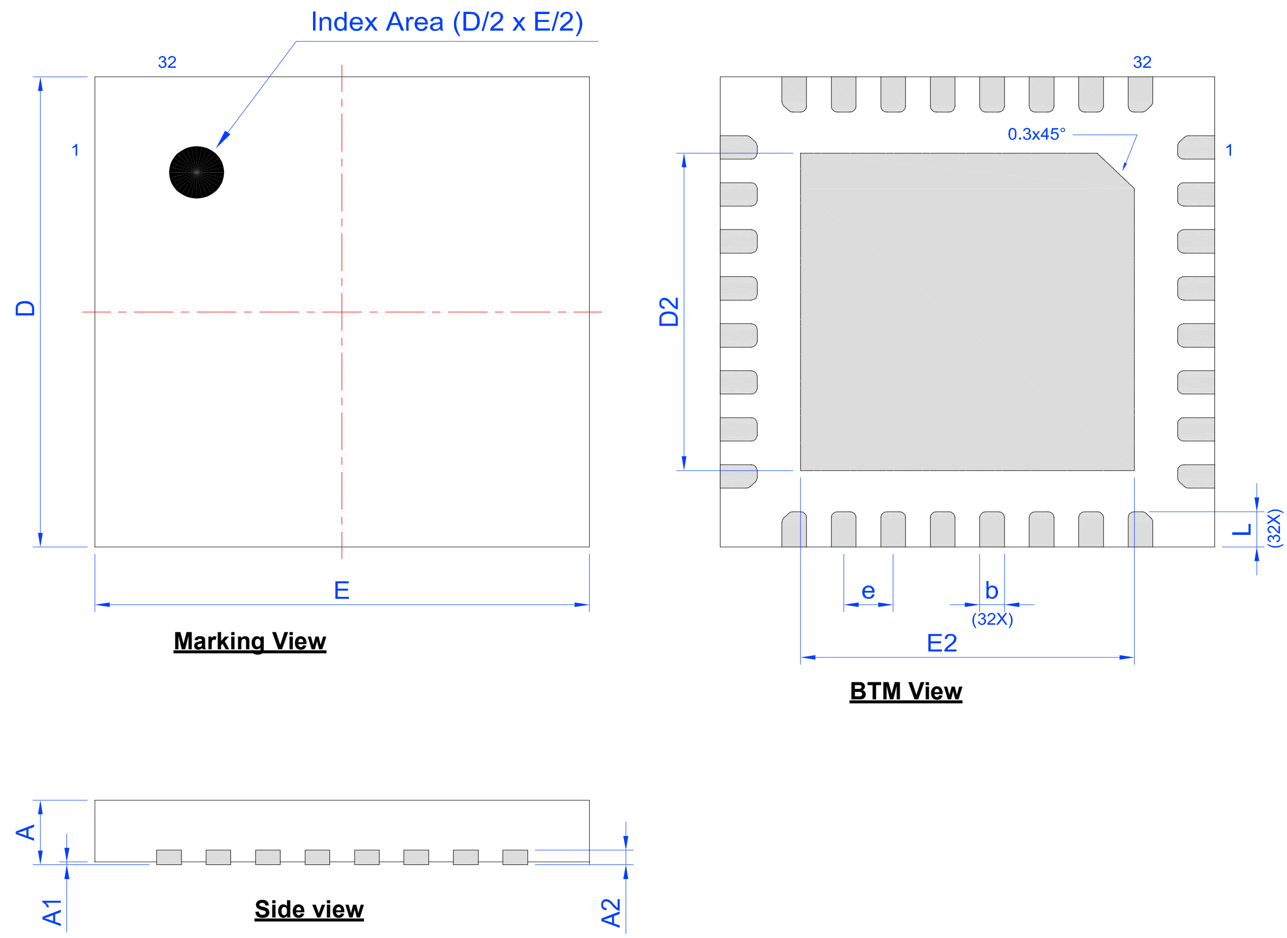
Address		Signal Function	Register Bit Definition
Byte	Register Bit		
1FE	4080	I^2C slave address	
	4081		
	4082		
	4083		
	4084	I^2C operation disable bit	0: I2C operation enable; matrix in 34(35) select I2C_virtual_0(1) Input 1: I2C operation disable; matrix in 34(35) select GPI2(3) digital input
	4085	NVM program disable	1: disable
	4086	code compare enable	1: enable
	4087	slave address selection	0: from Register 1: from Pin
1FF	4088	power sequency byte A5	A5 fixed
	4089		
	4090		
	4091		
	4092		
	4093		
	4094		
	4095		

22 Package Top Marking System Definition



23 Package Information

STQFN 32L 4 mm x 4 mm 0.4P Package
JEDEC MO-220, Variation WECE



Unit: mm

Symbol	Min.	Nom.	Max.	Symbol	Min.	Nom.	Max.
A	0.500	0.550	0.600	D	3.950	4.000	4.050
A1	0.00	-	0.050	E	3.950	4.000	4.050
A2	0.150 REF			D2	2.650	2.700	2.750
b	0.150	0.200	0.250	E2	2.650	0.270	2.750
e	0.400 BSC			L	0.250	0.300	0.350

24 STQFN Handling

Be sure to handle STQFN package only in a clean, ESD-safe environment. Tweezers or vacuum pick-up tools are suitable for handling. Do not handle STQFN package with fingers as this can contaminate the package pins and interface with solder reflow.

25 Soldering Information

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.85 mm^3 (nominal). More information can be found at www.jedec.org.

26 Ordering Information

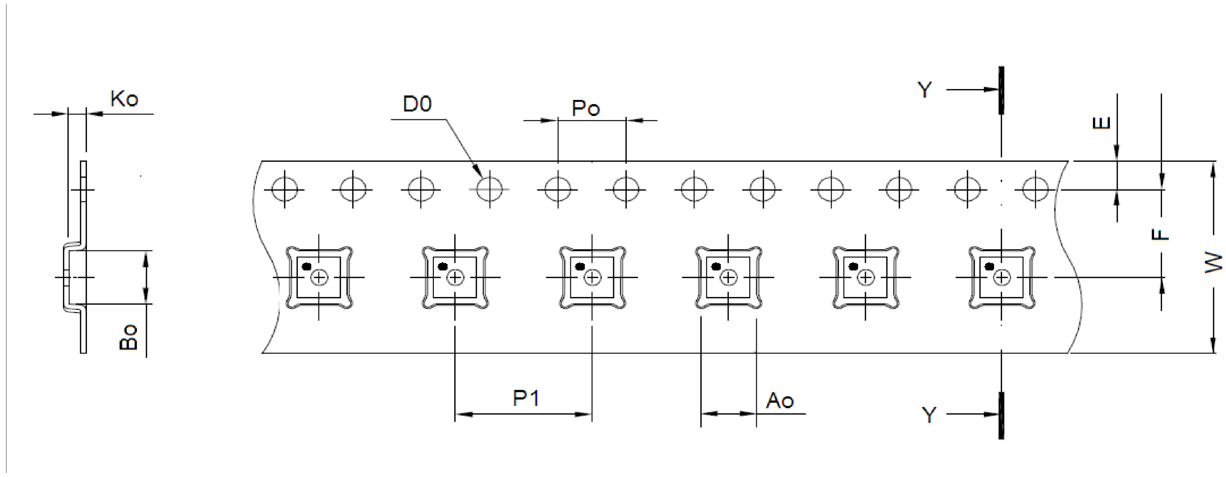
Part Number	Type
SLG46880V	32-Pin STQFN
SLG46880VTR	32-Pin STQFN - Tape and Reel (3k units)
SLG46881V	32-Pin STQFN
SLG46881VTR	32-Pin STQFN - Tape and Reel (3k units)

26.1 TAPE AND REEL SPECIFICATIONS

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Leader (min)		Trailer (min)		Tape Width (mm)	Part Pitch (mm)
			per Reel	per Box		Pockets	Length (mm)	Pockets	Length (mm)		
STQFN 32L 4 mm x4 mm 0.4P Green	32	4 x 4 x 0.55	5,000	10,000	330/100	42	336	42	336	12	8

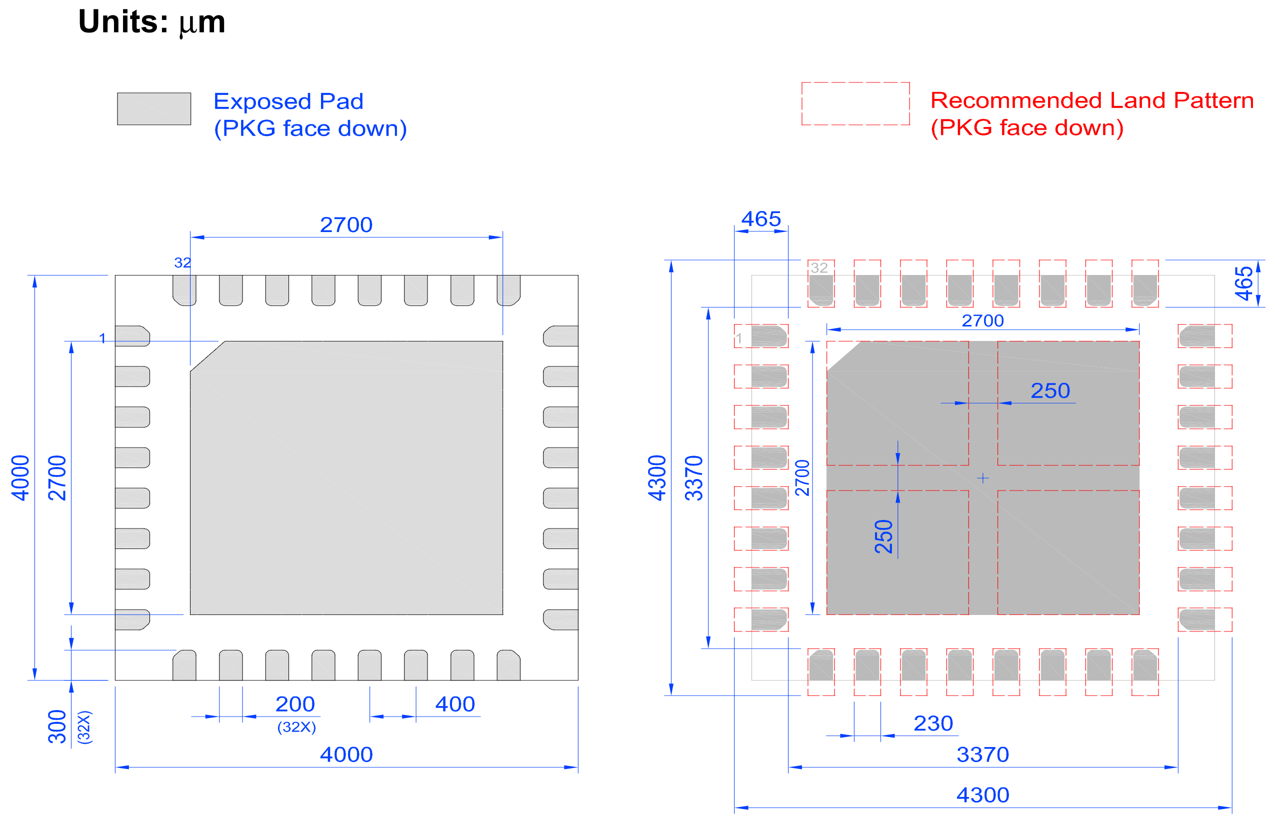
26.2 CARRIER TAPE DRAWING AND DIMENSIONS

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 32L 2 mm x3 mm 0.4P Green	4.25	4.25	0.75	4	8	1.5	1.75	5.5	12



Refer to EIA-481 specification

27 Layout Guidelines



Glossary

ACK	Acknowledge bit
ACMP	Analog Comparator
ACMPH	Analog Comparator High Speed
ACMPL	Analog Comparator Low Power
ASM	Asynchronous State Machine
BG	Bandgap
CLK	Clock
CMO	Connection matrix output
CNT	Counter
DFF	D Flip-Flop
DLY	Delay
DM	Dynamic Memory
EC	Electrical Characteristics
ERSE	Erase Enable
ERSR	Erase Register
ESD	Electrostatic discharge
EV	End Value
FSM	Finite State Machine
GPI	General Purpose Input
GPIO	General Purpose Input/Output
GPO	General Purpose Output
IN	Input
IO	Input/Output
LPF	Low Pass Filter
LSB	Least Significant Bit
LUT	Look-Up Table
LV	Low Voltage
MSB	Most Significant Bit
MTP	Multiple-Time-Programmable
MUX	Multiplexer
NPR	Non-Volatile Memory Read/Write/Erase Protection
nRST	Reset
NVM	Non-Volatile Memory
OD	Open Drain
OE	Output Enable
OSC	Oscillator
OUT	Output
PD	Power Down

PGEN	Pattern Generator
POR	Power-On Reset
PP	Push Pull
PRL	Protect Lock Bit
PWR	Power
P DLY	Programmable Delay
RPR	Register Read/Write Protection
RPRB	Register Read/Write Protection Bit
RPRL	Register Protection Read/Write/Erase Lock
R/W	Read/Write
SCL	I^2C Clock Input
SDA	I^2C Data Input/Output
SLA	Slave Address
SMT	With Schmitt Trigger
SV	nSET Value
TS	Temperature Sensor
Vref	Voltage Reference
WOSMT	Without Schmitt Trigger
WPB	Write Protect Bit
WPR	Write Protection Register
WPRE	Write Protect Enable
WS	Wake and Sleep Controller

Revision History

Revision	Date	Description
3.3	9-Aug-2018	Fixed typos
3.2	27-Jul-2018	Updated TS Structure Diagram Added STQFN Handling section Updated ACMP Electrical Spec Fixed formatting Updated R_{PULL} in Electrical Spec
3.1	30-Apr-2018	Updated TS Electrical Spec
3.0	18-Apr-2018	Final version

Status Definitions

Version	Datasheet Status	Product Status	Definition
1.[n]	Target	Development	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
2.[n]	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.[n]	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.dialog-semiconductor.com.
4.[n]	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

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Contacting Dialog Semiconductor

United Kingdom (Headquarters)
Dialog Semiconductor (UK) LTD
Phone: +44 1793 757700

Germany
Dialog Semiconductor GmbH
Phone: +49 7021 805-0

The Netherlands
Dialog Semiconductor B.V.
Phone: +31 73 640 8822

Email:
enquiry@diasemi.com

North America
Dialog Semiconductor Inc.
Phone: +1 408 845 8500

Japan
Dialog Semiconductor K. K.
Phone: +81 3 5769 5100

Taiwan
Dialog Semiconductor Taiwan
Phone: +886 281 786 222

Web site:
www.dialog-semiconductor.com

Hong Kong
Dialog Semiconductor Hong Kong
Phone: +852 2607 4271

Korea
Dialog Semiconductor Korea
Phone: +82 2 3469 8200

China (Shenzhen)
Dialog Semiconductor China
Phone: +86 755 2981 3669

China (Shanghai)
Dialog Semiconductor China
Phone: +86 21 5424 9058

