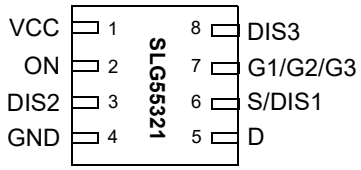
Triple Rail High Voltage Gate Driver

Features

- 5 V Power supply
- Drain Voltage Range 1.0 V to 20 V
- Internal Gate Voltage Charge Pump
- Controlled Load Discharge Rate
- Controlled Turn on Slew Rate
- TDFN-8 Package

Pin Configuration



8-pin TDFN
(Top View)

Application Functions

- Power Supply Sequencing with ramp/delay/discharge control
- Power Rail “Soft” Switch
- Hot Plugging Applications
- Low Transient Load Switching
- Replace high cost P-channel MOSFETs with lower cost N-channel MOSFETs

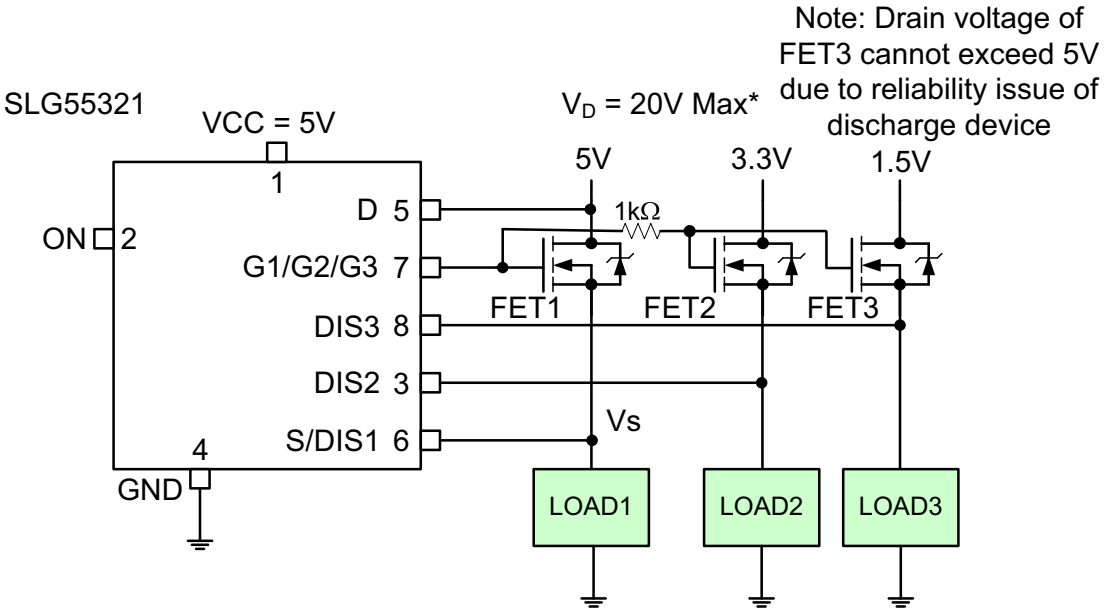
Environmental

- Pb-Free / RoHS Compliant
- Halogen Free

Target Application Products

- Notebook & Netbook Battery Packs
- Notebook & Netbook Sleep Mode Circuits
- Server Load Switches
- Gaming Sleep Mode Power Switches
- Communications Power Switches

Block Diagram



The highest V_D being switched must be at FET1 and pin 5

SLG55321
V_G is pumped to V_D + 8 V min

Pin Description

Pin Name	Pin Number	Type	Pin Description
VCC	1	Power	Supply Voltage
ON	2	Input	CMOS Logic Level
DIS2	3	Output	Discharge Connection for Load2.
GND	4	GND	Ground
D	5	Input	FET Drain Connection (Connect to FET with highest V_D voltage)
S/DIS1	6	Input/Output	Source Connection, Discharge Connection for Load1
G1/G2/G3	7	Output	FET Gate Drive for FET1, FET2, FET3. A minimum of a 1 kΩ resistor must be placed between the gate of MOSFET 1 and the gate of MOSFET 2 and another 1 kΩ resistor between the gate of MOSFET 2 and the gate of MOSFET 3.
DIS3	8	Output	Discharge Connection for Load3. Cannot exceed 5V.

Overview

The SLG55321 N-Channel FET Gate Drivers are used for controlling and ramping slew rate of the source voltage on N-Channel FET switches from a CMOS logic level input. Intended as a supporting control element for switched voltage rails in energy efficient, advanced power management systems, the SLG55321 also integrates circuits to discharge opened switched voltage rails. The gate driver is available in a variety of configurations supporting a range of turn-on slew rates from 0.80 V/ms up to 2 V/ms which, depending on load supplying source voltages in the range of 1.0 V to 20 V results in ramp times from 200 µs to over 20ms (see Application Section). Additionally, an internal discharge circuit provides a controlled path to remove charge from open power rails. The SLG55321 gate drive is packaged in an 8 pin DFN package.

When used with external N-Channel FETs, the SLG55321 supports low transient, energy efficient switching of high current loads at source voltages ranging from 1.0 V to 20 V.

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Ordering Information

Part Number	Ramp Slew Rate (Volts/ms)	Delay Time (ms)	Discharge Resistor (ohms)	Package Type
SLG55321-130010V	1.30	0.5	200	TDFN-8
SLG55321-130010VTR	1.30	0.5	200	TDFN-8 - Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
V_D or V_S to GND	-0.3	40.0	V
Voltage at Logic Input pins	-0.3	6.5	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	150	°C
Operating temperature range	-55	125	°C
Junction temperature	--	150	°C
ESD Human Body Model	--	2000	V
ESD Machine Model	--	200	V
Moisture Sensitivity Level	1		

Electrical Characteristics (-10°C to 75°C)

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		4.75	5.0	5.25	V
T_{VCC_RAMP}	V_{CC} Ramp-up Rate	See Note 1	0.25	--	--	V/ms
I_q	Quiescent Current	V_G not ramping FET = ON	--	--	80	µA
		V_G not ramping FET = OFF		0.1	1	µA
		V_G ramping FET = OFF to ON		600	1500	µA
V_D	FET Drain Voltage		1.0	--	21	V
V_{GS}	Gate-Source Voltage		8.0	11.5	13	V
C_G	FET Gate Capacitance		500	--	18000	pF
R_{ISO}	Isolation Resistor	External	1	--	--	kΩ
T_{DELAY}	Ramp Delay Range		0.25	0.5	0.75	ms
T_{SLEW}	FET Turn on Slew Rate		0.91	1.3	1.69	V/ms
$I_{DISCHARGE}$	Internal Discharge Resistor	Nominal discharge time of ~100ms 10mA max rate	140	200	260	Ω
		DIS3	40	--	600	Ω
V_{IH}	HIGH-level input voltage	ON (200mV Hysteresis)	2.4	--	5.5	V
V_{IL}	LOW-level Input voltage	ON (200mV Hysteresis)	--	--	0.4	V
I_{G_OL}	Gate Drive Sink Current		400	--	--	µA
I_{G_OH}	Gate Drive Source Current		32	--	--	µA
I_{D_IH}	Drain Pin Current	V_D = 20V in Standby	--	--	<1.0	µA
I_{S_IH}	Source Pin Current Quiesent	V_S = 20V	--	--	<1.0	µA

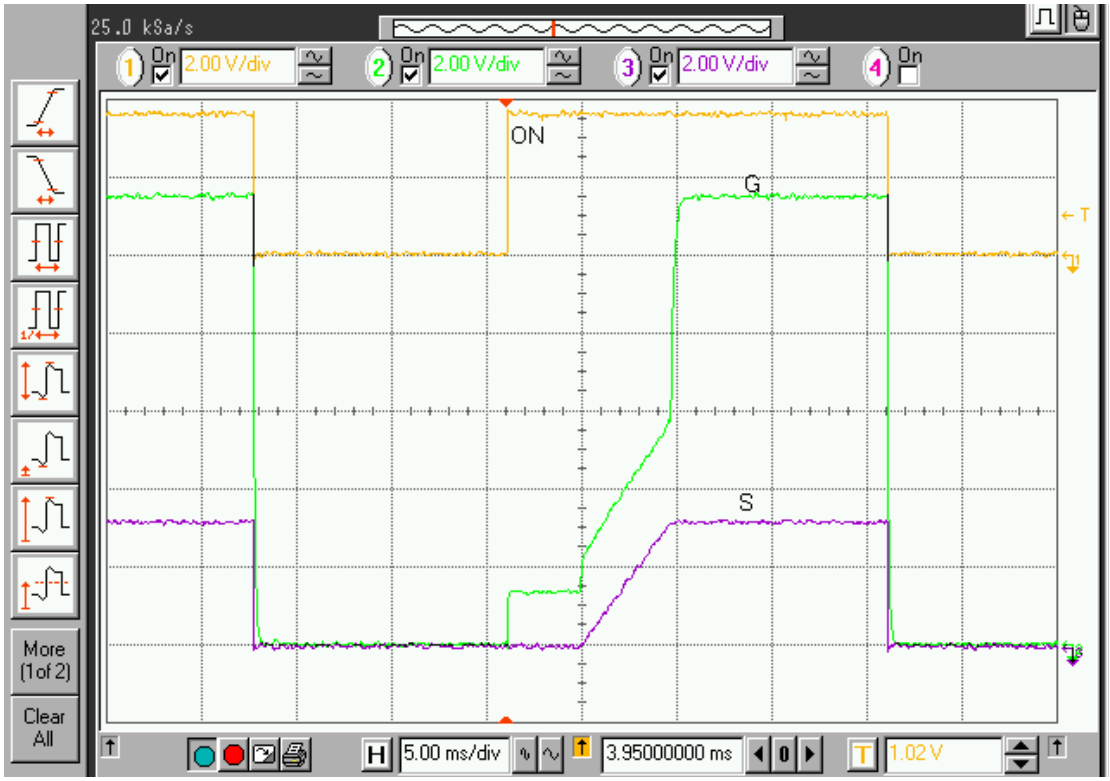
Note 1: If T_{VCC_RAMP} > 5 V/ms and ON is asserted, Gate charging will begin after 1 ms.

Application Example

In a typical application, de-asserting ON (low) turns off the external power N-FET. When the FET is turned off, the voltage at the load is discharged through a resistor (400 Ohms to 1000 Ohms or Open) internal to the SLG55321 with the discharge current limited to a maximum of 10mA. When ON is asserted (high), gate voltage is not applied to the gate of the external power N-FET until after DLY_t then the gate source (Vgs) voltage is ramped up to 11.5 V above the source voltage V_S at a slew rate determined by the internal slew rate control element internal to the SLG55321. Monotonic rise of Vs is maintained even as ID increases dramatically after the load device turn on threshold voltage is reached. After the source voltage has ramped up to its maximum steady state value, the Open Drain PG (Power Good) signal is asserted. PG may be used as the ON control of a second SLG55321 thereby providing power on sequence control of a number of switched power rails, or used in a 'wired and' with other PG signals to indicate all switched power rails are in a power good condition.

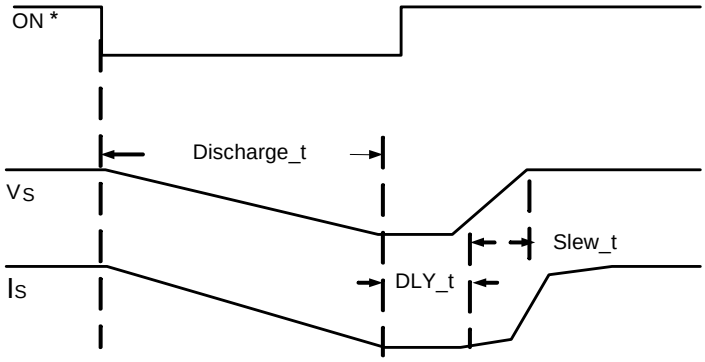
The devices will not operate if Vcc is below 3.5 V and will not operate until V_D reaches 0.8 V.

The waveforms shown illustrate the monotonic rise of the source voltage of a FET as gate voltage is controlled to accommodate for variations in load current as the voltage is applied.



Delay Time and Slew Rates

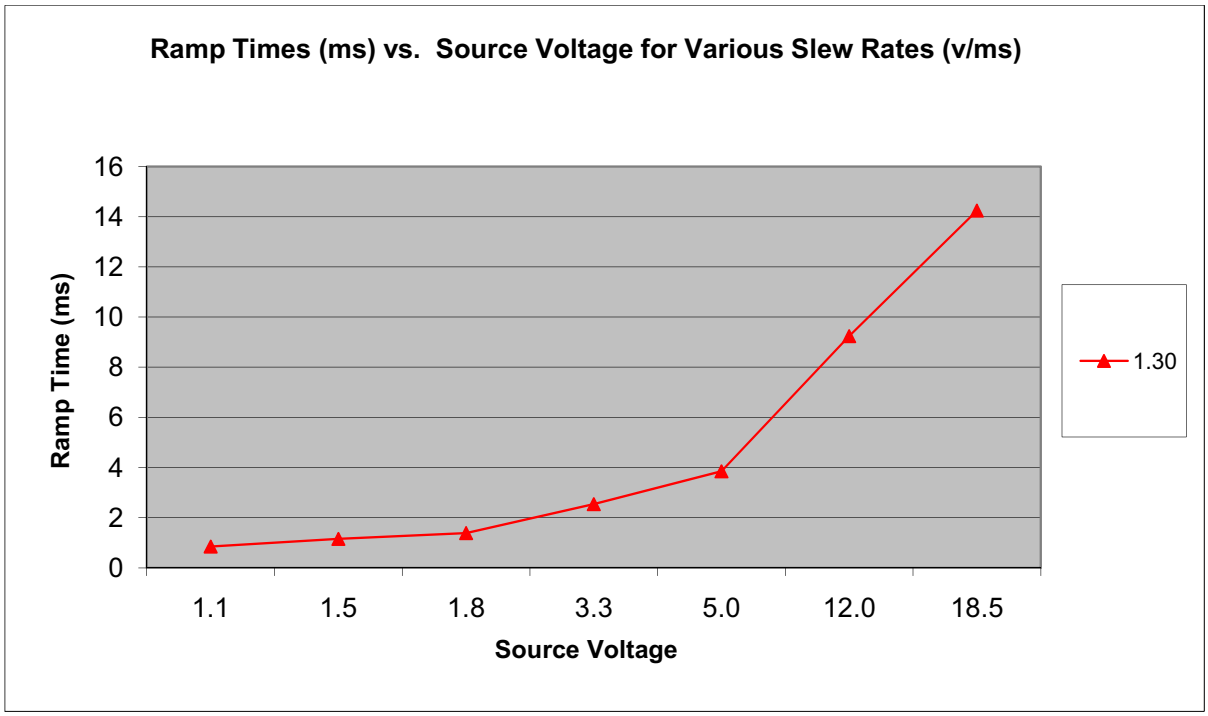
The two components of controlling the application of FET source voltage to the load are a fixed time delay before beginning turn on of the FET (DLY_t below) and the Slew Time of the source voltage (Slew_t below). The Delay Time before gate voltage to the FET is applied is 250 µs independent of FET drain voltage, source voltage or SLG55321 supply voltage.



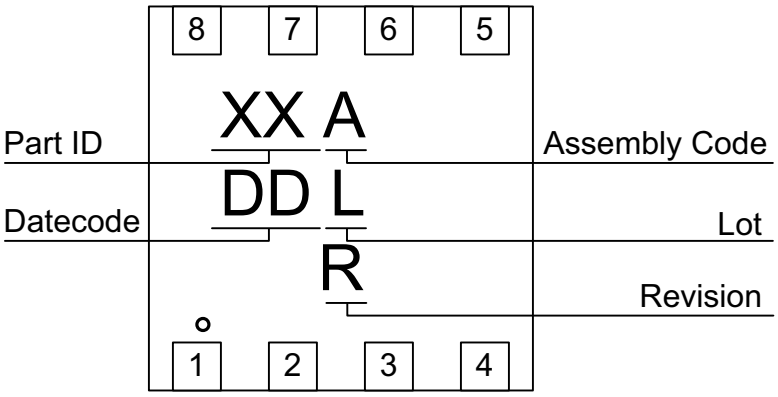
Having control over the Slew Rate of the FET's source voltage as the FET is turning on is important in controlling dv/dt caused transients. A power FET, for example, switching a 5 V rail which has a total of 500 µF of decoupling, fully on in 10 µs will generate a 250 A current surge which is very undesirable. If the FET turn on time can be stretched to 1ms, the current surge to charge the decoupling capacitors is reduced to 2.5 A. The SLG55321 controls slew rate of a FET's source voltage as it is turned on. A range of slew rates are available as device order options. Obviously the time to fully slew the source voltage to fully on is a function of the drain supply voltage. The table and graph below shows source voltage ramp times for various slew rates supported by the SLG55321 for a range of specific source voltages.

Slew Rates (V/ms)	Ramp Times (ms) vs. Source Voltages (V)						
	1.1 V	1.5 V	1.8 V	3.3 V	5.0 V	12 V	18.5 V
1.30	0.83	1.13	1.35	2.48	3.75	9.00	13.88

* The minimum time that ON can be de-asserted between switching cycles is 100 ms.



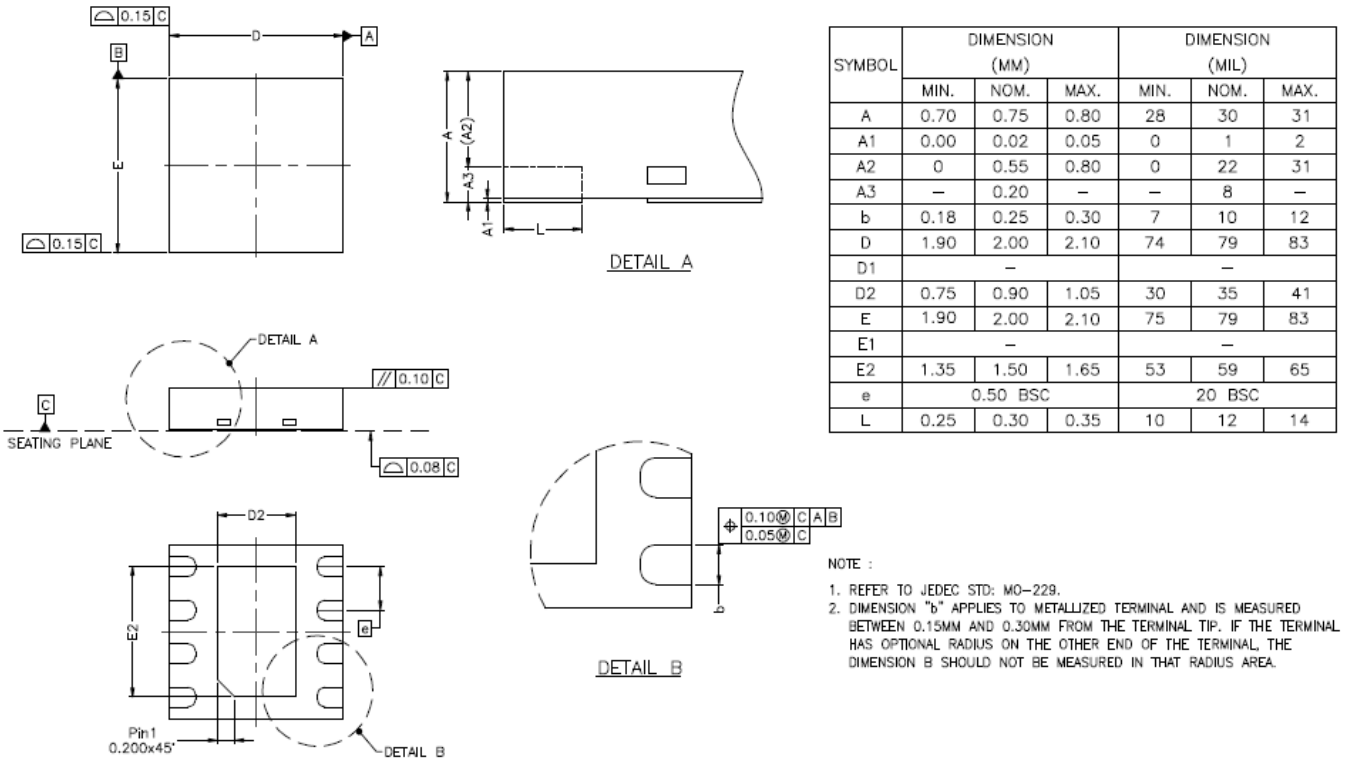
Package Top Marking System Definition



XX – Part ID Field: identifies the specific device configuration
A – Assembly Code Field: Assembly Location of the device.
DD – Date Code Field: Coded date of manufacture
L – Lot Code: Designates Lot #
R – Revision Code: Device Revision

Package Drawing and Dimensions

8 Lead TDFN Package



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	28	30	31
A1	0.00	0.02	0.05	0	1	2
A2	0	0.55	0.80	0	22	31
A3	–	0.20	–	–	8	–
b	0.18	0.25	0.30	7	10	12
D	1.90	2.00	2.10	74	79	83
D1		–			–	
D2	0.75	0.90	1.05	30	35	41
E	1.90	2.00	2.10	75	79	83
E1		–			–	
E2	1.35	1.50	1.65	53	59	65
e	0.50 BSC			20 BSC		
L	0.25	0.30	0.35	10	12	14

NOTE :
1. REFER TO JEDEC STD: MO–229.
2. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15MM AND 0.30MM FROM THE TERMINAL TIP. IF THE TERMINAL HAS OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION B SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

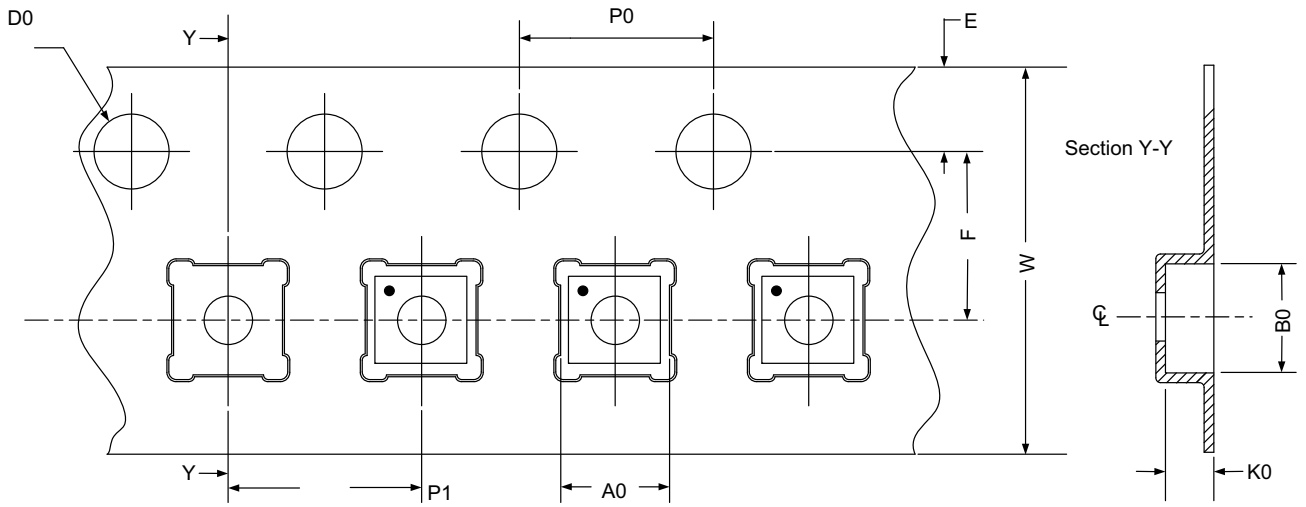
Note: Bottom side metal plate is at ground potential

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
TDFN 8L Green	8	2 x 2 x 0.75	3,000	3,000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
TDFN 8L Green	2.3	2.3	1.05	4	4	1.55	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.00 mm^3 (nominal). More information can be found at www.jedec.org.

Revision History

Date	Version	Change
2/9/2022	1.02	Updated Company name and logo Fixed typos
7/29/2017	1.01	Added MSL

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