Ultra-small 17 mΩ 2.5 A Load Switch with Discharge in Lo-Z™ Ultra-thin Package

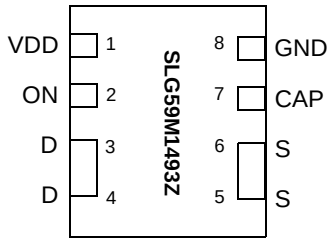
General Description

The SLG59M1493Z is a 17 mΩ 2.5 A single-channel load switch that is able to switch 1 to 5 V power rails. The product is packaged in an ultra-small 1.0 x 1.6 mm ETDFN package.

Features

- 1.0 x 1.6 x 0.3 mm ETDFN 8L package (2 fused pins for drain and 2 fused pins for source)
- Logic level ON pin capable of supporting 0.85 V CMOS Logic
- User selectable ramp rate with external capacitor
- 17 mΩ RDS_{ON}while supporting 2.5 A
- Discharges load when off
- Two Over Current Protection Modes
  - Short Circuit Current Limit
  - Active Current Limit
- Over Temperature Protection
- Pb-Free / Halogen-Free / RoHS compliant
- Operating Temperature: -20 °C to 70°C
- Operating Voltage: 2.5 V to 5.25 V

Pin Configuration

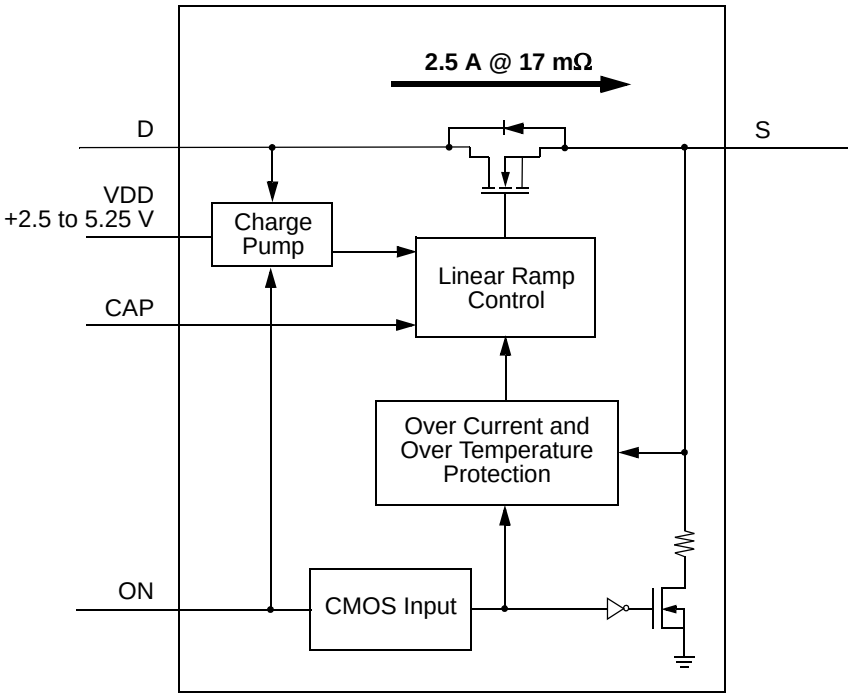


8-pin ETDFN
(Top View)

Applications

- Notebook Power Rail Switching
- Tablet Power Rail Switching
- Smartphone Power Rail Switching

Block Diagram



Advanced

Pin Description

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	V_{DD} power for load switch control (2.5 V to 5.25 V)
2	ON	Input	Turns MOSFET ON (4 MΩ pull down resistor) CMOS input with V_{IL} < 0.3 V, V_{IH} > 0.85 V
3	D	MOSFET	Drain of Power MOSFET (fused with pin 4)
4	D	MOSFET	Drain of Power MOSFET (fused with pin 3)
5	S	MOSFET	Source of Power MOSFET (fused with pin 6)
6	S	MOSFET	Source of Power MOSFET (fused with pin 5)
7	CAP	Input	Capacitor for controlling power rail ramp rate
8	GND	GND	Ground

Ordering Information

Part Number	Type	Production Flow
SLG59M1493Z	ETDFN 8L	Commercial, -20 °C to 70 °C
SLG59M1493ZTR	ETDFN 8L (Tape and Reel)	Commercial, -20 °C to 70 °C

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply		--	--	6	V
T_S	Storage Temperature		-65	--	150	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	--	--	V
W_{DIS}	Package Power Dissipation		--	--	0.2	W
MOSFET IDS_{PK}	Peak Current from Drain to Source	For no more than 1 ms with 1% duty cycle	--	--	3.5	A

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

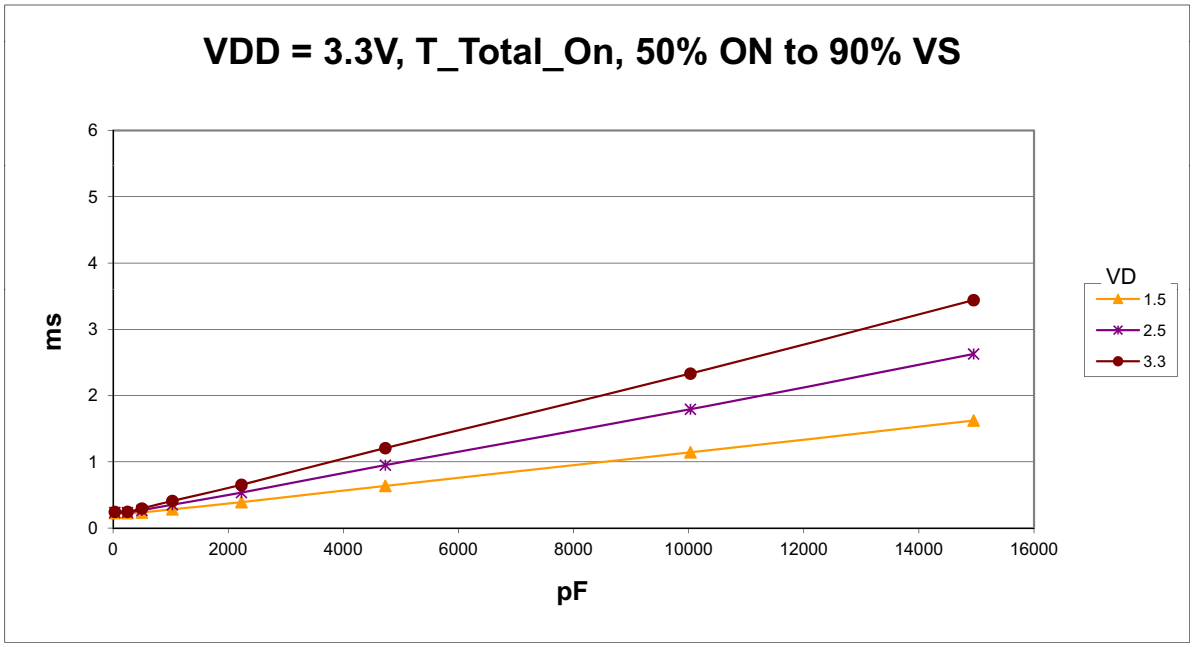
T_A = -20 to 70 °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage	-20 to 70°C	2.5	--	5.25	V
I_{DD}	Power Supply Current (PIN 1)	when OFF	--	--	1	µA
		when ON, No load	--	75	100	µA
RDS_{ON}	Static Drain to Source ON Resistance	T_A 25°C @ 100 mA	--	17	19	mΩ
		T_A 70°C @ 100 mA	--	18.5	20	mΩ
IDS	Operating Current	V_D = 1.0 V to 5.5 V	--	--	2.5	A
V_D	Drain Voltage		1.0	--	V_{DD}	V
T_{ON_Delay}	ON pin Delay Time	50% ON to Ramp Begin	0	300	500	µs
T_{Total_ON}	Total Turn On Time	50% ON to 90% V_S	Configurable [1]			ms
		Example: CAP (PIN 7) = 4 nF, V_{DD} = V_D = 5 V, C_{LOAD} = 10 µF, IDS = 100 mA	--	1.50	--	ms
$T_{SLEWRATE}$	Slew Rate	10% V_S to 90% V_S	Configurable [1]			V/ms
		Example: CAP (PIN 7) = 4 nF, V_{DD} = V_D = 5 V, C_{LOAD} = 10 µF, IDS = 100 mA	--	3.4	--	V/ms
C_{LOAD}	Output Load Capacitance	C_{LOAD} connected from V_S to GND	--	--	500	µF
R_{DIS}	Discharge Resistance		100	200	300	Ω
ON_V_{IH}	High Input Voltage on ON pin		0.85	--	V_{DD}	V
ON_V_{IL}	Low Input Voltage on ON pin		-0.3	0	0.3	V
I_{LIMIT}	Active Current Limit	MOSFET will automatically limit current when V_S > 250 mV	--	3.7	--	A
	Short Circuit Current Limit	MOSFET will automatically limit current when V_S < 250 mV	--	0.9	--	A
$THERM_{ON}$	Thermal shutoff turn-on temperature		--	125	--	°C
$THERM_{OFF}$	Thermal shutoff turn-off temperature		--	100	--	°C
$THERM_{TIME}$	Thermal shutoff time		--	--	1	ms
T_{OFF_Delay}	OFF Delay Time	50% ON to V_S Fall, V_{DD} = V_D = 5 V	--	8	--	µs
T_{FALL}	V_S Fall Time	90% V_S to 10% V_S, V_{DD} = V_D = 5 V	--	33	--	µs

Notes:
1. Refer to table for configuration details.

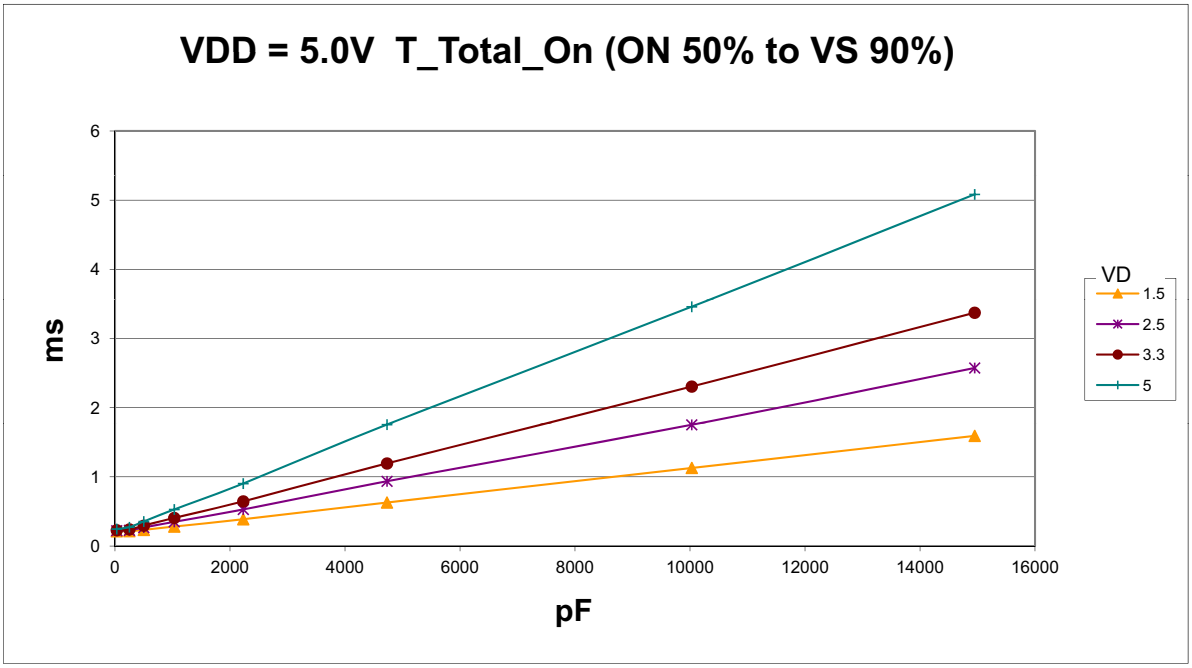
T_{Total_ON} vs. CAP @ V_{DD} = 3.3 V

SLG59M1493Z T_{Total_ON}: ON (50%) - V_S (90%)
V_{DD} = 3.3 V, T_A = 25 °C. C_{LOAD} = 10 µF, IDS = 100 mA



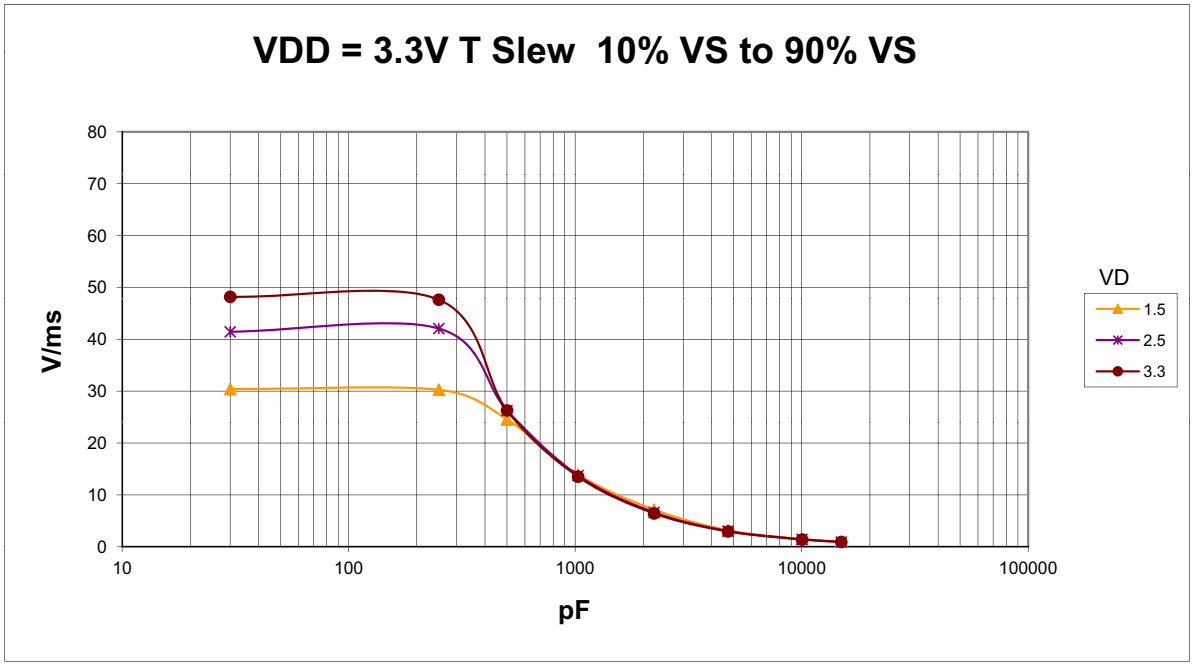
T_{Total_ON} vs. CAP @ V_{DD} = 5.0 V

SLG59M1493Z T_{Total_ON}: ON (50%) - V_S (90%)
V_{DD} = 5.0 V, T_A = 25 °C. C_{LOAD} = 10 µF, IDS = 100 mA



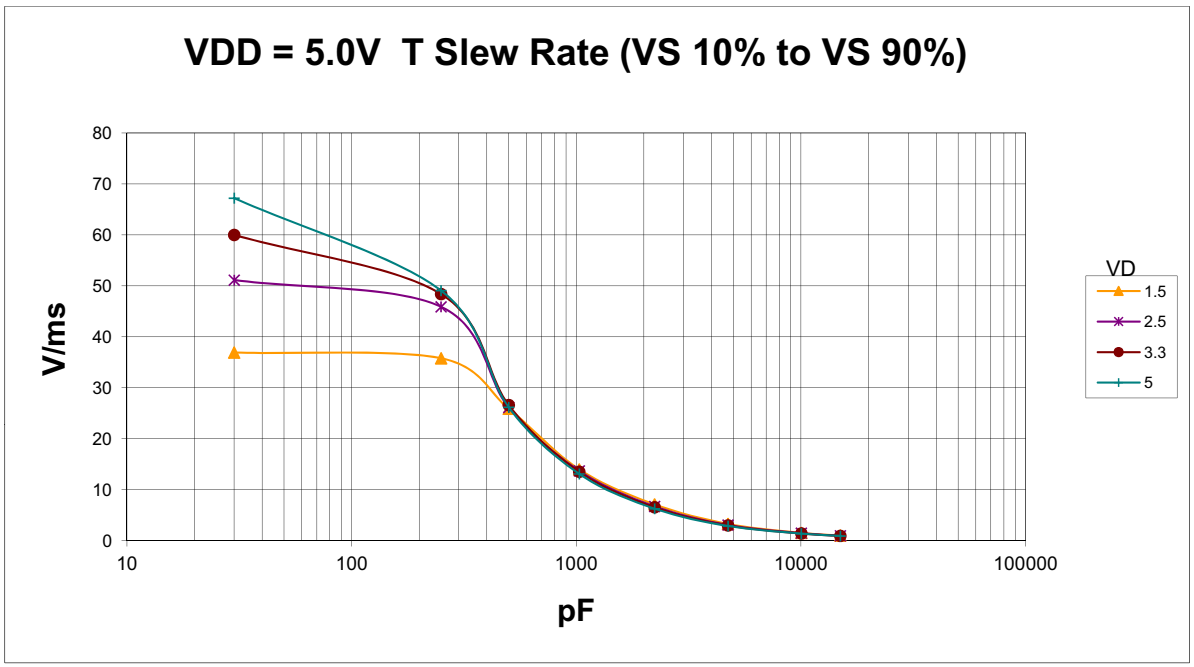
$T_{SLEWRATE}$ vs. CAP @ V_{DD} = 3.3 V

SLG59M1493Z $T_{SLEWRATE}$: V_S (10%) - V_S (90%)
V_{DD} = 3.3 V, T_A = 25 °C. C_{LOAD} = 10 µF, IDS = 100 mA

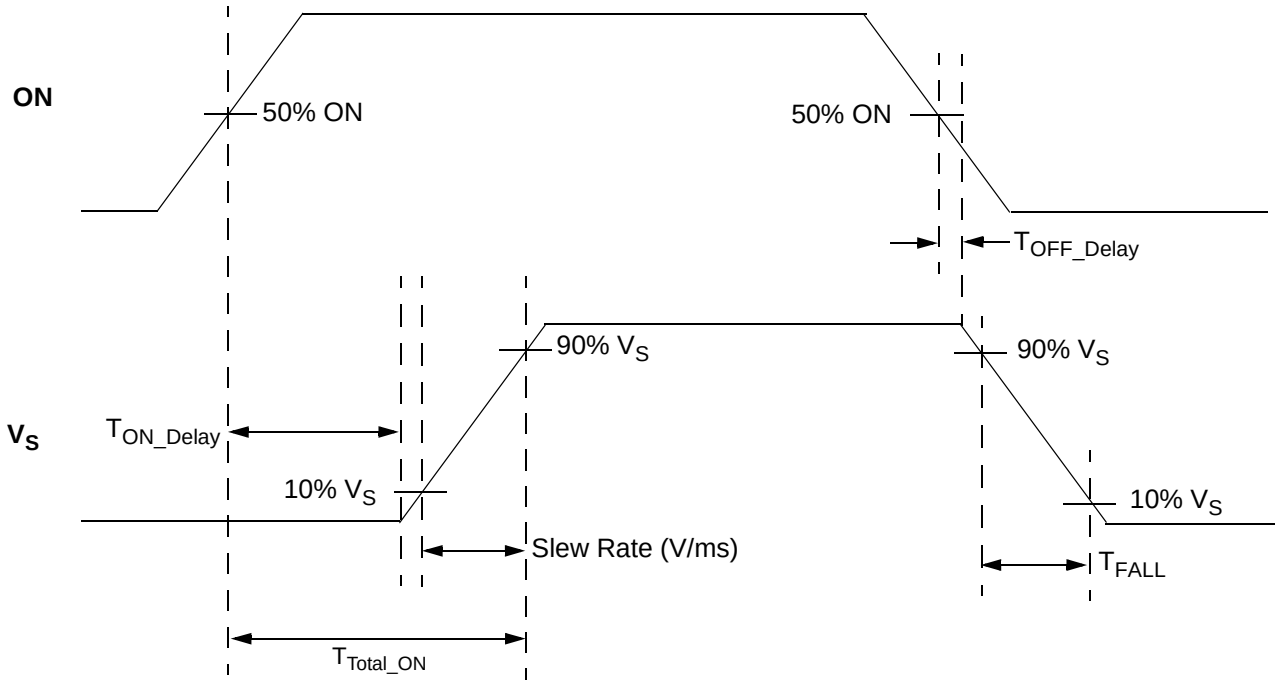


$T_{SLEWRATE}$ vs. CAP @ V_{DD} = 5.0 V

SLG59M1493Z $T_{SLEWRATE}$: V_S (10%) - V_S (90%)
V_{DD} = 5.0 V, T_A = 25 °C. C_{LOAD} = 10 µF, IDS = 100 mA



T_{Total_ON}, T_{ON_Delay} and Slew Rate Measurement



SLG59M1493Z Power-Up/Power-Down Sequence Considerations

To ensure glitch-free power-up under all conditions, apply V_{DD} first, followed by V_D after V_{DD} exceeds 1 V. Then allow V_D to reach 90% of its max value before toggling the ON pin from Low-to-High. Likewise, power-down in reverse order.

If V_{DD} and V_D need to be powered up simultaneously, glitching can be minimized by having a suitable load capacitor. A 10 µF C_{LOAD} will prevent glitches for rise times of V_{DD} and V_D less than 2 ms.

If the ON pin is toggled HIGH before V_{DD} and V_D have reached their steady-state values, the IPS timing parameters may differ from datasheet specifications.

The slew rate of output V_S follows a linear ramp set by a capacitor connected to the CAP pin. A larger capacitor value at the CAP pin produces a slower ramp, reducing inrush current from capacitive loads.

SLG59M1493Z Current Limiting

The SLG59M1493Z has two modes of current limiting, differentiated by the output (Source pin) voltage.

1. Standard Current Limiting Mode (with Thermal Protection)

When V(S) > 250 mV, the output current is initially limited to the Active Current Limit specification given in the Electrical Characteristics table. The current limiting circuit is very fast and responds within a few micro-seconds to sudden loads. When overload is sensed, the current limiting circuit increases the FET resistance to keep the current from exceedng the Active Current Limit.

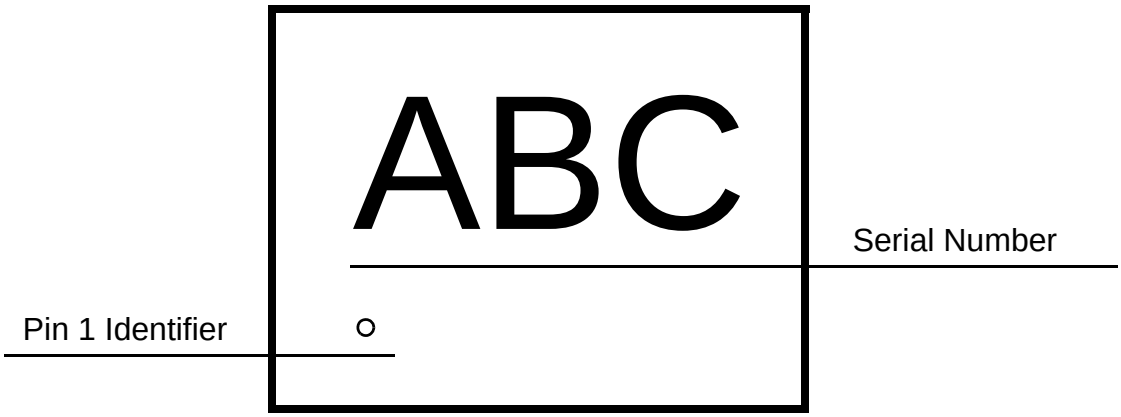
However, if an overload condition persists, the die temperature rise due to the increased FET resistance while at maximum current can activate Thermal Protection. If the die temperature exceeds the $THERM_{ON}$ specification, the FET is shut completely OFF, allowing the die to cool. When the die cools to the $THERM_{OFF}$ temperature, the FET is allowed to turn back on. This process may repeat as long as the overload condition is present.

2. Short Circuit Current Limiting Mode (with Thermal Protection)

When V(S) < 250 mV (which is the case with a hard short, such as a solder bridge on the power rail), the current is limited to approximately 500 mA. Thermal Protection is also present, but since the Short Circuit Current Limit is much lower than Standard Current Limit, activation may only occur at higher ambient temperatures.

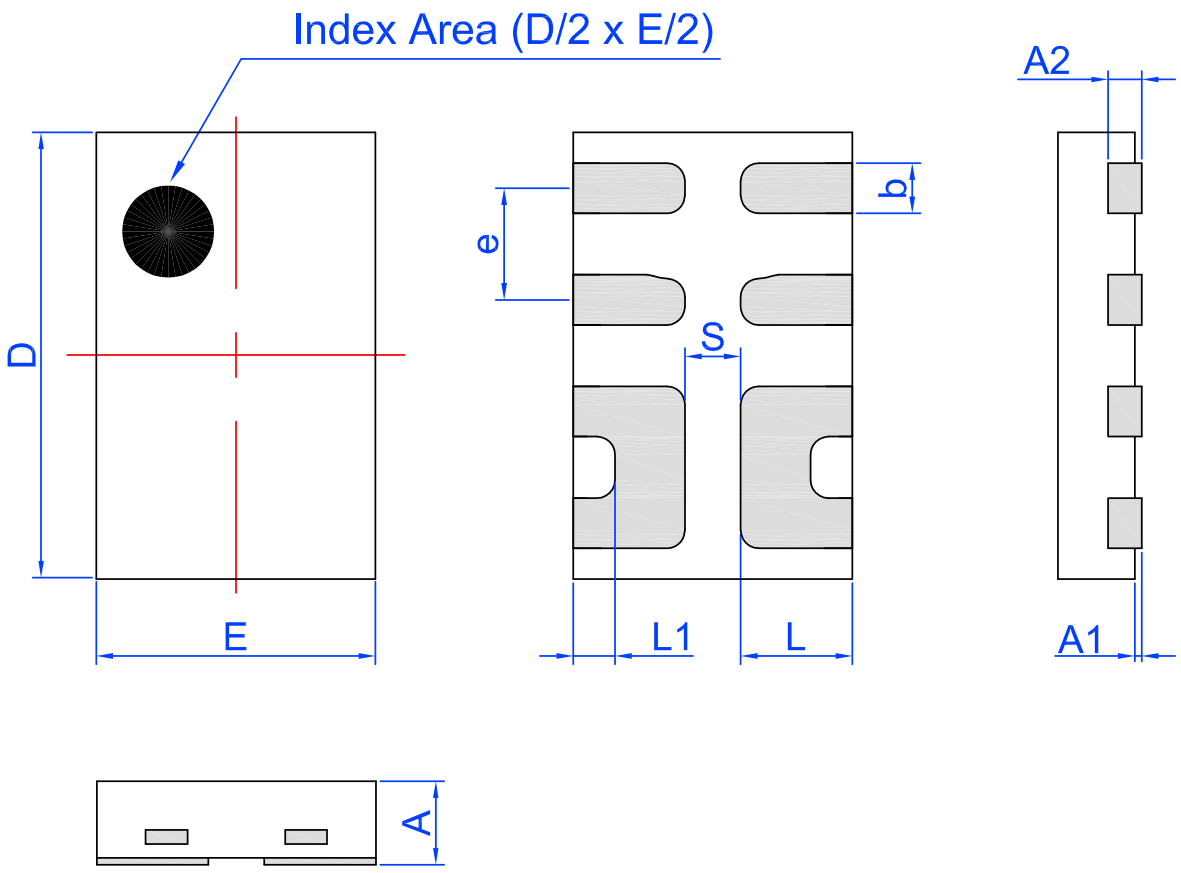
For more information on Silego GreenFET3 integrated power switch features, please visit our Application Notes page at our website and see App Note “AN-1068 GreenFET3 Integrated Power Switch Basics”.

Package Top Marking System Definition



Package Drawing and Dimensions

8 Lead ETDFN Package 1.0 x 1.6 mm (Fused Lead)



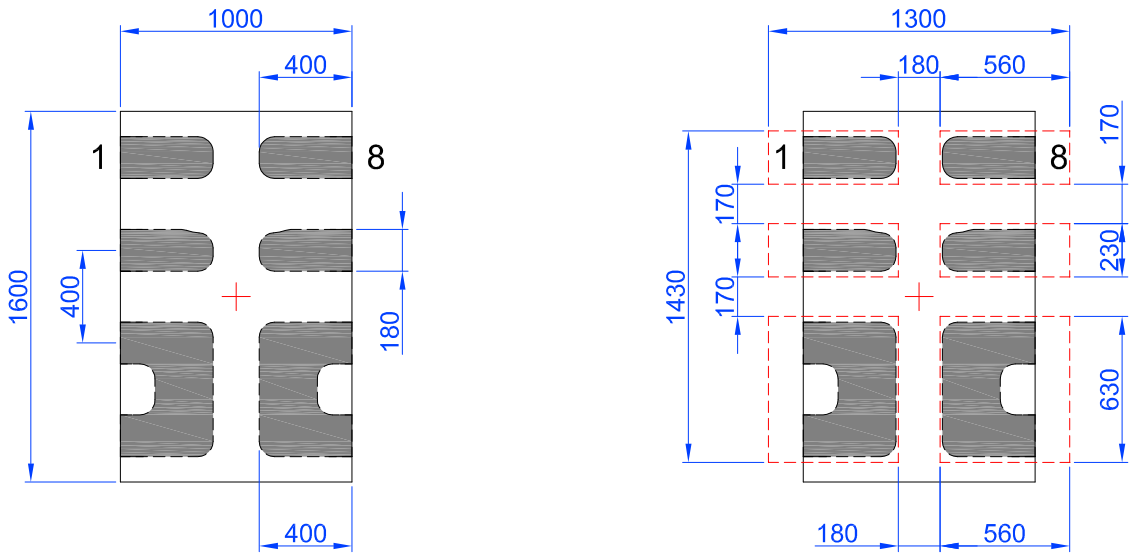
Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.25	0.275	0.30	D	1.55	1.60	1.65
A1	0.005	-	0.050	E	0.95	1.00	1.05
A2	0.10	0.15	0.20	L	0.35	0.40	0.45
b	0.13	0.18	0.23	L1	0.10	0.15	0.20
e	0.40 BSC			S	0.2 REF		

SLG59M1493Z 8-pin ETDFN PCB Landing Pattern

Exposed Pad
(PKG face down)

Recommended Land Pattern
(PKG face down)



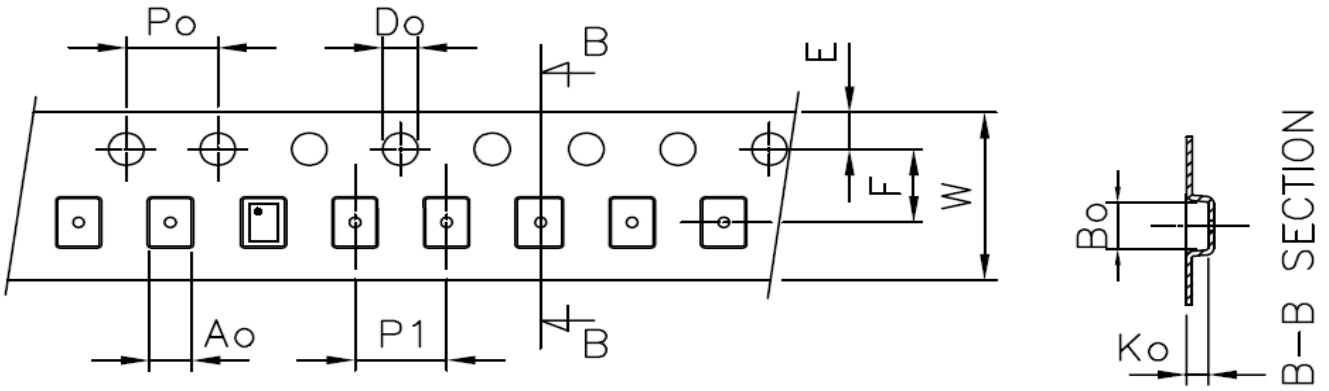
Unit: um

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
ETDFN 8L 1 x1.6 mm 0.4P FC Green	8	1.0 x 1.6 x 0.275	5,000	5,000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
ETDFN 8L 1 x1.6 mm 0.4P FC Green	1.15	1.78	0.42	4	4	1.55	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.48 mm^3 (nominal). More information can be found at www.jedec.org.

Revision History

Date	Version	Change
9/1/2016	0.15	Updated Power Up/Down Sequencing Considerations Updated Current Limiting Description Updated text and parameter names for clarity
6/16/2016	0.14	Updated POD dimensions Added Landing Pattern