SLG59M1563V

Ultra-small 22.5 mΩ 2.5 A Load Switch with Reverse Blocking

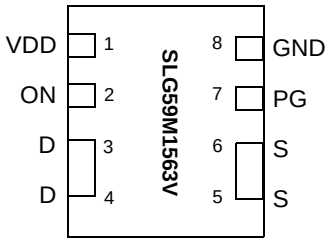
General Description

The SLG59M1563V is a 22.5 mΩ 2.5 A single-channel load switch that is able to switch 1 to 5 V power rails. The product is packaged in an ultra-small 1.0 x 1.6 mm package.

Features

- 1.0 x 1.6 x 0.55 mm STDFN 8L package (2 fused pins for drain and 2 fused pins for source)
- Logic level ON pin capable of supporting 0.85 V CMOS Logic
- 22.5 mΩ RDS_{ON}while supporting 2.5 A
- Power Good Output
- Pb-Free / Halogen-Free / RoHS compliant
- Operating Temperature: -40 °C to 85°C
- Operating Voltage: 1.5 V to 5.5 V

Pin Configuration

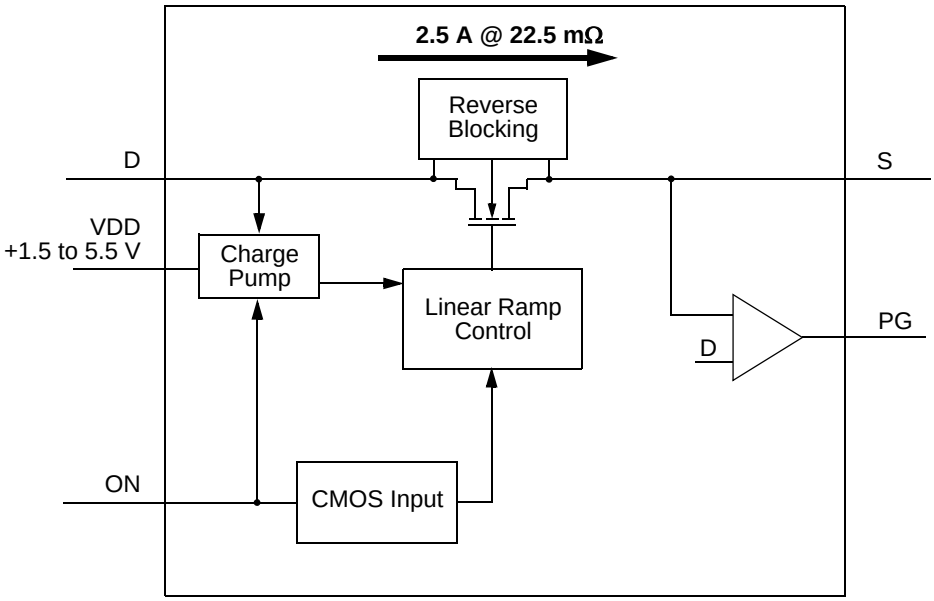


8-pin STDFN
(Top View)

Applications

- Notebook Power Rail Switching
- Tablet Power Rail Switching
- Smartphone Power Rail Switching

Block Diagram



Pin Description

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	V_{DD} power for load switch control (1.5 V to 5.5 V)
2	ON	Input	Turns MOSFET ON (4 MΩ pull down resistor) CMOS input with V_{IL} < 0.3 V, V_{IH} > 0.85 V
3	D	MOSFET	Drain of Power MOSFET (fused with pin 4)
4	D	MOSFET	Drain of Power MOSFET (fused with pin 3)
5	S	MOSFET	Source of Power MOSFET (fused with pin 6)
6	S	MOSFET	Source of Power MOSFET (fused with pin 5)
7	PG	Output	Power Good Output. Active High. Pin drives HIGH when V_{OUT} > 95% V_{IN}
8	GND	GND	Ground

Ordering Information

Part Number	Type	Production Flow
SLG59M1563V	STDFN 8L	Industrial, -40 °C to 85 °C
SLG59M1563VTR	STDFN 8L (Tape and Reel)	Industrial, -40 °C to 85 °C

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply		--	--	7	V
T_S	Storage Temperature		-65	--	150	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	--	--	V
W_{DIS}	Package Power Dissipation		--	--	0.4	W
MOSFET IDS_{PK}	Peak Current from Drain to Source	For no more than 1 ms with 1% duty cycle	--	--	3.5	A

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

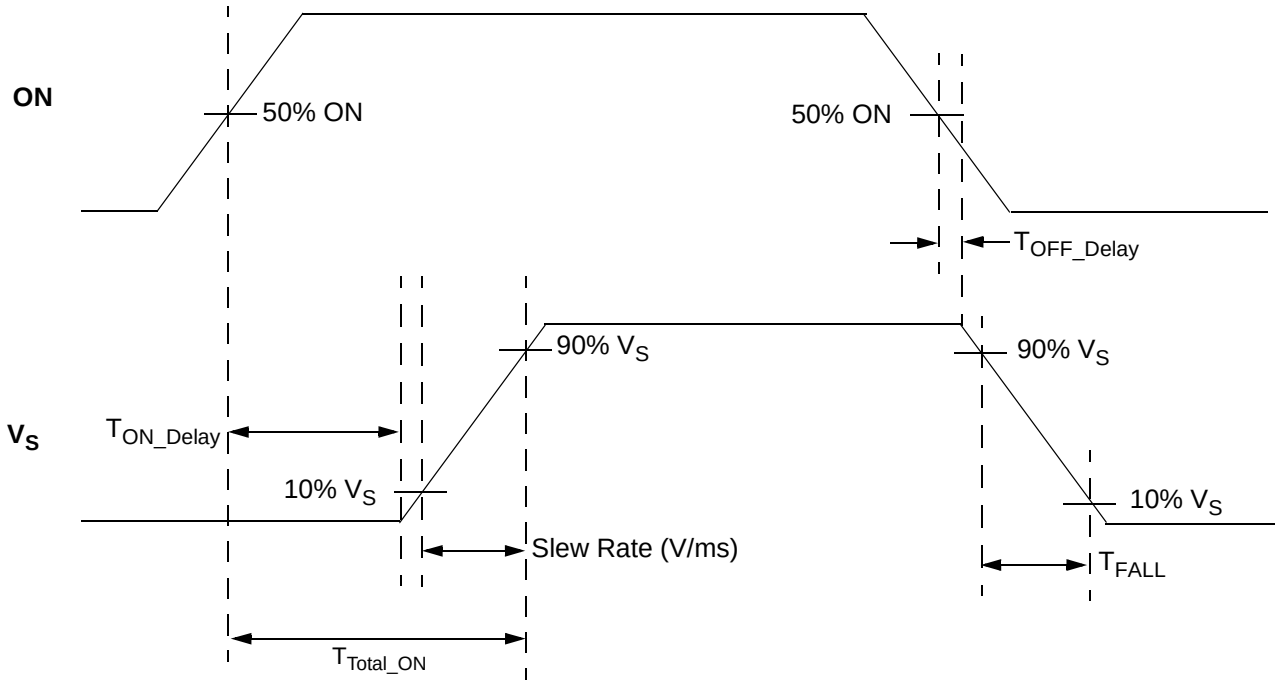
Electrical Characteristics

T_A = -40 °C to 85 °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage	-40 °C to 85 °C	1.5	--	5.5	V
I_{DD}	Power Supply Current (PIN 1)	when OFF	--	--	1	µA
		when ON, No load	--	14	30	µA
RDS_{ON}	Static Drain to Source ON Resistance	T_A 25°C @ 100 mA	--	22.5	25	mΩ
		T_A 70°C @ 100 mA	--	25.6	30	mΩ
		T_A 85°C @ 100 mA	--	25.6	30	mΩ
IDS	Operating Current	V_D = 1.0 V to 5.5 V	--	--	2.5	A
ISD_{LKG}	ISD Leakage (Reverse Blocking Enabled)	V_S = 1. 0 V to 5.5 V, V_D = 0 V, V_{DD} = 0 V, @ 25°C; ON = 0 V	--	0.29	0.50	µA
		V_S = 1. 0 V to 5.5 V, V_D = 0 V, V_{DD} = 0 V, @ 85°C; ON = 0 V	--	0.85	1.30	µA
		V_S = 1. 0 V to 5.5 V, V_D = 0 V, V_{DD} = 0 V, @ -40°C; ON = 0 V	--	3.35	5.00	µA
V_D	Drain Voltage		1.0	--	V_{DD}	V
T_{ON_Delay}	ON pin Delay Time	50% ON to Ramp Begin	0	300	500	µs
T_{Total_ON}	Total Turn On Time	Example: V_{DD} = V_D = 5 V, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω	2.1	2.6	3.1	ms
$T_{SLEWRATE}$	Slew Rate	Example: V_{DD} = V_D = 5 V, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω	1.4	1.95	2.2	V/ms
C_{LOAD}	Output Load Capacitance	C_{LOAD} connected from V_S to GND	--	--	500	µF
ON_V_{IH}	High Input Voltage on ON pin		0.85	--	V_{DD}	V
ON_V_{IL}	Low Input Voltage on ON pin		-0.3	0	0.3	V
V_{OL}	High Output Voltage on PG pin	V_{DD} = 5 V, I_{OL} = -0.1 mA	--	--	0.4	V
V_{OH}	High Output Voltage on PG pin	V_{DD} = 5 V, I_{OH} = 0.1 mA	V_{DD}-0.4	--	V_{DD}	V
$THERM_{ON}$	Thermal shutoff turn-on temperature		--	125	--	°C
$THERM_{OFF}$	Thermal shutoff turn-off temperature		--	100	--	°C
$THERM_{TIME}$	Thermal shutoff time		--	--	1	ms
T_{OFF_Delay}	OFF Delay Time	50% ON to V_S Fall, V_{DD} = V_D = 5 V	--	8	--	µs
$PG_{TRIGGER}$	Power Good Trigger Level	V_{OUT} % of V_{IN}	--	92	--	%

Notes:
1. Refer to table for configuration details.

T_{Total_ON}, T_{ON_Delay} and Slew Rate Measurement



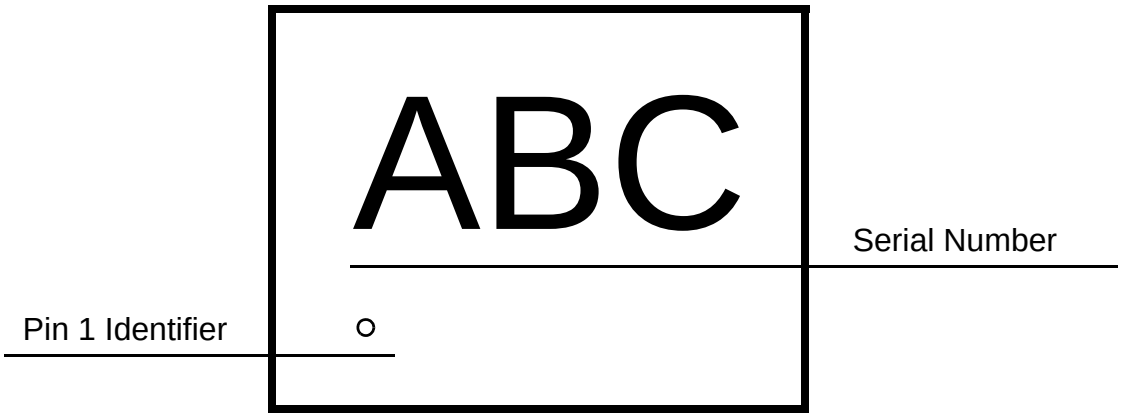
SLG59M1563V Power-Up/Power-Down Sequence Considerations

To ensure glitch-free power-up under all conditions, apply V_{DD} first, followed by V_D after V_{DD} exceeds 1 V. Then allow V_D to reach 90% of its max value before toggling the ON pin from Low-to-High. Likewise, power-down in reverse order.

If V_{DD} and V_D need to be powered up simultaneously, glitching can be minimized by having a suitable load capacitor. A 10 µF C_{LOAD} will prevent glitches for rise times of V_{DD} and V_D less than 2 ms.

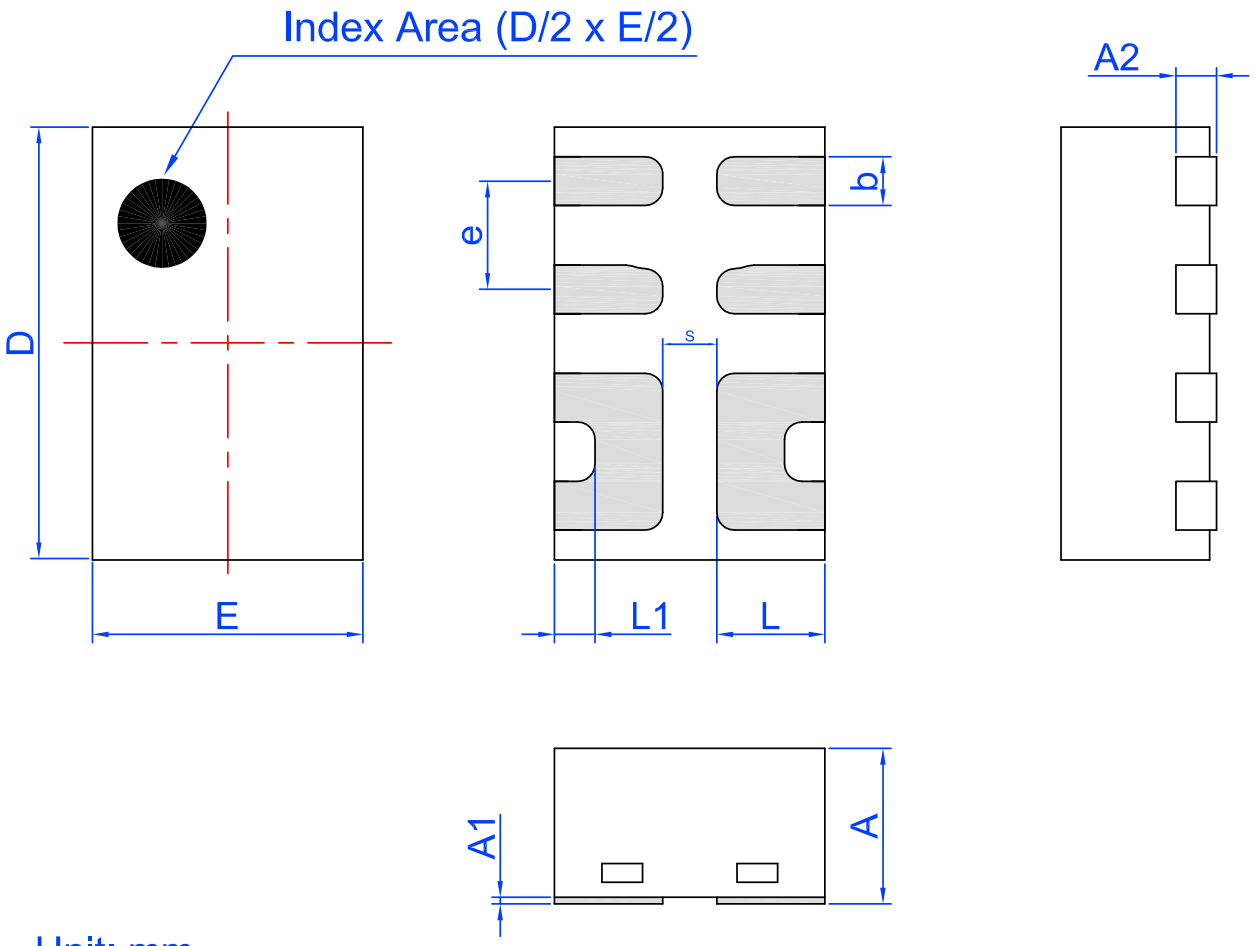
If the ON pin is toggled HIGH before V_{DD} and V_D have reached their steady-state values, the IPS timing parameters may differ from datasheet specifications.

Package Top Marking System Definition



Package Drawing and Dimensions

8 Lead STDFN Package 1.0 x 1.6 mm (Fused Lead)
IC Net Weight: 0.0025 g



Unit: mm

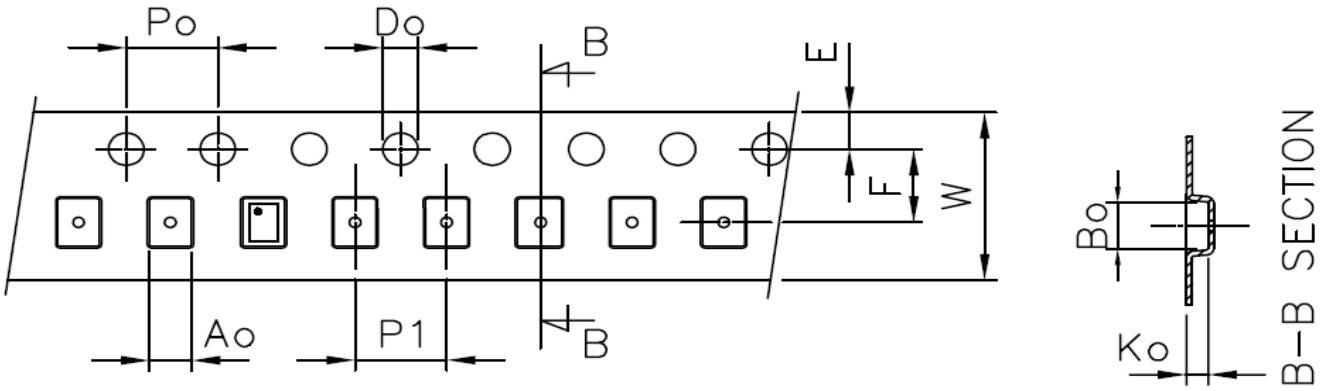
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.55	1.60	1.65
A1	0.005	-	0.060	E	0.95	1.00	1.05
A2	0.10	0.15	0.20	L	0.35	0.40	0.45
b	0.13	0.18	0.23	L1	0.10	0.15	0.20
e	0.40 BSC			S	0.2 REF		

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STDFN 8L 1x1.6mm 0.4P FC Green	8	1.0 x 1.6 x 0.55	3,000	3,000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STDFN 8L 1x1.6mm 0.4P FC Green	1.12	1.72	0.7	4	4	1.55	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.88 mm^3 (nominal). More information can be found at www.jedec.org.

Revision History

Date	Version	Change
9/13/2016	1.02	Added Power Up/Down Sequencing Considerations Updated text and parameter names for clarity
3/9/2016	1.01	Updated IDSlkg conditions