



An Ultra-small 3 mm², 8.4 mΩ, 4 A, 125°C-Rated Internally-protected Integrated Power Switch

General Description

The SLG59M1657V is a high performance 8.4 mΩ, 4 A single-channel nFET integrated power switch which can operate with a 2.5 V to 5.5 V V_{DD} supply to switch power rails from as low as 0.9 V up to the supply voltage. The SLG59M1657V incorporates two-level overload current protection, thermal shutdown protection, and in-rush current control which can easily be adjusted by a small external capacitor.

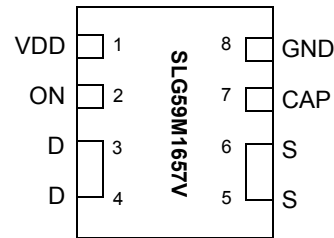
Using a proprietary MOSFET design, the SLG59M1657V achieves a stable 8.4 mΩ RDS_{ON} across a wide input voltage range. In addition, the SLG59M1657V's package also exhibits low thermal resistance for high-current operation using Silego's proprietary CuFET technology.

Fully specified over the -40 °C to 125 °C temperature range, the SLG59M1657V is packaged in a space-efficient, low thermal resistance, RoHS-compliant 1.5 mm x 2.0 mm STDFN package.

Features

- 1.5 x 2.0 mm FC-TDFN 8L package (2 fused pins for drain and 2 fused pins for source)
- Logic level ON pin capable of supporting 0.9 V CMOS Logic
- User selectable ramp rate with external capacitor
- 8.4 mΩ RDS_{ON} while supporting 4 A
- Two Over Current Protection Modes
 - Short Circuit Current Limit
 - Active Current Limit
- Over Temperature Protection
- Pb-Free / Halogen-Free / RoHS compliant
- Operating Temperature: -40 °C to 125°C
- Operating Voltage: 2.5 V to 5.5 V

Pin Configuration

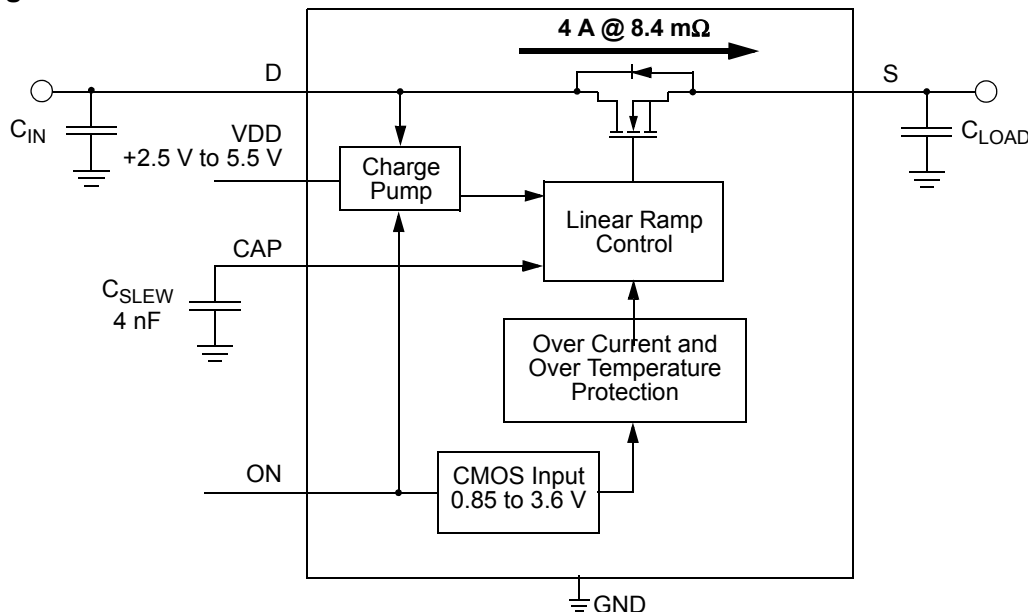


8-pin FC-TDFN
(Top View)

Applications

- Notebook Power Rail Switching
- Tablet Power Rail Switching
- Smartphone Power Rail Switching

Block Diagram





Pin Description

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	With an internal 1.8 V UVLO threshold, VDD supplies the power for the operation of the power switch and internal control circuitry. Bypass the VDD pin to GND with a 0.1 μ F (or larger) capacitor.
2	ON	Input	A low-to-high transition on this pin initiates the operation of the SLG59M1657V's state machine. ON is a CMOS input with $V_{IL} < 0.25$ V and $V_{IH} > 0.85$ V thresholds. While there is an internal pull-down circuit to GND (~ 4 M Ω), connect this pin directly to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller. Do not allow this pin to be open-circuited.
3, 4	D	MOSFET	Drain terminal connection of the n-channel MOSFET (2 pins fused for V_D). Connect at least a low-ESR 0.1 μ F capacitor from this pin to ground. Capacitors used at V_D should be rated at 10 V or higher.
5, 6	S	MOSFET	Source terminal connection of the n-channel MOSFET (2 pins fused for V_S). Connect a low-ESR capacitor from this pin to ground and consult the Electrical Characteristics table for recommended C_{LOAD} range. Capacitors used at V_S should be rated at 10 V or higher.
7	CAP	Input	A low-ESR, stable dielectric, ceramic surface-mount capacitor connected from CAP pin to GND sets the V_S slew rate and overall turn-on time of the SLG59M1657V. For best performance C_{SLEW} value should be ≥ 1.5 nF and voltage level should be rated at 10 V or higher.
8	GND	GND	Ground connection. Connect this pin to system analog or power ground plane.

Ordering Information

Part Number	Type	Production Flow
SLG59M1657V	FC-TDFN 8L	Extended Industrial, -40 °C to 125 °C
SLG59M1657VTR	FC-TDFN 8L (Tape and Reel)	Extended Industrial, -40 °C to 125 °C



Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V _{DD}	Power Supply		--	--	7	V
V _D to GND	Power Switch Input Voltage to GND		-0.3	--	7	V
V _S to GND	Power Switch Output Voltage to GND		-0.3	--	V _D	V
ON and CAP to GND	ON and CAP Pin Voltages to GND		-0.3	--	7	V
T _O	Operating Temperature		-40	--	125	°C
T _S	Storage Temperature		-65	--	150	°C
T _A	Rated Operating Temperature		-40	--	125	°C
ESD _{HBM}	ESD Protection	Human Body Model	2000	--	--	V
ESD _{CDM}	ESD Protection	Charged Device Model	1000	--	--	V
MSL	Moisture Sensitivity Level		1			
θ _{JA}	Thermal Resistance	1.5 x 2 mm, 8L TDFN; Determined using 1 in ² , 1 oz. copper pads under each VD and VS terminals and FR4 pcb material	--	69	--	°C/W
W _{DIS}	Package Power Dissipation		--	--	1	W
MOSFET IDS	Max Continuous Switch Current		--	--	4	A
MOSFET IDS _{PK}	Peak Current from Drain to Source	For no more than 1 ms with 1% duty cycle	--	--	4.5	A

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

T_A = -40 to 125 °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V _{DD}	Power Supply Voltage	-40 to 125°C	2.5	--	5.5	V
V _{DD_UVLO}	V _{DD} Undervoltage Lockout Threshold	V _{DD} ↑	--	1.8	--	V
I _{DD}	Power Supply Current	when OFF; T _A = 70 °C; V _S = 0 V; V _D = V _{DD} = 5.5 V	--	--	1	μA
		when OFF; T _A = 85 °C; V _S = 0 V; V _D = V _{DD} = 5.5 V	--	--	1	μA
		when OFF; T _A = 125 °C; V _S = 0 V; V _D = V _{DD} = 5.5 V	--	--	1.5	μA
		when ON, no Load	--	70	120	μA
RDS _{ON}	ON Resistance	T _A 25°C @ 100 mA	--	8.4	10	mΩ
		T _A 85°C @ 100 mA	--	10	12	mΩ
		T _A 125°C @ 100 mA	--	12	14.4	mΩ
V _D	Drain Voltage		0.9	--	V _{DD}	V

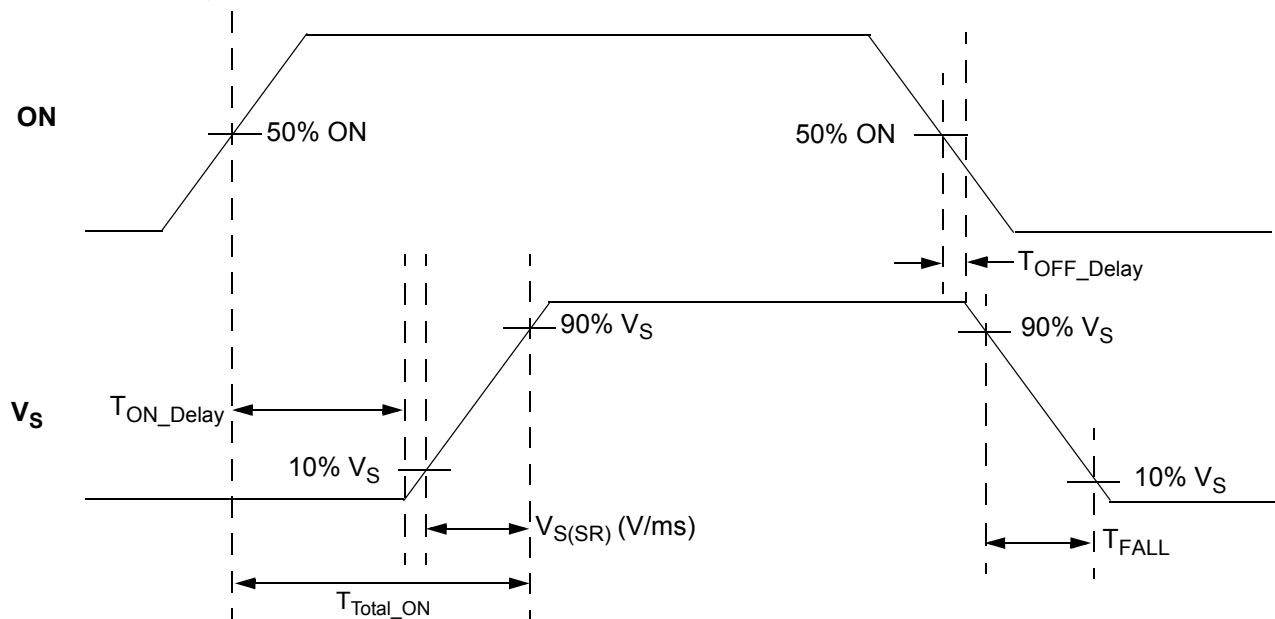


Electrical Characteristics (continued)

T_A = -40 to 125 °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I _{FET_OFF}	MOSFET OFF Leakage Current	V _D = V _{DD} = 5.5 V; V _S = 0 V; ON = 0 V; T _A = 70°C	--	--	1	μA
		V _D = V _{DD} = 5.5 V; V _S = 0 V; ON = 0 V; T _A = 85°C	--	--	1	μA
		V _D = V _{DD} = 5.5 V; V _S = 0 V; ON = 0 V; T _A = 125°C	--	--	20	μA
V _{S(SR)}	Slew Rate	C _{SLEW} = 4 nF, V _{DD} = V _D = 5 V, C _{LOAD} = 10 μF, R _{LOAD} = 20 Ω	--	3	--	V/ms
T _{ON_Delay}	ON pin Delay Time	50% ON to Ramp Begin	--	200	--	μs
T _{OFF_Delay}	OFF Delay Time	50% ON to V _S Fall Start, V _{DD} = V _D = 5 V, no C _{LOAD} , R _{LOAD} = 20 Ω	--	22	--	μs
T _{FALL}	V _S Fall Time	90% V _S to 10% V _S , V _{DD} = V _D = 5 V, no C _{LOAD} , R _{LOAD} = 20 Ω	--	10	--	μs
C _{LOAD}	Output Capacitive Load to GND		--	--	500	μF
ON_V _{IH}	High Input Voltage on ON pin		0.85	--	V _{DD}	V
ON_V _{IL}	Low Input Voltage on ON pin		-0.3	0	0.25	V
I _{LIMIT}	Active Current Limit (I _{ACL})	MOSFET will automatically limit current when V _S > 250 mV	--	6.0	--	A
	Short Circuit Current Limit (I _{SCL})	MOSFET will automatically limit current when V _S < 250 mV	--	0.5	--	A
THERM _{ON}	Thermal shutoff turn-on temperature		--	150	--	°C
THERM _{OFF}	Thermal shutoff turn-off temperature		--	130	--	°C
THERM _{TIME}	Thermal shutoff time		--	--	1	ms

T_{Total_ON}, T_{ON_Delay} and Slew Rate Measurement

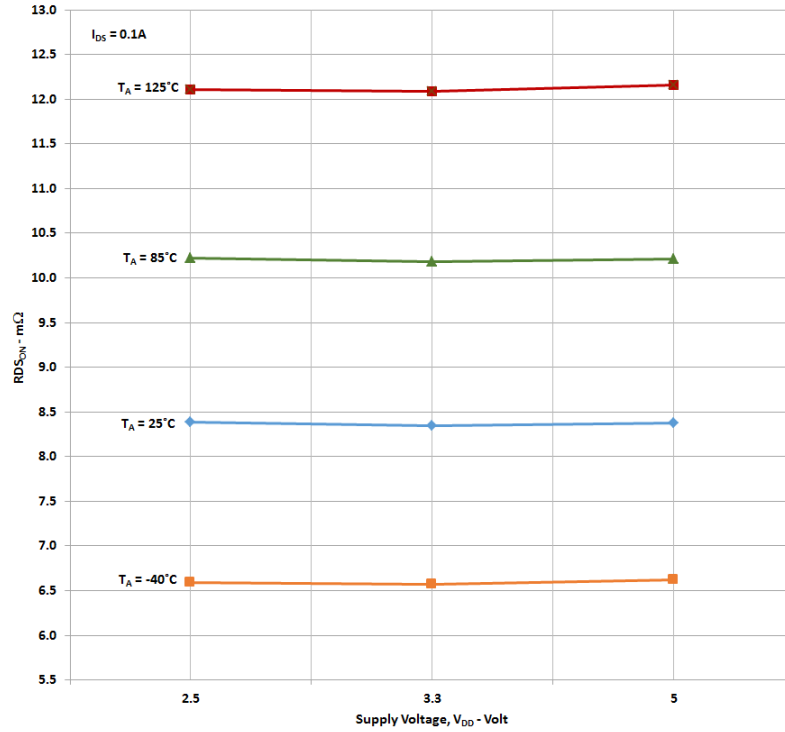


Note: Rise and Fall times of the ON signal are 100 ns

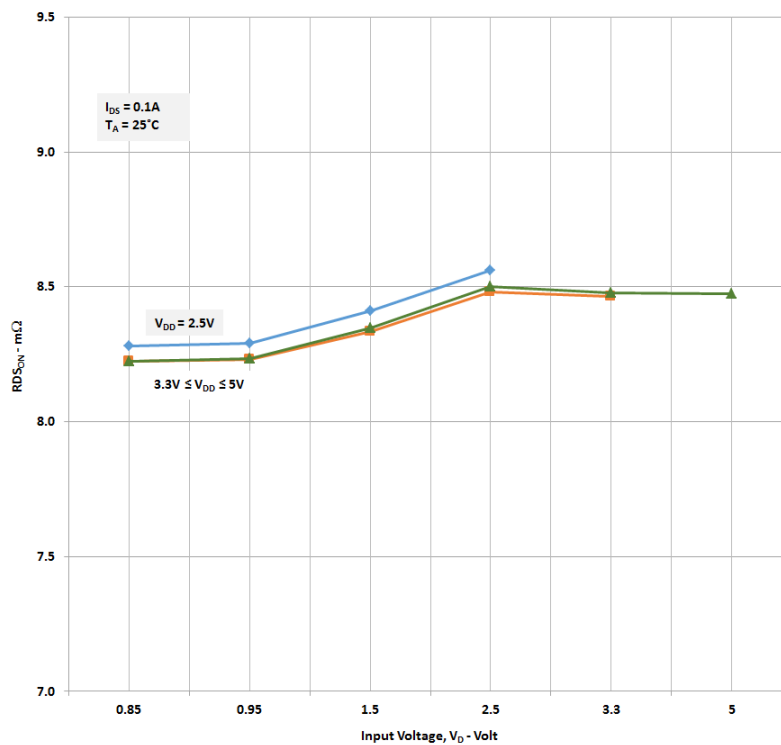


Typical Performance Characteristics

$R_{DS(ON)}$ vs. V_{DD} , and Temperature

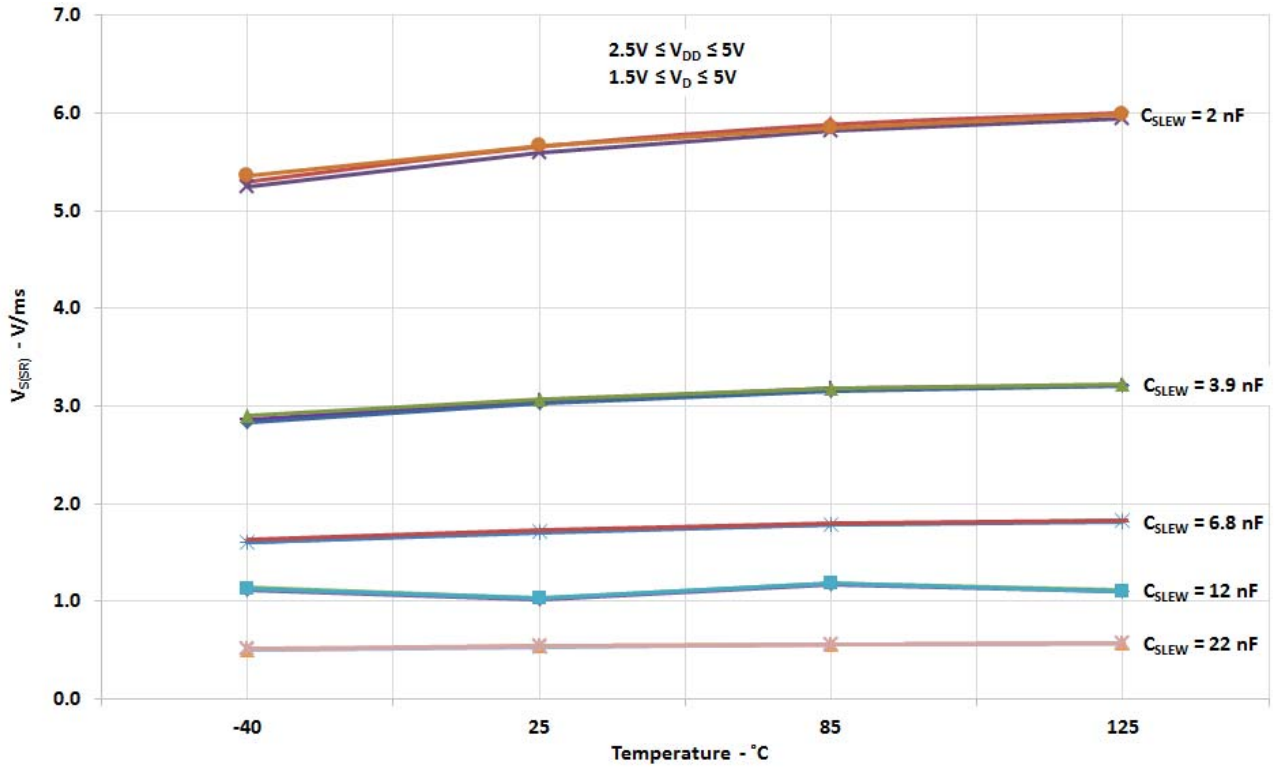


$R_{DS(ON)}$ vs. V_D and V_{DD}

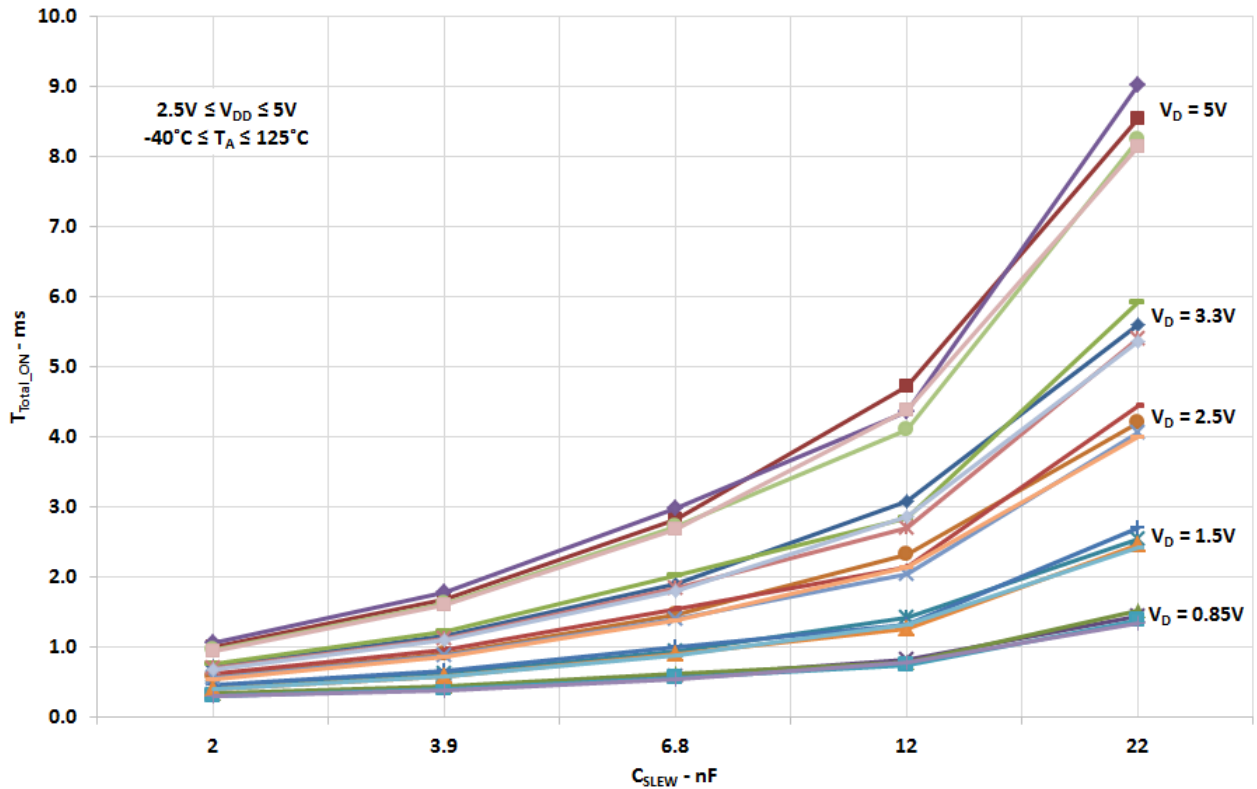




$V_{S(SR)}$ vs. Temperature, V_D , V_{DD} , and C_{SLEW}



$T_{Total\ ON}$ vs. C_{SLEW} , V_D , V_{DD} , and Temperature





Typical Operation Waveforms

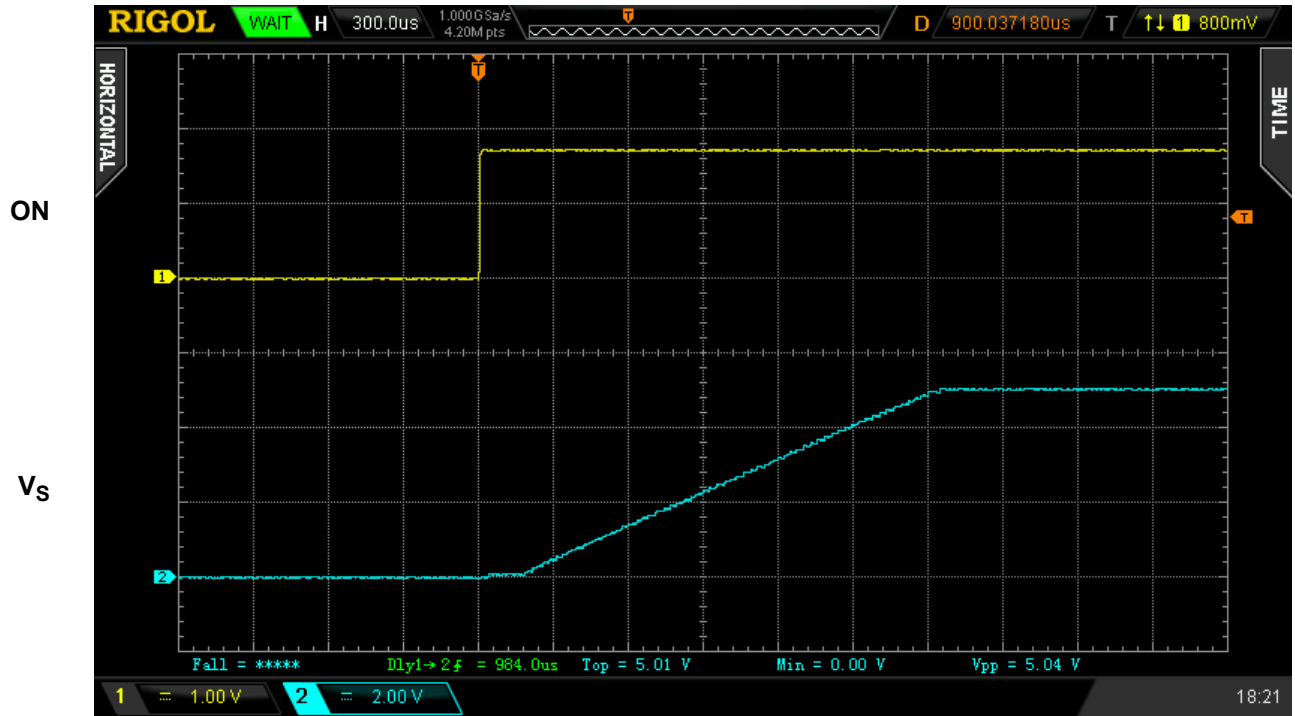


Figure 1. Typical Turn ON operation waveform for $V_{DD} = V_D = 5\text{ V}$, $C_{SLEW} = 4\text{ nF}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 20\text{ }\Omega$

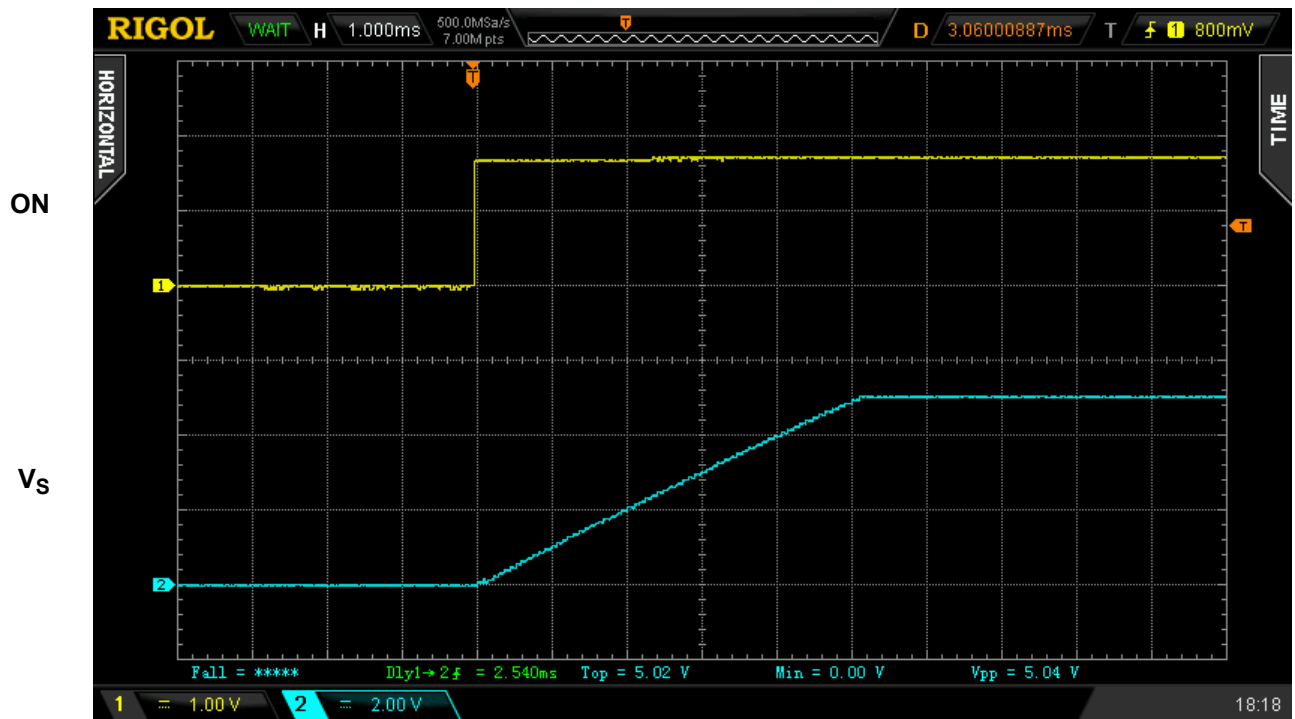


Figure 2. Typical Turn ON operation waveform for $V_{DD} = V_D = 5\text{ V}$, $C_{SLEW} = 12\text{ nF}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 20\text{ }\Omega$

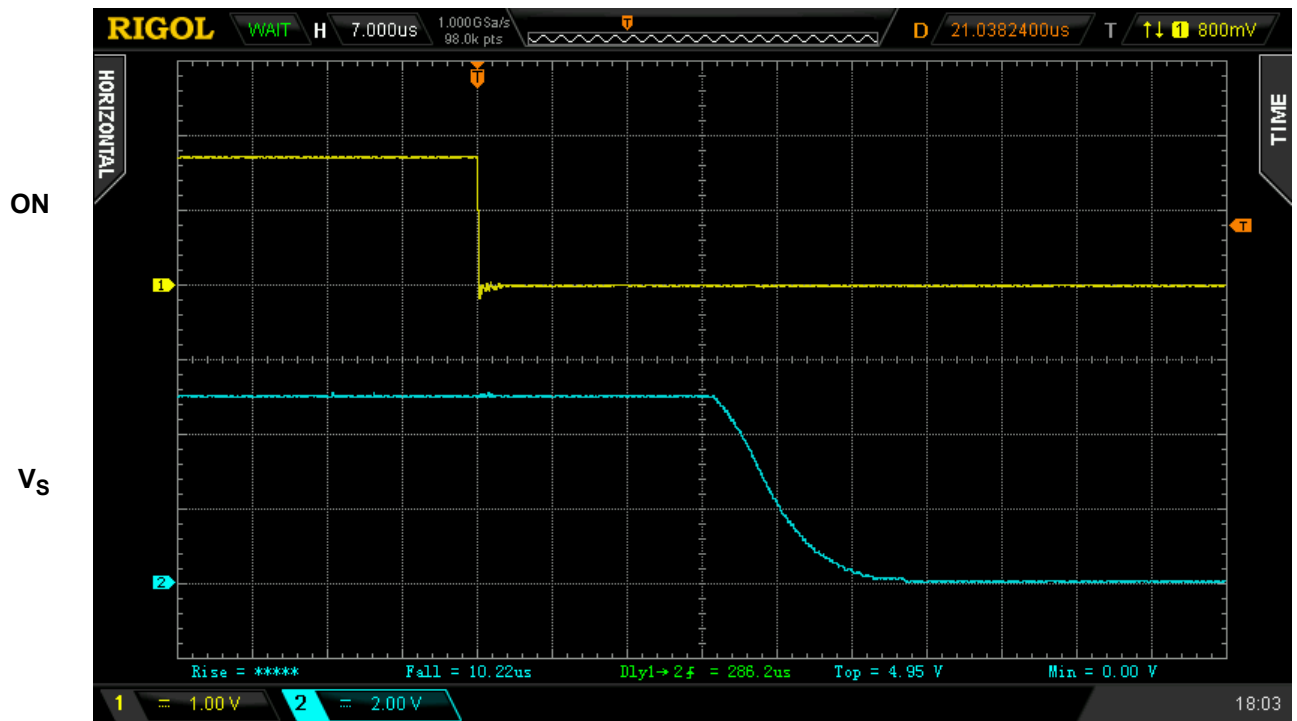


Figure 3. Typical Turn OFF operation waveform for $V_{DD} = V_D = 5\text{ V}$, $C_{SLEW} = 4\text{ nF}$, no C_{LOAD} , $R_{LOAD} = 20\ \Omega$

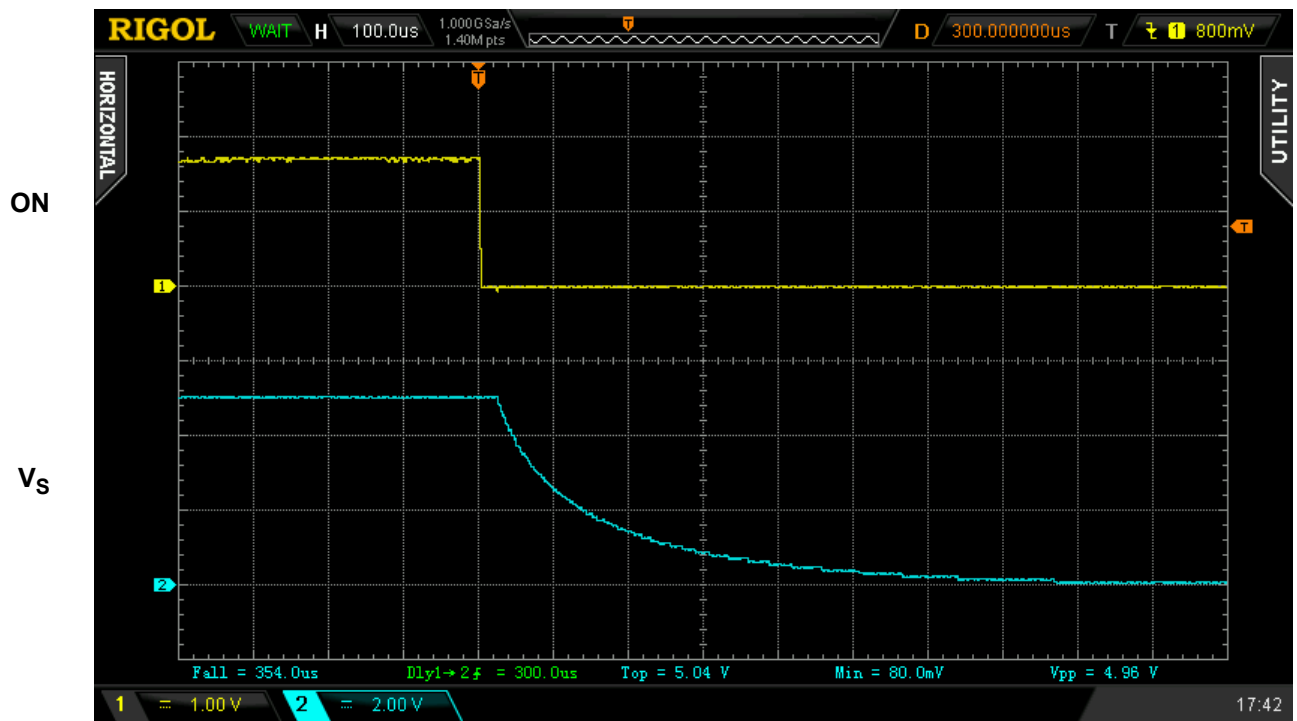


Figure 4. Typical Turn OFF operation waveform for $V_{DD} = V_D = 5\text{ V}$, $C_{SLEW} = 4\text{ nF}$, $C_{LOAD} = 10\ \mu\text{F}$, $R_{LOAD} = 20\ \Omega$



SLG59M1657V Power-Up/Power-Down Sequence Considerations

A nominal power-up sequence is to apply V_{DD} first, followed by V_D only after V_{DD} is > 1 V, and finally toggling the ON pin LOW-to-HIGH after V_D is at least 90% of its final value.

A nominal power-down sequence is the power-up sequence in reverse order. It is important that the SLG59M1657V's ON pin is toggled HIGH only after V_{DD} and V_D have reached their steady-state values; otherwise, the power switch will spend an undesirable amount of time in high-resistance mode while powering up, heating up, and possibly reaching its thermal shutdown before ever fully turning on.

If V_{DD} and V_D are applied at the same time, a voltage glitch may appear on the output pin at V_S . To prevent glitches at the output, it is recommended to connect a 10 μ F capacitor from the V_S pin to GND and to keep the V_{DD} & V_D ramp times less than 2 ms.

The V_S output follows a linear ramp when the power switch is turned on, provided that the V_S slew time set by C_{SLEW} is less than the RC time constant formed by the $R_{DS_{ON}}$ of the power switch and load capacitance C_{LOAD} .

SLG59M1657V Current Limiting Operation

The SLG59M1657V has two types of current limiting triggered by the output V_S pin voltage.

1. Standard Current Limiting Mode (with Thermal Shutdown Protection)

When the V_S pin voltage > 250 mV, the output current is initially limited to the Active Current Limit (I_{ACL}) specification listed in the Electrical Characteristics table. The ACL monitor's response time is very fast and is triggered within a few microseconds to sudden (transient) changes in load current. When a load current overload is detected, the ACL monitor increases the FET resistance to keep the current from exceeding the power switch's I_{ACL} threshold.

However, if a load-current overload condition persists where the die temperature rises because of the increased FET resistance, the power switch's internal Thermal Shutdown Protection circuit can be activated. If the die temperature exceeds the listed $THERM_{ON}$ specification, the FET is shut OFF completely, thereby allowing the die to cool. When the die cools to the listed $THERM_{OFF}$ temperature threshold, the FET is allowed to turn back on. This process may repeat as long as the output current overload condition persists.

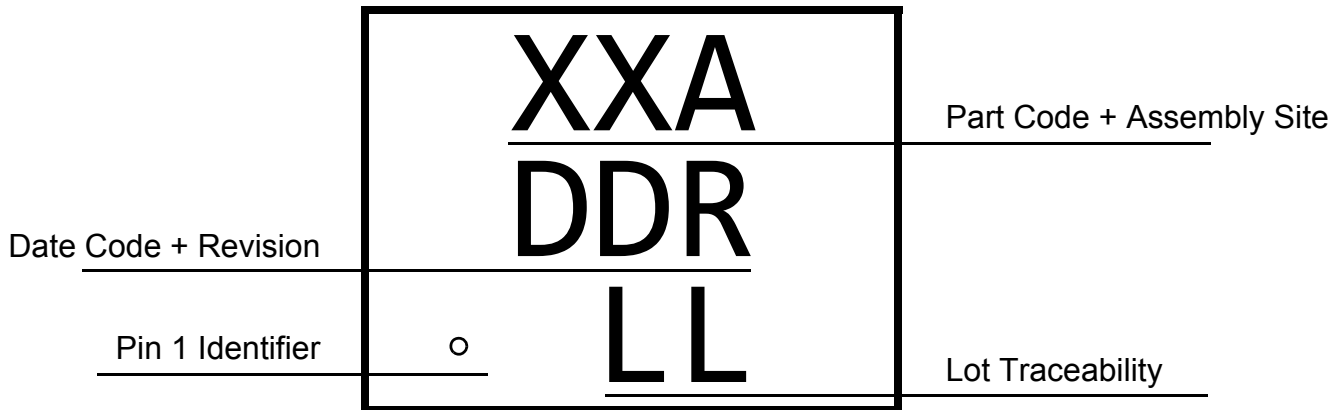
2. Short Circuit Current Limiting Mode (with Thermal Shutdown Protection)

When the V_S pin voltage < 250 mV (which is the case with a hard short, such as a solder bridge on the power rail), the power switch's internal Short-circuit Current Limit (SCL) monitor limits the FET current to approximately 500 mA (the I_{SCL} threshold). While the internal Thermal Shutdown Protection circuit remains enabled and since the I_{SCL} threshold is much lower than the I_{ACL} threshold, thermal shutdown protection may become activated only at higher ambient temperatures.

For more information on Silego GreenFET3 integrated power switch features, please visit our [Application Notes](#) page at our website and see [App Note "AN-1068 GreenFET3 Integrated Power Switch Basics"](#).



Package Top Marking System Definition



- XX - Part Code Field¹
- A - Assembly Site Code Field²
- DD - Date Code Field¹
- R - Part Revision Code Field²
- LL - Lot Traceability Field¹

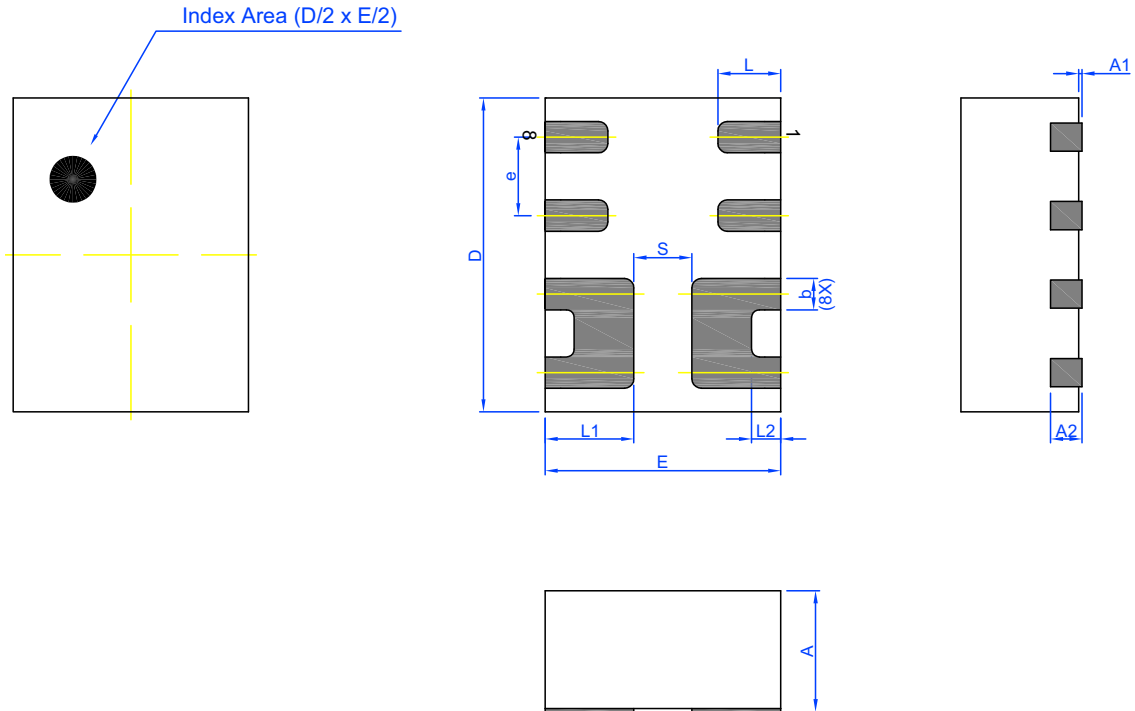
Note 1: Each character in code field can be alphanumeric A-Z and 0-9

Note 2: Character in code field can be alphabetic A-Z



Package Drawing and Dimensions

8 Lead TDFN Package 1.5 x 2.0 mm (Fused Lead)
JEDEC MO-252



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.70	0.75	0.80	L	0.35	0.40	0.45
A1	0.005	-	0.060	L1	0.515	0.565	0.615
A2	0.15	0.20	0.25	L2	0.135	0.185	0.235
b	0.15	0.20	0.25	e	0.50 BSC		
D	1.95	2.00	2.05	S	0.37 REF		
E	1.45	1.50	1.55				

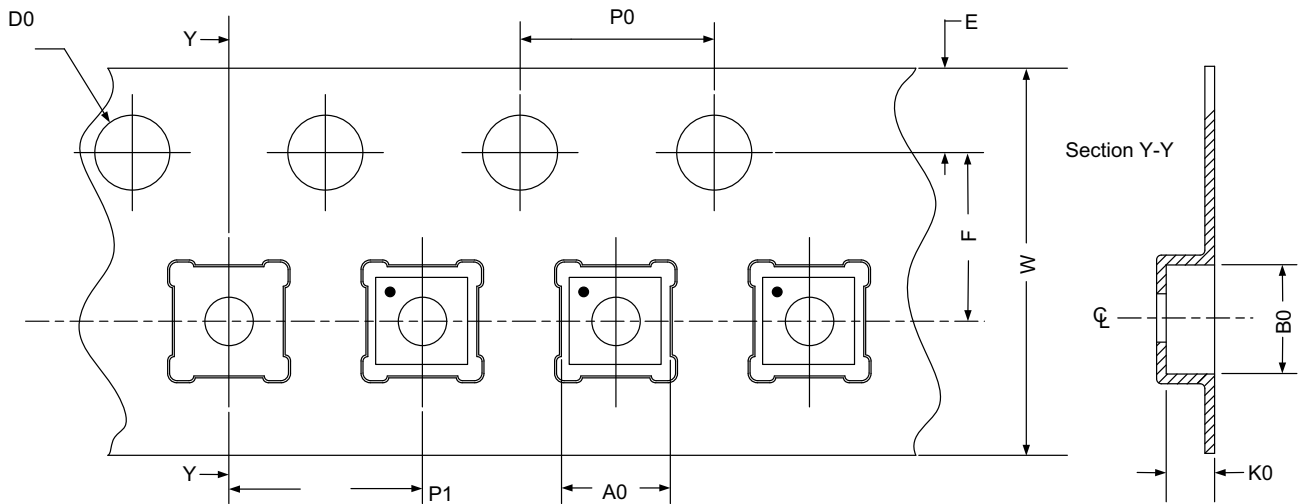


Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
TDFN 8L FC Green	8	1.5 x 2.0 x 0.75	3000	3000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
TDFN 8L FC Green	1.68	2.18	0.9	4	4	1.5	1.75	3.5	8



Refer to EIA-481 specification

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.25 mm³ (nominal). More information can be found at www.jedec.org.



Revision History

Date	Version	Change
2/23/2017	1.00	Production Release