SLG59M1693C

A 2 V, 17.4 mΩ, 1.0 A pFET Integrated Power Switch with Discharge in a 0.56 mm² WLCSP

General Description

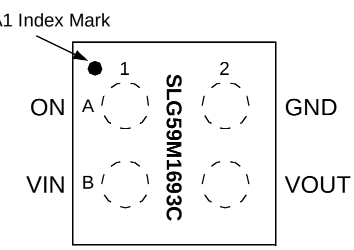
Operating from a 0.8 V to 2.0 V power supply, the SLG59M1693C is a self-powered, high-performance 17.4 mΩ, 1.0 A single-channel pFET integrated power switch. The SLG59M1693C's low supply current makes it an ideal pFET integrated power switch in small form-factor personal health monitor and watch applications.

Using a proprietary MOSFET design, the SLG59M1693C achieves a low RDS_{ON} across the entire input voltage range. Through the application of Silego's proprietary CuFET technology, the SLG59M1693C can be used in applications up to 1 A with a very-small 0.56 mm^2 WLCSP form factor.

Features

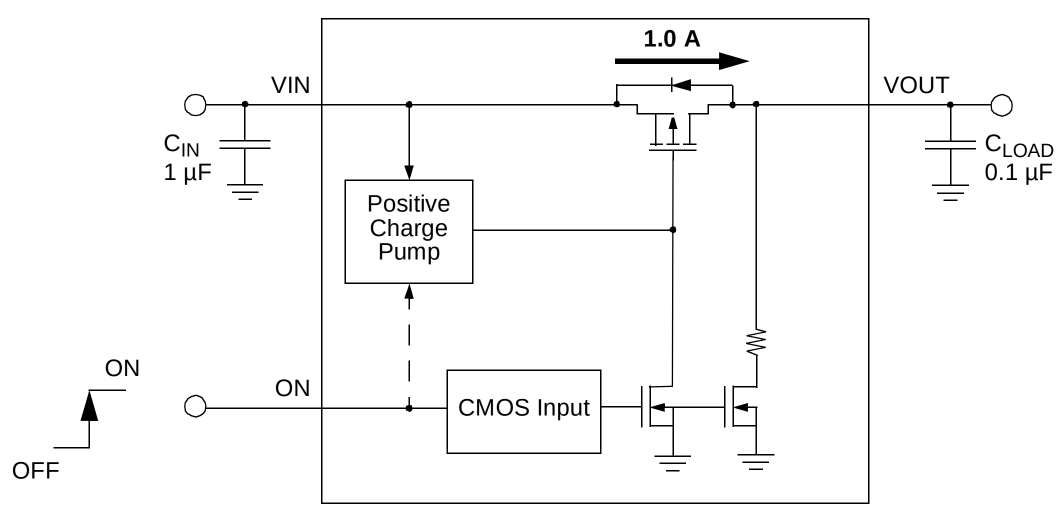
- Integrated 1 A Continuous I_{DS} pFET Power Switch
- Low Typical RDS_{ON}:
  - 17.4 mΩ at V_{IN} = 2.0 V
  - 40 mΩ at V_{IN} = 0.8 V
- Input Voltage: 0.8 V to 2.0 V
- Low Typical No-load Supply Current
  - When ON: 5.5 nA
  - When OFF: 0.83 µA
- Integrated V_{OUT} Discharge Resistor
- Operating Temperature: -40 °C to 85 °C
- Low θ_{JA}, 4-pin 0.75 mm x 0.75 mm, 0.4 mm pitch 4L WLCSP Packaging
  - Pb-Free / Halogen-Free / RoHS compliant

Pin Configuration



4L WLCSP
(Laser Marking View)

Block Diagram



Pin Description

Pin #	Pin Name	Type	Pin Description
A1	ON	Input	A low-to-high transition on this pin initiates the operation of the SLG59M1693C. ON is an asserted HIGH, level-sensitive CMOS input with V_{IL} < 0.3 V and V_{IH} > 0.85 V. As the ON pin input circuit does not have an internal pull-down resistor, connect this pin to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller – do not allow this pin to be open-circuited.
B1	VIN	MOSFET	Input terminal connection of the p-channel MOSFET. Connect a 1 µF (or larger) low-ESR capacitor from this pin to ground.
B2	VOUT	MOSFET	Output terminal connection of the p-channel MOSFET.
A2	GND	GND	Ground connection. Connect this pin to system analog or power ground plane.

Ordering Information

Part Number	Type	Production Flow
SLG59M1693C	WLCSP 4L	Industrial, -40 °C to 85 °C
SLG59M1693CTR	WLCSP 4L (Tape and Reel)	Industrial, -40 °C to 85 °C

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Power Switch Input Voltage		--	--	2.5	V
V_{OUT} to GND	Power Switch Output Voltage to GND		-0.3	--	V_{IN}	V
ON to GND	ON Pin Voltage to GND		-0.3	--	V_{IN}	V
T_S	Storage Temperature		-65	--	150	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	--	--	V
ESD_{CDM}	ESD Protection	Charged Device Model	1000	--	--	V
MSL	Moisture Sensitivity Level		1			
θ_{JA}	Package Thermal Resistance, Junction-to-Ambient	0.75 x 0.75 mm 4L WLCSP; Determined using a 1 in^2, 2 oz .copper pad under each VIN and VOUT terminal and FR4 pcb material.	--	110	--	°C/W
W_{DIS}	Package Power Dissipation		--	--	0.5	W
MOSFET IDS_{PK}	Peak Current from VIN to VOUT	Maximum pulsed switch current, pulse width < 1 ms, 1% duty cycle	--	--	1.5	A

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

T_A = -40 °C to 85 °C (unless otherwise stated)

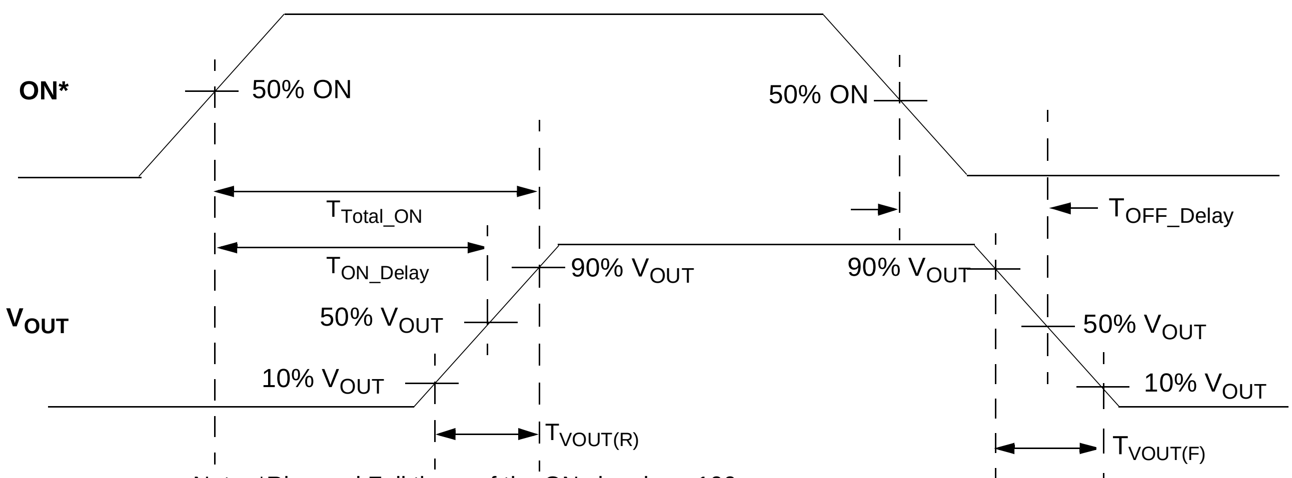
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Power Switch Input Voltage		0.8	--	2.0	V
I_{IN}	Power Switch Current (Pin B1)	When OFF, V_{IN} = 0.8 V, No load	--	0.18	0.39	µA
		When OFF, V_{IN} = 1.2 V, No load	--	0.31	0.54	µA
		When OFF, V_{IN} = 1.5 V, No load	--	0.42	0.70	µA
		When OFF, V_{IN} = 1.8 V, No load	--	0.59	0.99	µA
		When OFF, V_{IN} = 2.0 V, No load	--	0.83	1.34	µA
		ON = 1.8 V, V_{IN} = 0.8 V, No load	--	2.2	226	nA
		ON = 1.8 V, V_{IN} = 1.2 V, No load	--	3.3	266	nA
		ON = 1.8 V, V_{IN} = 1.5 V, No load	--	3.3	301	nA
		ON = 1.8 V, V_{IN} = 1.8 V, No load	--	4.4	312	nA
		ON = 1.8 V, V_{IN} = 2.0 V, No load	--	5.5	335	nA
I_{ON_LKG}	ON Pin Input Leakage		--	--	0.7	µA
RDS_{ON}	ON Resistance @ T_A 25°C	@ 2.0 V, I_{DS} = 100 mA	--	17.4	19.3	mΩ
		@ 0.8 V, I_{DS} = 100 mA	--	40	41.7	mΩ
RDS_{ON}	ON Resistance @ T_A 85°C	@ 2.0 V, I_{DS} = 100 mA	--	20.1	22.5	mΩ
		@ 0.8 V, I_{DS} = 100 mA	--	42.9	44.9	mΩ
MOSFET IDS	Current from VIN to VOUT	Continuous	--	--	1.0	A

Electrical Characteristics (continued)

T_A = -40 °C to 85 °C (unless otherwise stated)

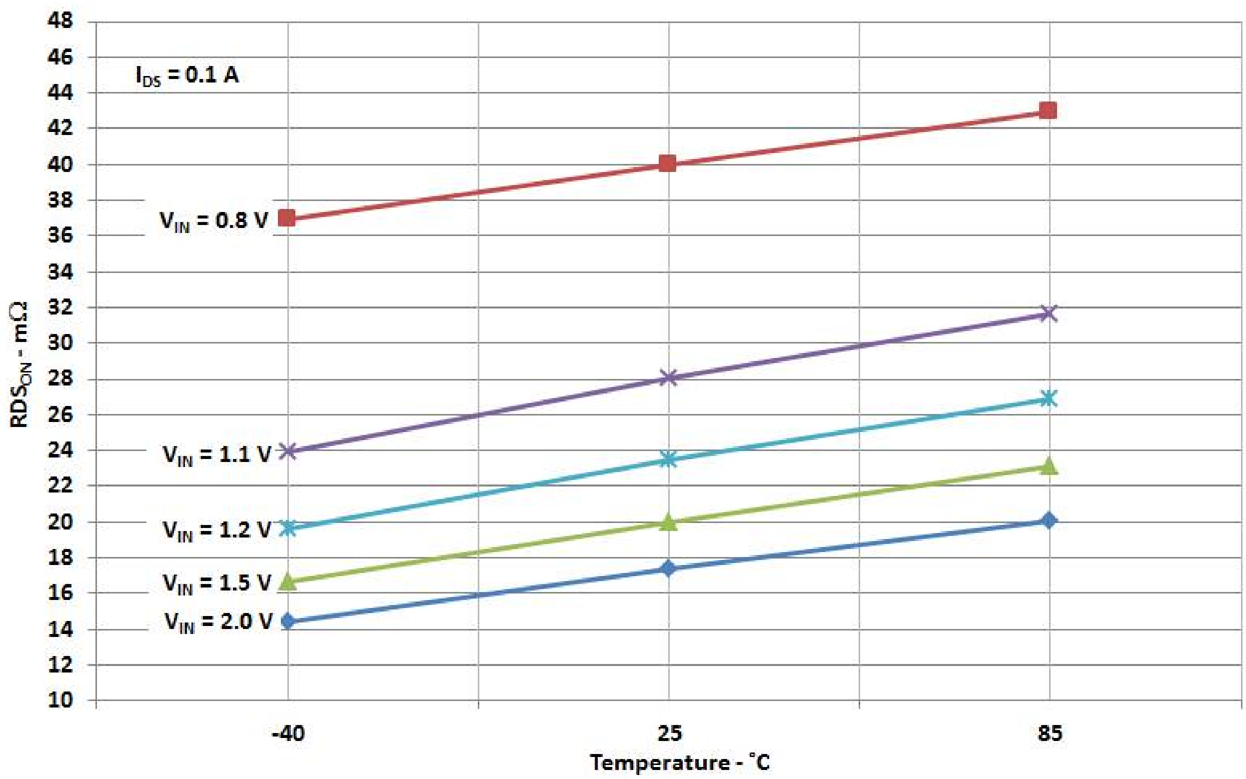
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
$V_{OUT(SR)}$	Slew Rate	10% V_{OUT} to 90% V_{OUT} ↑; V_{IN} = 2.0 V; R_{LOAD} = 10 Ω; C_{LOAD} = 0.1 µF	4	5.9	9.1	V/ms
		10% V_{OUT} to 90% V_{OUT} ↑; V_{IN} = 0.8 V; R_{LOAD} = 10 Ω; C_{LOAD} = 0.1 µF	2.4	3.6	5.3	V/ms
T_{Total_ON}	Total Turn On Time	50% ON to 90% V_{OUT} ↑; V_{IN} = 2.0 V; R_{LOAD} = 10 Ω; C_{LOAD} = 0.1 µF	0.31	0.44	0.66	ms
		50% ON to 90% V_{OUT} ↑ V_{IN} = 0.8 V; R_{LOAD} = 10 Ω; C_{LOAD} = 0.1 µF	0.24	0.36	0.58	ms
T_{ON_Delay}	ON Delay Time	50% ON to 50% V_{OUT} ↑; V_{IN} = 2.0 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	--	0.30	0.47	ms
		50% ON to 50% V_{OUT} ↑; V_{IN} = 0.8 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	--	0.27	0.45	ms
$T_{VOUT(R)}$	V_{OUT} Rise Time	10% to 90% V_{OUT} ↑; V_{IN} = 2.0 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	--	0.27	0.37	ms
		10% to 90% V_{OUT} ↑; V_{IN} = 0.8 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	--	0.18	0.24	ms
$T_{VOUT(F)}$	V_{OUT} Fall Time	90% to 10% V_{OUT} ↓; V_{IN} = 2.0 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	--	11.8	14.9	µs
		90% to 10% V_{OUT} ↓; V_{IN} = 0.8 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	--	11.0	15.9	µs
T_{OFF_Delay}	OFF Delay Time	50% ON to 50% V_{OUT} ↓; V_{IN} = 2.0 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1µF	--	32.8	74.5	µs
		50% ON to 50% V_{OUT} ↓; V_{IN} = 0.8 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	--	23.3	43.9	µs
C_{LOAD}	Output Load Capacitance	C_{LOAD} connected from VOUT to GND	--	--	30	µF
R_{DIS}	Discharge Resistance (ON = LOW)	V_{IN} = 0.8 V, V_{OUT} = 0.4 V Input Bias	121	147	165	Ω
		V_{IN} = 2.0 V, V_{OUT} = 0.4 V Input Bias	52	63	75	Ω
ON_V_{IH}	Initial Turn On Voltage		0.85	--	V_{IN}	V
ON_V_{IL}	Low Input Voltage on ON pin		-0.3	0	0.3	V

T_{Total_ON}, T_{ON_Delay} and Slew Rate Measurement

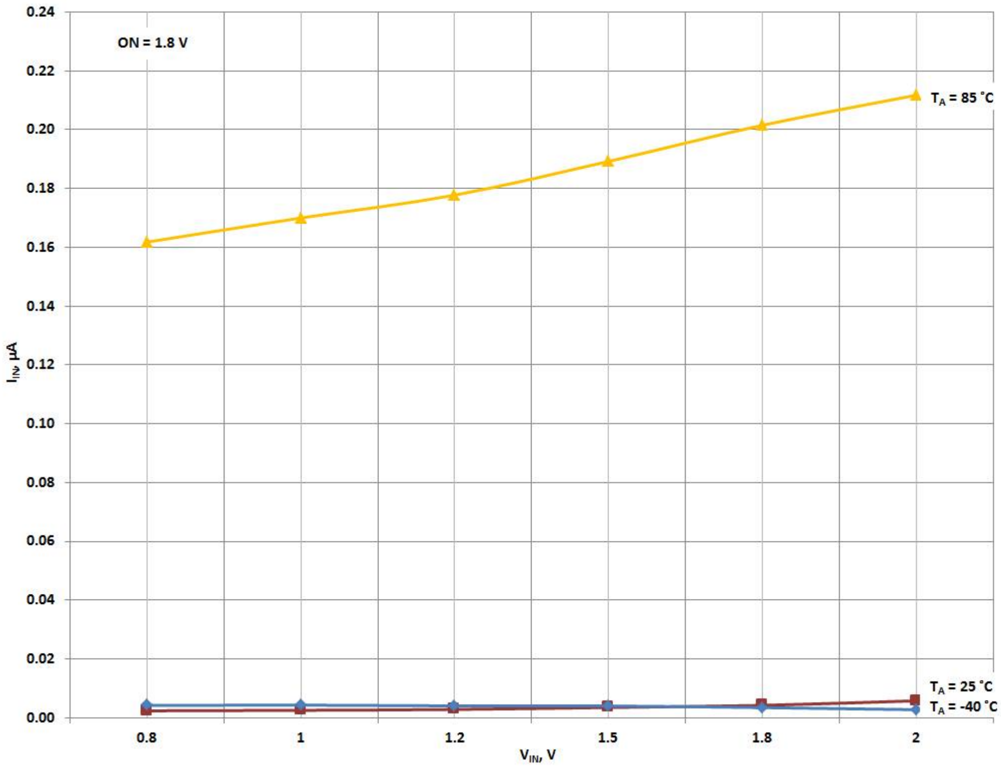


Note: *Rise and Fall times of the ON signal are 100 ns

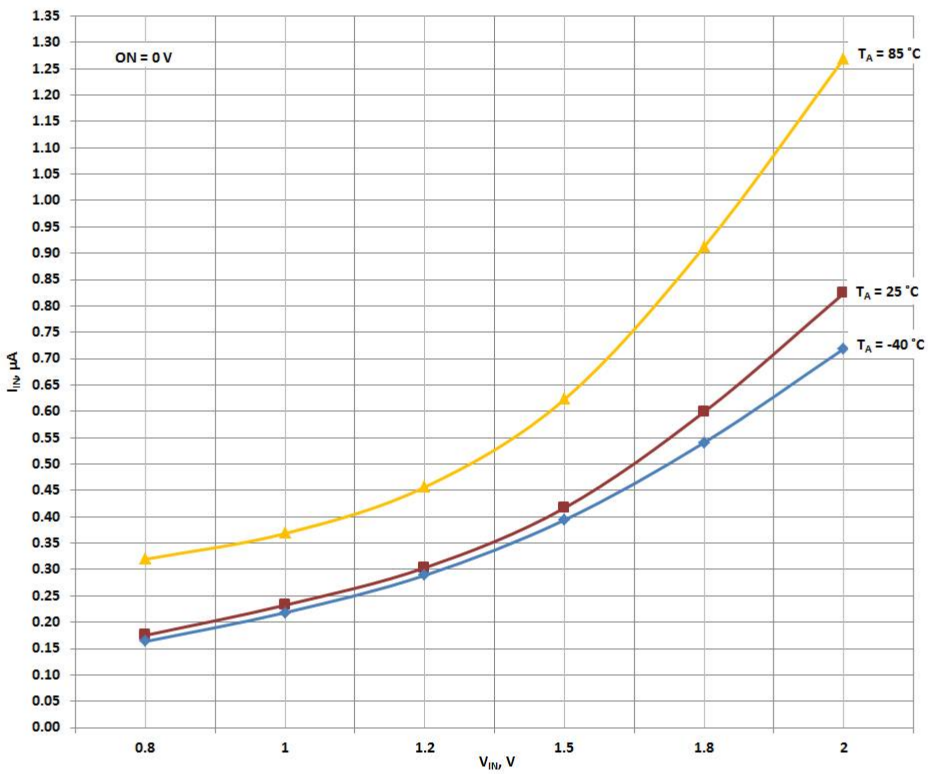
RDS_{ON} vs. Temperature and V_{IN}



I_{IN} when ON = 1.8 V vs. V_{IN} and Temperature



I_{IN} when OFF vs. V_{IN} and Temperature



Typical Turn-on Waveforms

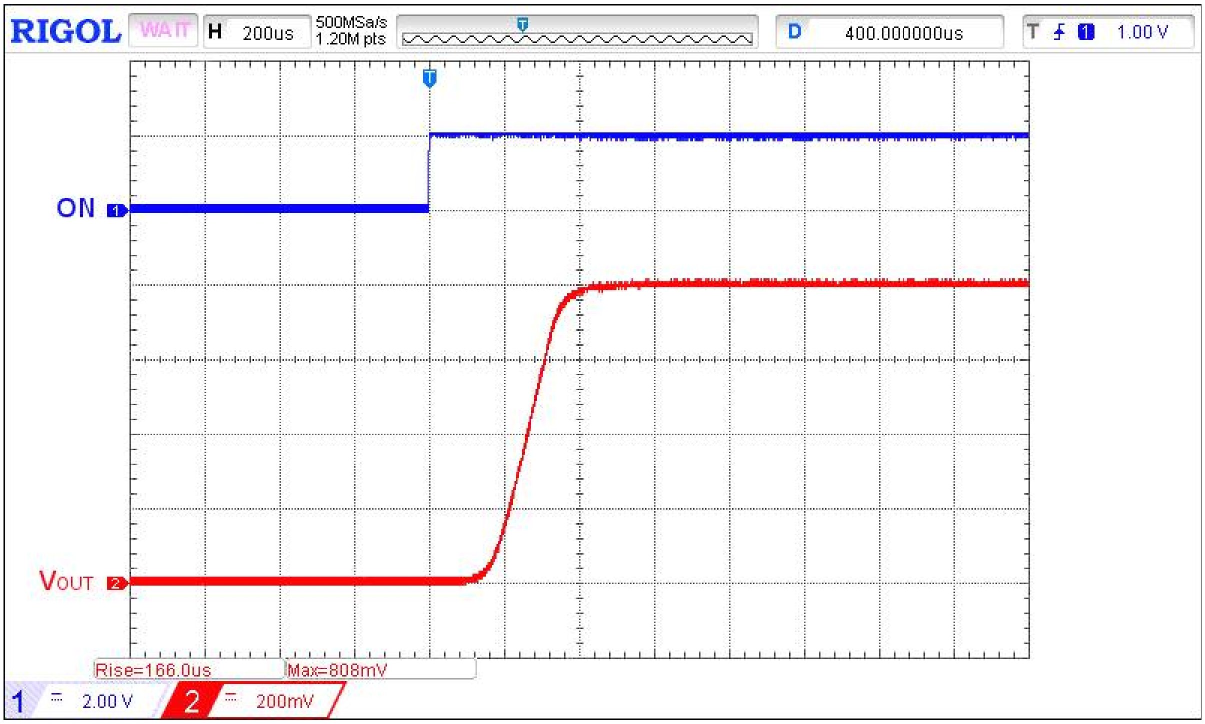


Figure 1. Typical Turn ON operation waveform for V_{IN} = 0.8 V, R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF

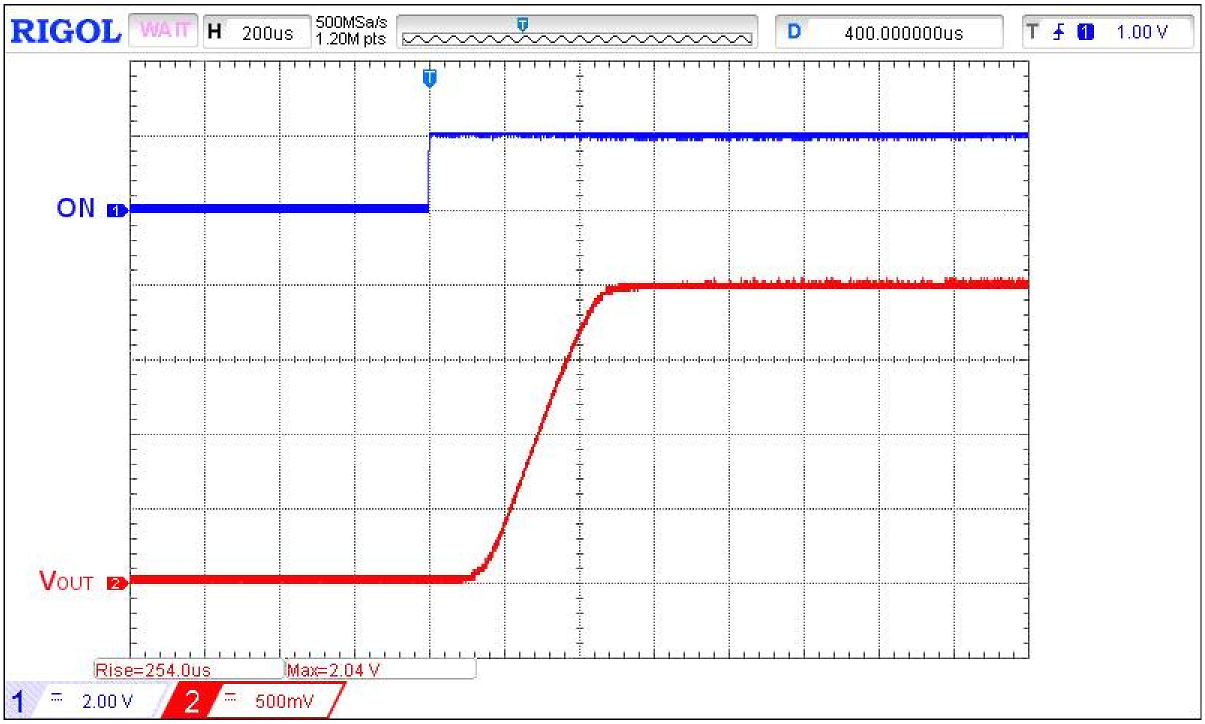


Figure 2. Typical Turn ON operation waveform for V_{IN} = 2.0 V, R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF

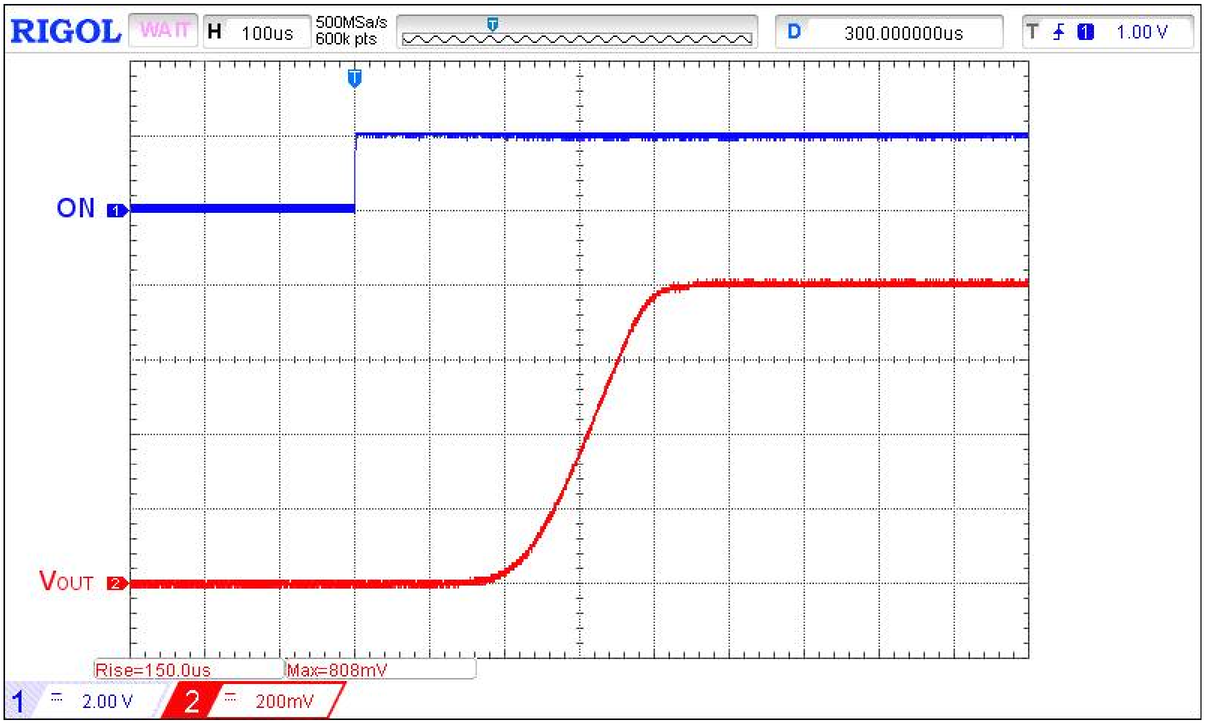


Figure 3. Typical Turn ON operation waveform for V_{IN} = 0.8 V, R_{LOAD} = 10 Ω, C_{LOAD} = 30 μF

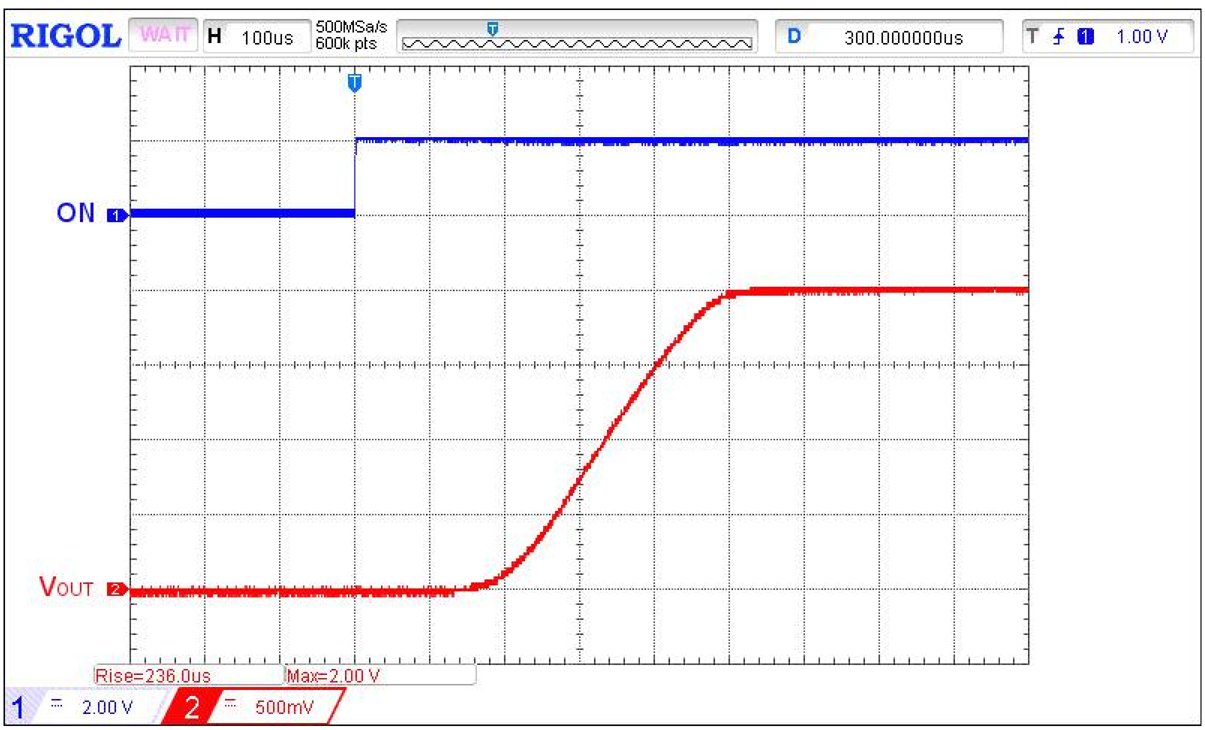


Figure 4. Typical Turn ON operation waveform for V_{IN} = 2.0 V, R_{LOAD} = 10 Ω, C_{LOAD} = 30 μF

Typical Turn-off Waveforms

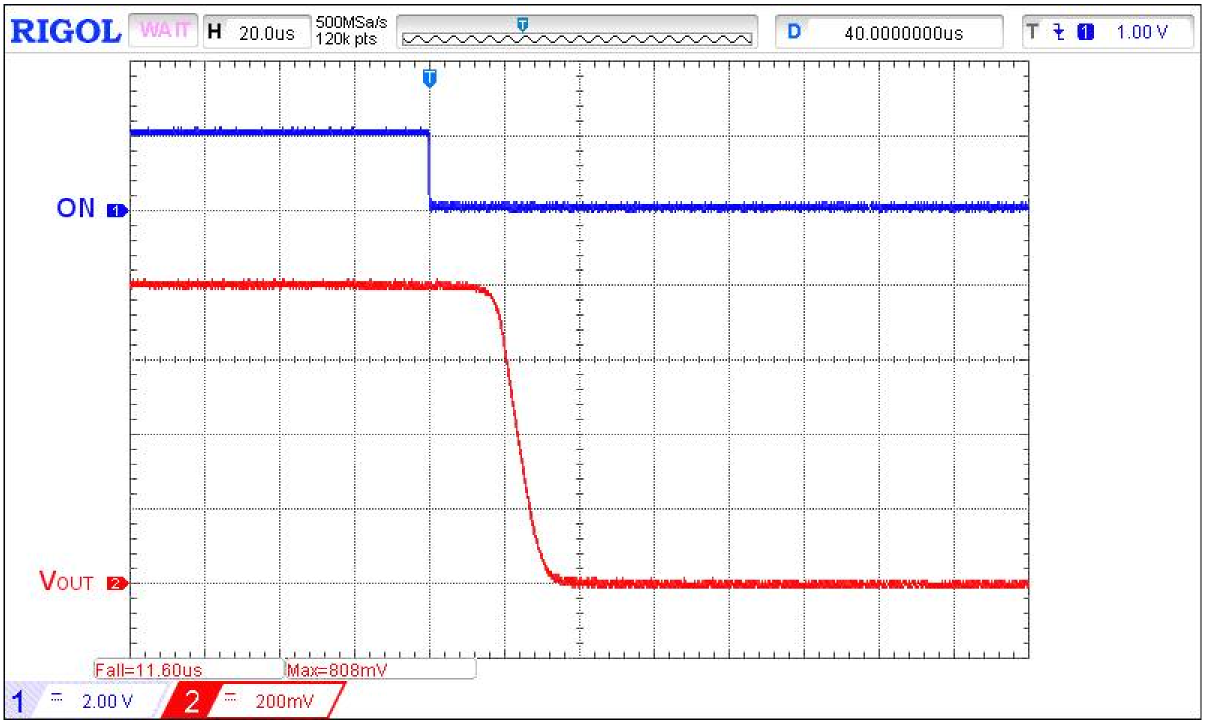


Figure 5. Typical Turn OFF operation waveform for V_{IN} = 0.8 V, R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 μF

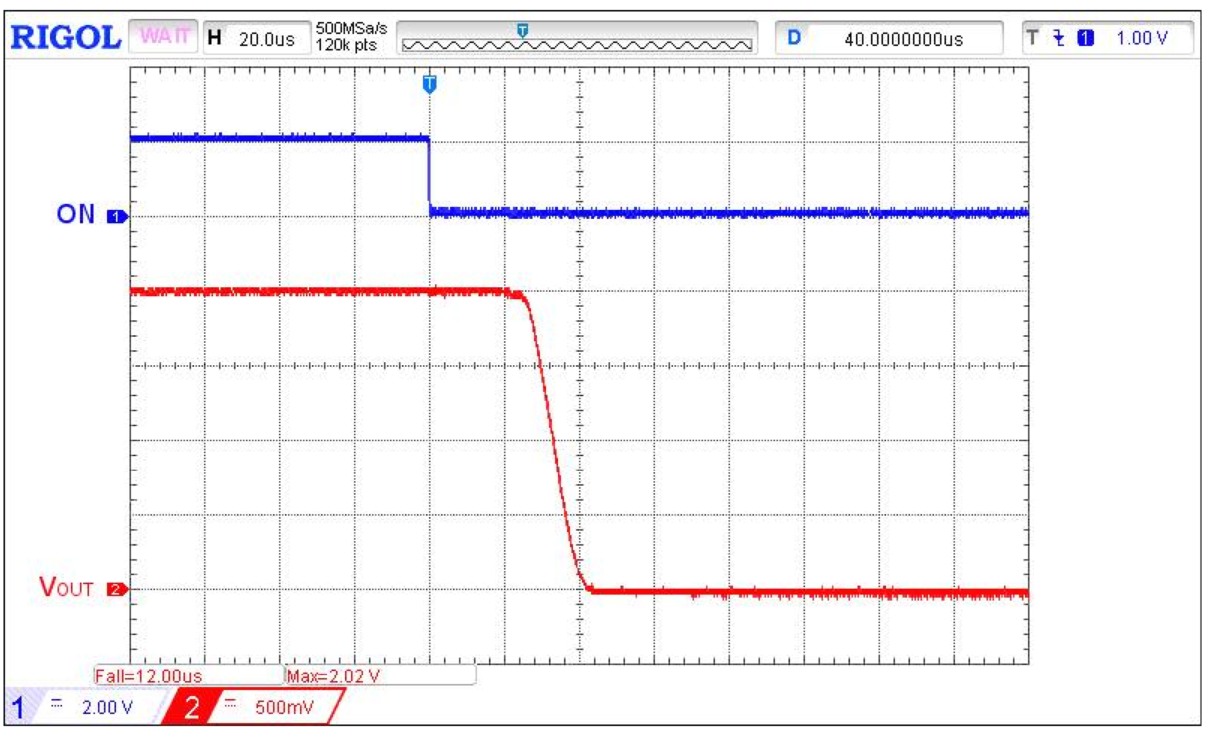


Figure 6. Typical Turn OFF operation waveform for V_{IN} = 2.0 V, R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 μF

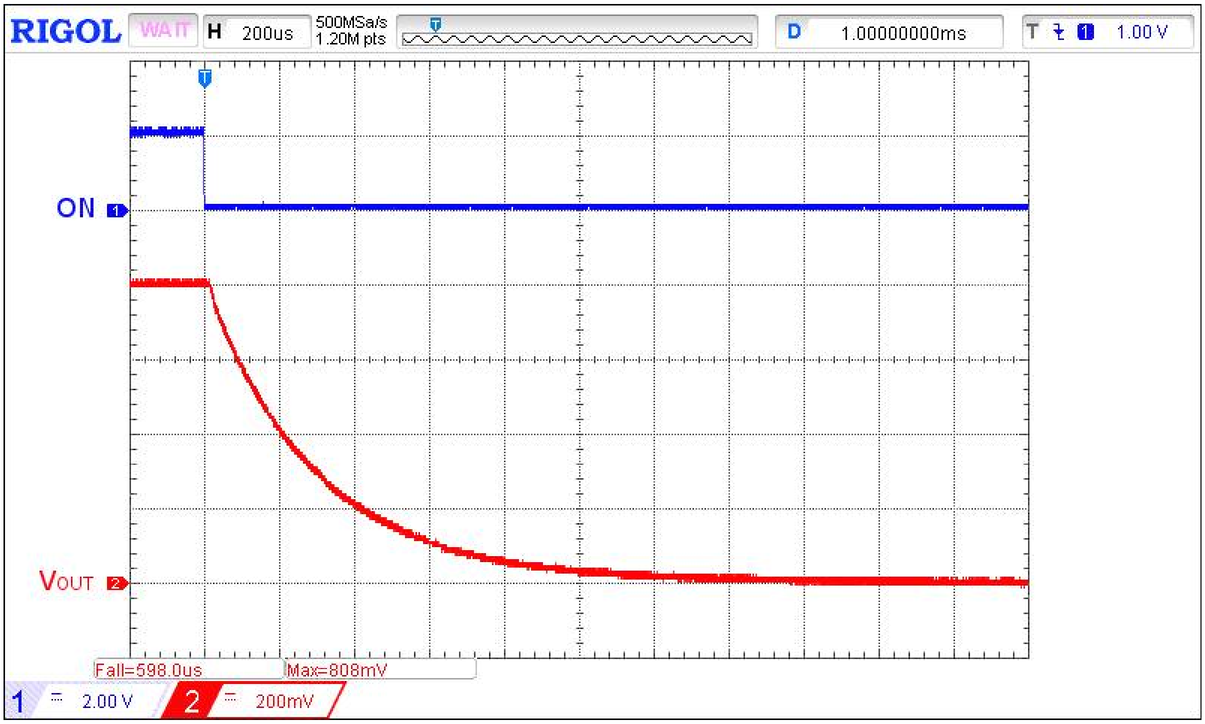


Figure 7. Typical Turn OFF operation waveform for V_{IN} = 0.8 V, R_{LOAD} = 10 Ω, C_{LOAD} = 30 µF

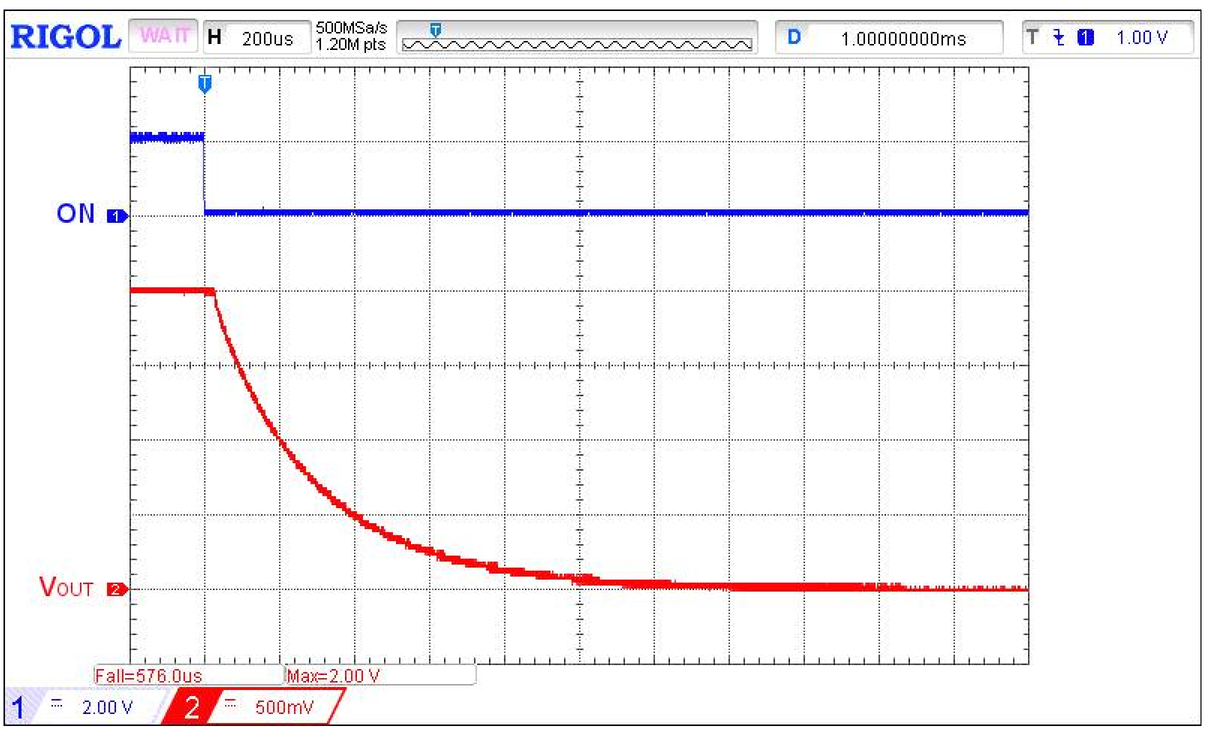


Figure 8. Typical Turn OFF operation waveform for V_{IN} = 2.0 V, R_{LOAD} = 10 Ω, C_{LOAD} = 30 µF

Applications Information

Power Dissipation Considerations

The junction temperature of the SLG59M1693C depends on factors such as board layout, ambient temperature, external air flow over the package, load current, and the RDS_{ON}-generated voltage drop across the power MOSFET. While the primary contributor to the increase in the junction temperature of the SLG59M1693C is the power dissipation of its power MOSFETs, its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD_{TOTAL} = RDS_{ON} \times I_{DS}^2$$

where:

PD_{TOTAL} = Total package power dissipation, in Watts (W)

RDS_{ON}= Power MOSFET ON resistance, in Ohms (Ω)

I_{DS} = Output current, in Amps (A)

and

$$T_J = PD_{TOTAL} \times \theta_{JA} + T_A$$

where:

T_J = Die junction temperature, in Celsius degrees (°C)

θ_{JA} = Package thermal resistance, in Celsius degrees per Watt (°C/W) – highly dependent on pcb layout

T_A = Ambient temperature, in Celsius degrees (°C)

In nominal operating mode, the SLG59M1693C's power dissipation can also be calculated by taking into account the voltage drop across the switch (V_{IN} - V_{OUT}) and the magnitude of the switch's output current (I_{DS}):

$$PD_{TOTAL} = (V_{IN} - V_{OUT}) \times I_{DS} \text{ or}$$

$$PD_{TOTAL} = (V_{IN} – (R_{LOAD} \times I_{DS})) \times I_{DS}$$

where:

PD_{TOTAL} = Total package power dissipation, in Watts (W)

V_{IN} = Switch input Voltage, in Volts (V)

R_{LOAD} = Output Load Resistance, in Ohms (Ω)

I_{DS} = Switch output current, in Amps (A)

V_{OUT} = Switch output voltage, or $R_{LOAD} \times I_{DS}$

Extending the SLG59M1693C's Maximum Operating Current Range

Some applications require an integrated power switch (IPS) to deliver currents higher than 1 A. One way to address this requirement is to use an IPS with higher current capability. However, such a part may occupy more PCB area or consume more power than optimal for the desired current rating. Another way to obtain higher current capability is to parallel two IPSs as illustrated in Figure 9. This parallel arrangement divides the current between each IPS accordingly to its RDS_{ON}.

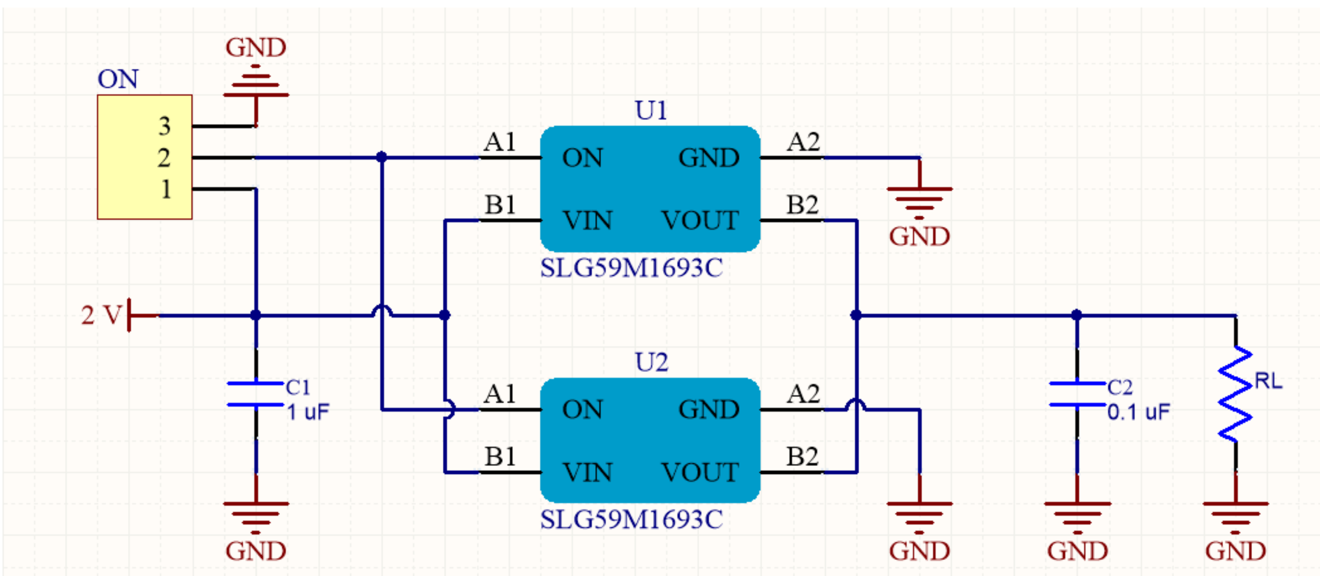


Figure 9. Schematic layout of connecting two SLG59M1693C IPSs in parallel

Using two IPSs in parallel lowers the overall RDS_{ON} while maintaining low current consumption when ON, for any applications up to 2 A. A typical RDS_{ON} vs. Temperature and V_{IN} for this configuration is illustrated in Figure 10.

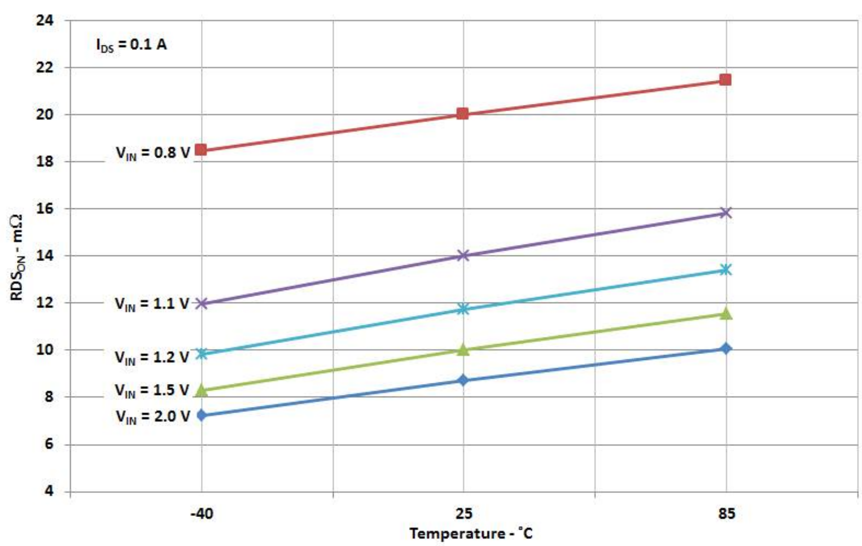


Figure 10. RDS_{ON} vs. Temperature and V_{IN}

All PCB traces have the elements of resistance, capacitance and inductance. If there were a difference in path length from the voltage source to the IPSs pads, this delta trace length would create a current imbalance. In this case, the PCB layout should be designed properly to minimize parasitic impedance and especially parasitic inductance on VIN and VOUT pins. Excess trace inductance may cause a delay effect during on/off operation. Figure 11 shows a recommended PCB layout for applications using two SLG59M1693Cs in parallel.

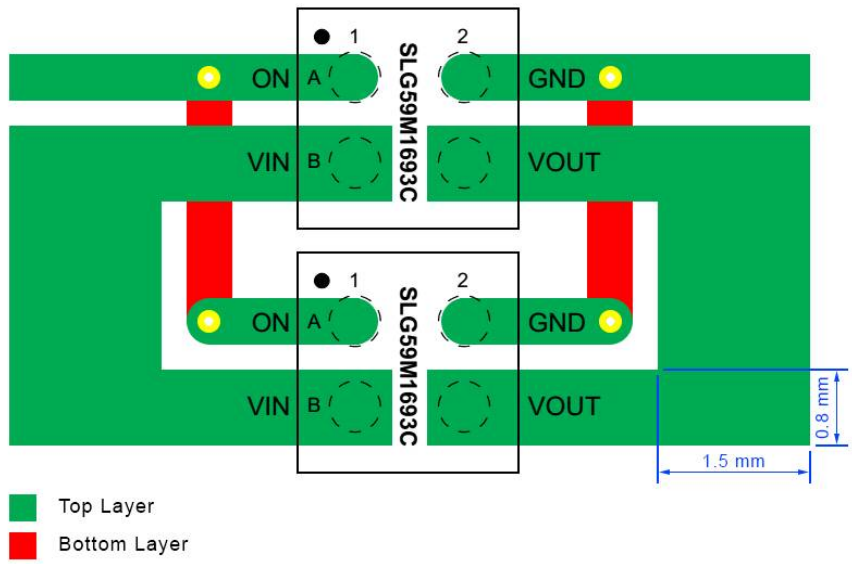


Figure 11. PCB layout for using SLG59M1693C in parallel.

Typical operational waveforms of this two IPS solution are illustrated in Figure 12 and Figure 13.

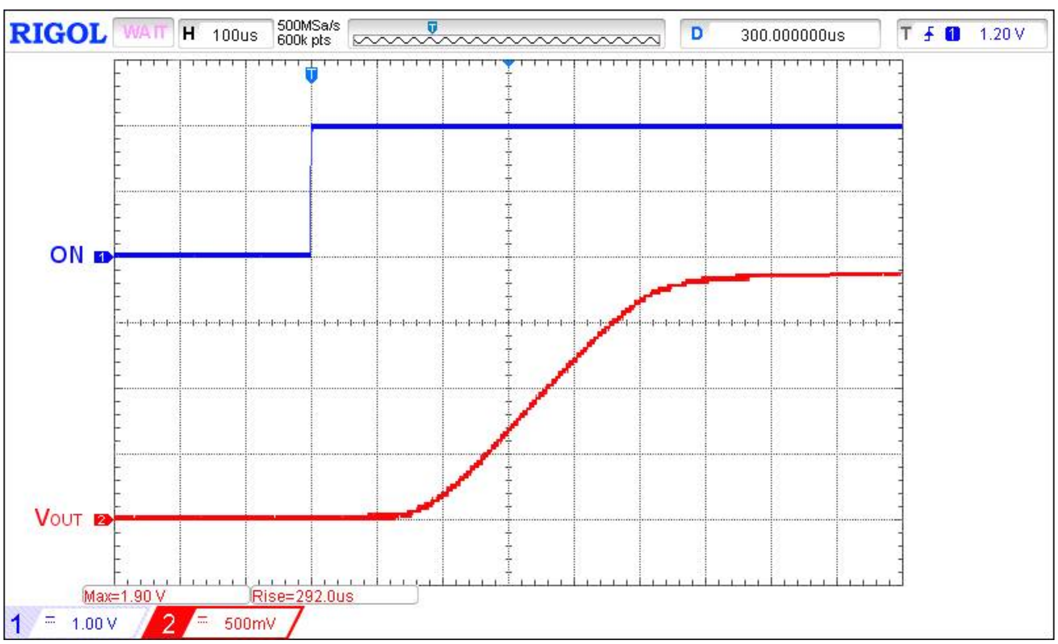


Figure 12. Turn ON operation waveform for V_{IN} = 2 V, C_{LOAD} = 0.1 µF, R_{LOAD} = 1 Ω

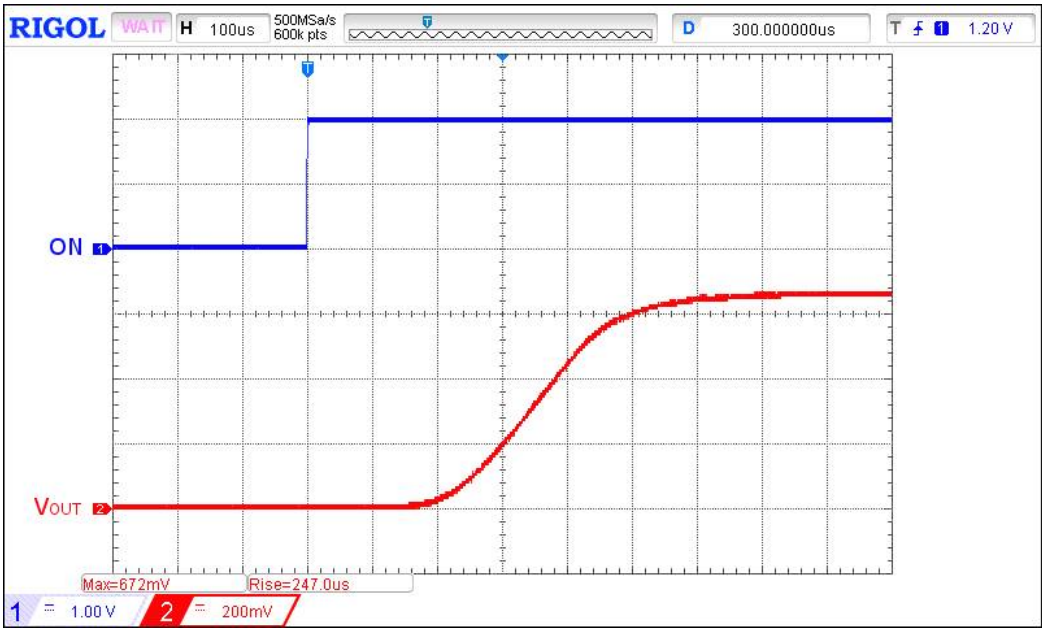
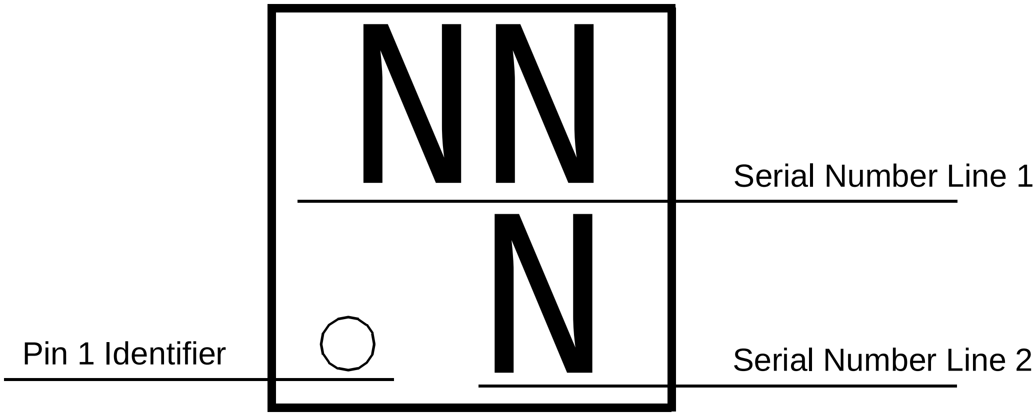


Figure 13. Turn ON operation waveform for V_{IN} = 0.8 V, C_{LOAD} = 0.1 µF, R_{LOAD} = 0.4 Ω

Package Top Marking System Definition



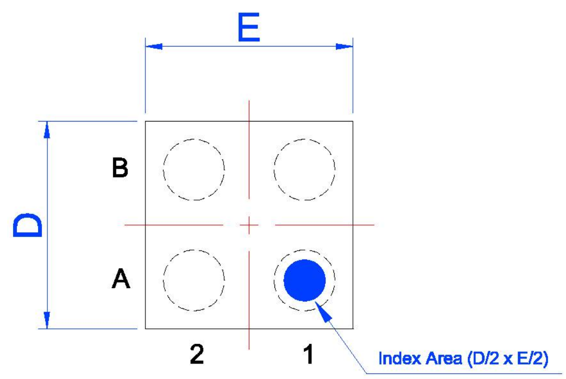
NN - Part Serial Number Field Line 1
where each “N” character can be A-Z and 0-9

N - Part Serial Number Field Line 2
where each “N” character can be A-Z and 0-9

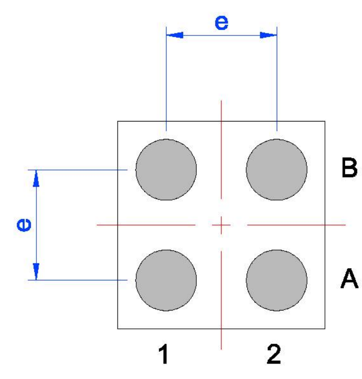
Package Drawing and Dimensions

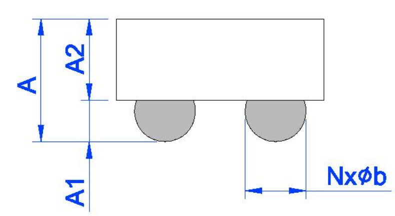
4 Pin WLCSP Green Package 0.75 x 0.75 mm

Laser Marking View



Bump View



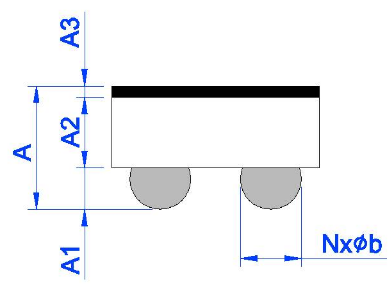


SIDE View

Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.400	0.450	0.500	D	0.72	0.75	0.78
A1	0.125	0.150	0.175	E	0.72	0.75	0.78
A2	0.275	0.300	0.325	e	0.40 BSC		
b	0.195	0.220	0.245	N	4 (Bump)		

With BSC

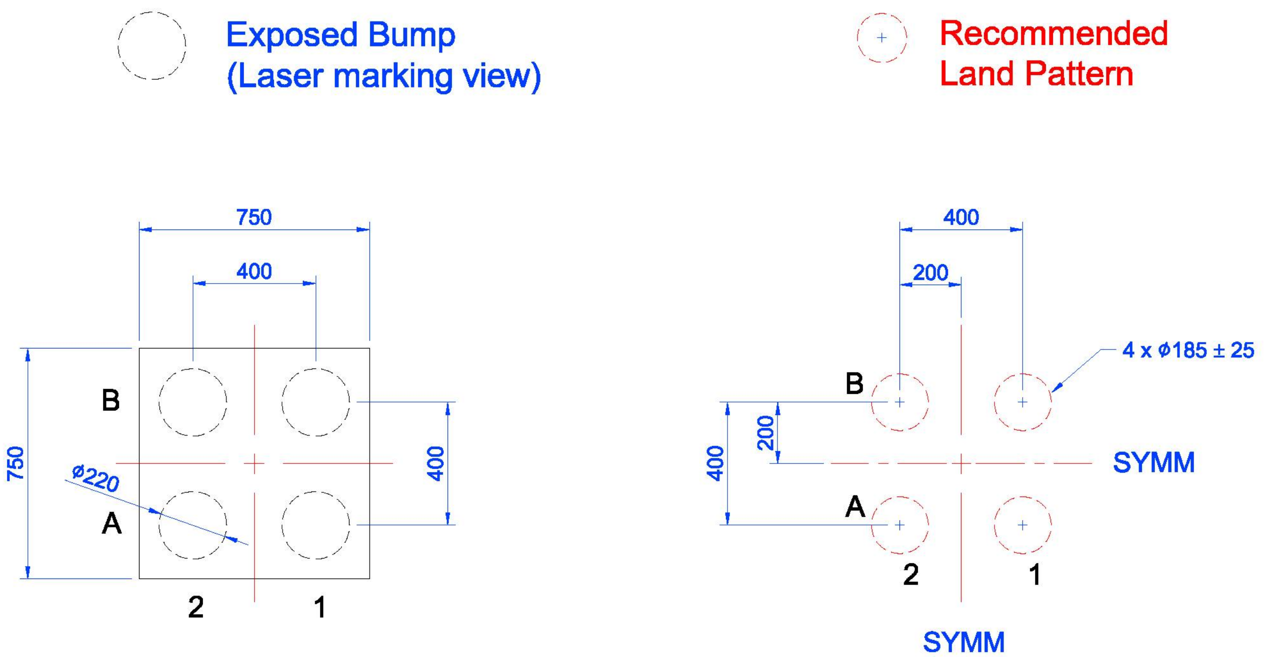


SIDE View

Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.390	0.445	0.500	D	0.72	0.75	0.78
A1	0.125	0.150	0.175	E	0.72	0.75	0.78
A2	0.245	0.270	0.295	e	0.40 BSC		
A3	0.020	0.025	0.030	N	4 (Bump)		
b	0.195	0.220	0.245				

SLG59M1693C 4 Pin WLCSP PCB Landing Pattern

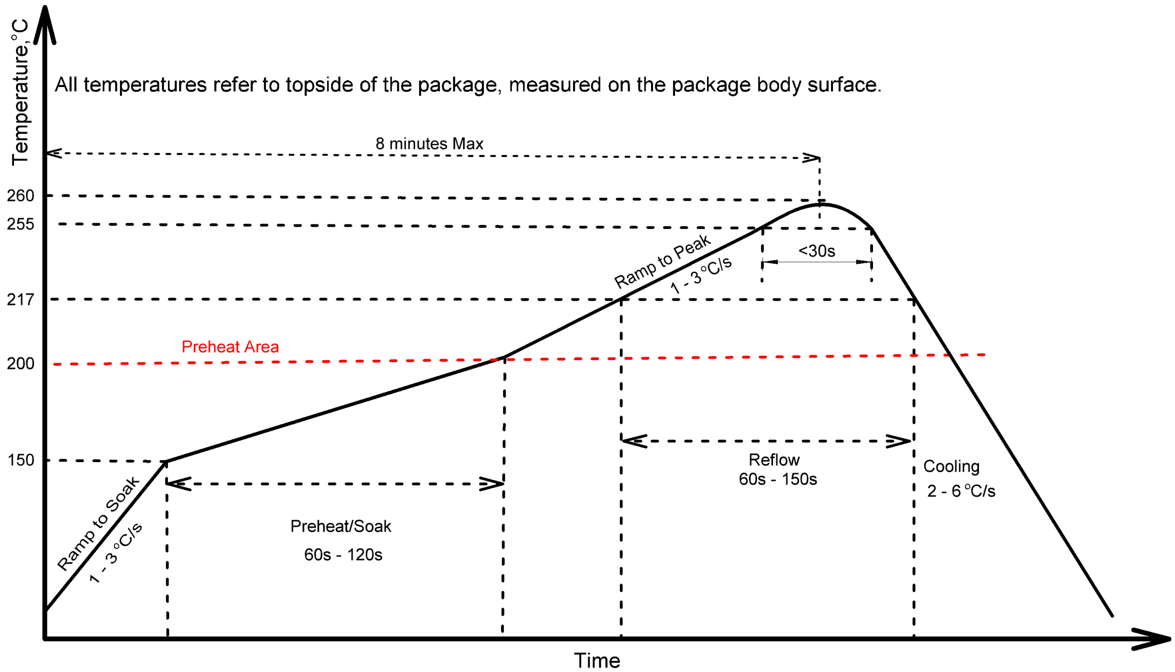


Solder mask detail (not to scale)

Unit: um

Recommended Reflow Soldering Profile

For successful reflow of the SLG59M1693C a recommended thermal profile is illustrated below:



Note: This reflow profile is for classification/preconditioning and are not meant to specify board assembly profile. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed parameters depicted on figure above.

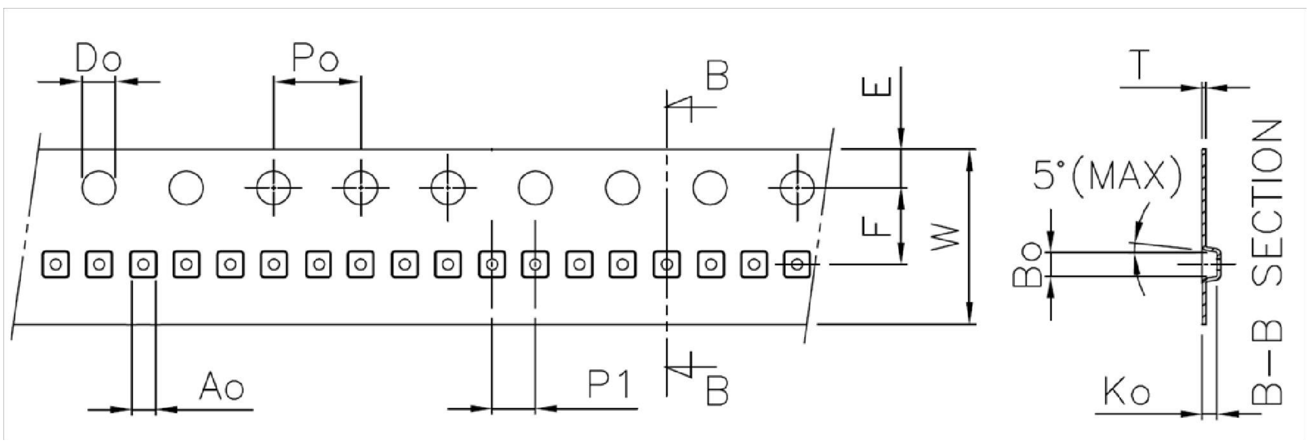
Please see more information on IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.352 mm^3 (nominal).

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
WLCSP 4L 0.75 x 0.75 mm 0.4P Green	4	0.75 x 0.75 x 0.44	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width	Tape Thickness
	A0	B0	K0	P0	P1	D0	E	F	W	T
WLCSP 4L 0.75 x 0.75 mm 0.4P Green	0.84	0.84	0.53	4	4	1.5	1.75	3.5	8	0.2



Refer to EIA-481 specification

Revision History

Date	Version	Change
3/5/2018	1.00	Production Release