SLG74190

1 to 19
Differential Clock Buffer

Features

- Intel DB1900Z Clock Specification Revision 1.0
- 1:19 Differential Zero Delay Buffer
- PCIe Gen 2/Gen3 & Intel ® QPI
- 100ps Input to Output Delay
- HCSL Output Buffer
- Configuration PLL (ZDB) and Bypass Mode
- Programmable PLL Bandwidth
- 72 pin QFN package (6/6 RoHS Compliant)

Output Summary

- 19 - differential clock output pairs @ 0.7V
- 8 - OE# input pins to control output
- 1 - differential external feedback output pair

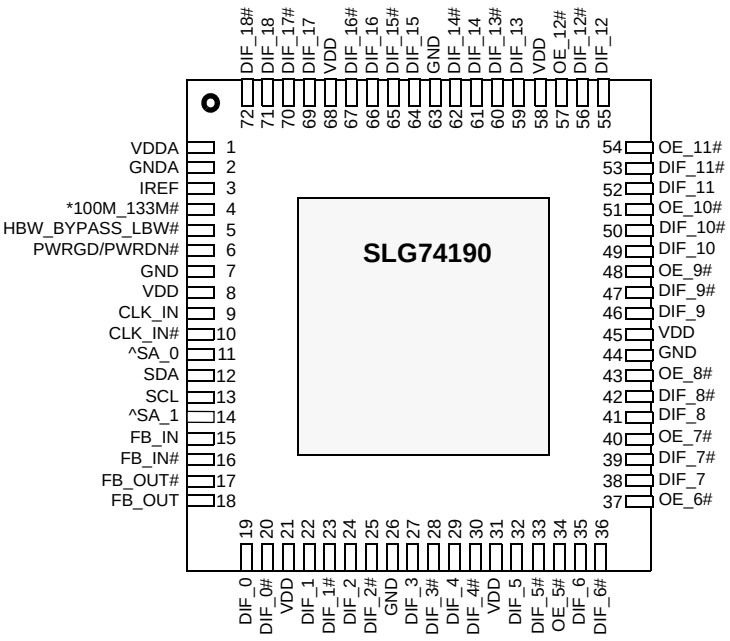
SMBus Address Table

SA_1	SA_0	SMBus Address
L	L	D8
L	M	DA
L	H	DE
M	L	C2
M	M	C4
M	H	C6
H	L	CA
H	M	CC
H	H	CE

Note: SA_1 & SA_0 have an integrated pull-down resistor @100kΩ

Pin Configuration

(Top View)



72-Pin QFN

Note: Signals with "*" have internal pull-up resistors
Signals with "^" have internal pull-down resistors

Pin Description

Pin #	Name	Type	Description
1	VDDA	PWR	3.3V Power supply for PLL
2	GNDA	GND	Ground for PLL
3	IREF	I	A precision resistor is attached to this pin to set the differential output current. Use 475Ω , 1% for 100Ω trace. Use 412Ω, 1% for 85Ω trace.
4	100M_133M#	I	3.3V tolerant input for input/output frequency selection. An external pull-up or pull-down resistor is attached to this pin to select the input/output frequency. Contains internal weak pull-up 100kΩ resistor. High = 100MHz output. Low = 133MHz output.
5	HBW_BYPASS_LBW#	I	Tri-Level input for selecting the PLL bandwidth or bypass mode (refer to trilevel threshold table). High = High BW mode Med = Bypass mode Low = Low BW mode
6	PWRGD/PWRDN#	I	3.3 V LVTTL input to power up or power down the device.
7	GND	GND	Ground for outputs.
8	VDD	PWR	3.3V power supply for outputs.
9	CLK_IN	I	0.7V Differential Input.
10	CLK_IN#	I	0.7V Differential Input.
11	SA_0	I	3.3 V LVTTL input selecting the address. Tri-level input (refer to tri-level threshold table).
12	SDA	I/O, SE	Open collector SMBus data.
13	SCL	I	SMBus slave clock input.
14	SA_1	I	3.3 V LVTTL input selecting the address. Tri-level input (refer to tri-level threshold table).
15	FB_IN	I	External Feedback input.
16	FB_IN#	I	External Feedback input. Complement.
17	FB_OUT#	O, DIF	External Feedback output.
18	FB_OUT	O, DIF	External Feedback output. Complement.
19	DIF_0	O, DIF	0.7V Differential clock output.
20	DIF_0#	O, DIF	0.7V Differential clock output.
21	VDD	PWR	3.3V power supply for outputs.
22	DIF_1	O, DIF	0.7V Differential clock output.
23	DIF_1#	O, DIF	0.7V Differential clock output.
24	DIF_2	O, DIF	0.7V Differential clock output.
25	DIF_2#	O, DIF	0.7V Differential clock output.
26	GND	GND	Ground for outputs.
27	DIF_3	O, DIF	0.7V Differential clock output.
28	DIF_3#	O, DIF	0.7V Differential clock output.
29	DIF_4	O, DIF	0.7V Differential clock output.

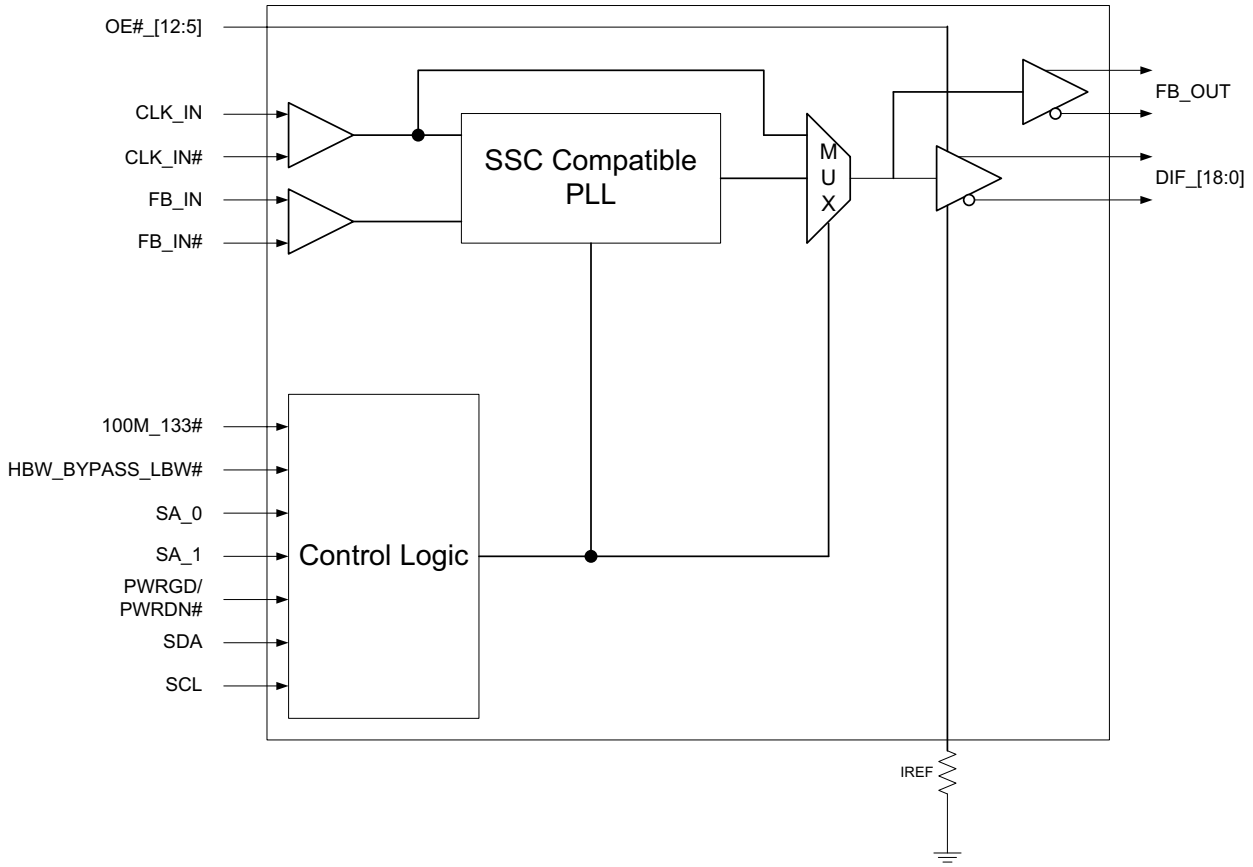
Pin Description (continued)

Pin #	Name	Type	Description
30	DIF_4#	O, DIF	0.7V Differential clock output.
31	VDD	PWR	3.3V power supply for outputs.
32	DIF_5	O, DIF	0.7V Differential clock output.
33	DIF_5#	O, DIF	0.7V Differential clock output.
34	OE_5#	I	3.3 V LVTTL active low input for enabling differential outputs (default). Controls the corresponding output pair.
35	DIF_6	O, DIF	0.7V Differential clock output.
36	DIF_6#	O, DIF	0.7V Differential clock output.
37	OE_6#	I	3.3 V LVTTL active low input for enabling differential outputs (default). Controls the corresponding output pair.
38	DIF_7	O, DIF	0.7V Differential clock output.
39	DIF_7#	O, DIF	0.7V Differential clock output.
40	OE_7#	I	3.3 V LVTTL active low input for enabling differential outputs (default). Controls the corresponding output pair.
41	DIF_8	O, DIF	0.7V Differential clock output.
42	DIF_8#	O, DIF	0.7V Differential clock output.
43	OE_8#	I	3.3 V LVTTL active low input for enabling differential outputs (default). Controls the corresponding output pair.
44	GND	GND	Ground for outputs.
45	VDD	PWR	3.3V power supply for outputs.
46	DIF_9	O, DIF	0.7V Differential clock output.
47	DIF_9#	O, DIF	0.7V Differential clock output.
48	OE_9#	I	3.3 V LVTTL active low input for enabling differential outputs (default). Controls the corresponding output pair.
49	DIF_10	O, DIF	0.7V Differential clock output.
50	DIF_10#	O, DIF	0.7V Differential clock output.
51	OE_10#	I	3.3 V LVTTL active low input for enabling differential outputs (default). Controls the corresponding output pair.
52	DIF_11	O, DIF	0.7V Differential clock output.
53	DIF_11#	O, DIF	0.7V Differential clock output.
54	OE_11#	I	3.3 V LVTTL active low input for enabling differential outputs (default). Controls the corresponding output pair.
55	DIF_12	O, DIF	0.7V Differential clock output.
56	DIF_12#	O, DIF	0.7V Differential clock output.
57	OE_12#	I	3.3 V LVTTL active low input for enabling differential outputs (default). Controls the corresponding output pair.
58	VDD	PWR	3.3V power supply for outputs.
59	DIF_13	O, DIF	0.7V Differential clock output.
60	DIF_13#	O, DIF	0.7V Differential clock output.
61	DIF_14	O, DIF	0.7V Differential clock output.

Pin Description (continued)

Pin #	Name	Type	Description
62	DIF_14#	O, DIF	0.7V Differential clock output.
63	GND	GND	Ground for outputs.
64	DIF_15	O, DIF	0.7V Differential clock output.
65	DIF_15#	O, DIF	0.7V Differential clock output.
66	DIF_16	O, DIF	0.7V Differential clock output.
67	DIF_16#	O, DIF	0.7V Differential clock output.
68	VDD	PWR	3.3V power supply for outputs.
69	DIF_17	O, DIF	0.7V Differential clock output.
70	DIF_17#	O, DIF	0.7V Differential clock output.
71	DIF_18	O, DIF	0.7V Differential clock output.
72	DIF_18#	O, DIF	0.7V Differential clock output.

Block Diagram



Serial Bus Interface

A two-wire serial interface is provided as the programming interface for the clock synthesizer. The serial interface is fully compliance to the SMBus 2.0 specification. The registers associated with the two-wire interface initializes to their default setting upon power-up, and therefore use of this interface is optional.

The serial interface supports block write and block read operation from any SMBus master devices. For block write and block read operations, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. The block write and block read protocol is outlined in *Table 1*. The slave receiver address is 11010010 (D2h).

Table 1. Block Read and Block Write protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 Bit '00000000' stands for block operation	11:18	Command Code - 8 Bit '00000000' stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29:36	Data byte 0 - 8 bits	28	Read
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 1 - 8 bits	30:37	Byte count from slave - 8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte N/Slave Acknowledge...	39:46	Data byte from slave - 8 bits
....	Data Byte N - 8 bits	47	Acknowledge
....	Acknowledge from slave	48:55	Data byte from slave - 8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave/Acknowledge
		....	Data byte N from slave - 8 bits
		....	Not Acknowledge
		....	Stop

Table 2. Byte Read and Byte Write protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bits '1xxxxxxx' stands for byte operationbit[6:0] of the command code represents the offset of the byte to be accessed	11:18	Command Code - 8 bits '1xxxxxxx' stands for byte operationbit[6:0] of the command code represents the offset of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte 0 - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		30:37	Data byte from slave - 8 bits
		38	Not Acknowledge
		39	Stop

Control Register Summary

Control Register 0

Bit	Type	Description/Function	Power up condition
7	R	HBW_BYPASS_LBW# Mode 1. See PLL Bandwidth and Readback Table.	*Latched status*
6	R	HBW_BYPASS_LBW# Mode 0. See PLL Bandwidth and Readback Table.	*Latched status*
5	RW	DIF_18 Output Enable 0 = Hi-Z 1 = Enabled	1
4	RW	DIF_17 Output Enable 0 = Hi-Z 1 = Enabled	1
3	RW	DIF_16 Output Enable 0 = Hi-Z 1 = Enabled	1
2	RW	Reserved	0
1	RW	Reserved	0
0	R	100M_133M# Frequency Select 0 = 133MHz 1 = 100MHz	*Latched status*

PLL Bandwidth and Readback Table

HBW_BYPASS_LBW# Pin	Mode	Byte 0, Bit 7	Byte 0 Bit, 6
L	LBW	0	0
M	BYPASS	0	1
H	HBW	1	1

Control Register 1

Bit	Type	Description/Function	Power up condition
7	RW	DIF_7 Output Enable 0 = Hi-Z 1 = Enabled	1
6	RW	DIF_6 Output Enable 0 = Hi-Z 1 = Enabled	1
5	RW	DIF_5 Output Enable 0 = Hi-Z 1 = Enabled	1
4	RW	DIF_4 Output Enable 0 = Hi-Z 1 = Enabled	1
3	RW	DIF_3 Output Enable 0 = Hi-Z 1 = Enabled	1
2	RW	DIF_2 Output Enable 0 = Hi-Z 1 = Enabled	1

Control Register 1 (continued)

Bit	Type	Description/Function	Power up condition
1	RW	DIF_1 Output Enable 0 = Hi-Z 1 = Enabled	1
0	RW	DIF_0 Output Enable 0 = Hi-Z 1 = Enabled	1

Control Register 2

Bit	Type	Description/Function	Power up condition
7	RW	DIF_15 Output Enable 0 = Hi-Z 1 = Enabled	1
6	RW	DIF_14 Output Enable 0 = Hi-Z 1 = Enabled	1
5	RW	DIF_13 Output Enable 0 = Hi-Z 1 = Enabled	1
4	RW	DIF_12 Output Enable 0 = Hi-Z 1 = Enabled	1
3	RW	DIF_11 Output Enable 0 = Hi-Z 1 = Enabled	1
2	RW	DIF_10 Output Enable 0 = Hi-Z 1 = Enabled	1
1	RW	DIF_9 Output Enable 0 = Hi-Z 1 = Enabled	1
0	RW	DIF_8 Output Enable 0 = Hi-Z 1 = Enabled	1

Control Register 3

Bit	Type	Description/Function	Power up condition
7	R	Realtime readback of OE_12# 0 = Low 1 = High	Realtime
6	R	Realtime readback of OE_11# 0 = Low 1 = High	Realtime
5	R	Realtime readback of OE_10# 0 = Low 1 = High	Realtime
4	R	Realtime readback of OE_9# 0 = Low 1 = High	Realtime

Control Register 3 (continued)

Bit	Type	Description/Function	Power up condition
3	R	Realtime readback of OE_8# 0 = Low 1 = High	Realtime
2	R	Realtime readback of OE_7# 0 = Low 1 = High	Realtime
1	R	Realtime readback of OE_6# 0 = Low 1 = High	Realtime
0	R	Realtime readback of OE_5# 0 = Low 1 = High	Realtime

Control Register 4

Bit	Type	Description/Function	Power up condition
7	RW	Reserved	0
6	RW	Reserved	0
5	RW	Reserved	0
4	RW	Reserved	0
3	RW	Reserved	0
2	RW	Reserved	0
1	RW	Reserved	0
0	RW	Reserved	0

Control Register 5

Bit	Type	Description/Function	Power up condition
7	R	Revision ID bit 3	0
6	R	Revision ID bit 2	0
5	R	Revision ID bit 1	0
4	R	Revision ID bit 0	0
3	R	Vendor ID bit 3	0
2	R	Vendor ID bit 2	1
1	R	Vendor ID bit 1	1
0	R	Vendor ID bit 0	0

Control Register 6

Bit	Type	Description/Function	Power up condition
7	R	Device ID bit 7	0
6	R	Device ID bit 6	0
5	R	Device ID bit 5	0
4	R	Device ID bit 4	0

Control Register 6 (continued)

Bit	Type	Description/Function	Power up condition
3	R	Device ID bit 3	0
2	R	Device ID bit 2	0
1	R	Device ID bit 1	0
0	R	Device ID bit 0	0

Control Register 7

Bit	Type	Description/Function	Power up condition
7:5	RW	Reserved	000
4:0	RW	Byte Count register for block read operation Note: The default value is 8. To read more than 8 bytes, system BIOS needs to change this register to the number of bytes it intends to read.	01000

Absolute Maximum Ratings

Storage Temperature:–65°C to + 150°C

Supply Voltage (VDDA):-0.5 to 4.6V

Supply Voltage (VDD):-0.5 to 4.6V

3.3V Input Voltage:-0.5 to 4.6V

Operating Temperature (Ambient):0°C to +70°C

ESD Protection (Min):2000V

DC Electrical Characteristics

Operating Conditions

Symbol	Description	Conditions	Min	Typ	Max	Unit
VDDA	3.3V Core Supply Voltage	3.3V±5%	3.135		3.465	V
VDD	3.3V I/O Supply Voltage	3.3V±5%	3.135		3.465	V
Vih	3.3V Input High Voltage	VDD	2.0		VDD+0.3	V
Vil	3.3V Input Low Voltage		VSS-0.3		0.8	V
Iil	Input Leakage Current	0 < Vin < VDD	-5		+5	µA
Vil_Tri	3.3V Input Low Voltage		0		0.9	V
Vim_Tri	3.3V Input Med Voltage		1.3		1.8	V
Vih_Tri	3.3V Input High Voltage		2.4		VDD	V
Voh	3.3V Output High Voltage	Ioh = -1mA	2.4			V
Vol	3.3V Output Low Voltage	Iol = 1mA			0.4	V
Cin	Input Pin Capacitance		2.5		4.5	pF
Cout	Output Pin Capacitance		2.5		4.5	pF
Lpin	Pin Inductance				7	nH
Idd	Full Active				450	mA
Idd_pd	Power Down Mode	Outputs = tristate		25		mA

AC Electrical Characteristics

Output Relational Timing Parameters (Skew and Differential Jitter Parameters)

Group	Description	Min.	Max.	Unit	Notes
CLK_IN, DIF[x:0]	Input-to-Output Delay in PLL mode, nominal value	-100	100*	ps	1, 2, 4, 5
CLK_IN, DIF[x:0]	Input-to-Output Delay in BYPASS mode, nominal value	2.5	4.5	ns	2, 3, 5
CLK_IN, DIF[x:0]	Input-to-Output Delay variation in PLL mode (over voltage and temperature), nominal value		|100|	ps	2, 3, 5
CLK_IN, DIF[x:0]	Input-to-Output Delay variation in BYPASS mode (over voltage and temperature), nominal value		|250|	ps	2, 3, 5
DIF[18:0]	Output-to-Output Skew across all 19 outputs (Common to Bypass and PLL mode)		|50|*	ps	1, 2, 3

NOTES:
1. Measured into fixed 2 pF load cap. Input to output skew is measured at the first output edge following the corresponding input.
2. Measured from differential cross-point to differential cross-point
3. All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.
4. This parameter is deterministic for a given device
5. Measured with scope averaging on to find mean value.
* Target

PLL Bandwidth, Peaking and Phase Jitter Impact

Group	Description	Target	Min.	Max.	Notes
DIF	PLL Jitter Peaking (HBW_BYPASS_LBW# = 0)	<1 dB	--	<2.0 dB	2
DIF	PLL Jitter Peaking (HBW_BYPASS_LBW# = 1)	<1 dB	--	<2.0 dB	2
DIF	PLL Bandwidth (HBW_BYPASS_LBW# = 1)	3MHz	2MHz	4MHz	1
DIF	PLL Bandwidth (HBW_BYPASS_LBW# = 0)	1MHz	700kHz	1.4MHz	1
DIF	Output PCIe* Gen1 REFCLK phase jitter with BER = 1E-12 (including PLL BW 8 - 16 MHz, ? = 0.54, Td=10 ns, Ftrk=1.5 MHz)		0ps	108ps	3, 5, 6
DIF	Output PCIe* Gen2 REFCLK phase jitter (including PLL BW 8 - 16 MHz, Jitter Peaking = 3dB, ? = 0.54, Td=10 ns), Low Band, F < 1.5MHz	2.0ps RMS	0ps	3.0ps RMS	3, 4, 6, 8
DIF	Output PCIe* Gen2 REFCLK phase jitter (including PLL BW 8 - 16 MHz, Jitter Peaking = 3dB, ? = 0.54, Td=10 ns) High Band, 1.5MHz < F < Nyquist	2.0ps RMS	0ps	3.1ps RMS	3, 4, 6, 8
DIF	Output phase jitter impact – PCIe* Gen3 including PLL BW 2 - 4 MHz, CDR = 10MHz)		0ps	1.0ps RMS	3, 4, 6, 8
DIF	Output Intel® QPI & Intel® SMI REFCLK accumulated jitter (4.8Gb/s or 6.4Gb/s, 100MHz or 133MHz, 12 UI)	0.35ps RMS	0ps	0.5ps RMS	3, 7, 9

NOTES:
1. Measured at 3 db down or half power point.
2. Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.
3. Post processed evaluation through Intel supplied Matlab* scripts. Tested with DB1900Z driven by a CK420BQ or equivalent.
4. PCIe* Gen3 filter characteristics are subject to final ratification by PCISIG. Please check the PCI* SIG for the latest specification.
5. These jitter numbers are defined for a BER of 1E-12. Measured numbers at a smaller sample size have to be extrapolated to this BER target.
6. $\zeta = 0.54$ is implying a jitter peaking of 3dB.
7. Measuring on 100MHz output using the template file in the Clock Jitter Tool.
8. Measuring on 100MHz PCIe SRC output using the template file in the Clock Jitter Tool.
9. Measuring on 100MHz, 133MHz output using the template file in the Clock Jitter Tool.

Differential Outputs Timing Characteristics (Non-SSC Clock Input, DIF, 100MHz, 133MHz)

Symbol	Description	Min.	Max.	Unit	Notes
Tstab	Clock Stabilization Tiime		1.8	ms	22
Laccuracy	Long Accuracy		100	ppm	4, 8, 16
Tabsmin	Absolute Minimum Host CLK Period	-2.5%		ns	4, 5, 8
Edge_rate	Edge Rate	1.0	4.0	ns	2, 4, 8
ΔTrise	Rise time variation		125	ps	4, 7, 18
ΔTfall	Fall time variation		125	ps	4, 7, 18
Rice/Fall Matching			20%		4, 7, 19, 21
VHigh	Voltage High (typ 0.70V)	660	850	mV	4, 7, 10
VLow	Voltage Low (typ 0.0V)	-150		mV	4, 7, 11
Vcross Abs	Absolute Crossing Point Voltage	250	550	mV	1, 3, 4, 7, 14
Vcross rel	Relative Crossing Point Voltage	Calc	Calc	mV	4, 6, 7, 14
Total Δ Vcross	Total Variation of Vcross Over all Edges		140	mV	4, 7, 15
Tccjitter	Cycle to Cycle Jitter		50	ps	4, 8, 20
Duty Cycle	Duty Cycle	45	55	%	4, 8
Vovs	Maximum Voltage (Overshoot)		Vhigh+0.3V		4, 7, 12
Vuds	Maximum Voltage (Undershoot)		Vlow-0.3V		4, 7, 13
Vrb	Ringback Voltage	±0.2	N/A	V	4, 7

NOTES:
1. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLK#
2. Measure taken from differential waveform on a component test board. The edge (slew) rate is measured from -150mV to +150mV on the differential waveform . Scope is set to average because the scope sample clock is making most of the dynamic wiggles along the clock edge Only valid for Rising clock and Falling Clock#. Signal must be monotonic through the Vol to Voh region for Trise and Tfall
3. This measurement refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing
4. Test configuration is Rs=33.2 O, Rp=49.9, 2 pF
5. The average period over any 1 µs period of time must be greater than the minimum and less than the maximum specified period
6. Vcross(rel) Min and Max are derived using the following, Vcross(rel) Min = 0.250 + 0.5 (Vhavg - 0.700), Vcross(rel) Max = 0.550 - 0.5 (0.700 – Vhavg), (see Figure 3-4 for further clarification)
7. Measurement taken from Single Ended waveform
8. Measurement taken from differential waveform
9. Unless otherwise noted, all specifications in this table apply to all processor frequencies
10. VHigh is defined as the statistical average High value as obtained by using the Oscilloscope VHigh Math function
11. VLow is defined as the statistical average Low value as obtained by using the Oscilloscope VLow Math function
12. Overshoot is defined as the absolute value of the maximum voltage
13. Undershoot is defined as the absolute value of the minimum voltage
14. The crossing point must meet the absolute and relative crossing point specifications simultaneously
15. ΔVcross is defined as the total variation of all crossing voltages of Rising CLOCK and Falling CLOCK#. This is the maximum allowed variance in Vcross for any particular system
16. Using frequency counter with the measurement interval equal or greater than 0.15 s, target frequencies are 100,000,000 Hz, 133,333,333 Hz
17. Using frequency counter with the measurement interval equal or greater than 0.15 s, target frequencies are 99,750,00 Hz, 133,000,000 Hz
18. Measured with oscilloscope, averaging off, using min max statistics. Variation is the delta between min and max.
19. Measured with oscilloscope, averaging on, The difference between the rising edge rate (average) of clock verses the falling edge rate (average) of clock#
20. Measured with device in PLL mode, in BYPASS mode jitter is additive
21. Rise/Fall matching is derived using the following, 2*(Trise – Tfall) / (Trise + Tfall)
22. This is the time from the valid CLK_IN input clocks and the assertion of the PWRGD signal level at 1.8V – 2.0V to the time that stable clocks are output from the buffer chip (PLL locked)

Differential Outputs Timing Characteristics (0.5% SSC Clock Input, DIF, 100MHz, 133MHz)

Symbol	Description	Min.	Max.	Unit	Notes
Tstab	Clock Stabilization Tiime		1.8	ms	22
Laccuracy	Long Accuracy		100	ppm	4, 8, 16
Tabsmin	Absolute Minimum Host CLK Period	(Period -0.125ns)		ns	4, 5, 8
Edge_rate	Edge Rate	1.0	4.0	ns	2, 4, 8
ΔTrise	Rise time variation		125	ps	4, 7, 18
ΔTfall	Fall time variation		125	ps	4, 7, 18
Rice/Fall Matching			20%		4, 7, 19, 21
VHigh	Voltage High (typ 0.70V)	660	850	mV	4, 7, 10
VLow	Voltage Low (typ 0.0V)	-150		mV	4, 7, 11
Vcross Abs	Absolute Crossing Point Voltage	250	550	mV	1, 3, 4, 7, 14
Vcross rel	Relative Crossing Point Voltage	Calc	Calc	mV	4, 6, 7, 14
Total Δ Vcross	Total Variation of Vcross Over all Edges		140	mV	4, 7, 15
Tccjitter	Cycle to Cycle Jitter		50	ps	4, 8, 20
Duty Cycle	Duty Cycle	45	55	%	4, 8
Vovs	Maximum Voltage (Overshoot)		Vhigh+0.3V		4, 7, 12
Vuds	Maximum Voltage (Undershoot)		Vlow-0.3V		4, 7, 13
Vrb	Ringback Voltage	Vx±0.2	N/A	V	4, 7

NOTES:
1. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLK#
2. Measure taken from differential waveform on a component test board. The edge (slew) rate is measured from -150mV to +150mV on the differential waveform . Scope is set to average because the scope sample clock is making most of the dynamic wiggles along the clock edge Only valid for Rising clock and Falling Clock#. Signal must be monotonic through the Vol to Voh region for Trise and Tfall
3. This measurement refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing
4. Test configuration is Rs=33.2 O, Rp=49.9, 2 pF
5. The average period over any 1 µs period of time must be greater than the minimum and less than the maximum specified period
6. Vcross(rel) Min and Max are derived using the following, Vcross(rel) Min = 0.250 + 0.5 (Vhavg - 0.700), Vcross(rel) Max = 0.550 - 0.5 (0.700 – Vhavg), (see Figure 3-4 for further clarification)
7. Measurement taken from Single Ended waveform
8. Measurement taken from differential waveform
9. Unless otherwise noted, all specifications in this table apply to all processor frequencies
10. VHigh is defined as the statistical average High value as obtained by using the Oscilloscope VHigh Math function
11. VLow is defined as the statistical average Low value as obtained by using the Oscilloscope VLow Math function
12. Overshoot is defined as the absolute value of the maximum voltage
13. Undershoot is defined as the absolute value of the minimum voltage
14. The crossing point must meet the absolute and relative crossing point specifications simultaneously
15. ΔVcross is defined as the total variation of all crossing voltages of Rising CLOCK and Falling CLOCK#. This is the maximum allowed variance in Vcross for any particular system
16. Using frequency counter with the measurement interval equal or greater than 0.15 s, target frequencies are 100,000,000 Hz, 133,333,333 Hz
17. Using frequency counter with the measurement interval equal or greater than 0.15 s, target frequencies are 99,750,00 Hz, 133,000,000 Hz
18. Measured with oscilloscope, averaging off, using min max statistics. Variation is the delta between min and max.
19. Measured with oscilloscope, averaging on, The difference between the rising edge rate (average) of clock verses the falling edge rate (average) of clock#
20. Measured with device in PLL mode, in BYPASS mode jitter is additive
21. Rise/Fall matching is derived using the following, 2*(Trise – Tfall) / (Trise + Tfall)
22. This is the time from the valid CLK_IN input clocks and the assertion of the PWRGD signal level at 1.8V – 2.0V to the time that stable clocks are output from the buffer chip (PLL locked)

Differential Clock Period (SSC Disabled)

SSC Off Center Freq. MHz	Measurement Window							Units
	1 Clock	1µs	0.1s	0.1s	0.1s	1µs	1Clock	
	- Jitterc-c AbsPerMin	- SSC ShortAvgMin	- ppm LongAvgMin	0 ppm Period	+ ppm LongAvgMax	+ SSC ShortAvgMax	+ Jitterc-c AbsPerMax	
100.00	9.94900		9.99900	10.00000	10.00100		10.05100	ns
133.33	7.44925		7.49925	7.50000	7.50075		7.55075	ns

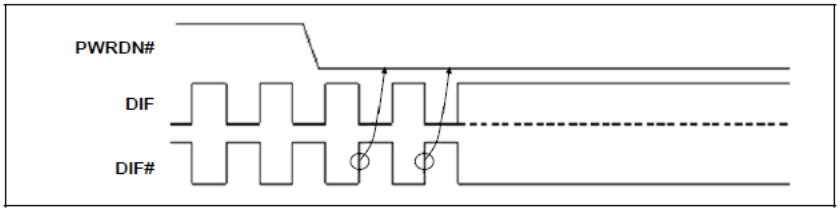
Differential Clock Period (SSC Enabled)

SSC Off Center Freq. MHz	Measurement Window							Units
	1 Clock	1µs	0.1s	0.1s	0.1s	1µs	1Clock	
	- Jitterc-c AbsPerMin	- SSC ShortAvgMin	- ppm LongAvgMin	0 ppm Period	+ ppm LongAvgMax	+ SSC ShortAvgMax	+ Jitterc-c AbsPerMax	
99.75	9.94906	9.99906	10.02406	10.02506	10.02607	10.05107	10.10107	ns
133.00	7.44930	7.49930	7.51805	7.51880	7.51955	7.53830	7.58830	ns

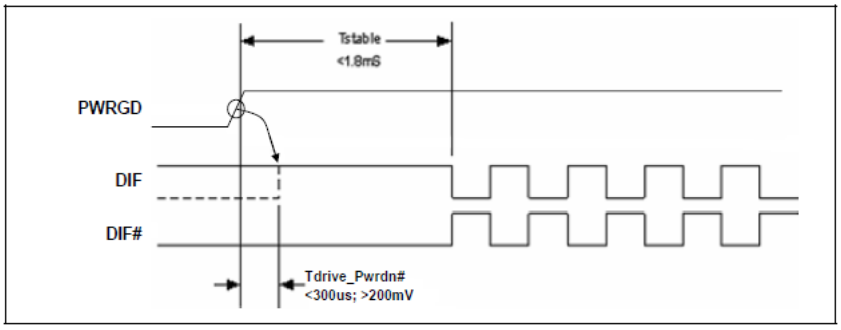
Input Edge Rate

Frequency	Min	Max	Unit
100 MHz	0.35	N/A	V/ns
133 MHz	0.35	N/A	V/ns

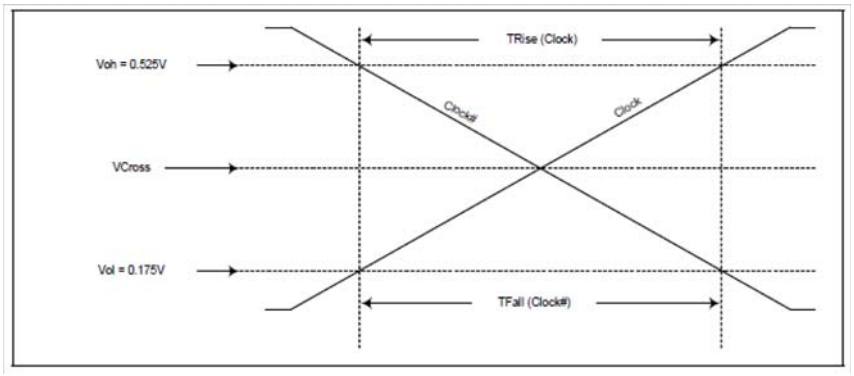
PWRDN# Assertion



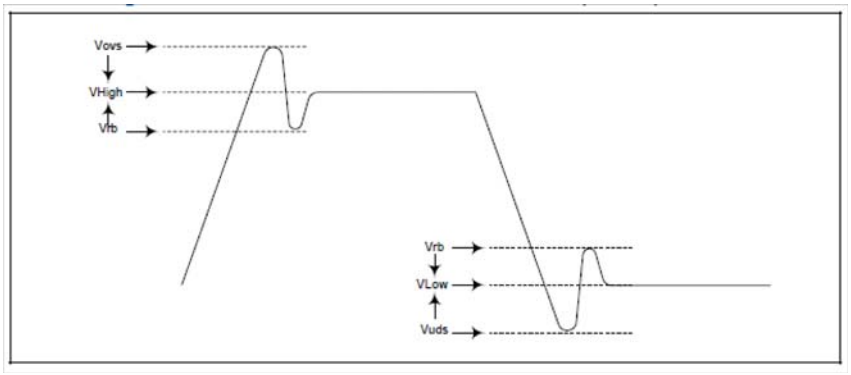
PWRGD Assertion (PWRDN# De-assertion)



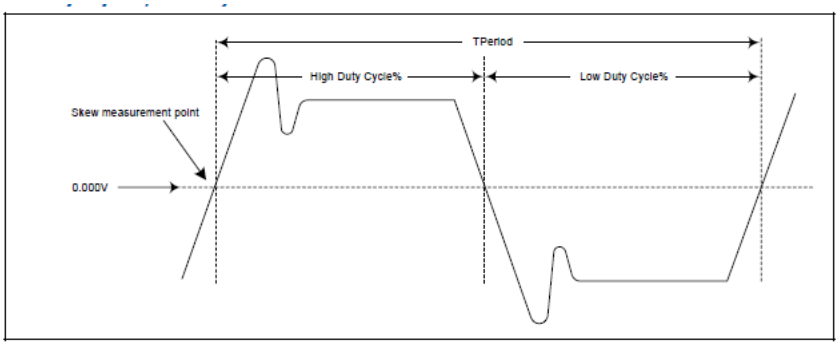
Single-ended Measurement Points for Trise, Tfall



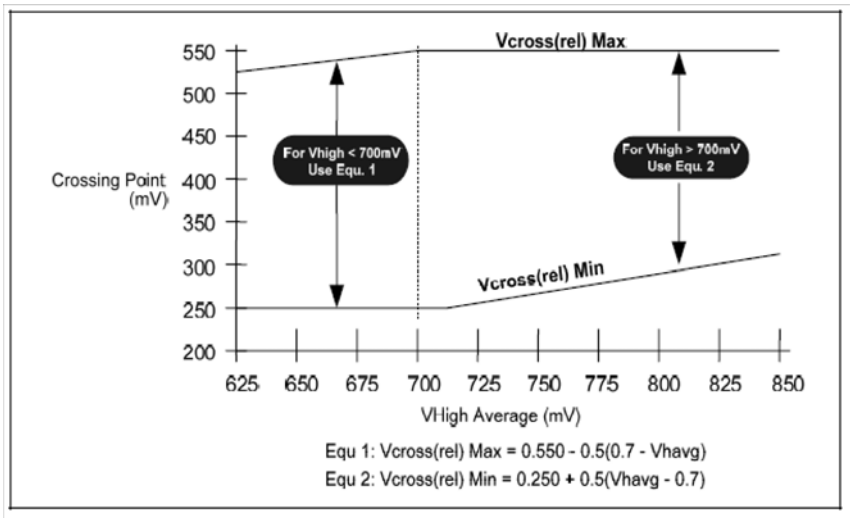
Single-ended Measurement Points for Vovs, Vuds, Vrb



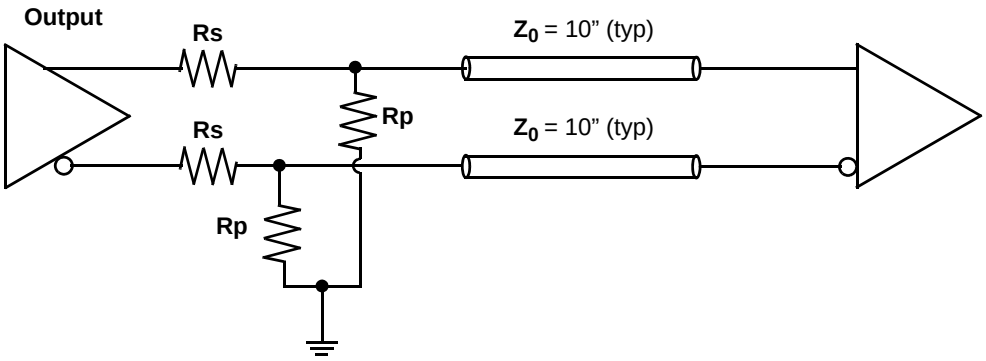
Differential (Clock - Clock#)Measurement Points for Tperiod, Duty Cycle, Jitter



Vcross Range Clarification



Test and Measurement - Differential Impedance Transmission Line



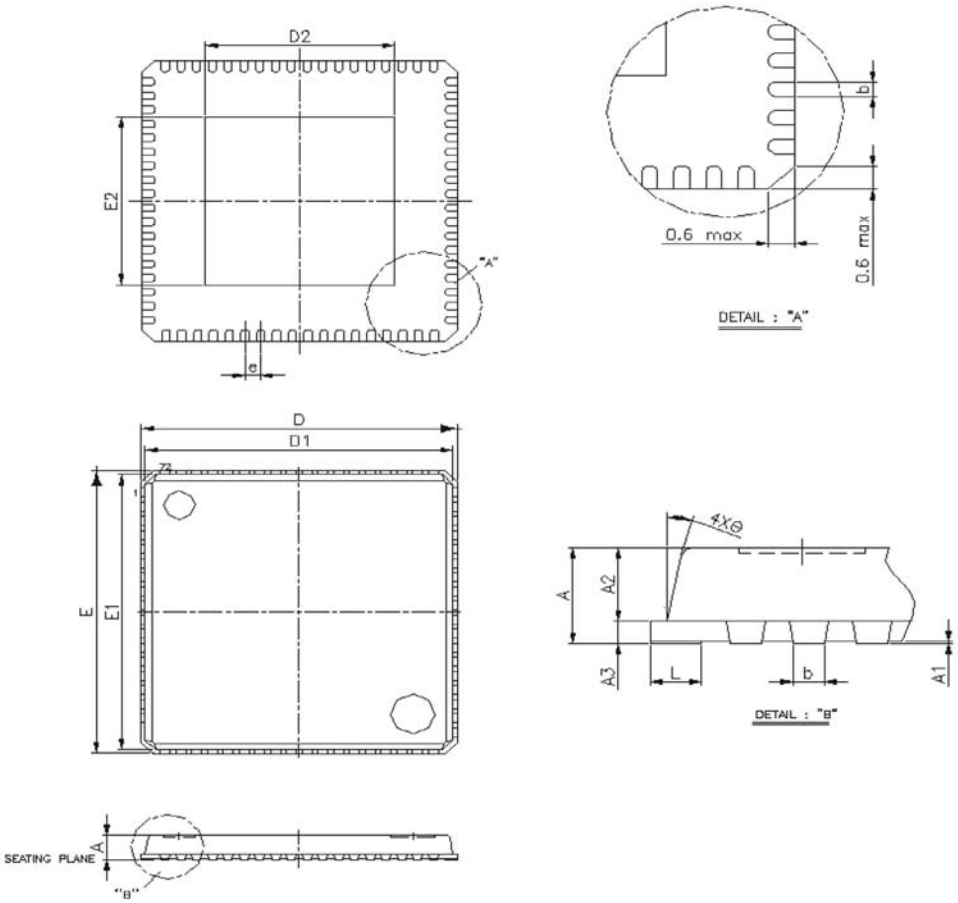
Clock	Board Trace Impedance	Rs	Rp	RIref	Units
DIFF Clocks 50Ω Configuration	100	33 (5%)	49.9 (1%)	475 (1%)	Ω
DIFF Clocks 43Ω Configuration	85	27 (5%)	42.2 (1%)	412 (1%)	Ω

Ordering Information

Part Number	Package Type	Temperature Range
SLG74190V	72 Lead Green Package QFN	Commercial, 0° to 70°C
SLG74190VTR	72 Lead Green Package QFN - Tape and Reel	Commercial, 0° to 70°C

Package Drawing and Dimensions

72 Lead QFN Package



Package Type: TQFN 10x10 72L

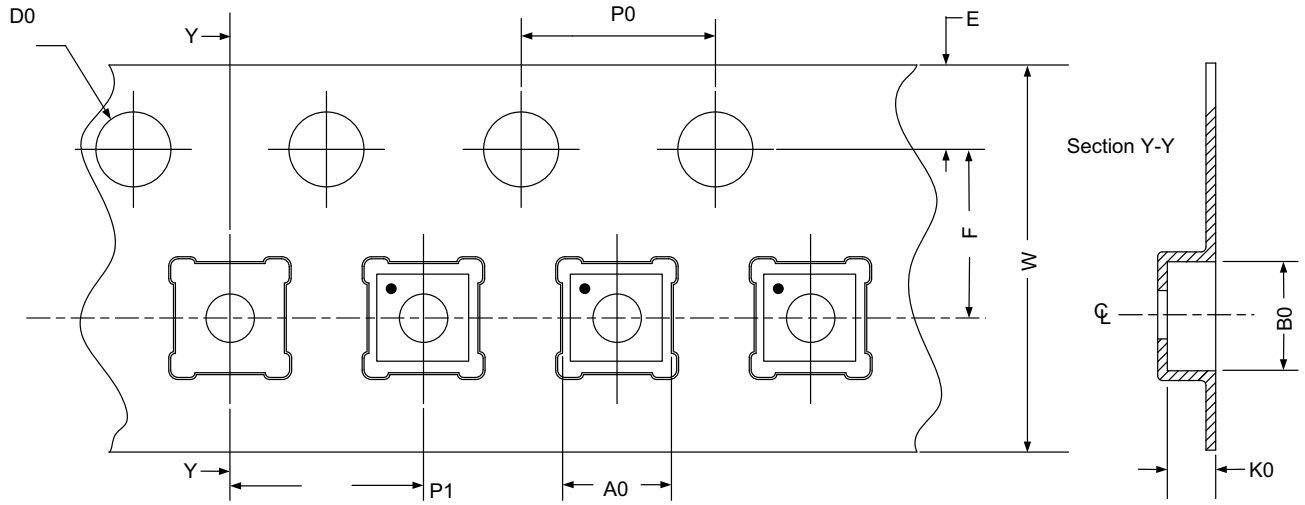
Unit: mm	Silego Spec (Comply to JEDEC MO-220) Dimension in MM		
Symbol	Min	NOM	Max
A	0.80	0.85	1.05
A1	0.00	-	0.05
A2	-	0.65	1.00
A3		0.20 REF	
b	0.15	0.25	0.30
D		10.00 BSC	
E		10.00 BSC	
D1		9.75 BSC	
E1		9.75 BSC	
D2	5.85	-	6.15
E2	5.85	-	6.15
e		0.50 BSC	
L	0.30	0.40	0.60
θ (Degree)	0	-	14

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Hub & Reel Size (mm)	Trailer A		Leader B		Pocket Tape (mm)	
			per reel	per box		Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
TQFN 72L Green	72	10x10x0.85	2,000	2,000	330/100	42	672	42	672	24	16

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
TQFN 72L Green	10.4	10.4	1.3	4	16	1.5	1.75	11.5	24



Revision History

Date	Version	Change
3/30/2016	1.02	Fixed typo in Tape and Reel Spec
4/29/2014	1.01	Updated Package Dimensions to fix typos
3/30/2012	1.00	Production Release