



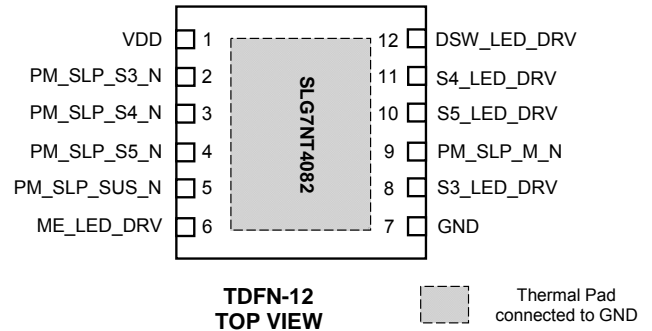
General Description

Silego SLG7NT4082 is a low power and small form device. The SoC is housed in a 2.5mm x 2.5mm TDFN package which is optimal for using with small devices.

Features

- Low Power Consumption
- 3.3V Supply Voltage
- RoHS Compliant / Halogen-Free
- Pb-Free TDFN-12 Package

Pin Configuration

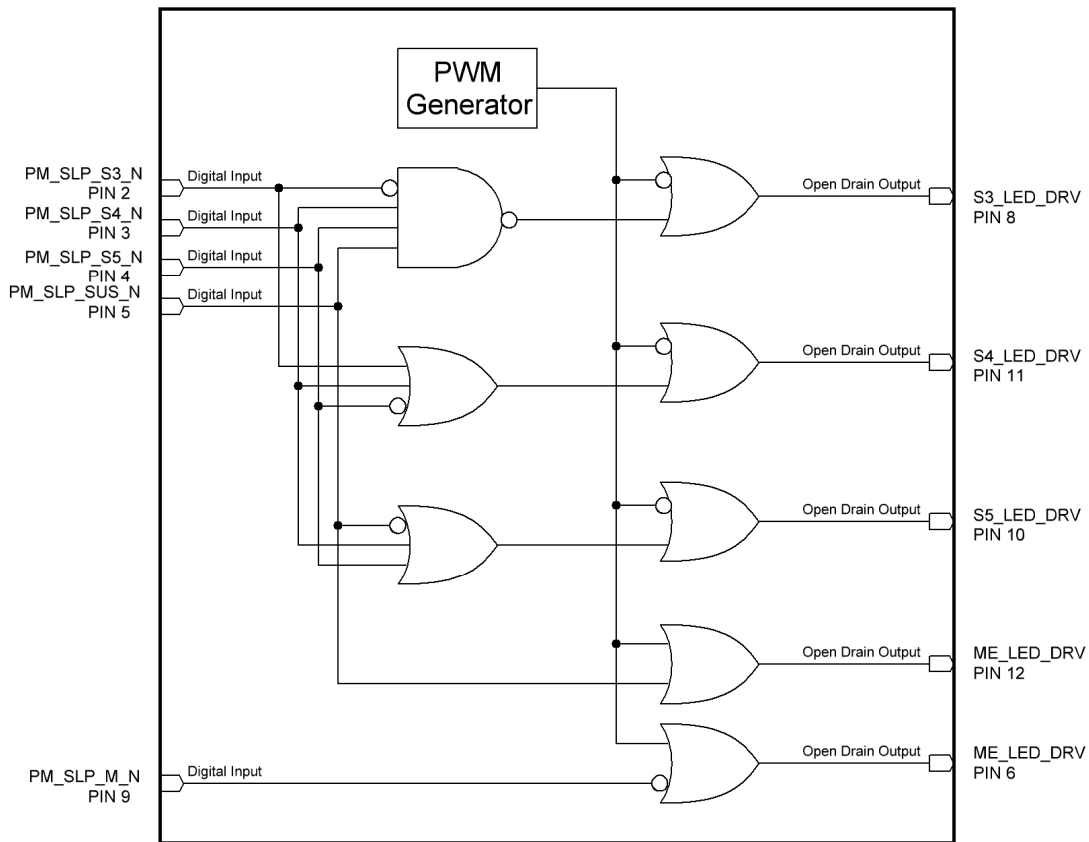


Output Summary

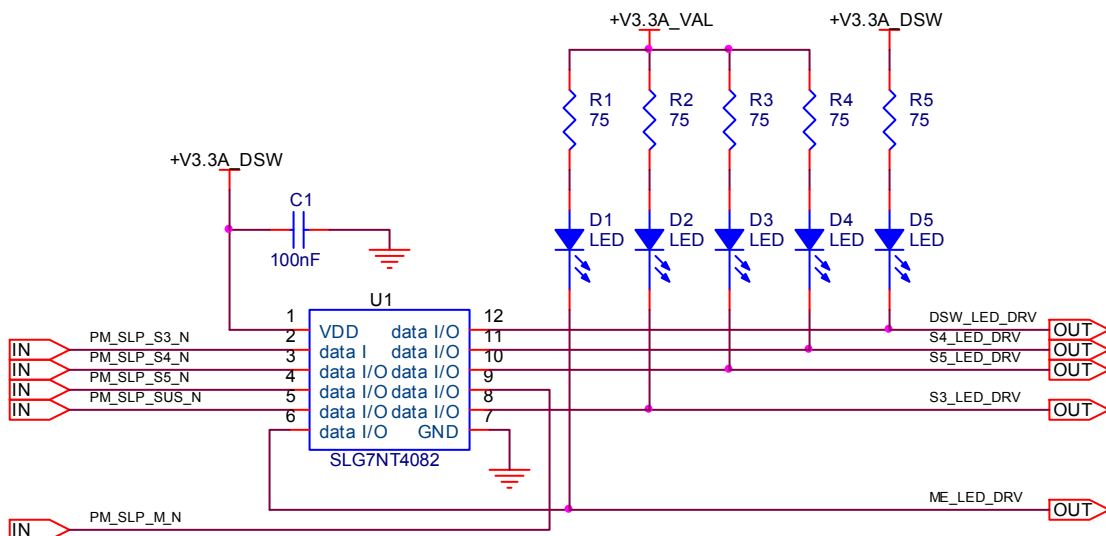
- 3 Outputs – Open Drain
- 2 Outputs – Open Drain Double Current



Block Diagram



Typical Application Circuit





Pin Configuration

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	Supply Voltage
2	PM_SLP_S3_N	Input	Digital Input
3	PM_SLP_S4_N	Input	Digital Input
4	PM_SLP_S5_N	Input	Digital Input
5	PM_SLP_SUS_N	Input	Digital Input
6	ME_LED_DRV	Output	Open Drain 2x current
7	GND	GND	Ground
8	S3_LED_DRV	Input	Open Drain
9	PM_SLP_M_N	Input	Digital Input
10	S5_LED_DRV	Output	Open Drain
11	S4_LED_DRV	Output	Open Drain
12	DSW_LED_DRV	Output	Open Drain 2x current
Exposed Bottom Pad	Exposed Bottom Pad	GND	Ground

Ordering Information

Part Number	Package Type
SLG7NT4082V	V = TDFN-12
SLG7NT4082VTR	VTR = TDFN-12 - Tape and Reel (3k units)



Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
V _{HIGH} to GND	-0.3	7	V
Voltage at input pins	-0.3	7	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	150	°C
Junction temperature	--	150	°C

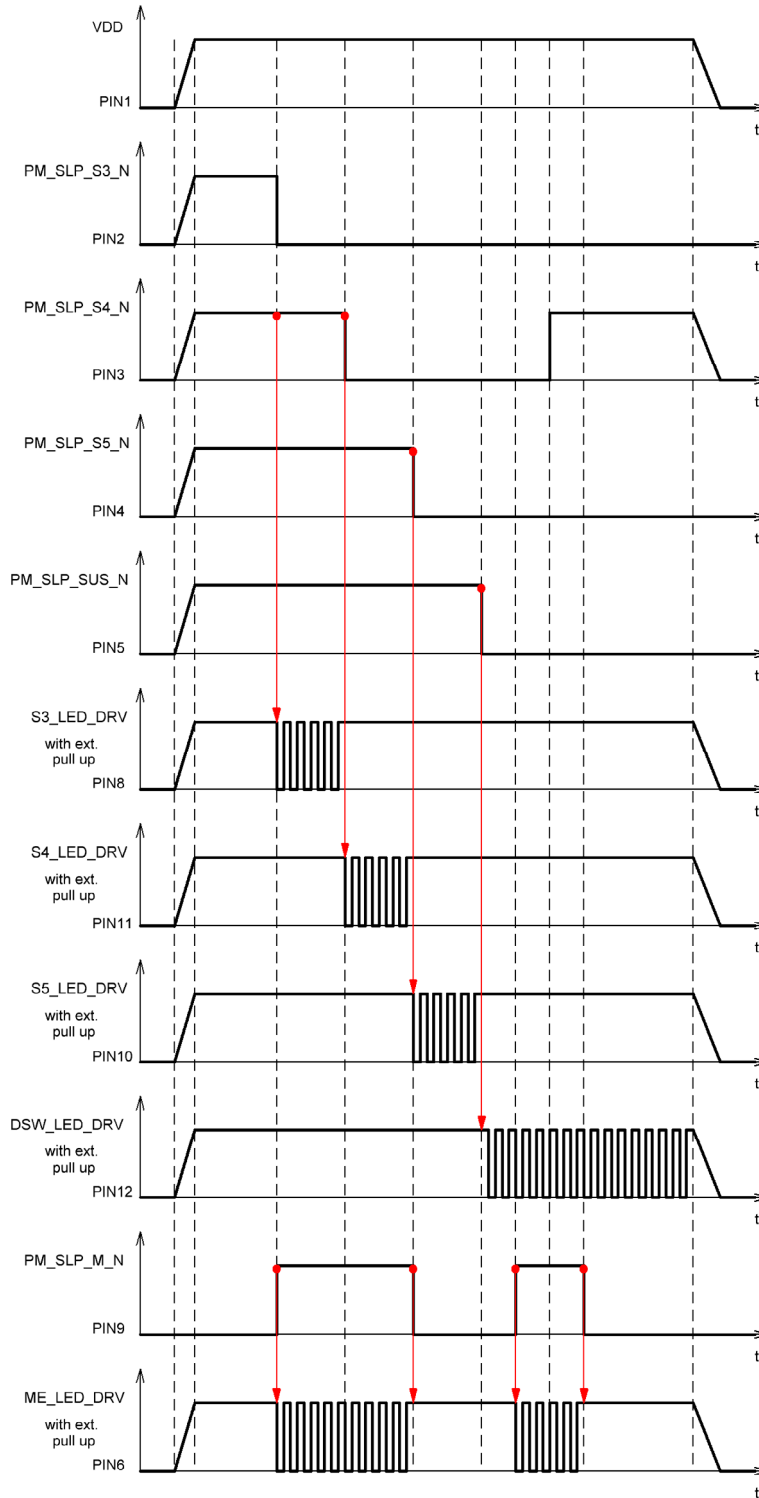
Electrical Characteristics

(@ 25°C, unless otherwise stated)

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage		3.0	3.3	3.6	V
I _Q	Quiescent Current	Static inputs and outputs	--	1	--	µA
T _A	Operating Temperature		-40	25	85	°C
I _L	Input Leakage Current	Leakage Current for Analog/Digital Inputs or outputs in High impedance state	-100	--	100	nA
V _{IH}	HIGH-Level Input Voltage	Logic Input at VDD=3.3V	1.8	--	--	V
V _{IL}	LOW-Level Input Voltage	Logic Input at VDD=3.3V	--	--	1.1	V
V _{OL}	Output Voltage Low	Open Drain Logic Level Output at VDD=3.3V, I _{OL} =20mA	--	--	0.605	V
V _{OL}	Output Voltage Low	Open Drain 2X Drive Logic Level Output at VDD=3.3V, I _{OL} =20mA	--	--	0.255	V
V _O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I _{OL}	LOW-Level Output Current	Open Drain Current at V _{OL} =0.605V	--	--	20	mA
I _{OL}	LOW-Level Output Current	Open Drain 2X Drive Current at V _{OL} =0.255V	--	--	20	mA
T _{SU}	Start up Time	After VDD reaches 1.6V	--	7	--	ms

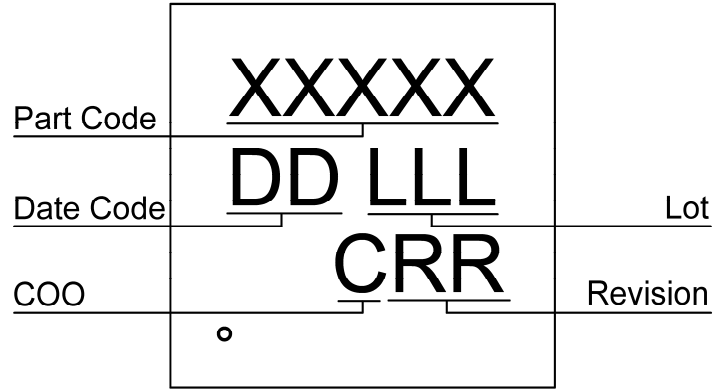


Timing Diagrams





Package Top Marking



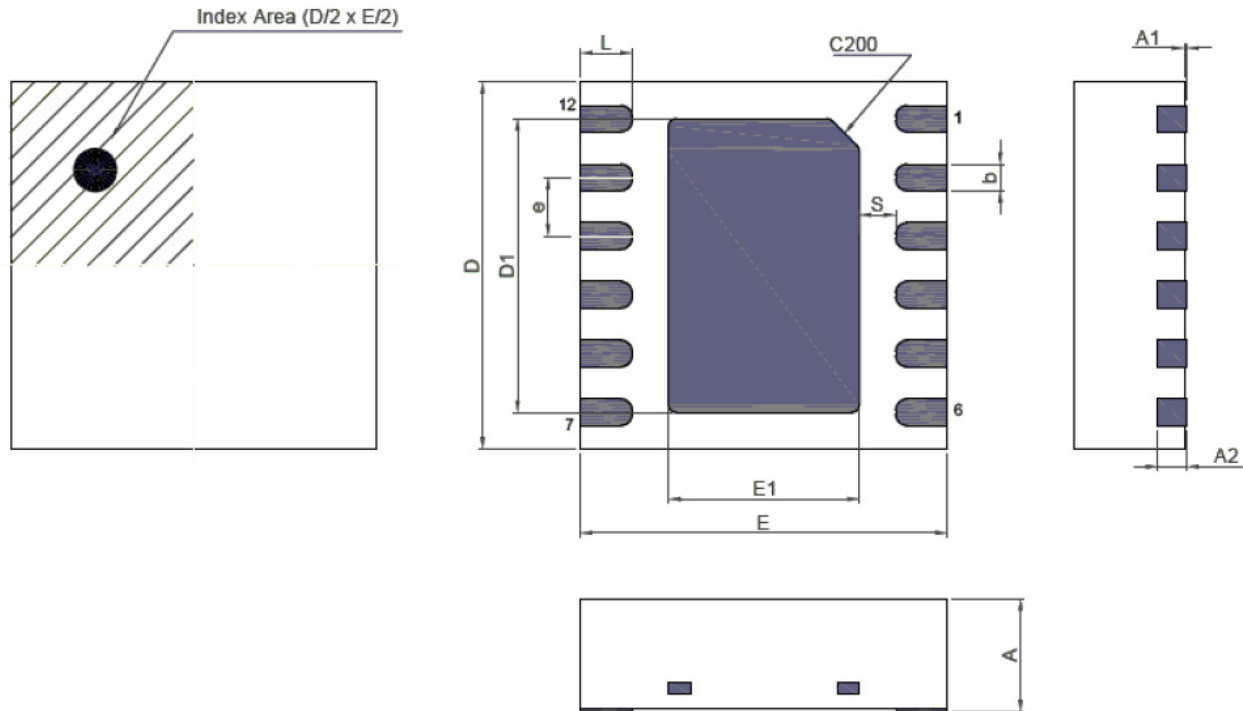
- XXXXX – Part Code Field: identifies the specific device configuration
- DD – Date Code Field: Coded date of manufacture
- LLL – Lot Code: Designates Lot #
- C – Assembly Site/COO: Specifies Assembly Site/Country of Origin
- RR – Revision Code: Device Revision

Datasheet Revision	Programming Code Number	Part Code	Revision	Date
1.01	06	4082V	AF	12/11/2012



Package Drawing and Dimensions

12 Lead TDFN Package JEDEC MO-229, Variation WDDE



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.70	0.75	0.80	D1	1.95	2.00	2.05
A1	0.005	-	0.060	E1	1.25	1.30	1.35
A2	0.15	0.20	0.25	e	0.40 BSC		
b	0.13	0.18	0.23	L	0.30	0.35	0.40
D	2.45	2.50	2.55	S	0.18	-	-
E	2.45	2.50	2.55				



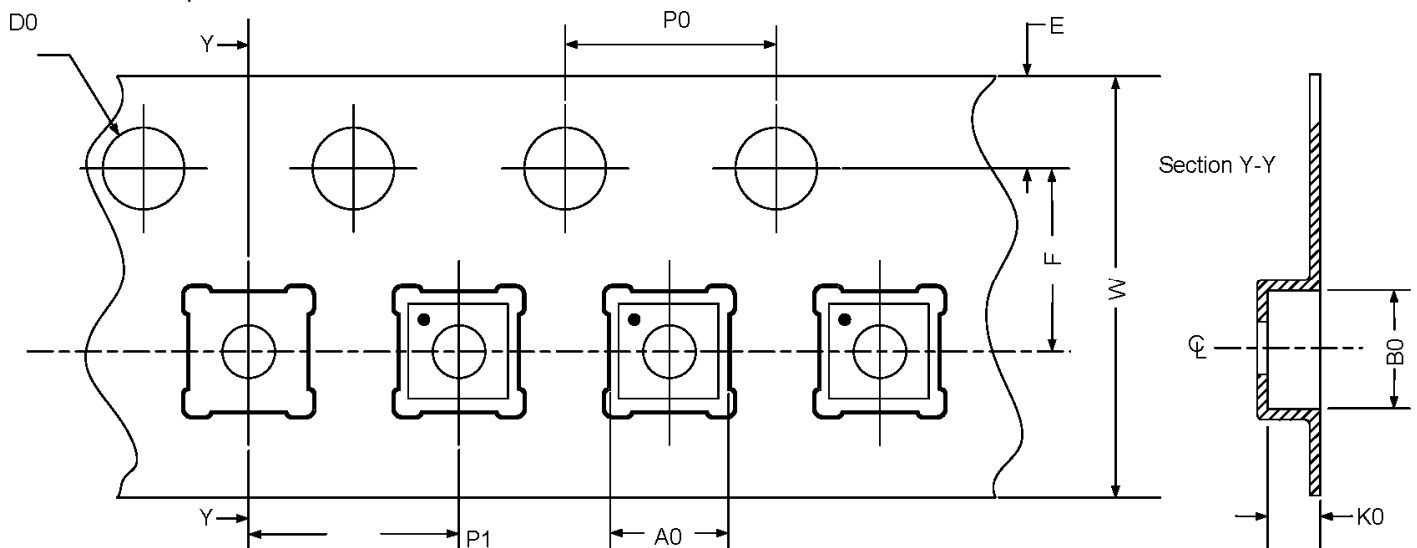
Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Trailer A		Leader B		Pocket (mm)	
			per reel	per box		Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
TDFN 12L 2.5x2.5mm 0.4P Green	12	2.5x2.5x0.75	3000	3000	178/60	42	168	42	168	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
TDFN 12L 2.5x2.5mm 0.4P Green	2.75	2.75	1.05	4	4	1.55	1.75	3.5	8

Refer to EIA-481 Specifications



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 4.6875 mm³ (nominal). More information can be found at www.jedec.org.



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