FOR INTERNAL USE ONLY

THIS DATASHEET IS FOR INTERNAL USE ONLY – DO NOT DISTRIBUTE OUTSIDE OF SILEGO AND INTEL.

SILEGO

Processor Power Validation

General Description

Silego SLG7NT41382 is a low power and small form device. The SoC is housed in a 2mm x 3mm STQFN package which is optimal for using with small devices.

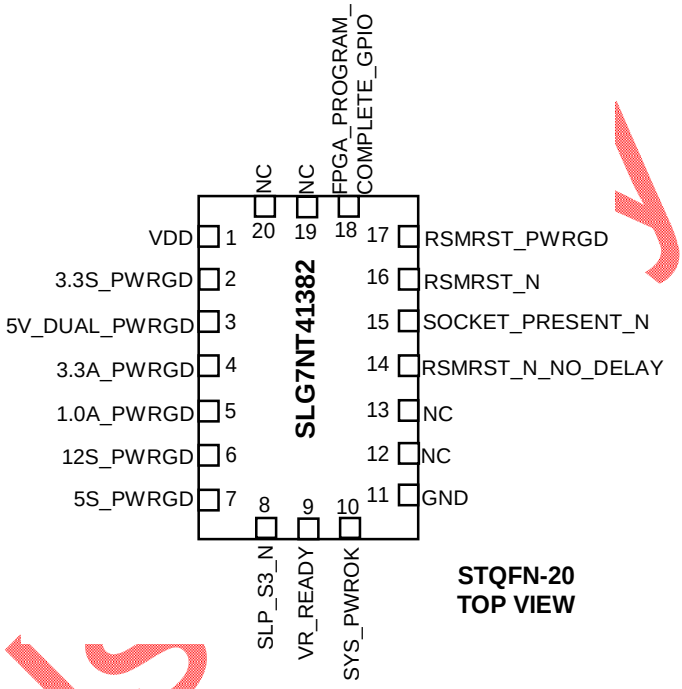
Features

- Low Power Consumption
- Pb-Free / RoHS Compliant
- Halogen-Free
- STQFN-20 Package

Output Summary

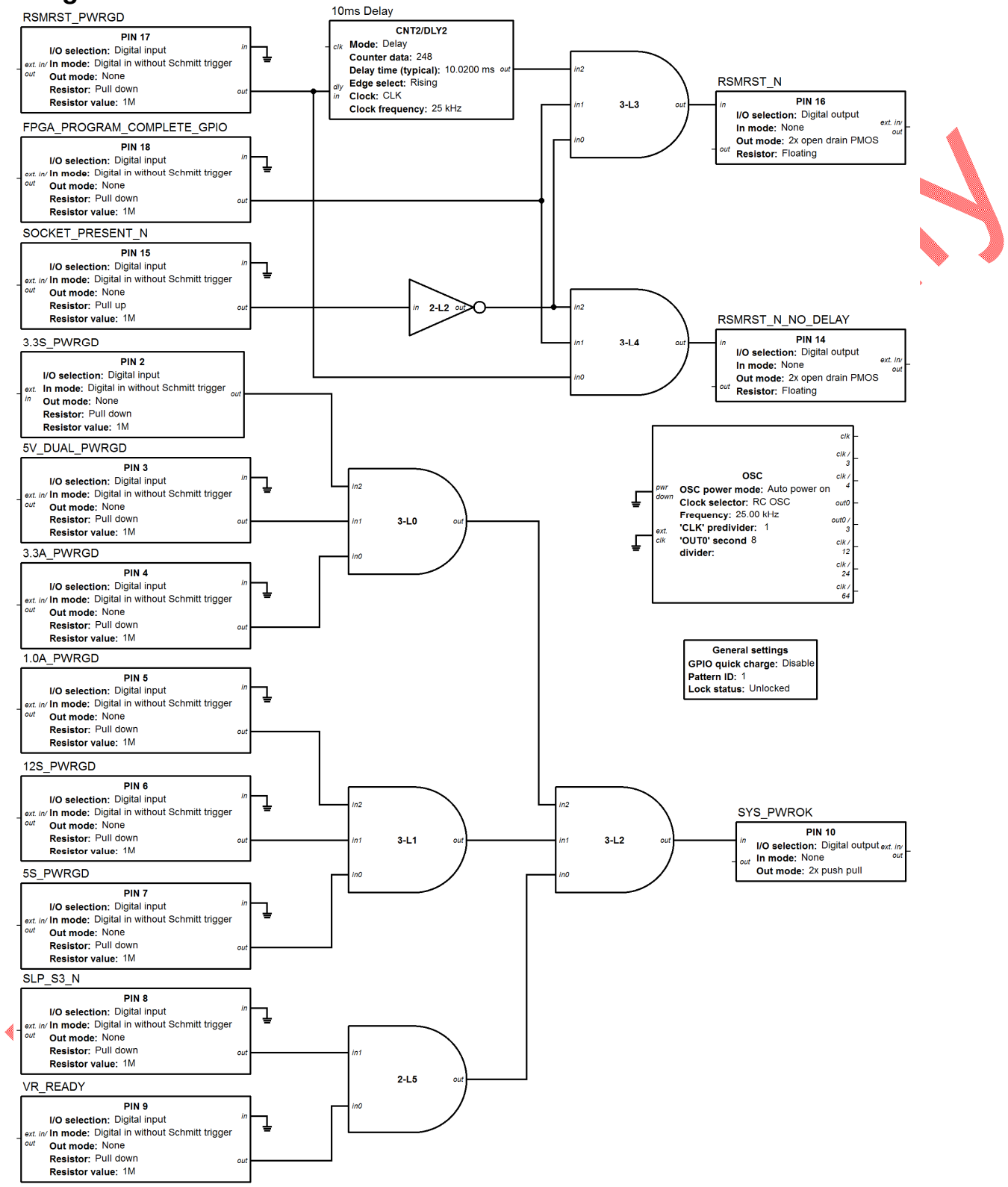
- 1 Output — Push Pull 2X
- 2 Outputs — Open Drain PMOS 2X

Pin Configuration



STQFN-20
TOP VIEW

Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	Supply Voltage
2	3.3S_PWRGD	Digital Input	Digital Input without Schmitt trigger
3	5V_DUAL_PWRGD	Digital Input	Digital Input without Schmitt trigger
4	3.3A_PWRGD	Digital Input	Digital Input without Schmitt trigger
5	1.0A_PWRGD	Digital Input	Digital Input without Schmitt trigger
6	12S_PWRGD	Digital Input	Digital Input without Schmitt trigger
7	5S_PWRGD	Digital Input	Digital Input without Schmitt trigger
8	SLP_S3_N	Digital Input	Digital Input without Schmitt trigger
9	VR_READY	Digital Input	Digital Input without Schmitt trigger
10	SYS_PWROK	Digital Output	Push Pull 2X
11	GND	GND	Ground
12	NC	--	Keep Floating or Connect to GND
13	NC	--	Keep Floating or Connect to GND
14	RSMRST_N_NO_DELAY	Digital Output	Open Drain PMOS 2X
15	SOCKET_PRESENT_N	Digital Input	Digital Input without Schmitt trigger
16	RSMRST_N	Digital Output	Open Drain PMOS 2X
17	RSMRST_PWRGD	Digital Input	Digital Input without Schmitt trigger
18	FPGA_PROGRAM_COMPLETE_GPIO	Digital Input	Digital Input without Schmitt trigger
19	NC	--	Keep Floating or Connect to GND
20	NC	--	Keep Floating or Connect to GND

Ordering Information

Part Number	Package Type
SLG7NT41382V	V=STQFN-20
SLG7NT41382VTR	VTR=STQFN-20 – Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
V_{HIGH} to GND	-0.3	7	V
Voltage at input pins	-0.3	7	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	125	°C
Junction temperature	--	150	°C
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1300	--	V
Moisture Sensitivity Level	1		

Electrical Characteristics

(@ 25°C, unless otherwise stated)

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.71	3.3	5.5	V
T_A	Operating Temperature		-40	25	85	°C
I_Q	Quiescent Current	Static inputs and outputs	--	1	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_O	Maximal Average or DC Current (note 1)	Per Each Chip Side (PIN2-PIN10, PIN12-PIN20)	--	--	90	mA
V_{IH}	HIGH-Level Input Voltage	Logic Input, at VDD=1.8V	1.10	--	VDD	V
		Logic Input, at VDD=3.3V	1.78	--	VDD	
		Logic Input, at VDD=5.0V	2.64	--	VDD	
V_{IL}	LOW-Level Input Voltage	Logic Input, at VDD=1.8V	--	--	0.69	V
		Logic Input, at VDD=3.3V	--	--	1.21	
		Logic Input, at VDD=5.0V	--	--	1.84	
I_{IH}	HIGH-Level Input Current	Logic Input PINs; V_{IN} = VDD	-1.0	--	1.0	µA
I_{IL}	LOW-Level Input Current	Logic Input PINs; V_{IN} = 0V	-1.0	--	1.0	µA
V_{OH}	HIGH-Level Output Voltage	Push Pull & PMOS OD, I_{OH} = 100uA, 2X Driver, at VDD=1.8 V	1.7	1.794	--	V
		Push Pull & PMOS OD, I_{OH} = 3mA, 2X Driver, at VDD=3.3 V	2.87	3.21	--	
		Push Pull & PMOS OD, I_{OH} = 5mA, 2X Driver, at VDD=5.0 V	4.32	4.89	--	
V_{OL}	LOW-Level Output Voltage	Push Pull, I_{OL} = 100uA, 2X Driver, at VDD=1.8 V	--	0.004	0.01	V
		Push Pull, I_{OL} = 3mA, 2X Driver, at VDD=3.3 V	--	0.060	0.108	
		Push Pull, I_{OL} = 5mA, 2X Driver, at VDD=5.0 V	--	0.076	0.140	
I_{OH}	HIGH-Level Output Current	Push Pull & PMOS OD, V_{OH} = V_{DD}-0.2, 2X Driver, at VDD=1.8 V	2.216	3.406	--	mA

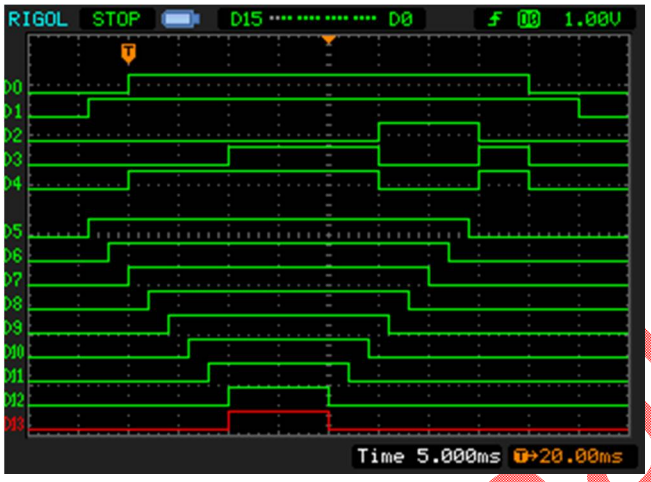
		Push Pull & PMOS OD, V_{OH} = 2.4 V, 2X Driver, at VDD=3.3 V	11.522	24.16	--	
		Push Pull & PMOS OD, V_{OH} = 2.4 V, 2X Driver, at VDD=5.0 V	41.69	68.08	--	
I_{OL}	LOW-Level Output Current	Push Pull, V_{OL} =0.15V, 2X Driver, at VDD=1.8 V	1.834	3.378	--	mA
		Push Pull, V_{OL} =0.4V, 2X Driver, at VDD=3.3 V	9.750	16.488	--	
		Push Pull, V_{OL} =0.4V, 2X Driver, at VDD=5.0 V	13.831	23.16	--	
R_{PULL_UP}	Internal Pull Up Resistance	Pull up on PIN 15	700	1000	1300	kΩ
R_{PULL_DOWN}	Internal Pull Down Resistance	Pull down on PINs 2, 3, 4, 5, 6, 7, 8, 9, 17, 18	700	1000	1300	kΩ
T_{DLY2}	Delay2 Time	At temperature 25°C	9.02	10.02	10.52	ms
		At temperature -40°C +85°C (note 1)	8.17	10.02	12.45	
T_{SU}	Start up Time	From VDD rising past 1.35V	--	0.3	--	ms

1. Guaranteed by Design.

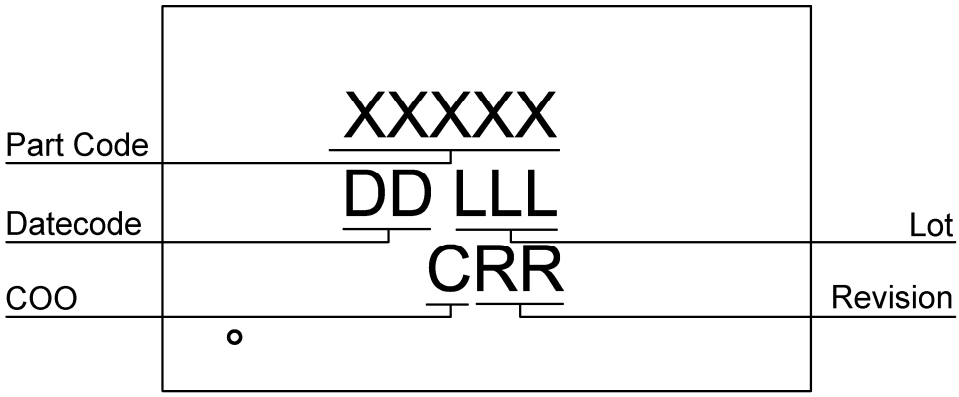
Functionality Waveforms

D0 – PIN#17 (RSMRST_PWRGD)
D1 – PIN#18 (FPGA_PROGRAM_COMPLETE_GPIO)
D2 – PIN#15 (SOCKET_PRESENT_N)
D3 – PIN#16 (RSMRST_N) with external 5kΩ pull down resistor
D4 – PIN#14 (RSMRST_N_NO_DELAY) with external 5kΩ pull down resistor
D5 – PIN#2 (3.3S_PWRGD)
D6 – PIN#3 (5V_DUAL_PWRGD)
D7 – PIN#4 (3.3A_PWRGD)
D8 – PIN#5 (1.0A_PWRGD)
D9 – PIN#6 (12S_PWRGD)
D10 – PIN#7 (5S_PWRGD)
D11 – PIN#8 (SLP_S3_N)
D12 – PIN#9 (VR_READY)
D13 – PIN#10 (SYS_PWROK)

1. Device functionality



Package Top Marking



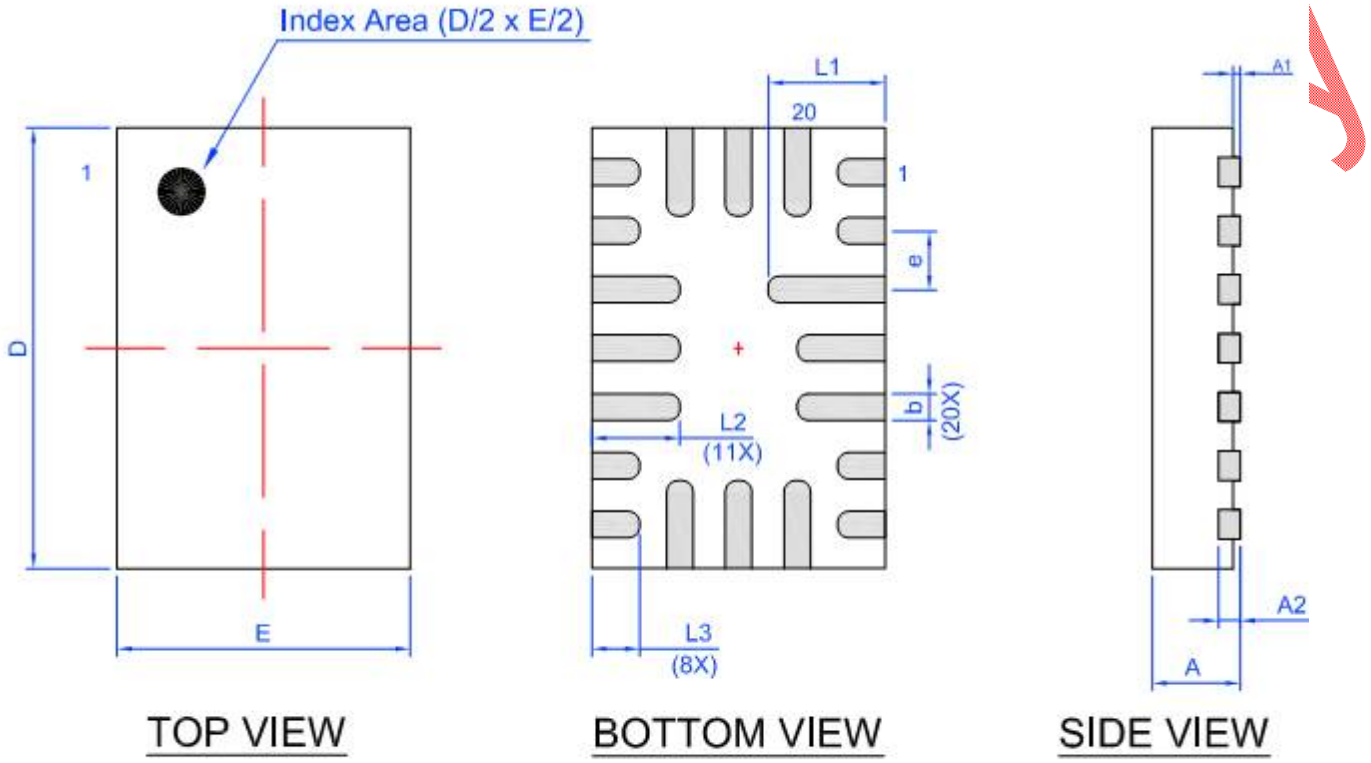
XXXXX – Part ID Field: identifies the specific device configuration
DD – Date Code Field: Coded date of manufacture
LLL – Lot Code: Designates Lot #
C – Assembly Site/COO: Specifies Assembly Site/Country of Origin
RR – Revision Code: Device Revision

Datasheet Revision	Programming Code Number	Locked Status	Part Code	Revision	Date
1.00	001	L	41382	AA	11/18/2016

The IC security bit is locked/set for code security for production unless otherwise specified. Revision number is not changed for bit locking.

Package Drawing and Dimensions

20 Lead STQFN Package
JEDEC MO-220, Variation WECE
IC Net Weight: 0.0086 g



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L1	0.75	0.80	0.85
b	0.13	0.18	0.23	L2	0.55	0.60	0.65
e	0.40 BSC			L3	0.275	0.325	0.375

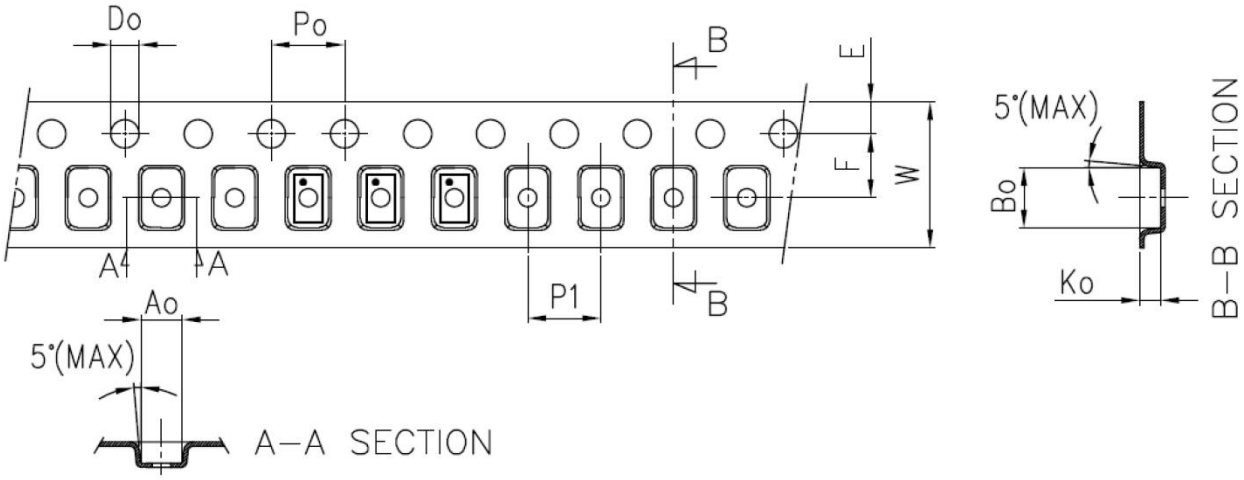
Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Trailer A		Leader B		Pocket (mm)	
			per reel	per box		Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
STQFN 20L 2x3mm 0.4P Green	20	2x3x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2x3mm 0.4P Green	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8

Refer to EIA-481 Specifications



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.3 mm^3 (nominal).
More information can be found at www.jedec.org.

Datasheet Revision History

Date	Version	Change
08/19/2016	0.10	New design for SLG46722 chip
09/12/2016	0.11	Updated Device Revision History
11/16/2016	0.12	Locked NVM
11/18/2016	1.00	Production Release

Silego Website & Support

Silego Technology Website

Silego Technology provides online support via our website at http://www.silego.com/.This website is used as a means to make files and information easily available to customers.

For more information regarding Silego Green products, please visit our website.

Our Green product lines feature:

GreenPAK1 / GreenPAK2 / GreenPAK3/ GreenPAK 4 / GreenPAK 5: Programmable Mixed Signal Matrix products
GreenFET1 / GreenFET3: MOSFET Drivers and ultra-small, low RDSon Load Switches
GreenCLK1 / GreenCLK2 / GreenCLK3: Crystal replacement technology

Products are also available for purchase directly from Silego at the Silego Online Store at http://www.silego.com/buy/ .

Silego Technical Support

Datasheets and errata, application notes and example designs, user guides, and hardware support documents and the latest software releases are available at the Silego website or can be requested directly at info@silego.com.

For specific GreenPAK design or applications questions and support please send e-mail requests to GreenPAK@silego.com

Users of Silego products can receive assistance through several channels:

Contact Your Local Sales Representative

Customers can contact their local sales representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. More information regarding your local representative is available at the Silego website or send a request to info@silego.com

Contact Silego Directly

Silego can be contacted directly via e-mail at info@silego.com or user submission form, located at the following URL: http://support.silego.com/

Other Information

The latest Silego Technology press releases, listing of seminars and events, listings of world wide Silego Technology offices and representatives are all available at http://www.silego.com/

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE

SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. SILEGO TECHNOLOGY DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. SILEGO TECHNOLOGY RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE