SILEGO

SLG7NT41502

CURIE BASED WEARABLE

General Description

Silego SLG7NT41502 is a low power and small form device. The SoC is housed in a 1.6 x 2.0 mm STQFN package which is optimal for using with small devices.

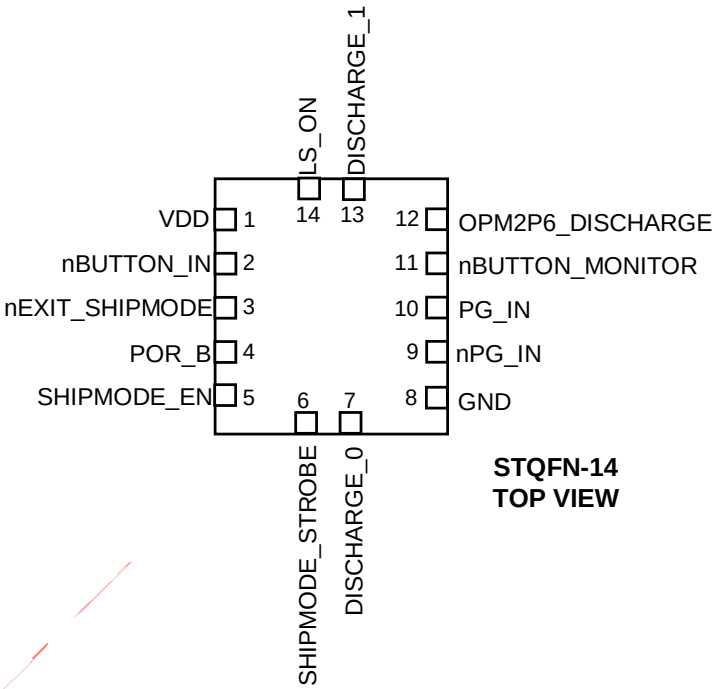
Features

- Low Power Consumption
- Pb-Free / RoHS Compliant
- Halogen-Free
- STQFN-14 Package

Output Summary

- 1 Output — Push Pull 2X
- 1 Output — Open Drain NMOS 1X
- 3 Outputs — Open Drain NMOS 2X

Pin Configuration



STQFN-14
TOP VIEW

Pin Configuration

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	Supply Voltage
2	nBUTTON_IN	Digital Input	Digital Input with Schmitt trigger
3	nEXIT_SHIPMODE	Digital Input	Digital Input with Schmitt trigger
4	POR_B	Digital Input	Low Voltage Digital input
5	SHIPMODE_EN	Digital Input	Low Voltage Digital input
6	SHIPMODE_STROBE	Digital Input	Low Voltage Digital input
7	DISCHARGE_0	Digital Output	Open Drain NMOS 2X
8	GND	GND	Ground
9	nPG_IN	Digital Input	Digital Input with Schmitt trigger
10	PG_IN	Digital Input	Digital Input with Schmitt trigger
11	nBUTTON_MONITOR	Digital Output	Open Drain NMOS 1X
12	OPM2P6_DISCHARGE	Digital Output	Open Drain NMOS 2X
13	DISCHARGE_1	Digital Output	Open Drain NMOS 2X
14	LS_ON	Digital Output	Push Pull 2X

Ordering Information

Part Number	Package Type
SLG7NT41502V	V=STQFN-14
SLG7NT41502VTR	STQFN-14 – Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
V_{HIGH} to GND	-0.3	7	V
Voltage at input pins	-0.3	7	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	125	°C
Junction temperature	--	150	°C
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1000	--	V
Moisture Sensitivity Level	1		

Electrical Characteristics

(@ 25°C, unless otherwise stated)

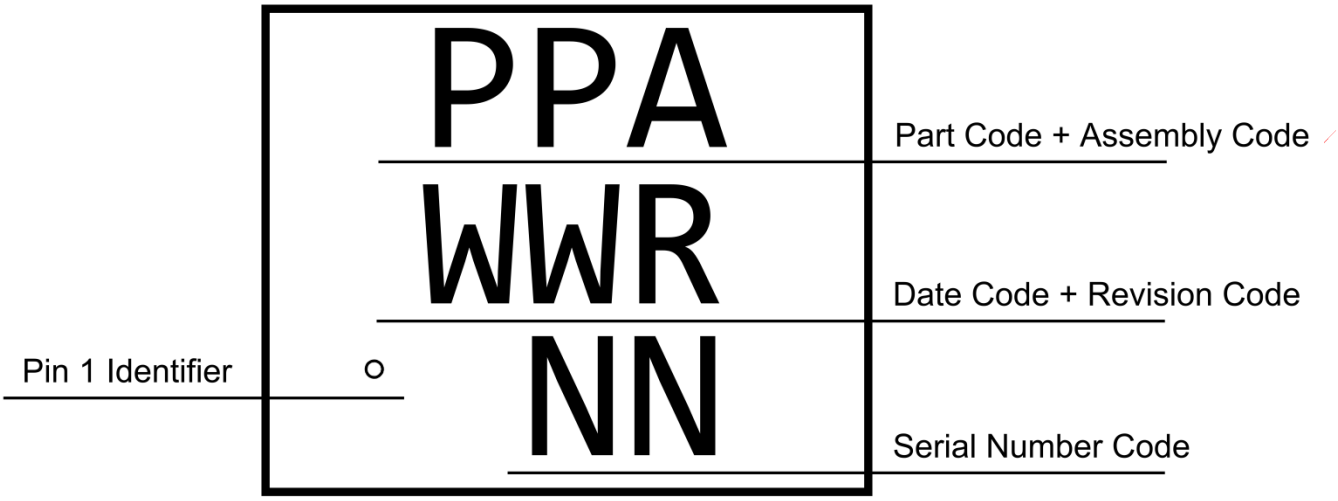
Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.71	3.6	5.5	V
T_A	Operating Temperature		-40	25	85	°C
I_Q	Quiescent Current	Static inputs and floating outputs PIN4 = 1; PIN14 = 1; DFF4 = 0 @VDD = 3.3V	--	1	--	µA
		Static inputs and outputs PIN4 = 0; PIN14 = 0; DFF4 = 1 @VDD = 3.3V	--	1	--	
		Static inputs and outputs PIN4 = 1; PIN14 = 1; DFF4 = 0 @VDD = 5.5V	--	1	--	
		Static inputs and outputs PIN4 = 0; PIN14 = 0; DFF4 = 1 @VDD = 5.5V	--	1	--	
I_A	Active Current	Static outputs PIN4 = 0; PIN14 = 1; DFF4 = 0 @VDD = 3.7V	--	50	--	µA
		Static outputs PIN4 = 0; PIN14 = 0; DFF4 = 0 @VDD = 3.3V	--	1.8	--	
		Static outputs PIN4 = 0; PIN14 = 1; DFF4 = 0 @VDD = 5.5V	--	50	--	
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_O	Maximal Average or DC Current (note 1)	Per Each Chip Side	--	--	90	mA
V_{IH}	HIGH-Level Input Voltage (Note 2)	Logic Input with Schmitt Trigger, at VDD=1.8V At temperature -45°C +85°C (note 1)	1.27	--	VDD	V
		Low-Level Logic Input, at VDD=1.8V At temperature -45°C +85°C (note 1)	0.98	--	VDD	
		Logic Input with Schmitt Trigger, at VDD=3.3V At temperature -45°C +85°C (note 1)	2.13	--	VDD	

		Low-Level Logic Input, at VDD=3.3V At temperature -45°C +85°C (note 1)	1.13	--	VDD	
		Logic Input with Schmitt Trigger, at VDD=5.0V At temperature -45°C +85°C (note 1)	3.16	--	VDD	
		Low-Level Logic Input, at VDD=5.0V At temperature -45°C +85°C (note 1)	1.23	--	VDD	
V_{IL}	LOW-Level Input Voltage (Note 2)	Logic Input with Schmitt Trigger, at VDD=1.8V	--	--	0.44	V
		Low-Level Logic Input, at VDD=1.8V At temperature -45°C +85°C (note 1)	--	--	0.52	
		Logic Input with Schmitt Trigger, at VDD=3.3V At temperature -45°C +85°C (note 1)	--	--	0.95	
		Low-Level Logic Input, at VDD=3.3V At temperature -45°C +85°C (note 1)	--	--	0.69	
		Logic Input with Schmitt Trigger, at VDD=5.0V At temperature -45°C +85°C (note 1)	--	--	1.51	
		Low-Level Logic Input, at VDD=5.0V At temperature -45°C +85°C (note 1)	--	--	0.78	
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.273	--	0.792	V
I_{IH}	HIGH-Level Input Current	Logic Input PINs; V_{IN} = VDD	-1.0	--	1.0	µA
I_{IL}	LOW-Level Input Current	Logic Input PINs; V_{IN} = 0V	-1.0	--	1.0	µA
V_{OH}	HIGH-Level Output Voltage (note 1)	Push Pull, I_{OH} = 100uA, 2X Driver, at VDD=1.8 V At temperature -45°C +85°C (note 1)	1.679	1.792	--	V
		Push Pull, I_{OH} = 3mA, 2X Driver, at VDD=3.3 V At temperature -45°C +85°C (note 1)	2.861	3.201	--	
		Push Pull, I_{OH} = 5mA, 2X Driver, at VDD=5.0 V At temperature -45°C +85°C (note 1)	4.330	4.878	--	
V_{OL}	LOW-Level Output Voltage (note 1)	Open Drain, I_{OL} = 100uA, 1X Driver, at VDD=1.8 V At temperature -45°C +85°C (note 1)	--	0.007	0.010	V
		Push Pull, I_{OL} = 100uA, 2X Driver, at VDD=1.8 V At temperature -45°C +85°C (note 1)	--	0.007	0.010	
		Open Drain, I_{OL} = 100uA, 2X Driver, at VDD=1.8 V At temperature -45°C +85°C (note 1)	--	0.002	0.010	
		Open Drain, I_{OL} = 3mA, 1X Driver, at VDD=3.3 V At temperature -45°C +85°C (note 1)	--	0.070	0.130	
		Push Pull, I_{OL} = 3mA, 2X Driver, at VDD=3.3 V At temperature -45°C +85°C (note 1)	--	0.079	0.130	

		Open Drain, I_{OL} = 3mA, 2X Driver, at VDD=3.3 V At temperature -45°C +85°C (note 1)	--	0.040	0.070	
		Open Drain, I_{OL} = 5mA, 1X Driver, at VDD=5.0 V At temperature -45°C +85°C (note 1)	--	0.090	0.160	
		Push Pull, I_{OL} = 5mA, 2X Driver, at VDD=5.0 V At temperature -45°C +85°C (note 1)	--	0.101	0.160	
		Open Drain, I_{OL} = 5mA, 2X Driver, at VDD=5.0 V At temperature -45°C +85°C (note 1)	--	0.050	0.080	
I_{OH}	HIGH-Level Output Current (note 1)	Push Pull & PMOS OD, V_{OH} = V_{DD}-0.2, 2X Driver, at VDD=1.8 V At temperature -45°C +85°C (note 1)	2.069	3.390	--	mA
		Push Pull & PMOS OD, V_{OH} = 2.4 V, 2X Driver, at VDD=3.3 V At temperature -45°C +85°C (note 1)	11.278	21.634	--	
		Push Pull & PMOS OD, V_{OH} = 2.4 V, 2X Driver, at VDD=5.0 V At temperature -45°C +85°C (note 1)	40.059	59.691	--	
I_{OL}	LOW-Level Output Current (note 1)	Push Pull, V_{OL} =0.15V, 2X Driver, at VDD=1.8 V At temperature -45°C +85°C (note 1)	1.52	2.840	--	mA
		Open Drain, V_{OL} =0.15V, 1X Driver, at VDD=1.8 V At temperature -45°C +85°C (note 1)	1.530	2.840	--	
		Open Drain, V_{OL} =0.15V, 2X Driver, at VDD=1.8 V At temperature -45°C +85°C (note 1)	3.060	5.680	--	
		Push Pull, V_{OL} =0.4V, 2X Driver, at VDD=3.3 V At temperature -45°C +85°C (note 1)	8.130	13.840	--	
		Open Drain, V_{OL} =0.4V, 1X Driver, at VDD=3.3 V At temperature -45°C +85°C (note 1)	8.130	13.850	--	
		Open Drain, V_{OL} =0.4V, 2X Driver, at VDD=3.3 V At temperature -45°C +85°C (note 1)	16.260	23.700	--	
		Push Pull, V_{OL} =0.4V, 2X Driver, at VDD=5.0 V At temperature -45°C +85°C (note 1)	12.020	19.460	--	
		Open Drain, V_{OL} =0.4V, 1X Driver, at VDD=5.0 V At temperature -45°C +85°C (note 1)	12.030	19.460	--	
		Open Drain, V_{OL} =0.4V, 2X Driver, at VDD=5.0 V At temperature -45°C +85°C (note 1)	24.060	38.920	--	

V_{ACMP0}	Analog Comparator Threshold Voltage	Low to High transition, at temperature 25°C.	3532.7	3582.9	3633.1	mV
		Low to High transition, at temperature -40 +85°C (note 1)	3519.7	3579.8	3644.2	
		High to Low transition, at temperature 25°C	2948.8	2991.5	3034.2	
		High to Low transition, at temperature -40 +85°C (note 1)	2937.1	2988.1	3040.9	
G_{ACMP0}	Analog Comparator0 IN+ gain	ACMP 0	--	0.33	--	
V_{HYST}	Analog Comparator Hysteresis Voltage (note 1)	ACMP 0	--	200	--	mV
R_{PULL_UP}	Internal Pull Up Resistance	Pull up on PIN 2, 3	70	100	130	kΩ
R_{PULL_DOWN}	Internal Pull Down Resistance	Pull down on PINs 5, 6	70	100	130	kΩ
RDIS	Discharge Resistance	External resistor on PIN7, PIN12 and PIN13	270	--	--	Ω
T_{CNT0}	Counter0 Period (WS Ctrl)	At temperature 25°C	153.14	176.87	207.44	ms
		At temperature -40°C +85°C (note 1)	153.14	178.87	217.81	
T_{DLY1}	Delay1 Time	At temperature 25°C	195.04	200.45	206.90	ms
		At temperature -40°C +85°C (note 1)	184.59	200.45	216.47	
T_{DLY2}	Delay2 Time	At temperature 25°C	486.52	500.02	516.10	ms
		At temperature -40°C +85°C (note 1)	460.44	500.02	539.10	
T_{DLY3}	Delay3 Time	At temperature 25°C	195.04	200.45	206.90	ms
		At temperature -40°C +85°C (note 1)	184.59	200.45	216.47	
T_{SU}	Start up Time	From VDD rising past PON_{THR}	0.462	1.4	4.999	ms
PON_{THR}	Power On Threshold	VDD Level Required to Start Up the Chip	0.961	1.312	1.659	V
$POFF_{THR}$	Power Off Threshold	VDD Level Required to Switch Off the Chip	0.875	1.109	1.288	V

1. Guaranteed by Design.
2. No hysteresis for Low Voltage Digital Input

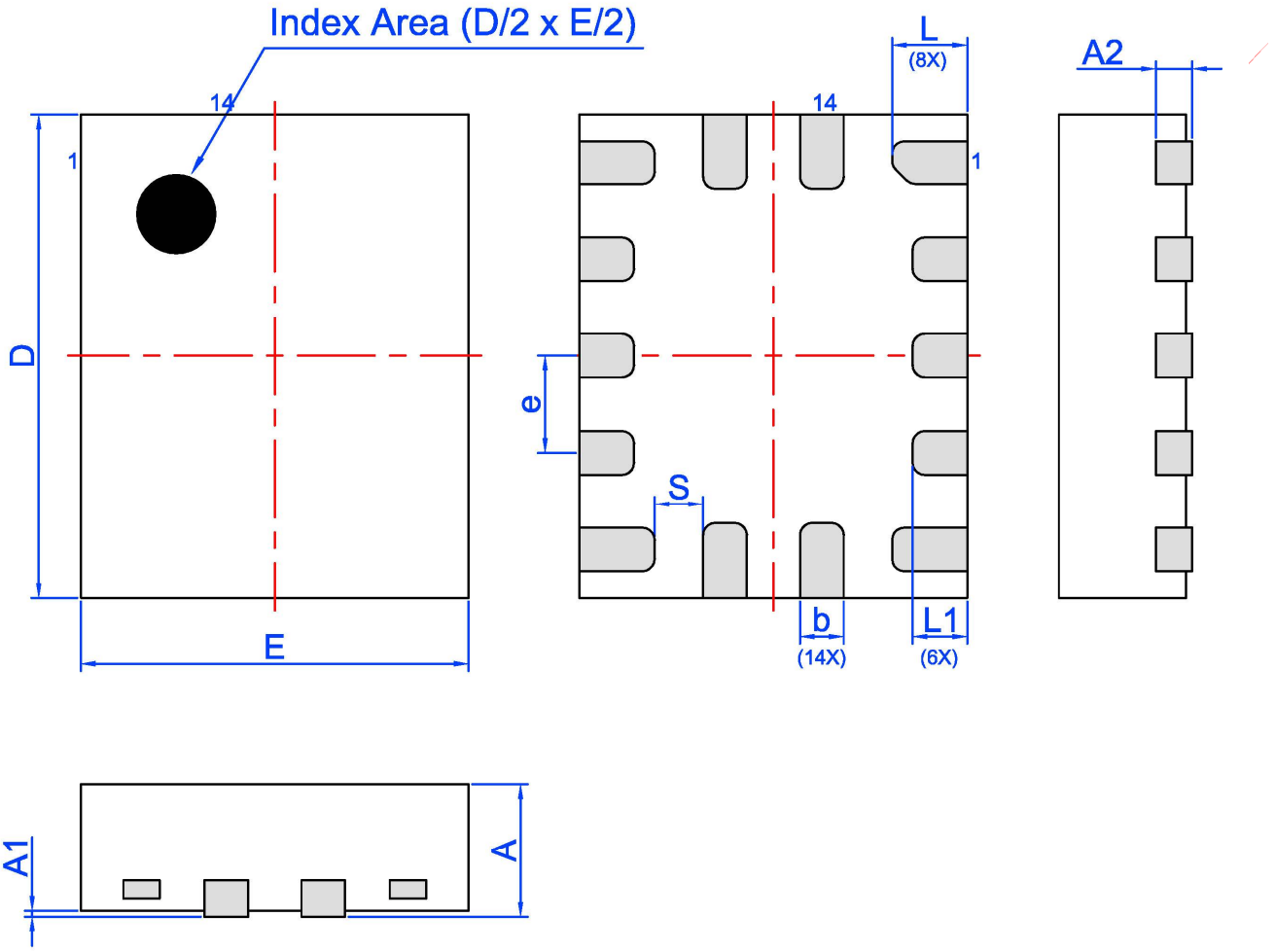


Datasheet Revision	Programming Code Number	Locked Status	Part Code	Revision	Date
1.04	002	L	V6	B	01/23/2017

The IC security bit is locked/set for code security for production unless otherwise specified. Revision number is not changed for bit locking.

Package Drawing and Dimensions

14 Lead STQFN Package



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.95	2.00	2.05
A1	0.005	-	0.060	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.26	0.31	0.36
b	0.13	0.18	0.23	L1	0.175	0.225	0.275
e	0.40 BSC			S	0.2 REF		

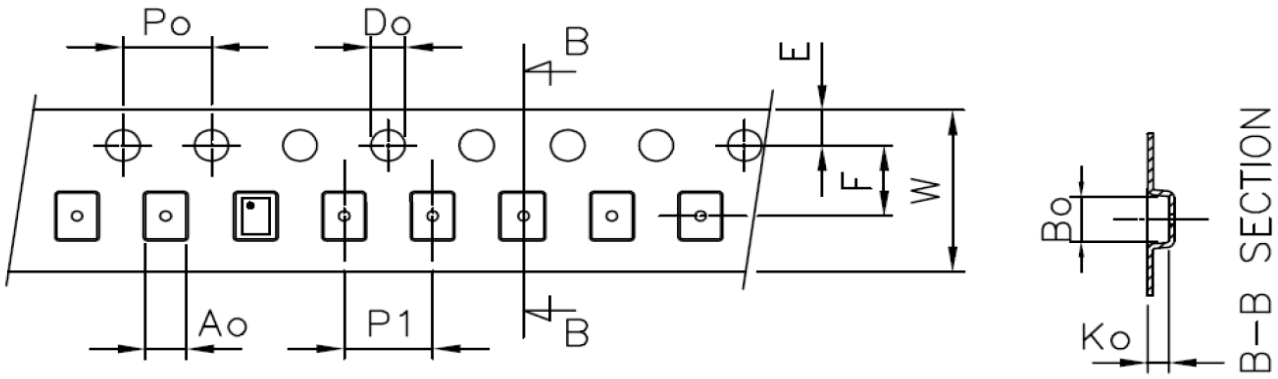
Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Trailer A		Leader B		Pocket (mm)	
			per reel	per box		Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
STQFN 14L FC 0.4P Green	14	1.6x2.0x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 14L FC 0.4P Green	1.9	2.3	0.8	4	4	1.5	1.75	3.5	8

Refer to EIA-481 Specifications



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 1.76 mm^3 (nominal). More information can be found at www.jedec.org.

Silego Website & Support

Silego Technology Website

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Datasheets and errata, application notes and example designs, user guides, and hardware support documents and the latest software releases are available at the Silego website or can be requested directly at info@silego.com.

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