

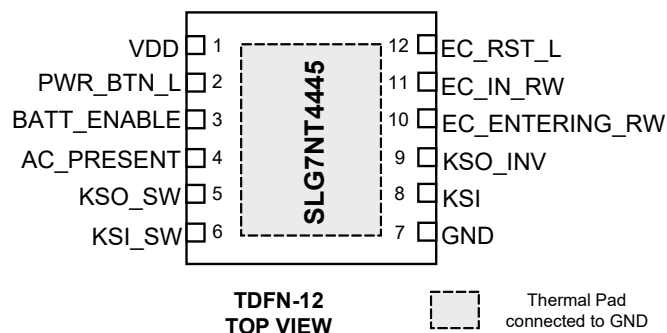
General Description

Renesas GreenPAK 2 SLG7NT4445 is a low power and small form device. The SoC is housed in a 2.5mm x 2.5mm TDFN package which is optimal for using with small devices.

Features

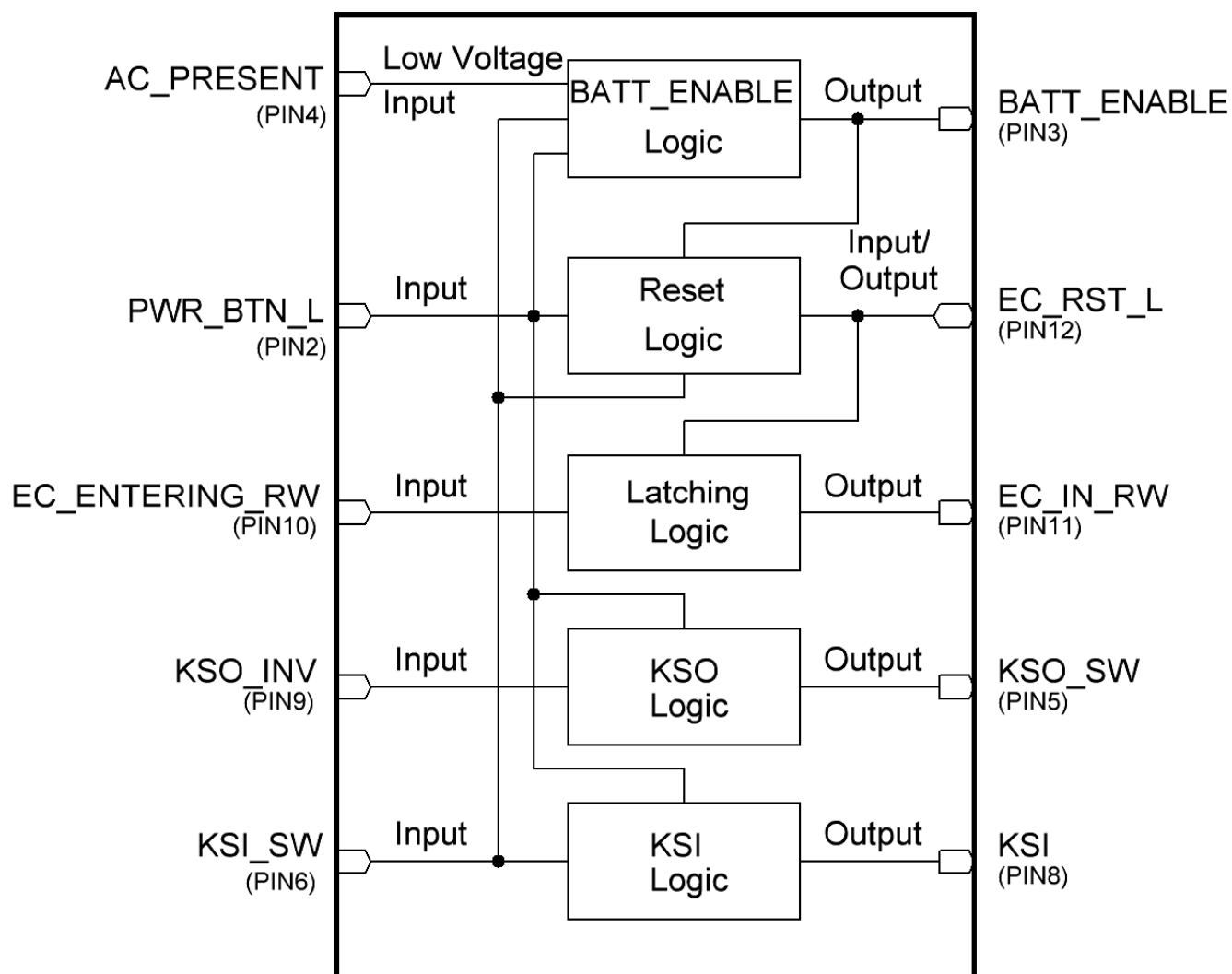
- Low Power Consumption
- Dynamic Voltage Supply Range
- RoHS Compliant / Halogen-Free
- Pb-Free TDFN-12 Package
- MSL1

Pin Configuration



Output Summary

- 1 Output — Push Pull 1X
- 4 Outputs — Open Drain NMOS 1X

Block Diagram



Reset IC with Latch and MUX

Pin Configuration

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	Supply Voltage
2	PWR_BTN_L	Digital Input	Digital Input with Schmitt trigger
3	BATT_ENABLE	Digital Output	Open Drain NMOS 1X
4	AC_PRESENT	Digital Input	Low Voltage Digital Input
5	KSO_SW	Digital Output	Open Drain NMOS 1X
6	KSI_SW	Digital Input	Digital Input with Schmitt trigger
7	GND	GND	Ground
8	KSI	Digital Output	Open Drain NMOS 1X
9	KSO_INV	Digital Input	Digital Input with Schmitt trigger
10	EC_ENTERING_RW	Digital Input	Digital Input with Schmitt trigger
11	EC_IN_RW	Digital Output	Open Drain NMOS 1X
12	EC_RST_L	Bi-directional	Digital Input with Schmitt trigger / Push Pull 1X
Exposed Bottom Pad	Exposed Bottom Pad	GND	Ground

Ordering Information

Part Number	Package Type
SLG7NT4445V	V = TDFN-12
SLG7NT4445VTR	VTR = TDFN-12 - Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
V_{HIGH} to GND	-0.3	7	V
Voltage at input pins	-0.3	7	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	150	°C
Junction temperature	--	150	°C

Electrical Characteristics

(@ 25°C, unless otherwise stated)

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.71	--	5.5	V
T_{A}	Operating Temperature		-40	25	85	°C
I_{Q}	Quiescent Current	Static inputs and outputs	--	1	--	μA
I_{A}	Active Current	Static inputs and outputs	--	15	--	μA
V_{O}	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_{O}	Maximal Average or DC Current (note 1)	Per Each Chip Side	--	--	24	mA
V_{IH}	HIGH-Level Low Voltage Input Voltage	Logic Input with Schmitt Trigger, at VDD=1.8V	1.35	--	VDD	V
		Low-Level Logic Input, at VDD=1.8V	1.1	--	VDD	
		Logic Input with Schmitt Trigger, at VDD=3.3V	2.3	--	VDD	
		Low-Level Logic Input, at VDD=3.3V	1.5	--	VDD	
		Logic Input with Schmitt Trigger, at VDD=5.0V	3.2	--	VDD	
		Low-Level Logic Input, at VDD=5.0V	1.7	--	VDD	
V_{IL}	LOW-Level Low Voltage Input Voltage	Logic Input with Schmitt Trigger, at VDD=1.8V	--	--	0.45	V
		Low-Level Logic Input, at VDD=1.8V	--	--	0.50	
		Logic Input with Schmitt Trigger, at VDD=3.3V	--	--	0.92	
		Low-Level Logic Input, at VDD=3.3V	--	--	0.66	
		Logic Input with Schmitt Trigger, at VDD=5.0V	--	--	1.3	



Reset IC with Latch and MUX

		Low-Level Logic Input, at VDD=5.0V	--	--	0.77	
I _{IH}	HIGH-Level Input Current	Logic Input Pins; V _{IN} = VDD	-1.0	--	1.0	μA
I _{IL}	LOW-Level Input Current	Logic Input Pins; V _{IN} = 0V	-1.0	--	1.0	μA
V _{OH}	HIGH-Level Output Voltage (note 1)	Push Pull, I _{OH} = 100uA, 1X Driver, at VDD=1.8 V	1.66	--	--	V
		Push Pull, I _{OH} = 700uA, 1X Driver, at VDD=1.8 V	1.21	--	--	
		Push Pull, I _{OH} = 3mA, 1X Driver, at VDD=3.3 V	2.1	--	--	
		Push Pull, I _{OH} = 5mA, 1X Driver, at VDD=5.0 V	3.6	--	--	
		Push Pull, I _{OH} = 8mA, 1X Driver, at VDD=5.0 V	2.9	--	--	
V _{OL}	LOW-Level Output Voltage (note 1)	Push Pull, I _{OL} = 100uA, 1X Driver, at VDD=1.8 V	--	--	0.040	V
		Push Pull, I _{OL} = 700uA, 1X Driver, at VDD=1.8 V	--	--	0.415	
		Open Drain, I _{OL} = 5mA, 1X Driver, at VDD=1.8 V	--	--	0.340	
		Push Pull, I _{OL} = 3mA, 1X Driver, at VDD=3.3 V	--	--	0.81	
		Open Drain, I _{OL} = 20mA, 1X Driver, at VDD=3.3 V	--	--	0.605	
		Push Pull, I _{OL} = 5mA, 1X Driver, at VDD=5.0 V	--	--	0.85	
		Push Pull, I _{OL} = 8mA, 1X Driver, at VDD=5.0 V	--	--	1.2	
		Open Drain, I _{OL} = 20mA, 1X Driver, at VDD=5.0 V	--	--	0.36	
I _{OL}	LOW-Level Output Current (note 1)	Push Pull, V _{OL} = 0.15V, 1X Driver, at VDD=1.8 V	0.34	--	--	mA
		Open Drain, V _{OL} = 0.15V, 1X Driver, at VDD=1.8 V	2.72	--	--	
		Push Pull, V _{OL} = 0.4V, 1X Driver, at VDD=3.3 V	1.836	--	--	
		Open Drain, V _{OL} = 0.4V, 1X Driver, at VDD=3.3 V	14.688	--	--	
		Push Pull, V _{OL} = 0.4V, 1X Driver, at VDD=5.0 V	2.745	--	--	



Reset IC with Latch and MUX

		Open Drain, V _{OL} =0.4V, 1X Driver, at VDD=5.0 V	21.96	--	--	
R _{PULL_UP}	Internal Pull Up Resistance	Pull up on PINs 6, 12	35	50	65	kΩ
R _{PULL_DOWN}	Internal Pull Down Resistance	Pull down on PIN10	35	50	65	kΩ
		Pull down on PIN9	210	300	390	
T _{DLY0}	Delay0 Time	At temperature 25°C	4.13	5	5.88	ms
T _{DLY1}	Delay1 Time	At temperature 25°C	8.27	10	11.7	ms
T _{DLY2}	Delay2 Time	At temperature 25°C	5	--	7.042	s
T _{DLY3}	Delay3 Time	At temperature 25°C	60	--	127	μs
T _{SU}	Start up Time	After VDD reaches 1.6V level	--	7	--	ms

1. Guaranteed by Design.



Reset IC with Latch and MUX

Description

This device is a reset IC with one shot function, internal Latching system, level shifter and multiplexor. The reset (active LOW) occurs when both PWR_BTN_L (PIN2) and KSI_SW (PIN6) are LOW. PWR_BTN_L (PIN2) has 5ms deglitch delay on its line. Also reset logics contains one more 100µs deglitch delay is used. The signal from this delay goes to 10ms one-shot system that creates 10ms LOW pulse on reset event. If PWR_BTN_L and KSI_SW are LOW, and AC_PRESENT (PIN4) transitions from HIGH to LOW, these three conditions will latch the BATT_ENABLE (PIN3) LOW for 5 seconds minimum. During this EC_RST_L will be asserted and EC_IN_RW will go LOW as well.

EC_RST_L is configured to be bidirectional, so it will operate as digital input with Schmitt trigger or as Low Level Digital Output.

Also SLG7NT4445 includes latching system. Its inputs are EC_RST_L and EC_ENTERING_RW. EC_IN_RW is an output configured as open drain. This system is initialized with logic HIGH on its output. It is latched LOW when EC_RST_L goes LOW until EC_ENTERING_RW goes HIGH.

Multiplexing system in this device follow the logic:

$KSO_SW = PWR_BTN_L \ \&\& \ !KSO_INV$

$KSI = !(PWR_BTN_L) \ | \ KSI_SW$

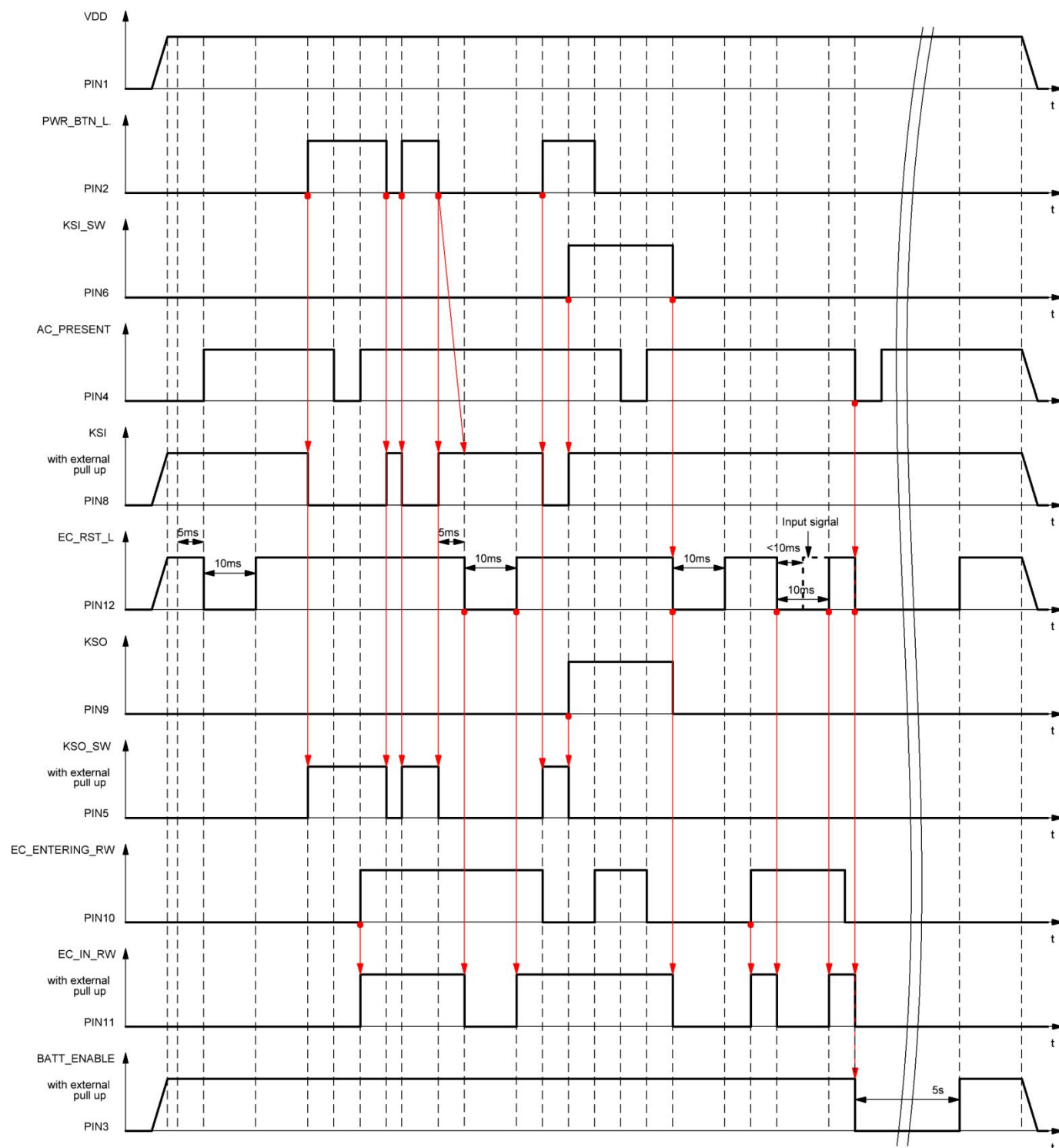
If the AC_PRESENT / BATTERY_ENABLE functionality is not needed, BATTERY_ENABLE can be left floating but AC_PRESENT should be tied low.

All pins are in a high impedance state until the chip has powered up.

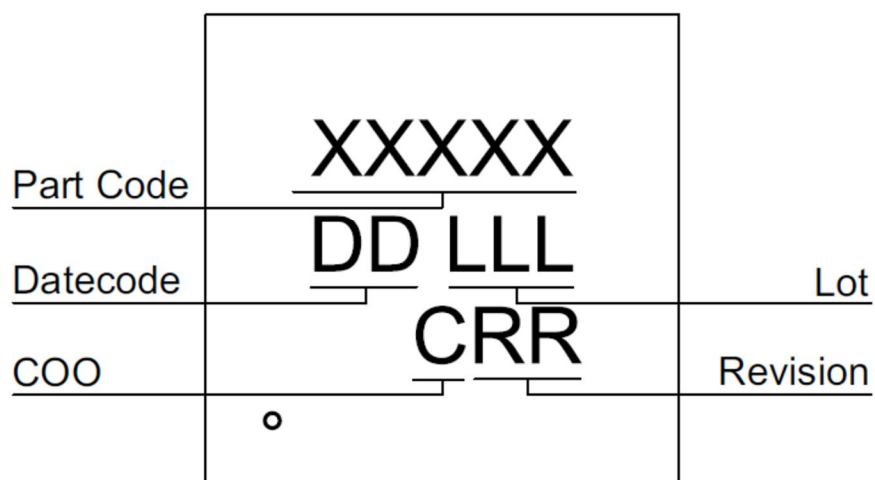


Reset IC with Latch and MUX

Timing Diagram



Package Top Marking



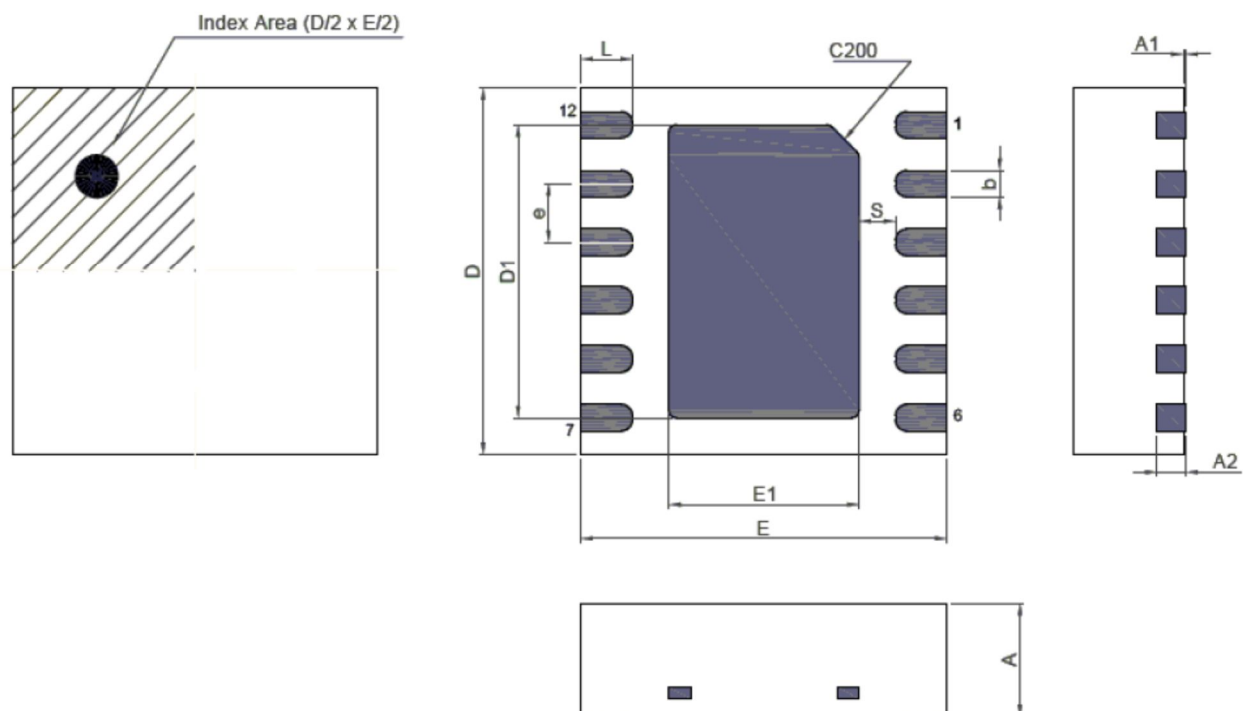
XXXXXX – Part ID Field: identifies the specific device configuration
 DD – Date Code Field: Coded date of manufacture
 LLL – Lot Code: Designates Lot #
 C – COO: Specifies Country of Origin
 RR – Revision Code: Device Revision

Datasheet Revision	Programming Code Number	Locked Status	Part Code	Revision	Date
1.03	002	L	4445V	AB	02/25/2022

The IC security bit is locked/set for code security for production unless otherwise specified. Revision number is not changed for bit locking.

Package Drawing and Dimensions

12 Lead TDFN Package
JEDEC MO-252, Variation 2525E



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.70	0.75	0.80	D1	1.95	2.00	2.05
A1	0.005	-	0.060	E1	1.25	1.30	1.35
A2	0.15	0.20	0.25	e	0.40 BSC		
b	0.13	0.18	0.23	L	0.30	0.35	0.40
D	2.45	2.50	2.55	S	0.18	-	-
E	2.45	2.50	2.55				

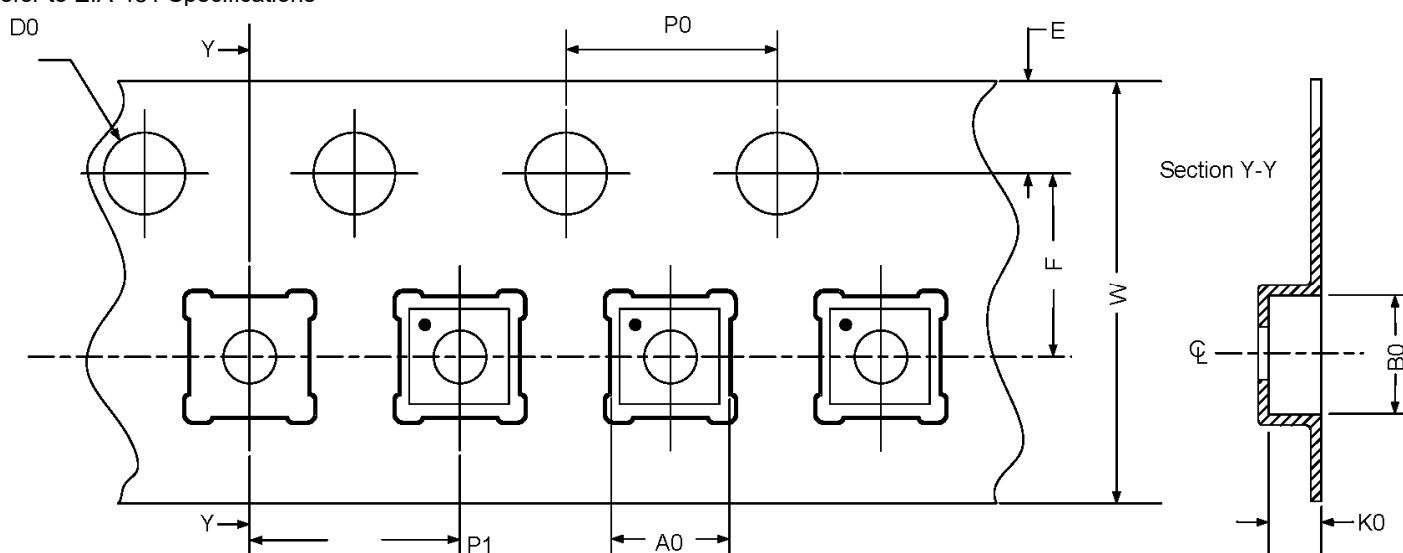
Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Trailer A		Leader B		Pocket (mm)	
			per reel	per box		Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
TDFN 12L 2.5x2.5mm 0.4P Green	12	2.5x2.5x0.75	3000	3000	178/60	42	168	42	168	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
TDFN 12L 2.5x2.5mm 0.4P Green	2.75	2.75	1.05	4	4	1.55	1.75	3.5	8

Refer to EIA-481 Specifications



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 4.6875 mm³ (nominal). More information can be found at www.jedec.org.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.