ALL_SYS_PWRGD and PCH_PWROK and SYS_PWROK Logic

General Description

Silego SLG7NT4774 is a low power and small form device. The SoC is housed in a 2mm x 3mm STQFN package which is optimal for using with small devices.

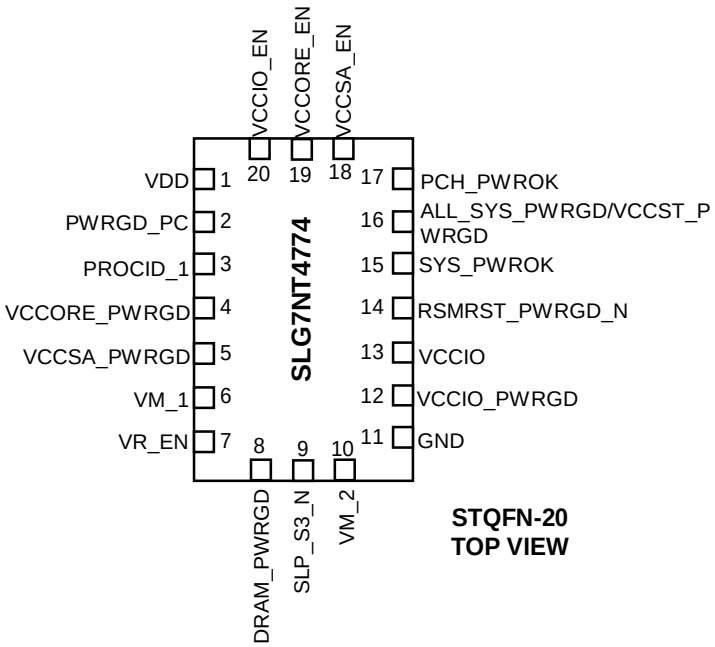
Features

- Low Power Consumption
- Pb-Free / RoHS Compliant
- Halogen-Free
- STQFN-20 Package

Output Summary

- 7 Outputs — Open Drain NMOS 1X

Pin Configuration



STQFN-20
TOP VIEW

Pin Configuration

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	Supply Voltage
2	PWRGD_PC	Digital Input	Digital Input without Schmitt trigger
3	PROCID_1	Digital Input	Digital Input without Schmitt trigger
4	VCCORE_PWRGD	Digital Input	Digital Input without Schmitt trigger
5	VCCSA_PWRGD	Digital Input	Digital Input without Schmitt trigger
6	VM_1	Analog Input/Output	Analog Input/Output
7	VR_EN	Digital Output	Open Drain NMOS 1X
8	DRAM_PWRGD	Digital Input	Digital Input without Schmitt trigger
9	SLP_S3_N	Digital Input	Digital Input without Schmitt trigger
10	VM_2	Analog Input/Output	Analog Input/Output
11	GND	GND	Ground
12	VCCIO_PWRGD	Digital Input	Digital Input without Schmitt trigger
13	VCCIO	Analog Input/Output	Analog Input/Output
14	RSMRST_PWRGD_N	Digital Input	Digital Input without Schmitt trigger
15	SYS_PWROK	Digital Output	Open Drain NMOS 1X
16	ALL_SYS_PWRGD/VCCST_PWRGD	Digital Output	Open Drain NMOS 1X
17	PCH_PWROK	Digital Output	Open Drain NMOS 1X
18	VCCSA_EN	Digital Output	Open Drain NMOS 1X
19	VCCORE_EN	Digital Output	Open Drain NMOS 1X
20	VCCIO_EN	Digital Output	Open Drain NMOS 1X

Ordering Information

Part Number	Package Type
SLG7NT4774V	V=STQFN-20
SLG7NT4774VTR	VTR=STQFN-20 – Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
V_{HIGH} to GND	-0.3	7	V
Voltage at input pins	-0.3	7	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	125	°C
Junction temperature	--	150	°C
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1300	--	V
Moisture Sensitivity Level	1		

Electrical Characteristics

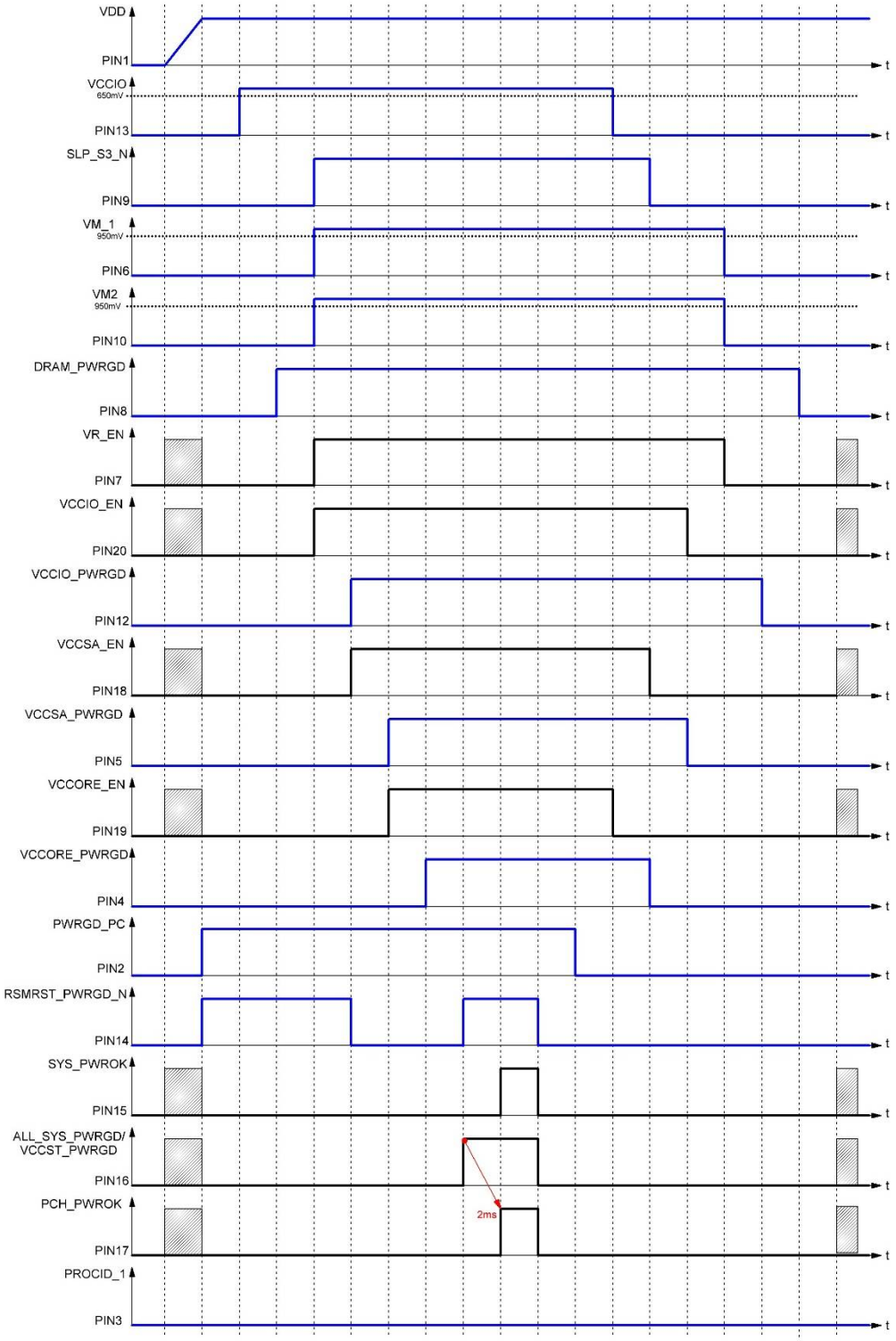
(@ 25°C, unless otherwise stated)

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3	3.3	3.6	V
T_A	Operating Temperature		-40	25	85	°C
I_Q	Quiescent Current	Static inputs and outputs	--	80	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_O	Maximal Average or DC Current (note 1)	Per Each Chip Side (PIN2-PIN10, PIN12-PIN20)	--	--	90	mA
V_{IH}	HIGH-Level Input Voltage	Logic Input, at VDD=3.3V	1.78	--	VDD	V
V_{IL}	LOW-Level Input Voltage	Logic Input, at VDD=3.3V	--	--	1.21	V
I_{IH}	HIGH-Level Input Current	Logic Input PINs; V_{IN} = VDD	-1.0	--	1.0	µA
I_{IL}	LOW-Level Input Current	Logic Input PINs; V_{IN} = 0V	-1.0	--	1.0	µA
V_{OL}	LOW-Level Output Voltage	Open Drain, I_{OL} = 3mA, 1X Driver, at VDD=3.3 V	--	0.080	0.147	V
I_{OL}	LOW-Level Output Current	Open Drain, V_{OL} =0.4V, 1X Driver, at VDD=3.3 V	7.313	12.37	--	mA
V_{ACMP0}	Analog Comparator Threshold Voltage	ACMP0 threshold including input offset, reference voltage variation and hysteresis, at temperature 25°C.	936	--	964	mV
V_{ACMP1}	Analog Comparator Threshold Voltage	ACMP1 threshold including input offset, reference voltage variation and hysteresis, at temperature 25°C.	936	--	964	mV
V_{ACMP2}	Analog Comparator Threshold Voltage	ACMP2 threshold including input offset, reference voltage variation and hysteresis, at temperature 25°C.	640	--	661	mV
T_{DLY0}	Delay0 Time	At temperature 25°C	1.9	1.98	2.07	ms
		At temperature -40°C +85°C (note 1)	1.71	1.98	2.44	
T_{DLY1}	Delay1 Time	At temperature 25°C	1.9	1.98	2.07	ms
		At temperature -40°C +85°C (note 1)	1.71	1.98	2.44	
T_{SU}	Start up Time	From VDD rising past 1.6V	--	1	--	ms

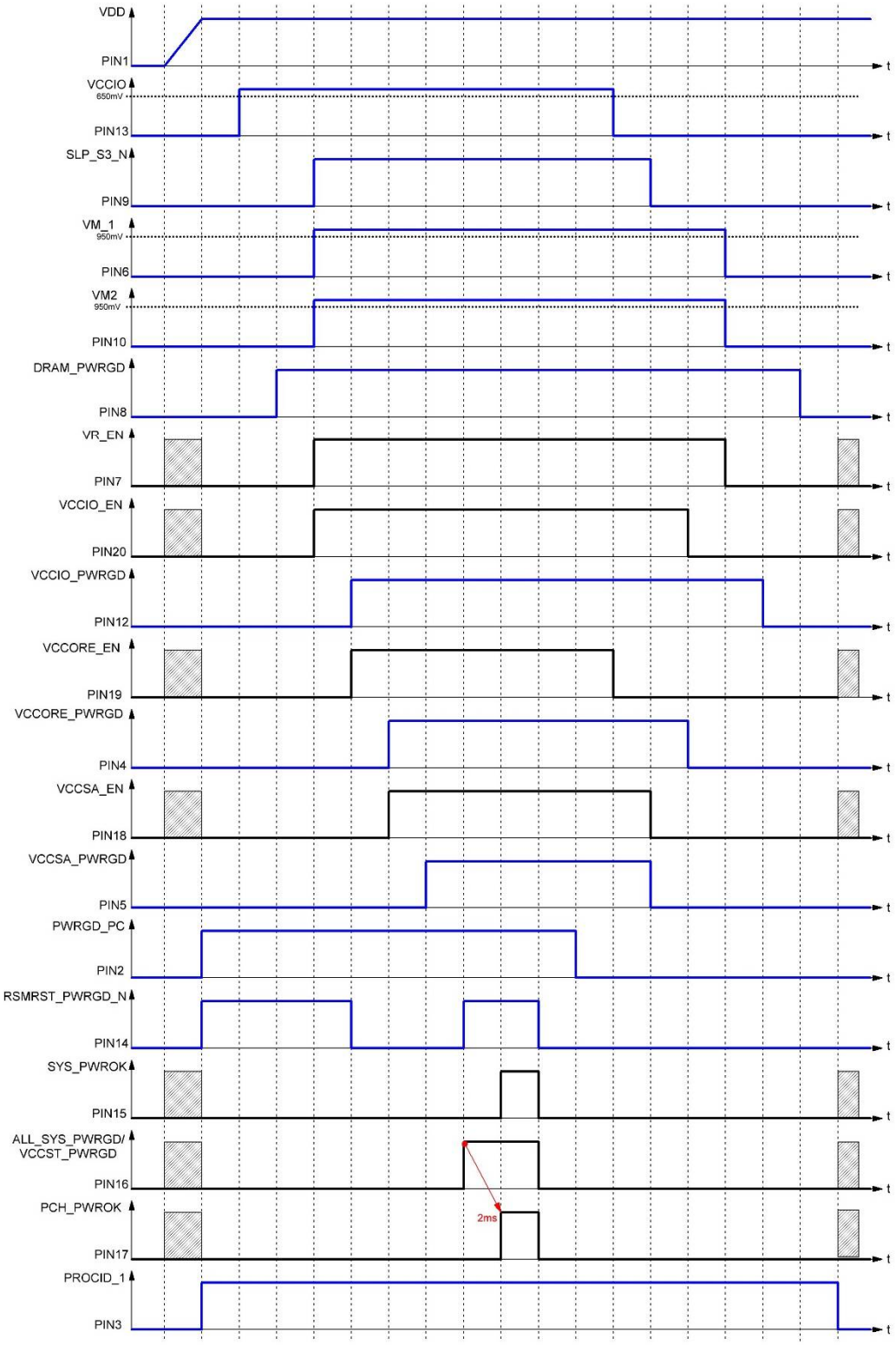
1. Guaranteed by Design.

Timing Diagram

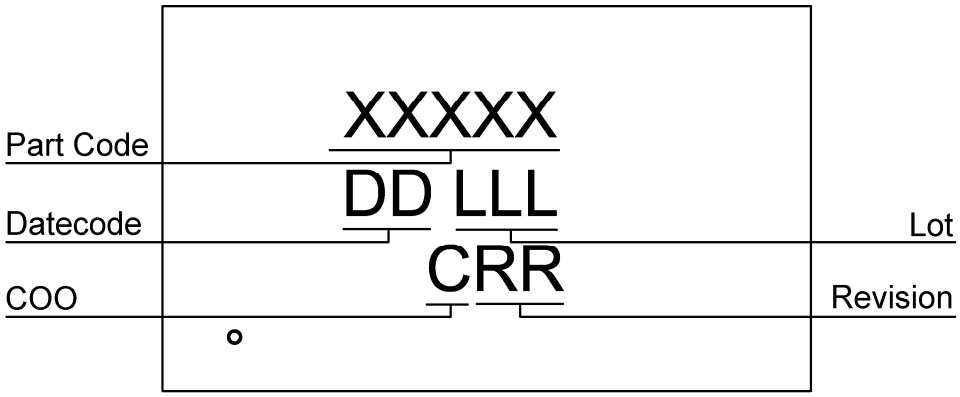
Case 1: PIN#3 (PROCID_1) – LOW



Case 2: PIN#3 (PROCID_1) – HIGH



Package Top Marking



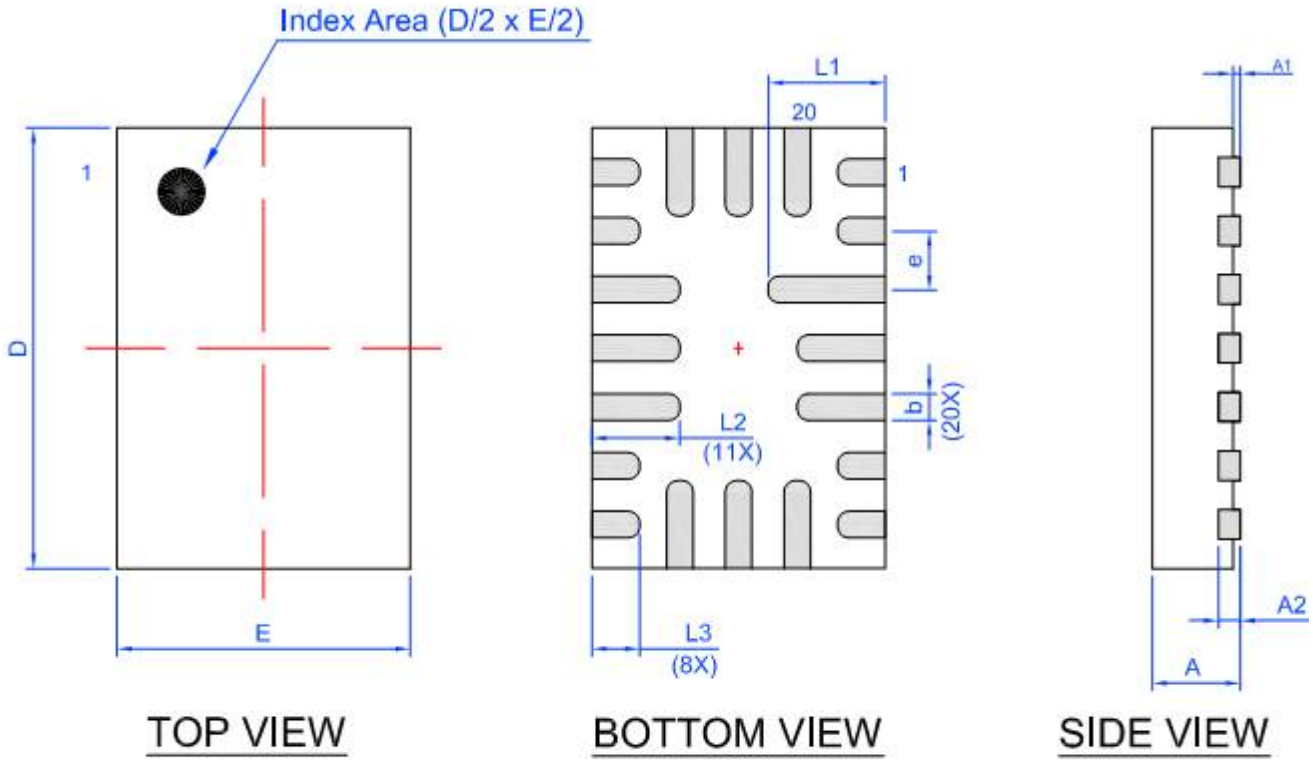
XXXXX – Part ID Field: identifies the specific device configuration
DD – Date Code Field: Coded date of manufacture
LLL – Lot Code: Designates Lot #
C – Assembly Site/COO: Specifies Assembly Site/Country of Origin
RR – Revision Code: Device Revision

Datasheet Revision	Programming Code Number	Locked Status	Part Code	Revision	Date
1.04	009	L	4774V	AB	03/16/2016

The IC security bit is locked/set for code security for production unless otherwise specified. Revision number is not changed for bit locking.

Package Drawing and Dimensions

20 Lead STQFN Package
JEDEC MO-220, Variation WECE
IC Net Weight: 0.015 g



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L1	0.75	0.80	0.85
b	0.13	0.18	0.23	L2	0.55	0.60	0.65
e	0.40 BSC			L3	0.275	0.325	0.375

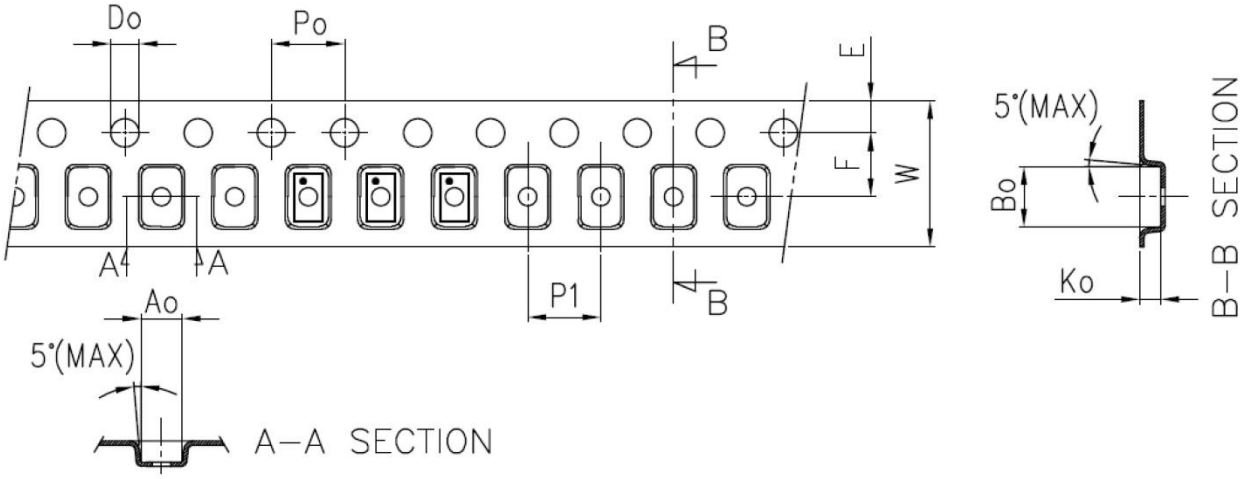
Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Trailer A		Leader B		Pocket (mm)	
			per reel	per box		Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
STQFN 20L 2x3mm 0.4P Green	20	2x3x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2x3mm 0.4P Green	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8

Refer to EIA-481 Specifications



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.3 mm^3 (nominal). More information can be found at www.jedec.org.

Silego Website & Support

Silego Technology Website
Silego Technology provides online support via our website at http://www.silego.com/.This website is used as a means to make files and information easily available to customers.

For more information regarding Silego Green products, please visit:
http://greenpak.silego.com/
http://greenpak2.silego.com/
http://greenpak3.silego.com/
http://greenfet.silego.com/
http://greenfet2.silego.com/
http://greenclk.silego.com/

Products are also available for purchase directly from Silego at the Silego Online Store at http://www.silego.com/

Silego Technical Support
Datasheets and errata, application notes and example designs, user guides, and hardware support documents and the latest software releases are available at the Silego website or can be requested directly at info@silego.com.

For specific GreenPAK design or applications questions and support please send e-mail requests to GreenPAK@silego.com

Users of Silego products can receive assistance through several channels:

Online Training
Silego Technology has live training assistance and sales support available at http://www.silego.com/. Please contact us to schedule a 1 on 1 training session with one of our application engineers.

Contact Your Local Sales Representative
Customers can contact their local sales representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. More information regarding your local representative is available at the Silego website or send a request to info@silego.com

Contact Silego Directly
Silego can be contacted directly via e-mail at info@silego.com or user submission form, located at the following URL:
http://support.silego.com/

Other Information
The latest Silego Technology press releases, listing of seminars and events, listings of worldwide Silego Technology offices and representatives are all available at http://www.silego.com/

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE

SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. SILEGO TECHNOLOGY DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. SILEGO TECHNOLOGY RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE