



DPWROK and RSMRST_N Logic

General Description

Silego SLG7NT4805 is a low power and small form device. The SoC is housed in a 2mm x 3mm STQFN package which is optimal for using with small devices.

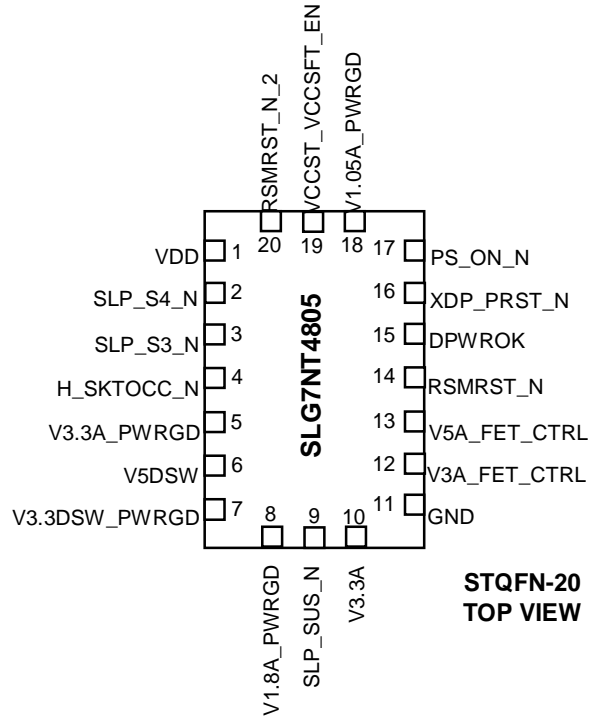
Features

- Low Power Consumption
- Pb-Free / RoHS Compliant
- Halogen-Free
- STQFN-20 Package

Output Summary

- 8 Outputs — Open Drain NMOS 1X

Pin Configuration





Pin Configuration

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	Supply Voltage
2	SLP_S4_N	Digital Input	Digital Input without Schmitt trigger
3	SLP_S3_N	Digital Input	Digital Input without Schmitt trigger
4	H_SKTOCC_N	Digital Input	Digital Input without Schmitt trigger
5	V3.3A_PWRGD	Digital Output	Open Drain NMOS 1X
6	V5DSW	Analog Input/Output	Analog Input/Output
7	V3.3DSW_PWRGD	Digital Input	Digital Input without Schmitt trigger
8	V1.8A_PWRGD	Digital Input	Digital Input without Schmitt trigger
9	SLP_SUS_N	Digital Input	Digital Input without Schmitt trigger
10	V3.3A	Analog Input/Output	Analog Input/Output
11	GND	GND	Ground
12	V3A_FET_CTRL	Digital Output	Open Drain NMOS 1X
13	V5A_FET_CTRL	Digital Output	Open Drain NMOS 1X
14	RSMRST_N	Digital Output	Open Drain NMOS 1X
15	DPWROK	Digital Output	Open Drain NMOS 1X
16	XDP_PRST_N	Digital Input	Digital Input without Schmitt trigger
17	PS_ON_N	Digital Output	Open Drain NMOS 1X
18	V1.05A_PWRGD	Digital Input	Digital Input without Schmitt trigger
19	VCCST_VCCSFT_EN	Digital Output	Open Drain NMOS 1X
20	RSMRST_N_2	Digital Output	Open Drain NMOS 1X

Ordering Information

Part Number	Package Type
SLG7NT4805V	V=STQFN-20
SLG7NT4805VTR	VTR=STQFN-20 – Tape and Reel (3k units)



Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
V _{HIGH} to GND	-0.3	7	V
Voltage at input pins	-0.3	7	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	125	°C
Junction temperature	--	150	°C
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1300	--	V
Moisture Sensitivity Level	1		

Electrical Characteristics

(@ 25°C, unless otherwise stated)

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage		4.5	5	5.5	V
T _A	Operating Temperature		-40	25	85	°C
I _Q	Quiescent Current	Static inputs and outputs	--	85	--	µA
V _O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I _O	Maximal Average or DC Current (note 1)	Per Each Chip Side (PIN2-PIN10, PIN12-PIN20)	--	--	90	mA
V _{IH}	HIGH-Level Input Voltage	Logic Input, at VDD=5.0V	2.64	--	VDD	V
V _{IL}	LOW-Level Input Voltage	Logic Input, at VDD=5.0V	--	--	1.84	V
I _{IH}	HIGH-Level Input Current	Logic Input PINs; V _{IN} = VDD	-1.0	--	1.0	µA
I _{IL}	LOW-Level Input Current	Logic Input PINs; V _{IN} = 0V	-1.0	--	1.0	µA
V _{OL}	LOW-Level Output Voltage	Open Drain, I _{OL} = 5mA, 1X Driver, at VDD=5.0 V	--	0.102	0.180	V
I _{OL}	LOW-Level Output Current	Open Drain, V _{OL} = 0.4V, 1X Driver, at VDD=5.0 V	10.82	17.38	--	mA
V _{ACMP0}	Analog Comparator Threshold Voltage	ACMP0 threshold including input offset, reference voltage variation and hysteresis, at temperature 25°C.	936	--	964	mV
		ACMP0 threshold including input offset, reference voltage variation and hysteresis, at temperature -40°C +85°C (note 1)	895	--	985	
V _{ACMP1}	Analog Comparator Threshold Voltage	ACMP1 threshold including input offset, reference voltage variation and hysteresis, at temperature 25°C.	936	--	964	mV
		ACMP1 threshold including input offset, reference voltage variation and hysteresis, at temperature -40°C +85°C (note 1)	895	--	985	

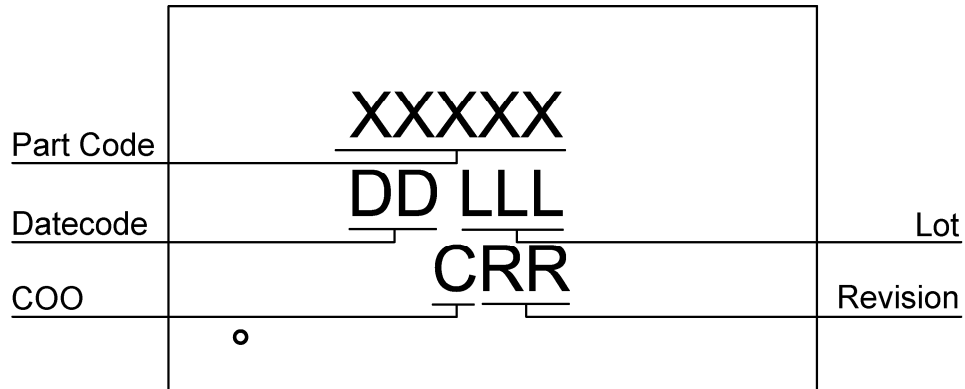


T _{DLY0}	Delay0 Time	At temperature 25°C	9.44	10	10.68	ms
		At temperature -40°C +85°C (note 1)	8.43	10	15.07	
T _{DLY1}	Delay1 Time	At temperature 25°C	9.44	10	10.68	ms
		At temperature -40°C +85°C (note 1)	8.43	10	15.07	
T _{DLY4}	Delay4 Time	At temperature 25°C	94.53	100.25	112.25	μs
		At temperature -40°C +85°C (note 1)	84.43	100.25	156.36	
T _{SU}	Start up Time	From VDD rising past 1.35V	--	0.31	--	ms

1. Guaranteed by Design.



Package Top Marking



- XXXXX – Part ID Field: identifies the specific device configuration
- DD – Date Code Field: Coded date of manufacture
- LLL – Lot Code: Designates Lot #
- C – Assembly Site/COO: Specifies Assembly Site/Country of Origin
- RR – Revision Code: Device Revision

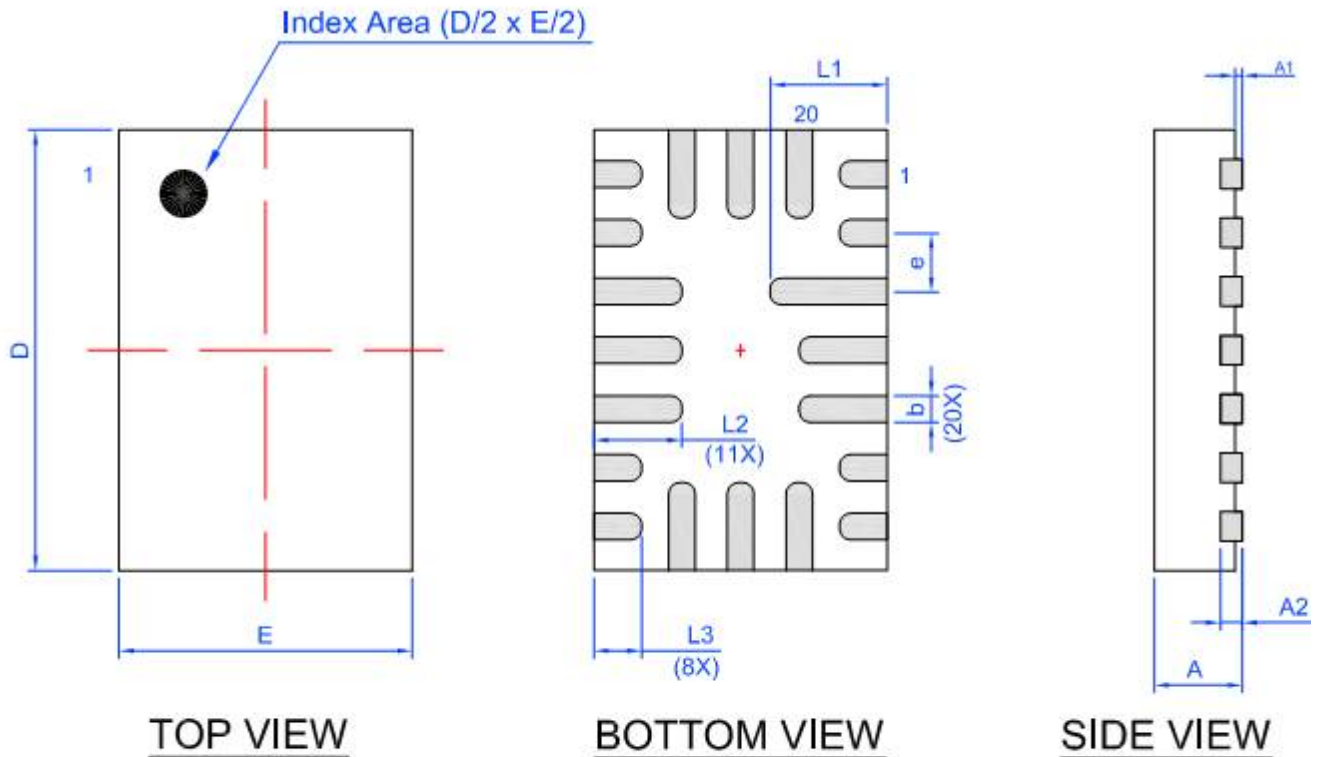
Datasheet Revision	Programming Code Number	Locked Status	Part Code	Revision	Date
1.01	006	L	4805V	AA	03/08/2016

The IC security bit is locked/set for code security for production unless otherwise specified. Revision number is not changed for bit locking.



Package Drawing and Dimensions

20 Lead STQFN Package
JEDEC MO-220, Variation WECE
IC Net Weight: 0.015 g



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L1	0.75	0.80	0.85
b	0.13	0.18	0.23	L2	0.55	0.60	0.65
e	0.40 BSC			L3	0.275	0.325	0.375



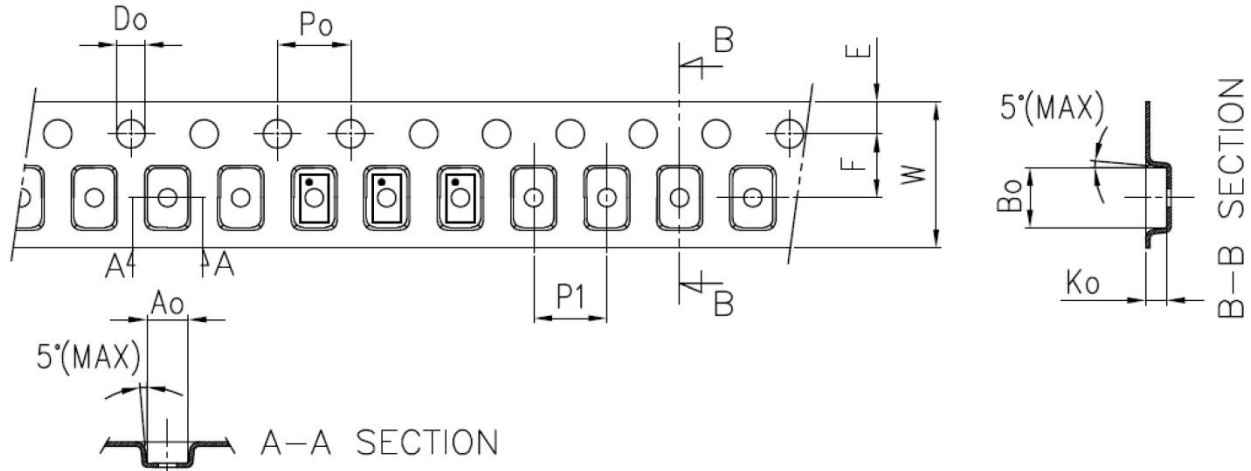
Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Trailer A		Leader B		Pocket (mm)	
			per reel	per box		Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
STQFN 20L 2x3mm 0.4P Green	20	2x3x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2x3mm 0.4P Green	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8

Refer to EIA-481 Specifications



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.3 mm^3 (nominal). More information can be found at www.jedec.org.



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