SILEGO

SLG7NT4964

DDR_RAIL SEQUENCING

General Description

Silego SLG7NT4964 is a low power and small form device. The SoC is housed in a 1.6 x 1.6 mm STQFN package which is optimal for using with small devices.

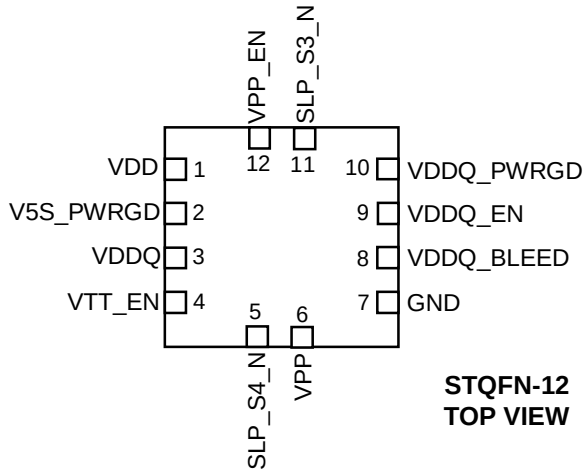
Features

- Low Power Consumption
- Pb-Free / RoHS Compliant
- Halogen-Free
- STQFN-12 Package

Output Summary

- 4 Outputs — Push Pull 1X

Pin Configuration



STQFN-12
TOP VIEW

Pin Configuration

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	Supply Voltage
2	V5S_PWRGD	Digital Input	Digital Input without Schmitt trigger
3	VDDQ	Analog Input/Output	Analog Input/Output
4	VTT_EN	Digital Output	Push Pull 1X
5	SLP_S4_N	Digital Input	Digital Input without Schmitt trigger
6	VPP	Analog Input/Output	Analog Input/Output
7	GND	GND	Ground
8	VDDQ_BLEED	Digital Output	Push Pull 1X
9	VDDQ_EN	Digital Output	Push Pull 1X
10	VDDQ_PWRGD	Digital Input	Digital Input without Schmitt trigger
11	SLP_S3_N	Digital Input	Digital Input without Schmitt trigger
12	VPP_EN	Digital Output	Push Pull 1X

Ordering Information

Part Number	Package Type
SLG7NT4964V	V=STQFN-12
SLG7NT4964VTR	STQFN-12 – Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
V_{HIGH} to GND	-0.3	7	V
Voltage at input pins	-0.3	7	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	125	°C
Junction temperature	--	150	°C
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1000	--	V
Moisture Sensitivity Level	1		

Electrical Characteristics

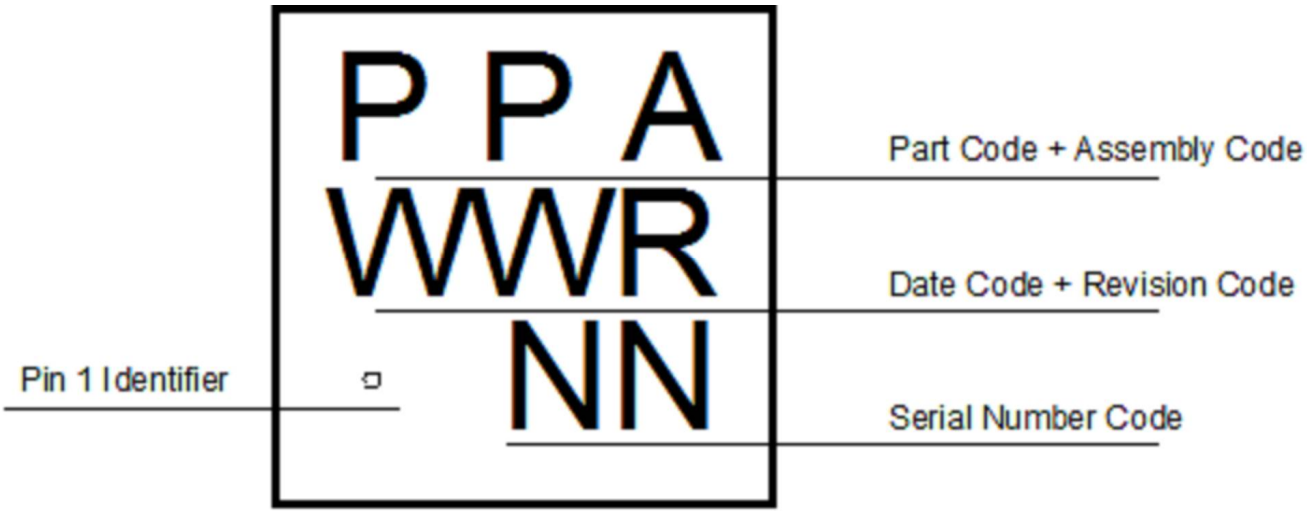
(@ 25°C, unless otherwise stated)

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3	3.3	3.6	V
T_A	Operating Temperature		-40	25	85	°C
I_Q	Quiescent Current	Static inputs and outputs	--	65	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_O	Maximal Average or DC Current (note 1)	Per Each Chip Side	--	--	90	mA
V_{IH}	HIGH-Level Input Voltage	Logic Input, at VDD=3.3V	1.78	--	VDD	V
V_{IL}	LOW-Level Input Voltage	Logic Input, at VDD=3.3V	--	--	1.21	V
I_{IH}	HIGH-Level Input Current	Logic Input PINs; V_{IN} = VDD	-1.0	--	1.0	µA
I_{IL}	LOW-Level Input Current	Logic Input PINs; V_{IN} = 0V	-1.0	--	1.0	µA
V_{OH}	HIGH-Level Output Voltage (note 1)	Push Pull & PMOS OD, I_{OH} = 3mA, 1X Driver, at VDD=3.3 V	2.71	3.09	--	V
V_{OL}	LOW-Level Output Voltage (note 1)	Push Pull, I_{OL} = 3mA, 1X Driver, at VDD=3.3 V	--	0.18	0.28	V
I_{OH}	HIGH-Level Output Current (note 1)	Push Pull & PMOS OD, V_{OH} = 2.4 V, 1X Driver, at VDD=3.3 V	5.83	10.158	--	mA
I_{OL}	LOW-Level Output Current (note 1)	Push Pull, V_{OL} =0.4V, 1X Driver, at VDD=3.3 V	4.06	6.44	--	mA
V_{ACMP0}	Analog Comparator Threshold Voltage	ACMP0 threshold including input offset, reference voltage variation and hysteresis, at temperature 25°C.	189	--	212	mV
		ACMP0 threshold including input offset, reference voltage variation and hysteresis, at temperature -40 +85°C (note 1)	186	--	214	
V_{ACMP1}	Analog Comparator Threshold Voltage	ACMP1 threshold including input offset, reference voltage variation and hysteresis, at temperature 25°C.	1164	--	1235	mV

		ACMP1 threshold including input offset, reference voltage variation and hysteresis, at temperature -40 +85°C (note 1)	1150	--	1246	
T_{DLY0}	Delay0 Time	At temperature 25°C	1.98	2.06	2.17	ms
		At temperature -40°C +85°C (note 1)	1.78	2.06	2.56	
T_{DLY1}	Delay1 Time	At temperature 25°C	116.88	140	185.5	µs
		At temperature -40°C +85°C (note 1)	105.11	140	215.2	
T_{SU}	Start up Time	From VDD rising past 1.35V	--	0.31	--	ms

1. Guaranteed by Design.

Package Top Marking

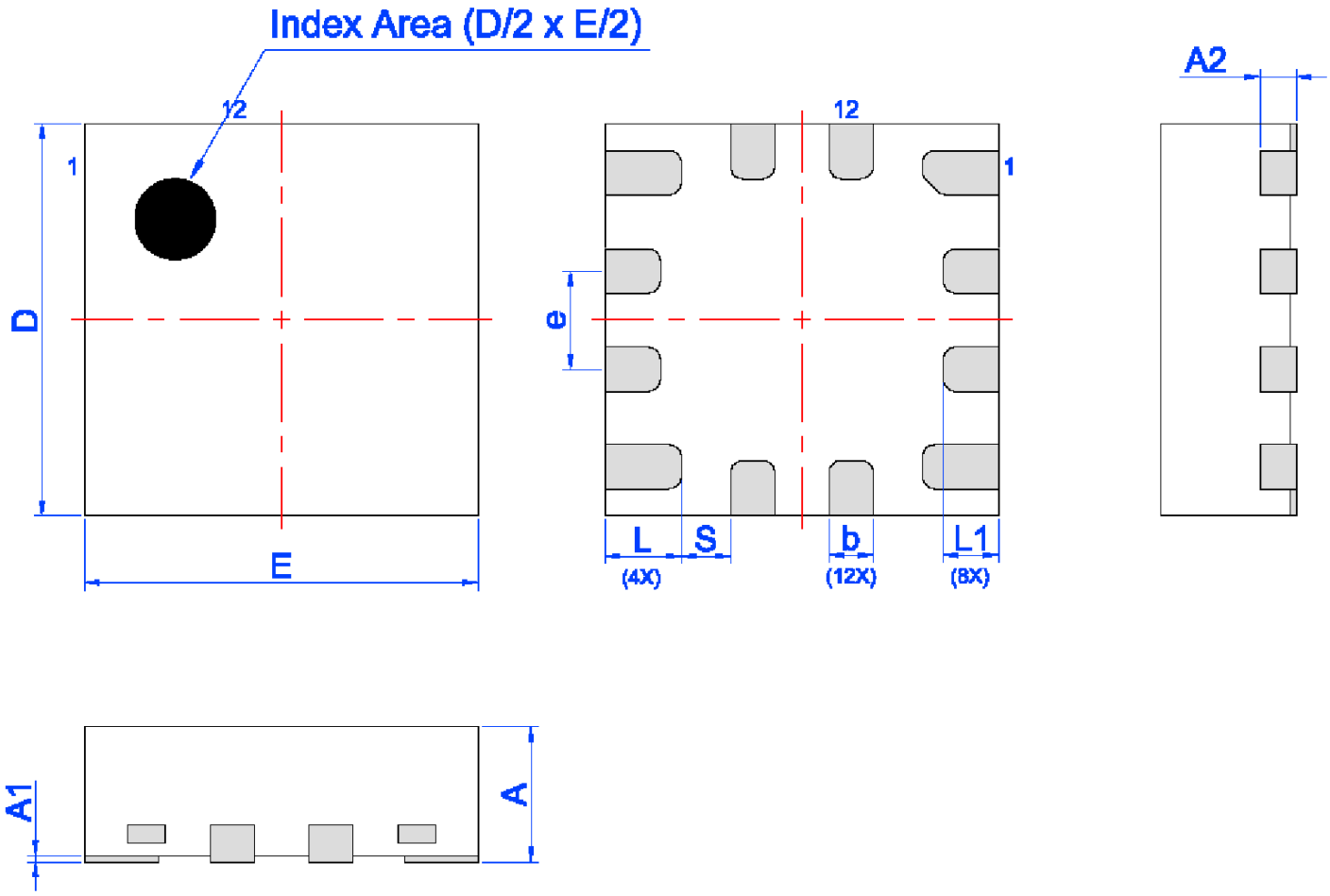


Datasheet Revision	Programming Code Number	Locked Status	Part Code	Revision	Date
1.01	002	L	SQ	A	03/08/2016

The IC security bit is locked/set for code security for production unless otherwise specified. Revision number is not changed for bit locking.

Package Drawing and Dimensions

12 Lead STQFN Package
JEDEC MO-220



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.55	1.60	1.65
A1	0.005	-	0.060	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.26	0.31	0.36
b	0.13	0.18	0.23	L1	0.175	0.225	0.275
e	0.40 BSC			S	0.2 REF		

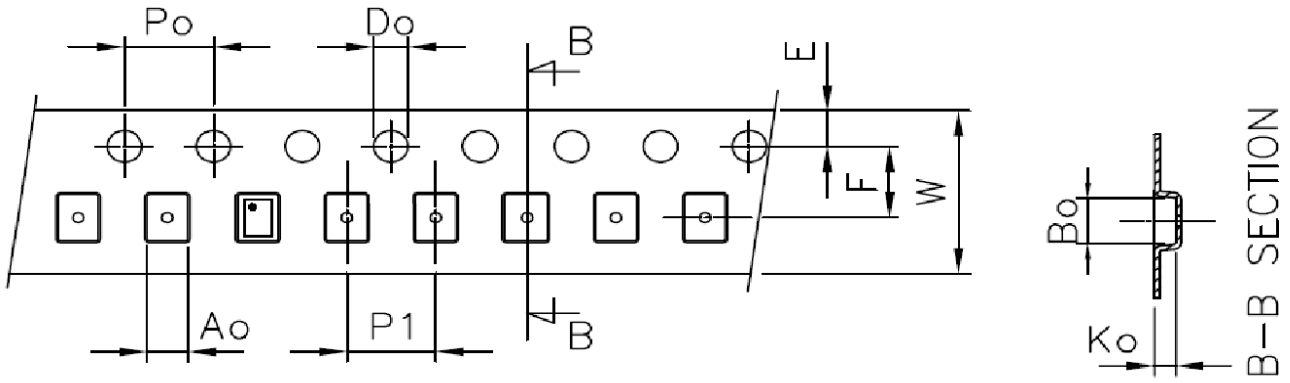
Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Trailer A		Leader B		Pocket (mm)	
			per reel	per box		Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
STQFN 12L FC 0.4P Green	12	1.6x1.6x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 12L FC 0.4P Green	1.9	1.9	0.8	4	4	1.5	1.75	3.5	8

Refer to EIA-481 Specifications



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 1.408 mm^3 (nominal). More information can be found at www.jedec.org.

Silego Website & Support

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