

DDR 13 to 26 Bit Registered Buffer

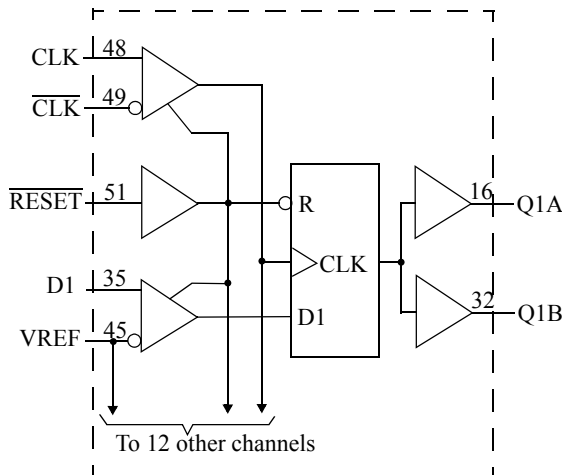
Applications:

- PC1600/2100/2700/3200 DDR memory modules
- 1:2 Outputs for stacked DDR DIMMS
- SSTL_2 compatible data registers

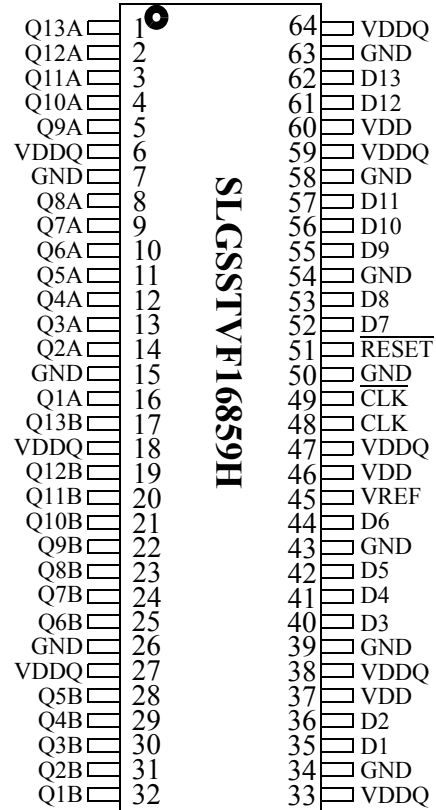
Features:

- Compatible with JEDEC standard SSTV16859
- Differential Clock inputs
- SSTL_2 data input signaling
- Supports SSTL_2 class I output specifications
- Output circuitry minimizes effects of SSO and unterminated lines
- LVCMOS input levels on $\overline{\text{RESET}}$ pin
- 2.3V-2.7V Operation for PC1600/2100/2700
- 2.5V-2.7V Operation for PC3200
- Max Clock frequency > 210MHz

Block Diagram



Pin Configuration



64-Pin TSSOP

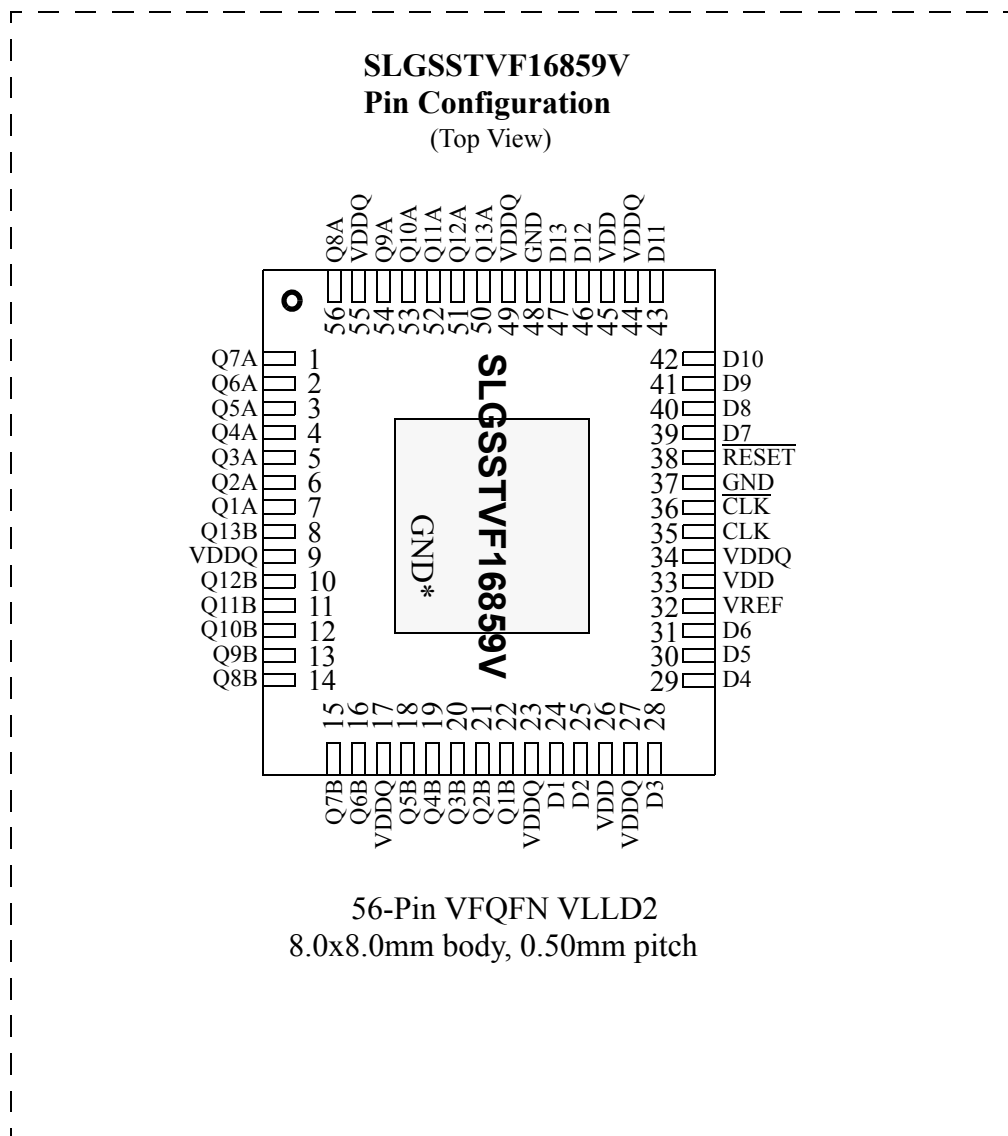
6.1mm body, 0.50mm pitch

Truth Table

Inputs				Q Outputs
$\overline{\text{RESET}}$	CLK	$\overline{\text{CLK}}$	D	Q
L	X, or Floating	X, or Floating	X, or Floating	L
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	$Q_0^{(2)}$

Notes:

1. H = High Signal Level
L = Low Signal Level
↑ = Transition LOW-to-HIGH
↓ = Transition HIGH-to-LOW
X = Don't care
2. Output level prior to indicated steady state input conditions established.



* Note: Connect center die pad to GND

General Description

The 14-bit SLGSSTVF16859 is a registered buffer designed for 2.3V to 2.7V V_{DD} operating range. Inputs are SSTL_2 levels, except for the LVC MOS $\overline{RESET}$ input.

Data propagation from D to Q is controlled by the differential clock (CLK/ $\overline{CLK}$) and a control signal ($\overline{RESET}$). The rising edge of CLK (crossing with $\overline{CLK}$ falling) is used to register the Data.

$\overline{RESET}$, an LVC MOS asynchronous signal, is intended for use at the time of power-up. $\overline{RESET}$ must be held at a logic “Low” level during power up. This ensures defined outputs before a stable CLK/ $\overline{CLK}$ is supplied.

The SLGSSTVF16859 supports low-power standby operation. Setting $\overline{RESET}$ pin to a logic “low” disables (CLK/ $\overline{CLK}$) receivers, and allows floating inputs to all other receivers as well (D, V_{REF} , CLK/ $\overline{CLK}$). Additionally, all internal registers are reset, and outputs (Q) are set “low”. $\overline{RESET}$ input pin must always be driven to a valid logic state “high” or “low”.

SLGSSTVF16859H Pin Description:

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1,17,2,19,3,20,4,21,5,22,8,23,9,24,10,25,11,28,12,29,13,30,14,31,16,32	QA/B (13:1)	OUTPUT	Q-Outputs
7,15,26,34,39,43,50,58,63	GND	POWER	Ground
6,18,27,33,38,47,59,64	VDDQ	POWER	Output supply voltage
62,61,57,56,55,53,52,44,42,41,40,36,35	D (13:1)	INPUT	D-Inputs
48	CLK	INPUT	Positive clock input
49	$\overline{CLK}$	INPUT	Negative clock input
37, 46	VDD	POWER	Core supply voltage
51	$\overline{RESET}$	INPUT	Reset (active low)
45	VREF	INPUT	Input reference voltage

Absolute Maximum Ratings

Storage Temperature	-65°C to +150°C
Supply Voltage	-0.5 to 3.6V
Input Voltage ^{1,2}	-0.5 to $V_{DD} + 0.5$
Output Voltage ^{1,2}	-0.5 to $V_{DDQ} + 0.5$
Input Clamp Current	-50 mA
Output Clamp Current	±50 mA
Continuous Output Current	±50 mA
V_{DD} , V_{DDQ} , or GND Current/Pin	±100 mA
TSSOP (H) Package Thermal Impedance ³	55°C/W
VLLD2 (V) Package Thermal Impedance ⁴	22°C/W

Notes:

1. The input and output negative voltage ratings may be exceeded if the input and output clamp currents are within limits.
2. Limited to 3.6V Max.
3. The package thermal impedance is calculated according to JESD 51-7
4. The package thermal impedance is calculated according to JESD 51-5.

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to this device. These ratings are stress specifications only and functional operation of the device at these or other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Recommended Operating Conditions:

PARAMETER	DESCRIPTION		MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage		V_{DDQ}		2.7	V
V_{DDQ}	Output Supply Voltage for PC1600/2100/2700		2.3		2.7	
V_{DDQ}	Output Supply Voltage for PC3200		2.5	2.6	2.7	
V_{REF}	Reference Voltage for PC1600/2100/2700		1.15	1.25	1.35	
V_{REF}	Reference Voltage for PC3200		1.25	1.3	1.35	
V_{TT}	Termination Voltage		$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	
V_I	Input Voltage		0		V_{DD}	
$V_{IH} (DC)$	DC Input High Voltage	Data Inputs	$V_{REF} + 0.15$			
$V_{IH} (AC)$	AC Input High Voltage		$V_{REF} + 0.31$			
$V_{IL} (DC)$	DC Input Low Voltage				$V_{REF} - 0.15$	
$V_{IL} (AC)$	AC Input Low Voltage				$V_{REF} - 0.31$	
V_{IH}	Input High Voltage Level	RESET	1.7			
V_{IL}	Input Low Voltage Level				0.7	
V_{ICR}	Common mode Input Range	CLK, CLK	0.97		1.53	
V_{ID}	Differential Input Voltage		0.36			
V_{IX}	Cross Point Voltage of Differential Clock Pair		$(V_{DD}/2) - 0.2$		$(V_{DD}/2) + 0.2$	
I_{OH}	High-Level Output Current				-16	mA
I_{OL}	Low-Level Output Current				16	
T_A	Operating Free-Air Temperature		0		70	°C

SLGSSTVF16859H/V DC Electrical Characteristics - (For PC1600/2100/2700)

$T_A = 0 - 70^{\circ}\text{C}$; $V_{DD} = 2.5 \pm 0.2\text{V}$, $V_{DDQ} = 2.5 \pm 0.2\text{V}$; (unless otherwise stated)

SMBL	PARAMETERS	CONDITIONS	V_{DDQ}	MIN	TYP	MAX	UNITS
V_{IK}		$I_I = -18\text{mA}$	2.3V			-1.2	V
V_{OH}		$I_{OH} = -100\mu\text{A}$	2.3V -2.7V	$V_{DDQ} - 0.2$			
		$I_{OH} = -8\text{mA}$	2.3V	1.95			
V_{OL}		$I_{OL} = 100\mu\text{A}$	2.3V -2.7V			0.2	
		$I_{OL} = 8\text{mA}$	2.3V			0.35	
I_I	All Inputs	$V_I = V_{DD}$ or GND	2.7V			± 5	μA
I_{DD}	Standby (Static)	$\overline{\text{RESET}} = \text{GND}$	2.7V			10	μA
	Operating (Static)	$V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, $\overline{\text{RESET}} = V_{DD}$			52		mA
I_{DDD}	Dynamic operating (clock only)	$\overline{\text{RESET}} = V_{DD}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK & $\overline{\text{CLK}}$ switching 50% duty cycle	2.5V		75		$\mu\text{A}/\text{MHz}$
	Dynamic Operating (per each data input)	$\overline{\text{RESET}} = V_{DD}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK & $\overline{\text{CLK}}$ switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle			15		$\mu\text{A}/\text{clock MHz}/\text{data}$
r_{OH}	Output High	$I_{OH} = -20\text{mA}$	2.3V-2.7V	7	13.5	20	Ω
r_{OL}	Output Low	$I_{OL} = 20\text{mA}$	2.3V-2.7V	7	13	20	Ω
$r_{O(D)}$	$[r_{OH} - r_{OL}]$ each separate bit	$I_O = 20\text{mA}$, $T_A = 25^{\circ}\text{C}$	2.5V			4	Ω
C_i	Data Inputs	$V_I = V_{REF} \pm 310\text{ mV}$	2.5V	2.5		3.5	pF
	CLK and $\overline{\text{CLK}}$	$V_{ICR}=1.25\text{V}$, $V_{I(PP)} = 360\text{mV}$		2.5		3.5	
	$\overline{\text{RESET}}$	$V_I = V_{DD}$ or GND		2.5		3.5	

SLGSSTVF16859V DC Electrical Characteristics - (For PC3200)

$T_A = 0 - 70^{\circ}\text{C}$; $V_{DD} = 2.6 \pm 0.1\text{V}$, $V_{DDQ} = 2.6 \pm 0.1\text{V}$; (unless otherwise stated)

SMBL	PARAMETERS	CONDITIONS	V_{DDQ}	MIN	TYP	MAX	UNITS
V_{IK}		$I_I = -18\text{mA}$	2.5V			-1.2	V
V_{OH}		$I_{OH} = -100\mu\text{A}$	2.5V -2.7V	$V_{DDQ} - 0.2$			
		$I_{OH} = -8\text{mA}$	2.5V	1.95			
V_{OL}		$I_{OL} = 100\mu\text{A}$	2.5V -2.7V			0.2	
		$I_{OL} = 8\text{mA}$	2.5V			0.35	
I_I	All Inputs	$V_I = V_{DD}$ or GND	2.7V			± 5	μA
I_{DD}	Standby (Static)	$\overline{\text{RESET}} = \text{GND}$	2.7V			10	μA
	Operating (Static)	$V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, $\overline{\text{RESET}} = V_{DD}$			52		mA
I_{DDD}	Dynamic operating (clock only)	$\overline{\text{RESET}} = V_{DD}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK & $\overline{\text{CLK}}$ switching 50% duty cycle	2.6V		75		$\mu\text{A}/\text{MHz}$
	Dynamic Operating (per each data input)	$\overline{\text{RESET}} = V_{DD}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK & $\overline{\text{CLK}}$ switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle			15		$\mu\text{A}/\text{clock MHz}/\text{data}$
r_{OH}	Output High	$I_{OH} = -20\text{mA}$	2.5V-2.7V	7	13.5	20	Ω
r_{OL}	Output Low	$I_{OL} = 20\text{mA}$	2.5V-2.7V	7	13	20	Ω
$r_{O(D)}$	$[r_{OH} - r_{OL}]$ each separate bit	$I_O = 20\text{mA}$, $T_A = 25^{\circ}\text{C}$	2.6V			4	Ω
C_i	Data Inputs	$V_I = V_{REF} \pm 310\text{ mV}$	2.5V	2.5		3.5	pF
	CLK and $\overline{\text{CLK}}$	$V_{ICR}=1.25\text{V}$, $V_{I(PP)} = 360\text{mV}$		2.5		3.5	
	$\overline{\text{RESET}}$	$V_I = V_{DD}$ or GND		2.5		3.5	

Timing Requirements¹:

(over recommended operating free-air temperature range, unless otherwise noted)

SYMBOL	PARAMETERS		$V_{DD} = 2.5V \pm 0.2V$		UNITS
			MIN	MAX	
f_{clock}	Clock frequency			210	MHz
t_W	Pulse duration	CLK, $\overline{CLK}$ high or low	2.5		ns
t_{ACT}	Differential active time ⁵			22	ns
t_{INACT}	Differential inactive time ⁶			22	ns
t_S	Setup time, fast slew rate ^{2 & 4}	Data before CLK $\uparrow$, $\overline{CLK}$ $\downarrow$	0.65		ns
	Setup time, slow slew rate ^{3 & 4}		0.75		ns
t_H	Hold time, fast slew rate ^{2 & 4}	Data after CLK $\uparrow$, $\overline{CLK}$ $\downarrow$	0.65		ns
	Hold time, slow slew rate ^{3 & 4}		0.8		ns

- Notes:**
- 1 - Guaranteed by design, not 100% tested in production.
 - 2 - For data signal input slew rate of $\geq 1V/ns$.
 - 3 - For data signal input slew rate of $\geq 0.5V/ns$ and $< 1V/ns$.
 - 4 - CLK, $\overline{CLK}$ signals input slew rate of $\geq 1V/ns$.
 - 5 - Data input must be held low for a minimum time ($t_{ACT} \max$) after $\overline{RESET}$ driven high
 - 6 - Data and CLK, $\overline{CLK}$ inputs must be held at valid logic (high or low) levels for a minimum time ($t_{INACT} \max$) after $\overline{RESET}$ driven low

Switching Characteristics:(For PC1600/2100/2700)

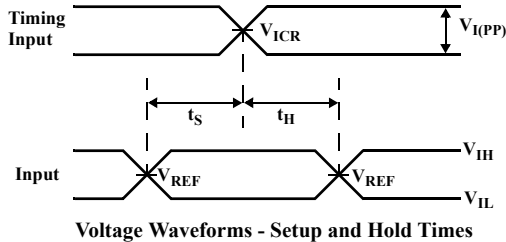
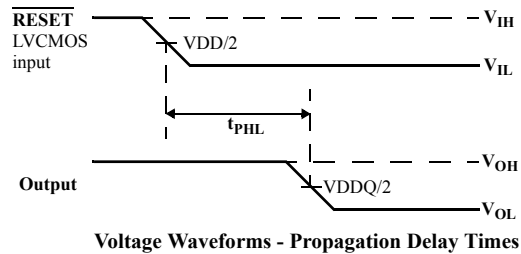
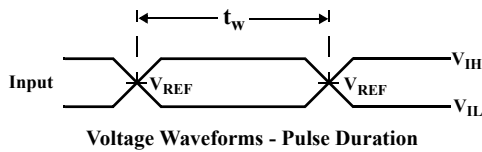
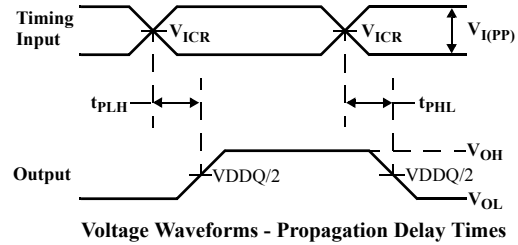
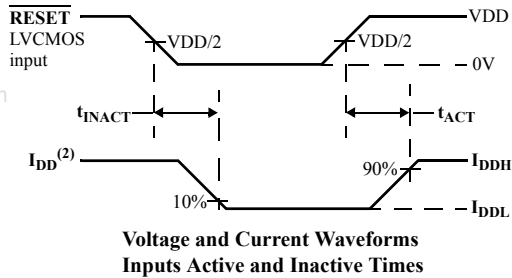
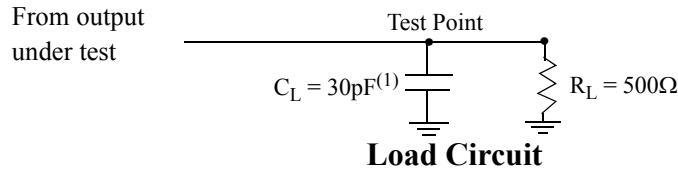
(over recommended operating free-air temperature range, unless otherwise noted)

SYMBOL	From (Input)	To (Output)	$V_{DD} = 2.5V \pm 0.2V$			UNITS
			MIN	TYP	MAX	
f_{max}			210			MHz
t_{PD}	CLK, $\overline{CLK}$	Q	1.1		2.6	ns
t_{PDSS}^1	CLK, $\overline{CLK}$	Q	1.1		2.9	ns
t_{PHL}	$\overline{RESET}$	Q			5	ns

Switching Characteristics:(For PC3200)

(over recommended operating free-air temperature range, unless otherwise noted)

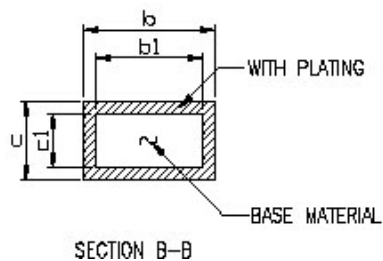
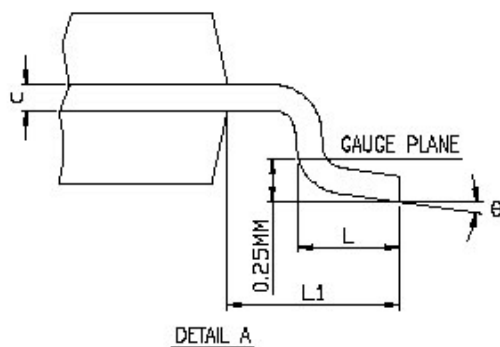
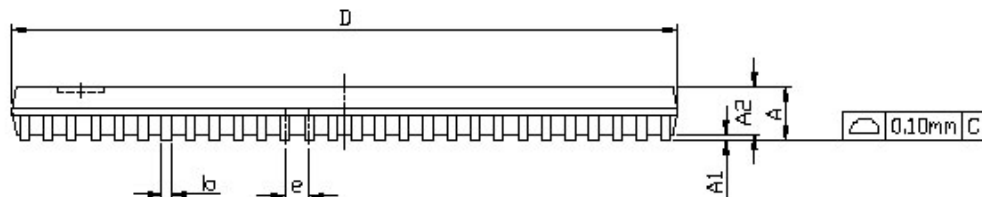
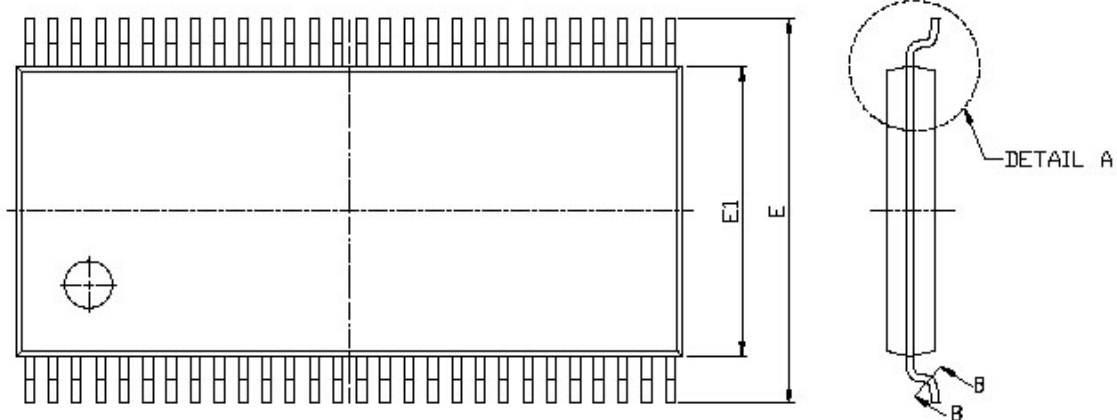
SYMBOL	From (Input)	To (Output)	$V_{DD} = 2.6V \pm 0.1V$			UNITS
			MIN	TYP	MAX	
f_{max}			210			MHz
t_{PD}	CLK, $\overline{CLK}$	Q	1.1		2.2	ns
t_{PDSS}^1	CLK, $\overline{CLK}$	Q	1.1		2.48	ns
t_{PHL}	$\overline{RESET}$	Q			5	ns



Notes:

1. C_L includes measurement probe and jig capacitance.
2. Conditions for I_{DD} testing are with clock and data inputs at V_{DD} or GND, and $I_O = 0\text{mA}$
3. All input pulses are supplied by generators having: $Z_o = 50\Omega$,
input slew rate = $1\text{ V/ns} \pm 20\%$ (unless otherwise specified).
4. The outputs are measured individually with one transition per measurement.
5. $V_{IH} = V_{REF} + 310\text{mV}$ (AC levels) for differential inputs. $V_{IH} = V_{DDQ}$ for LVC MOS input.
6. $V_{IL} = V_{REF} - 310\text{mV}$ (AC levels) for differential inputs. $V_{IL} = \text{GND}$ for LVC MOS input.
7. $t_{PLH} = t_{PHL} = t_{PD}$

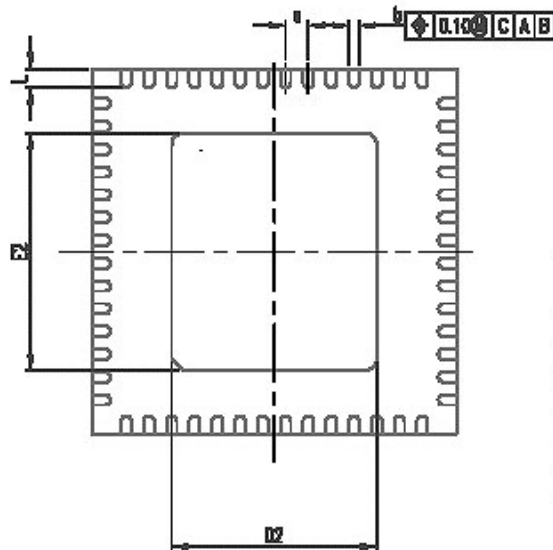
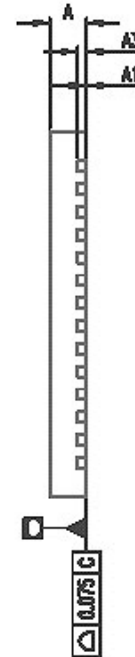
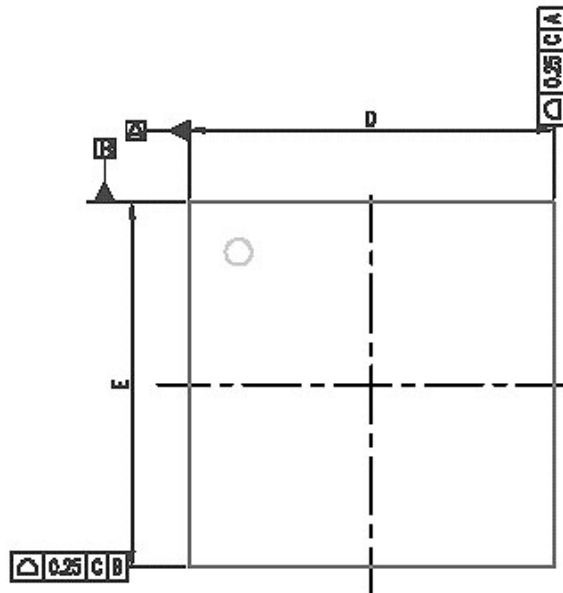
Package dimensions: SLGSSTVF16859H 64-TSSOP
(56-pin drawing shown for reference)



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
E	8.00	8.10	8.20	0.315	0.319	0.323
E1	6.00	6.10	6.20	0.236	0.240	0.244
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00 REF.			0.039 REF.	
b		0.20 TYP.			0.008 TYP.	
b1		0.15 TYP.			0.006 TYP.	
c	0.09		0.20	0.004		0.008
c1	0.05	0.15	0.16	0.002		0.006
e		0.50 BSC.			0.020 BSC.	
θ	0		8	0		8

N	D (MM)			JEDEC
	MIN.	NOM	MAX.	
48	12.40	12.50	12.60	MO-153ED
56	13.90	14.00	14.10	MO-153EE
64	16.90	17.00	17.10	MO-153EF

Package dimensions: SLGSSTVF16859V 52-VFQFN



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A		0.80	0.84		0.031	0.033
A1	0.00	0.02	0.04	0.0000	0.0008	0.0015
A2		0.20 REF.			0.008 REF.	
D	7.90	8.00	8.10	0.311	0.315	0.319
E	7.90	8.00	8.10	0.311	0.315	0.319
JEDEC	MO-220					

N	b			D2			E2			s	L			JEDEC
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
56L	0.18	0.23	0.30	4.35	4.50	4.65	5.05	5.20	5.35	0.500 BSC	0.35	0.40	0.45	MO-220MLD-5
56L1	0.18	0.23	0.30	6.40	6.55	6.70	6.40	6.55	6.70	0.500 BSC	0.35	0.40	0.45	MO-220MLD-5

Ordering Information:

Package type	Package suffix	Topside marking	Ordering code
TSSOP-64pin 6.1mm body	H	SLGSSTVF16859H	SLGSSTVF16859H-TR (2,000 pcs/Reel)
VFQFN VLLD-2 56pin 8.0x8.0mm body	V	SLGSSTVF16859V	SLGSSTVF16859V-TR (2,000 pcs/Reel)
VFQFN VLLD-2 56pin 8.0x8.0mm body	V	SLGSSTVF16859V	SLGSSTVF16859V (2,000 pcs/Tray)

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