

**600V 3-Phase Bridge Driver**
**PRODUCT SUMMARY**

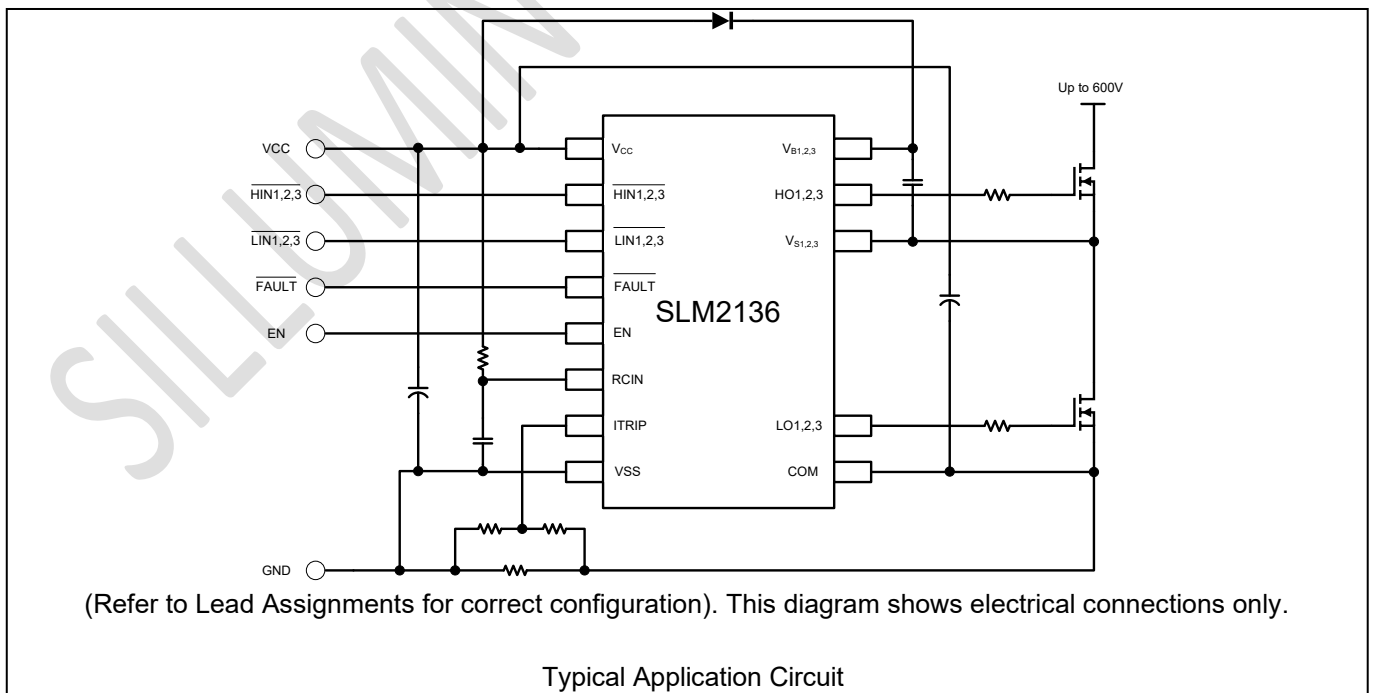
- $V_{\text{OFFSET}}$  600 V max.
- $I_{\text{O}+/-}$  250 mA / 350 mA
- $V_{\text{OUT}}$  10 V - 20 V
- $t_{\text{on/off}}$  (typ.) 400 ns / 380 ns
- **Deadtime** (typ.) 290 ns

**FEATURES**

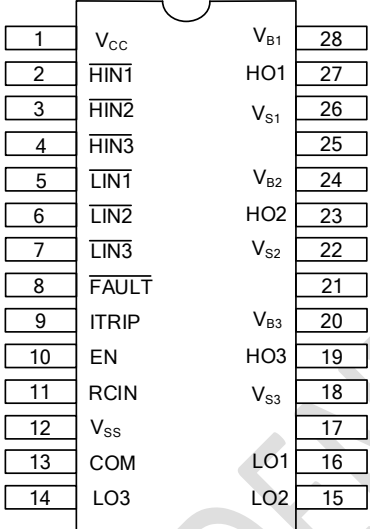
- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for all channels
- Low/high side output out of phase with inputs
- 3.3 V, 5 V, and 15 V logic compatible
- Lower di/dt gate drive for better noise immunity
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Externally programmable delay for automatic fault clear
- SOIC-28L package

**GENERAL DESCRIPTION**

The SLM2136 is a high voltage, high speed power MOSFET and IGBT drivers with three independent high- and low-side referenced output channels for 3-phase applications. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3 V logic. A current trip function which terminates all six outputs can be derived from an external current sense resistor. An enable function is available to terminate all six outputs simultaneously. An open-drain FAULT signal is provided to indicate that an overcurrent or undervoltage shutdown has occurred. Overcurrent fault conditions are cleared automatically after a delay programmed externally via an RC network connected to the RCIN input. The output drivers feature a high pulse current buffer stage designed for minimum driver cross conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

**TYPICAL APPLICATION CIRCUIT**


**PIN CONFIGURATION**

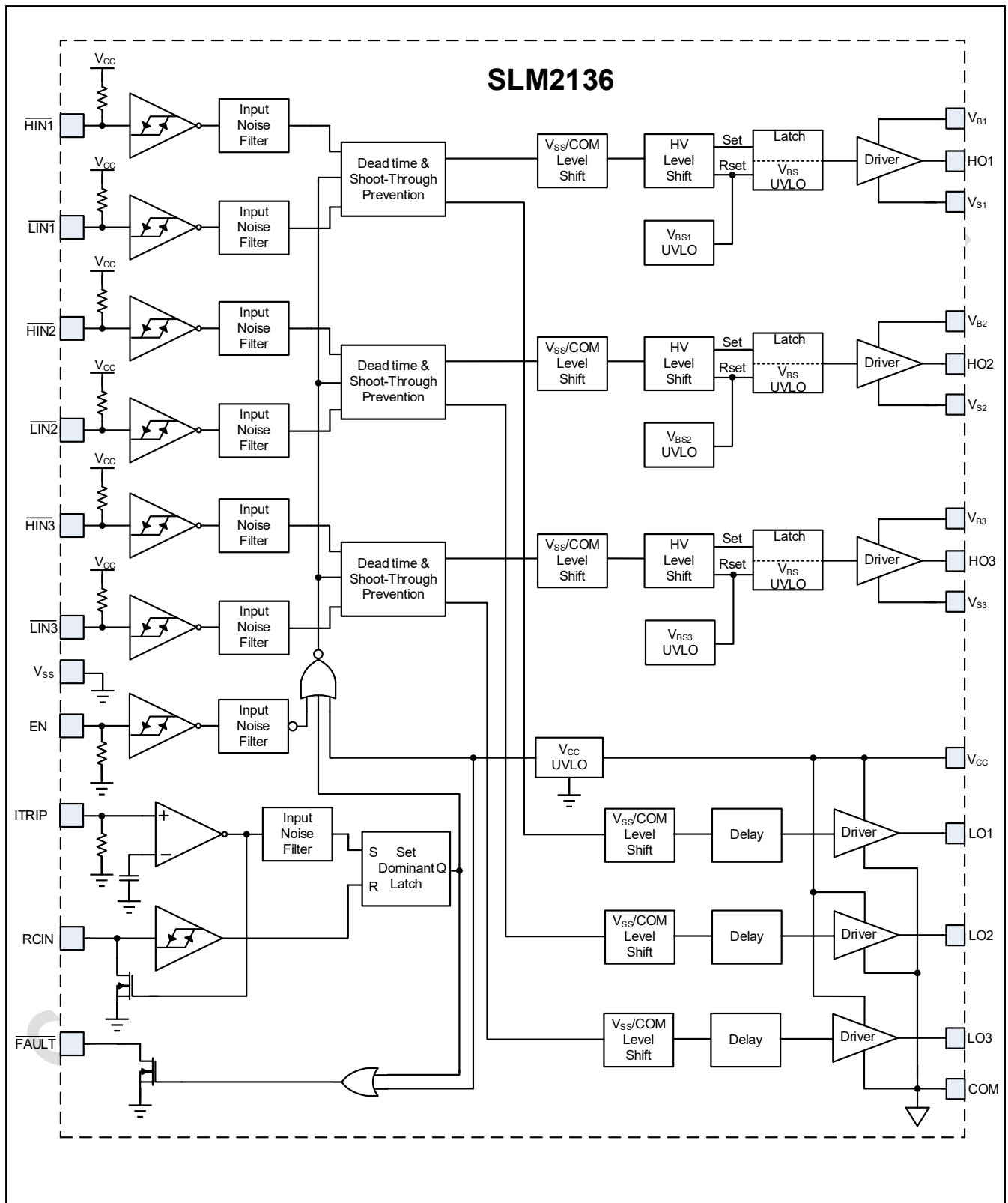
Package	Pin Configuration (Top View)
SOIC-28L	

**PIN DESCRIPTION**

No.	Pin	Description
1	V <sub>CC</sub>	Low-side and logic fixed supply.
2, 3, 4	$\overline{\text{HIN}}_{1, 2, 3}$	Logic input for high-side gate driver output (HO), out of phase.
5, 6, 7	$\overline{\text{LIN}}_{1, 2, 3}$	Logic input for low-side gate driver output (LO), out of phase.
8	$\overline{\text{FAULT}}$	Indicates over-current (ITRIP) or low-side undervoltage lockout has occurred. Negative logic, open-drain output.
9	ITRIP	Analog input for overcurrent shutdown. When active, ITRIP shuts down outputs and activates FAULT and RCIN low. When ITRIP becomes inactive, FAULT stays active low for an externally set time $T_{\text{FLTCLR}}$ , then automatically becomes inactive (open-drain high impedance).
10	EN	Logic input to enable I/O functionality. I/O logic functions when ENABLE is high. No effect on FAULT and not latched.
11	RCIN	External RC network input used to define FAULT CLEAR delay, $T_{\text{FLTCLR}}$ , approximately equal to $R \cdot C$ . When $\text{RCIN} > 8 \text{ V}$ , the FAULT pin goes back into open-drain high-impedance.
12	V <sub>SS</sub>	Logic ground.
13	COM	Low-side gate drivers return.
14, 15, 16	LO <sub>1, 2, 3</sub>	Low-side gate driver outputs.
18, 22, 26	V <sub>S1, 2, 3</sub>	High-side floating supply return.
19, 23, 27	HO <sub>1, 2, 3</sub>	High-side gate driver outputs.
20, 24, 28	V <sub>B1, 2, 3</sub>	High-side floating supply.

**ORDERING INFORMATION**
**Industrial Range: -40°C to +125°C**

Order Part No.	Package	QTY
SLM2136CF-DG	SOIC-28L, Pb-Free	1000/Reel

**FUNCTIONAL BLOCK DIAGRAM**


**ABSOLUTE MAXIMUM RATINGS**

Symbol	Definition	Min.	Max.	Units	
$V_B$	High-side floating absolute voltage	-0.3	625	V	
$V_S$	High-side floating supply offset voltage	$V_{B1,2,3} - 25$	$V_{B1,2,3} + 0.3$		
$V_{HO}$	High-side floating output voltage	$V_{S1,2,3} - 0.3$	$V_{B1,2,3} + 0.3$		
$V_{CC}$	Low-side and logic fixed supply voltage	-0.3	25		
$V_{SS}$	Logic ground	$V_{CC} - 25$	$V_{CC} + 0.3$		
$V_{IN}$	Logic input voltage (LIN, HIN, ITRIP, EN)	$V_{SS} - 0.3$	Lower of ( $V_{SS} + 15$ ) or ( $V_{CC} + 0.3$ )		
$V_{LO1,2,3}$	Low-side output voltage	-0.3	$V_{CC} + 0.3$		
$V_{RCIN}$	RCIN input voltage	$V_{SS} - 0.3$	$V_{CC} + 0.3$		
$V_{FLT}$	FAULT output voltage	$V_{SS} - 0.3$	$V_{CC} + 0.3$		
$dV_S/dt$	Allowable offset supply voltage transient	---	50		V/ns
$P_D$	Package power dissipation @ $T_A \leq +25^\circ\text{C}$	SOIC-28L	---	1.6	W
$R_{thJA}$	Thermal resistance, junction to ambient	SOIC-28L	---	75	$^\circ\text{C}/\text{W}$
$T_J$	Junction temperature	---	150	$^\circ\text{C}$	
$T_S$	Storage temperature	-55	150		
$T_L$	Lead temperature (soldering, 10 seconds)	---	300		

**Note:**

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High-side floating supply voltage	$V_{S1,2,3} + 10$	$V_{S1,2,3} + 20$	V
$V_{S1,2,3}$	High-side floating supply offset voltage	Note 1	600	
$V_{HO1,2,3}$	High-side floating output voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	
$V_{LO1,2,3}$	Low-side output voltage	0	$V_{CC}$	
$V_{CC}$	Low-side and logic fixed supply voltage	10	20	
$V_{SS}$	Logic ground	-5	5	
$V_{FLT}$	FAULT output voltage	$V_{SS}$	$V_{CC}$	
$V_{RCIN}$	RCIN input voltage	$V_{SS}$	$V_{CC}$	
$V_{ITRIP}$	ITRIP input voltage	$V_{SS}$	$V_{SS} + 5V$	
$V_{IN}$	Logic input voltage $\overline{LIN1, 2, 3}$ , $\overline{HIN1, 2, 3}$	$V_{SS}$	$V_{SS} + 5V$	
$T_A$	Ambient temperature	-40	125	$^\circ\text{C}$

**Note:**

- Logic operational for  $V_S$  of (COM - 5 V) to (COM + 600V). Logic state held for  $V_S$  of (COM-5V) to (COM -  $V_{BS}$ ).
- All input pins and the ITRIP and EN pins are internally clamped with a 5.2V zener diode.
- The input/output logic timing diagram is shown in Fig. 1.
- For proper operation the device should be used within the recommended conditions.
- The  $V_S$  offset rating is tested with all supplies biased at a 15 V differential.

**DYNAMIC ELECTRICAL CHARACTERISTICS**
 $V_{BIAS} (V_{CC}, V_{BS}) = 15\text{ V}$ ,  $V_{S1,2,3} = V_{SS} = \text{COM}$ ,  $C_L = 1000\text{ pF}$  and  $T_A = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$t_{on}$	Turn-on propagation delay	$V_S = 0\text{ V}$	300	425	550	ns
$t_{off}$	Turn-off propagation delay	$V_S = 600\text{ V}$	250	400	550	
$t_r$	Turn-on rise time		---	125	190	
$t_f$	Turn-off fall time		---	50	75	
$t_{EN}$	Enable low to output shutdown propagation delay	$V_{IN}, V_{EN} = 0\text{ V or }5\text{ V}$	300	450	600	
$t_{ITRIP}$	ITRIP to output shutdown propagation delay	$V_{ITRIP} = 5\text{ V}$	500	750	1000	
$t_{bl}$	ITRIP blanking time	$V_{IN} = 0\text{ V or }5\text{ V}$ $V_{ITRIP} = 5\text{ V}$	100	150	---	
$t_{FLT}$	ITRIP to $\overline{\text{FAULT}}$ propagation delay	$V_{IN} = 0\text{ V or }5\text{ V}$ $V_{ITRIP} = 5\text{ V}$	400	600	800	
$t_{FILIN}$	Input filter time (HIN, LIN)	$V_{IN} = 0\text{ V \& }5\text{ V}$	100	200	---	
$t_{FLTCLR}$	FAULT clear time RCIN: R = 2 M $\Omega$ , C = 1nF	$V_{IN} = 0\text{ V or }5\text{ V}$ $V_{ITRIP} = 0\text{ V}$	1.3	1.65	2	ms
DT	Deadtime, LS turn-off to HS turn-on & HS turn-on to LS turn-off	$V_{IN} = 0\text{ V \& }5\text{ V}$	220	290	360	ns
MT	Matching delay, HS & LS turn-on/off	External dead time > 400 ns	---	40	75	
MDT	Matching delay, max ( $t_{on}, t_{off}$ ) – min ( $t_{on}, t_{off}$ ), ( $t_{on}, t_{off}$ are applicable to all 3 channels)		---	25	70	
PM	Output pulse width matching (pwin - pwout) (Fig. 2)		---	40	75	

**STATIC ELECTRICAL CHARACTERISTICS**
 $V_{BIAS} (V_{CC}, V_{BS1,2,3}) = 15\text{ V}$  and  $T_A = 25^\circ\text{C}$  unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$ , and  $I_{IN}$  parameters are referenced to  $V_{SS}$  and are applicable to all 6 channels ( $\overline{\text{LIN1, 2, 3}}$  and  $\overline{\text{HIN1, 2, 3}}$ ). The  $V_O$  and  $I_O$  parameters are referenced to COM and  $V_{S1,2,3}$  and are applicable to the respective output leads: HO1,2,3 and LO1,2,3.

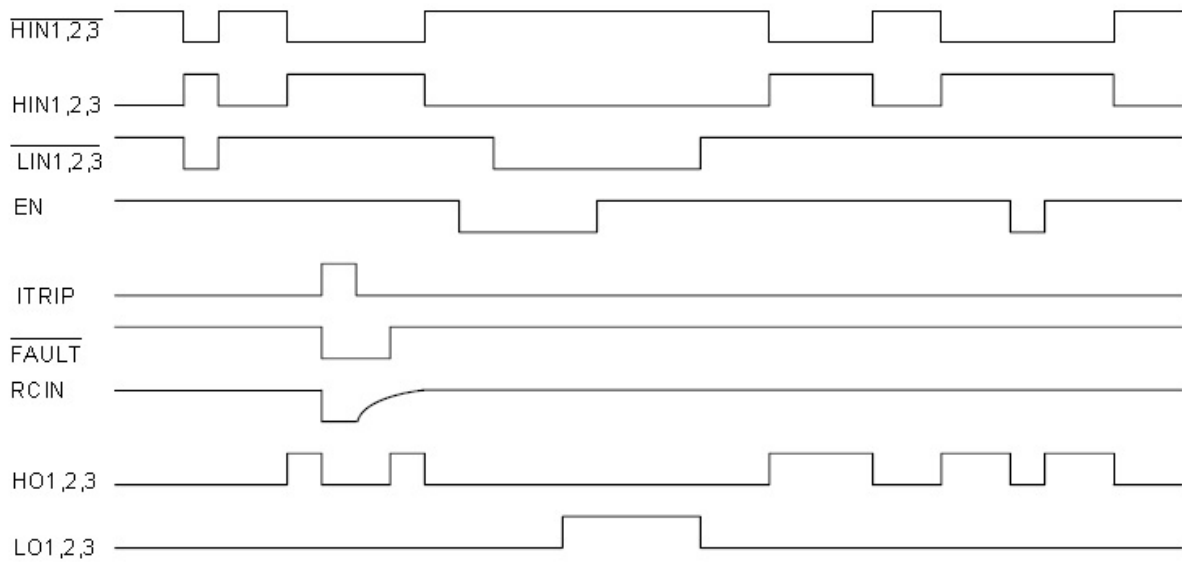
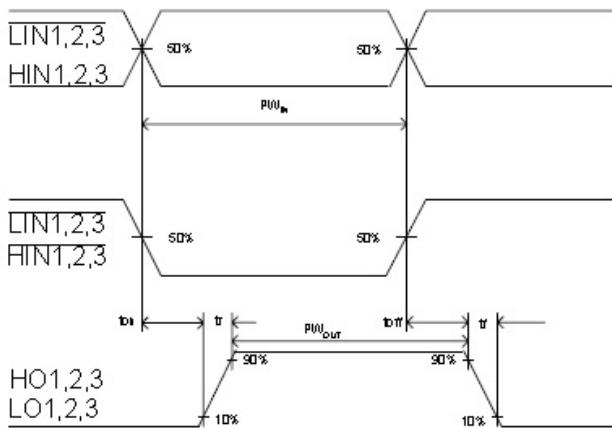
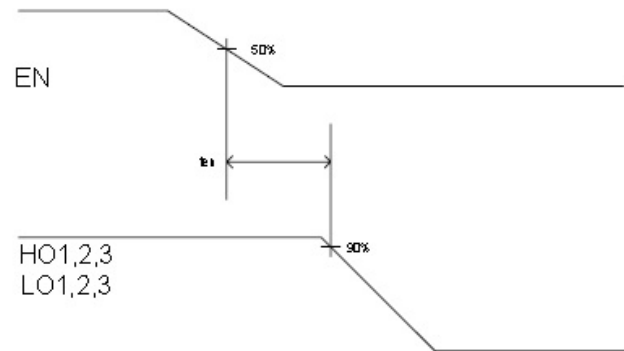
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{IH}$	Logic "0" input voltage ( $\overline{\text{LIN1, 2, 3}}$ and $\overline{\text{HIN1, 2, 3}}$ )	$V_{CC} = 10\text{ V to }20\text{ V}$	2.0	---	---	V
$V_{IL}$	Logic "1" input voltage ( $\overline{\text{LIN1, 2, 3}}$ and $\overline{\text{HIN1, 2, 3}}$ )		---	---	1.0	
$V_{EN, TH+}$	Enable positive going threshold		---	---	1.7	
$V_{EN, TH-}$	Enable negative going threshold		1.0	---	---	
$V_{IT, TH+}$	ITRIP positive going threshold		0.4	0.5	0.6	

$V_{IT, HYS}$	ITRIP input hysteresis		---	0.1	---	V	
$V_{RCIN, TH+}$	RCIN positive going threshold		---	8	---		
$V_{RCIN, HYS}$	RCIN input hysteresis		---	1	---		
$V_{OH}$	High level output voltage, $V_{BIAS} - V_O$	$I_O = 20 \text{ mA}$	---	0.5	1.0		
$V_{OL}$	Low level output voltage, $V_O$		---	0.3	0.6		
$V_{CCUV+}$ $V_{BSUV+}$	$V_{CC}$ and $V_{BS}$ supply undervoltage positive going threshold		8.0	8.9	9.8		
$V_{CCUV-}$ $V_{BSUV-}$	$V_{CC}$ and $V_{BS}$ supply undervoltage negative going threshold		7.4	8.2	9.0		
$V_{CCUVH}$ $V_{BSUVH}$	$V_{CC}$ and $V_{BS}$ supply undervoltage lockout hysteresis		0.3	0.7	---		
$V_{IN\_CLAMP}$	Input clamp voltage (HIN, LIN, ITRIP and EN)	$I_{IN} = 100 \mu\text{A}$	---	5.8	---		
$I_{LK}$	Offset supply leakage current	$V_{B1,2,3} = V_{S1,2,3} = 600 \text{ V}$	---	---	50	$\mu\text{A}$	
$I_{QBS}$	Quiescent $V_{BS}$ supply current	$V_{IN} = 0 \text{ V or } 5 \text{ V}$	---	60	75		
$I_{QCC}$	Quiescent $V_{CC}$ supply current		---	1.6	2.3	mA	
$I_{IN+}$	Logic "1" input bias current	$\overline{HIN1, 2, 3} = 0 \text{ V},$ $\overline{LIN1, 2, 3} = 0 \text{ V}$	---	150	200	$\mu\text{A}$	
$I_{IN-}$	Logic "0" input bias current	$\overline{HIN1, 2, 3} = 5 \text{ V},$ $\overline{LIN1, 2, 3} = 5 \text{ V}$	---	200	300		
$I_{ITRIP+}$	"High" ITRIP input bias current	$V_{ITRIP} = 5 \text{ V}$	---	30	100		
$I_{ITRIP-}$	"Low" ITRIP input bias current	$V_{ITRIP} = 0 \text{ V}$	---	0	1		
$I_{EN+}$	"High" ENABLE input bias current	$V_{ENABLE} = 5 \text{ V}$	---	35	100		
$I_{EN-}$	"Low" ENABLE input bias current	$V_{ENABLE} = 0 \text{ V}$	---	0	1		
$I_{RCIN}$	RCIN input bias current	$V_{RCIN} = 0 \text{ V or } 15 \text{ V}$	---	0	1		
$I_{O+}$	Output high short circuit pulsed current	$V_O = 0 \text{ V}, V_{IN} = V_{IH}$ $PW \leq 10 \mu\text{s}$	120	200	---		mA
$I_{O-}$	Output low short circuit pulsed current	$V_O = 15 \text{ V}, V_{IN} = V_{IL}$ $PW \leq 10 \mu\text{s}$	250	350	---		
$R_{on\_RCIN}$	RCIN low on resistance		---	50	100	$\Omega$	
$R_{on\_FAULT}$	FAULT low on resistance		---	50	100		

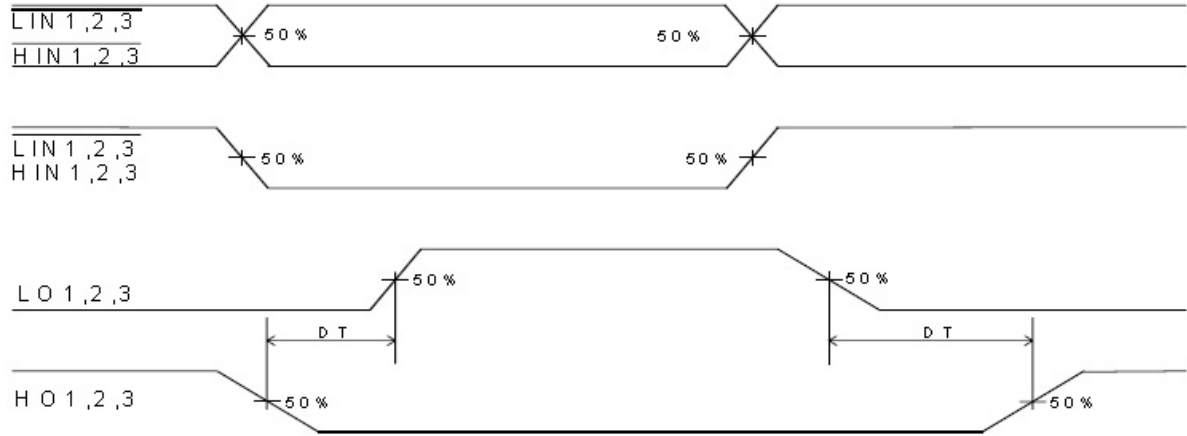
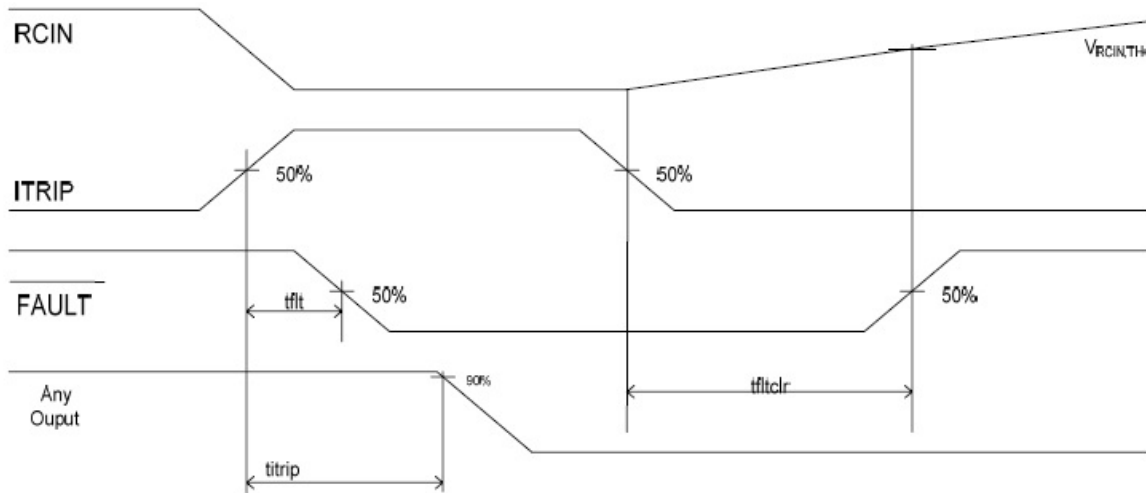
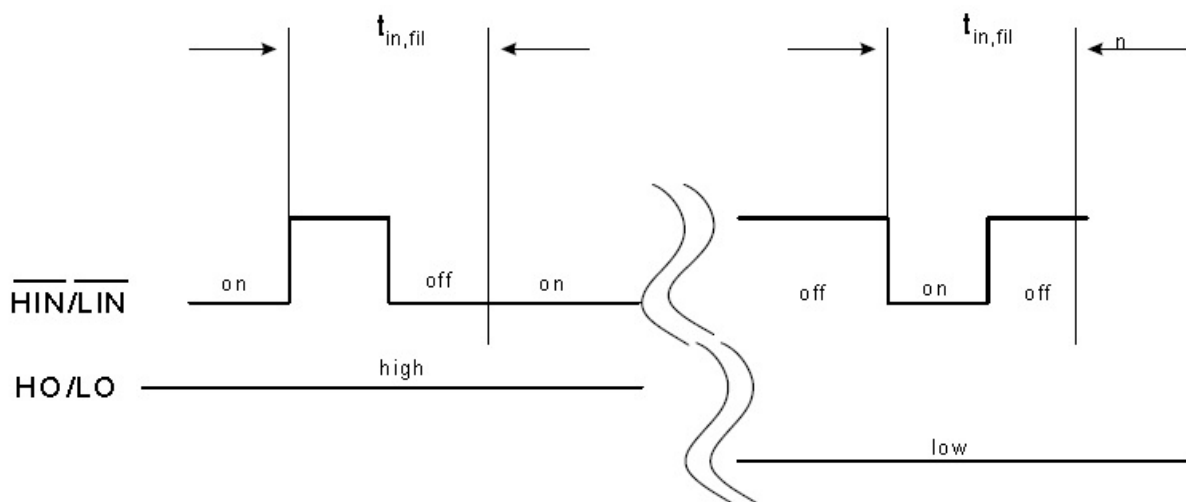
VCC	VBS	ITRIP	ENABLE	FAULT	LO1,2,3	HO1,2,3
< UVCC	X	X	X	0 (note 1)	0	0
15 V	< UVBS	0 V	5 V	High imp	LIN1,2,3	0
15 V	15 V	0 V	5 V	High imp	LIN1,2,3	HIN1,2,3
15 V	15 V	> V <sub>ITRIP</sub>	5 V	0 (note 2)	0	0
15 V	15 V	0 V	0 V	High imp	0	0

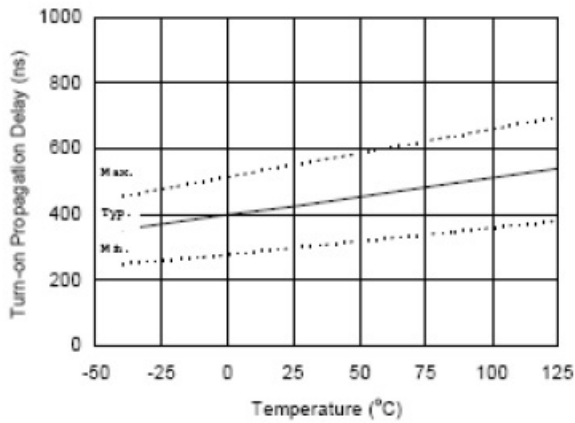
**Note:**

1. A shoot-through prevention logic prevents LO1,2,3 and HO1,2,3 for each channel from turning on simultaneously.
2. UVCC is not latched, when V<sub>CC</sub> > UV<sub>CC</sub>, FAULT returns to high impedance.
3. When ITRIP < V<sub>ITRIP</sub>, FAULT returns to high-impedance after RCIN pin becomes greater than 8 V (@ V<sub>CC</sub> = 15 V).

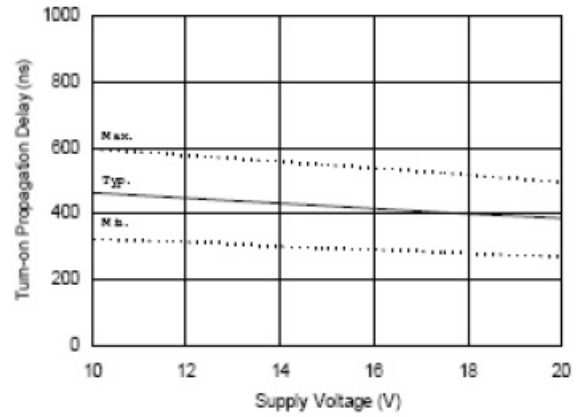

**Fig. 1. Input/Output Timing Diagram**

**Fig. 2. Switching Time Waveforms**

**Fig. 3. Output Enable Timing Waveform**



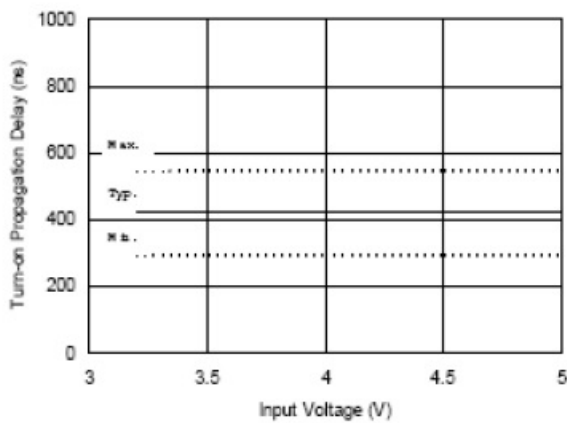


**Fig. 4. Internal Deadtime Timing Waveforms**

**Fig. 5. ITRIP/RCIN Timing Waveforms**

**Fig. 6. Input Filter Function**



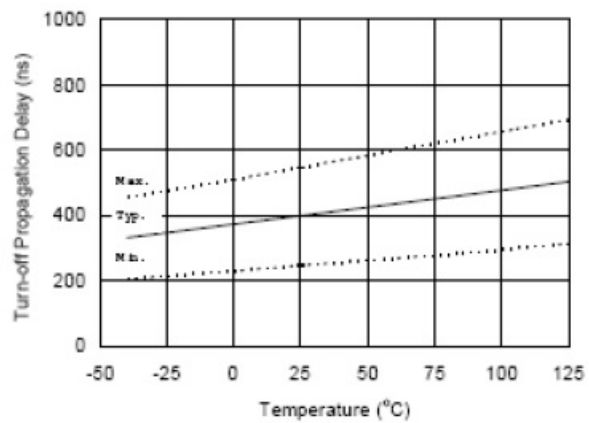
**Figure 6A. Turn-on Propagation Delay vs. Temperature**



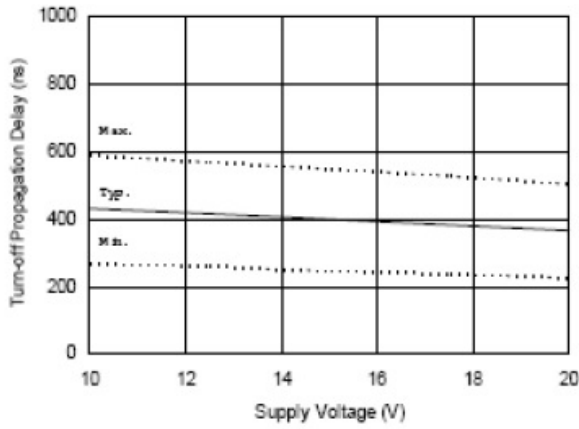
**Figure 6B. Turn-on Propagation Delay vs. Supply Voltage**



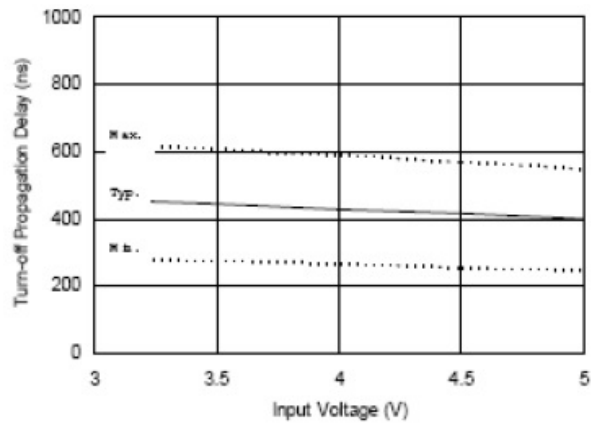
**Figure 6C. Turn-on Propagation Delay vs. Input Voltage**



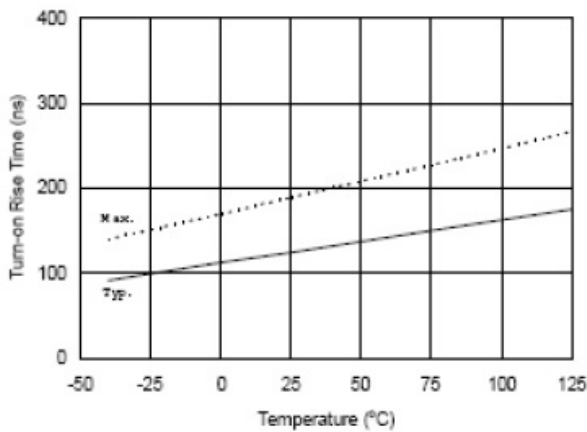
**Figure 7A. Turn-off Propagation Delay vs. Temperature**



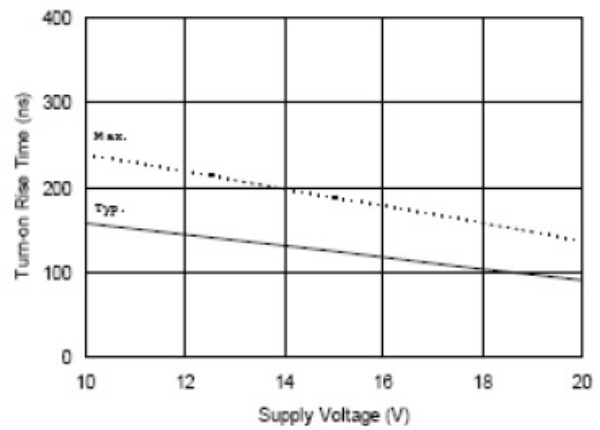
**Figure 7B. Turn-off Propagation Delay vs. Supply Voltage**



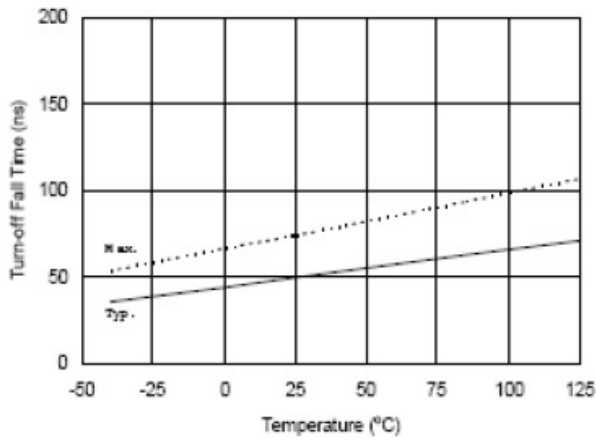
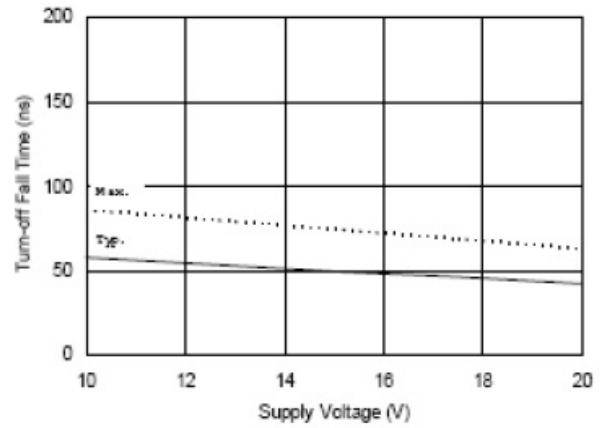
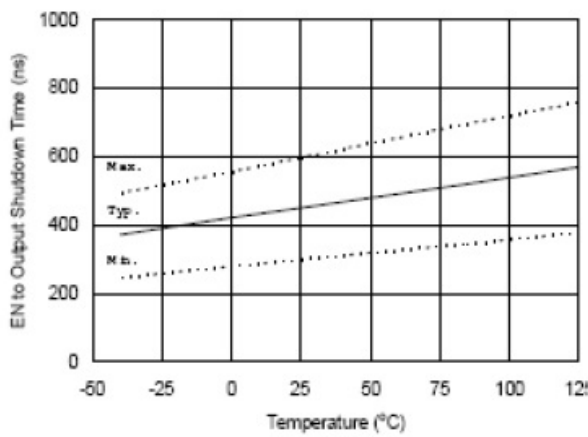
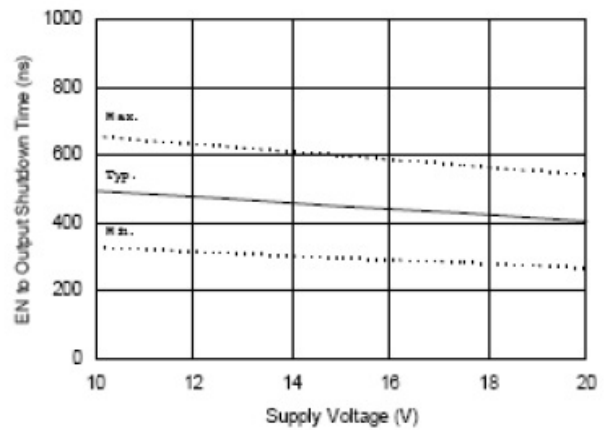
**Figure 7C. Turn-off Propagation Delay vs. Input Voltage**

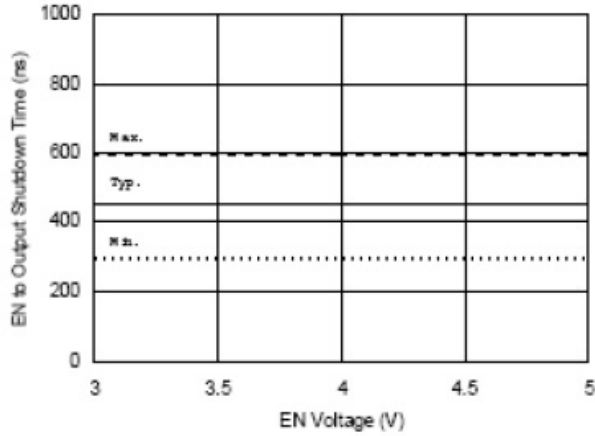


**Figure 8A. Turn-on Rise Time vs. Temperature**

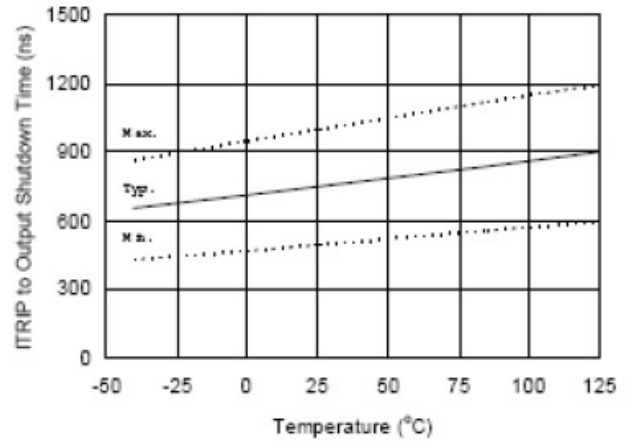


**Figure 8B. Turn-on Rise Time vs. Supply Voltage**

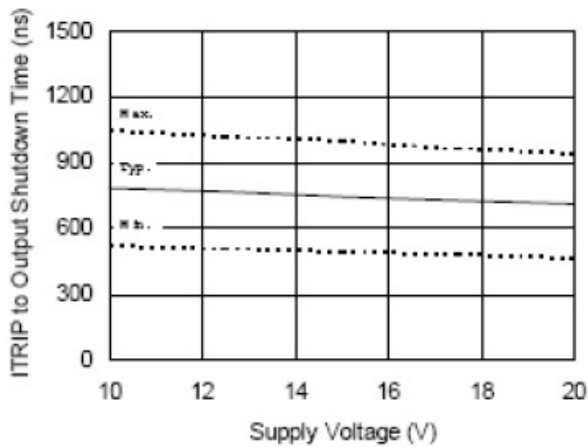

**Figure 9A. Turn-off Fall Time vs. Temperature**

**Figure 9B. Turn-off Fall Time vs. Supply Voltage**

**Figure 10A. EN to Output Shutdown Time vs. Temperature**

**Figure 10B. EN to Output Shutdown Time vs. Supply Voltage**



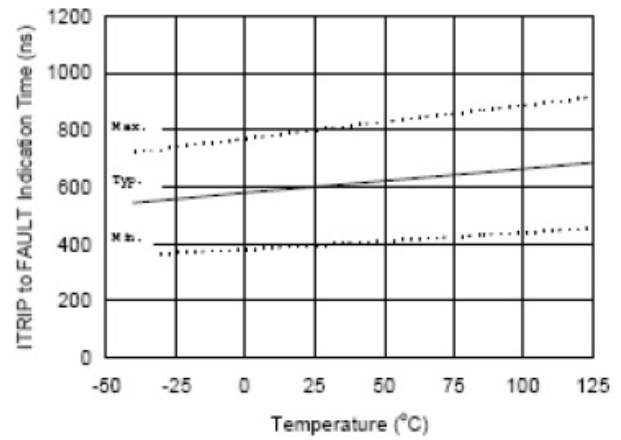
**Figure 10C. EN to Output Shutdown Time vs. EN Voltage**



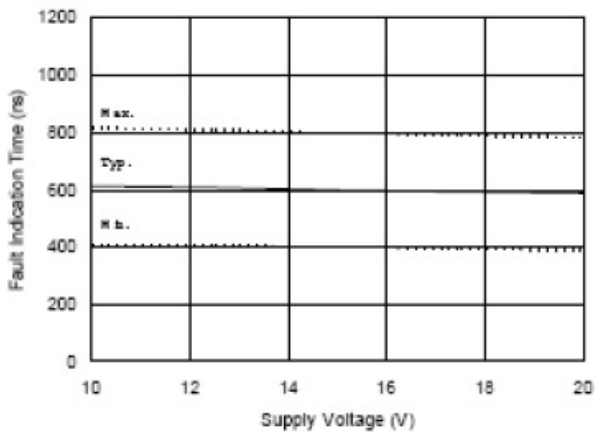
**Figure 11A. ITRIP to Output Shutdown Time vs. Temperature**



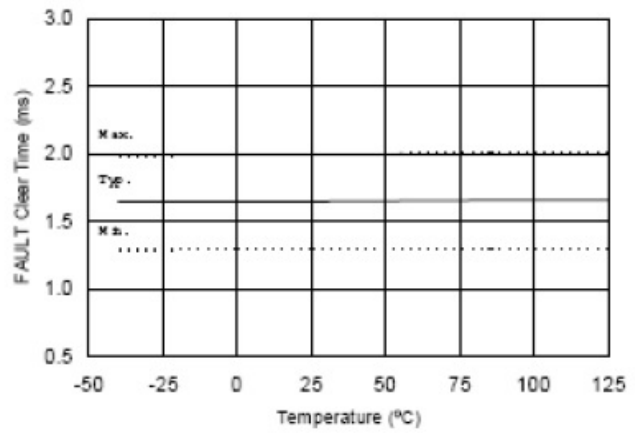
**Figure 11B. ITRIP to Output Shutdown Time vs. Supply Voltage**



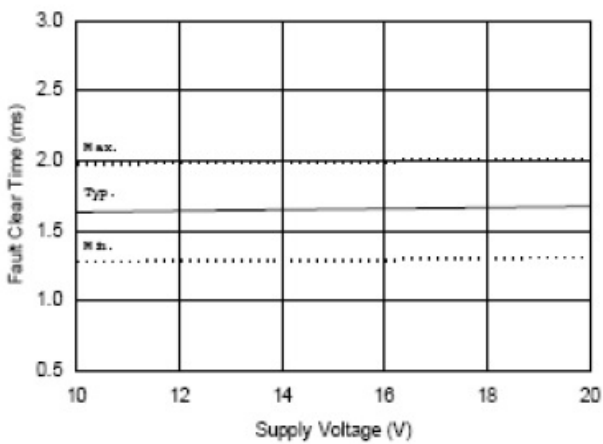
**Figure 12A. ITRIP to FAULT Indication Time vs. Temperature**



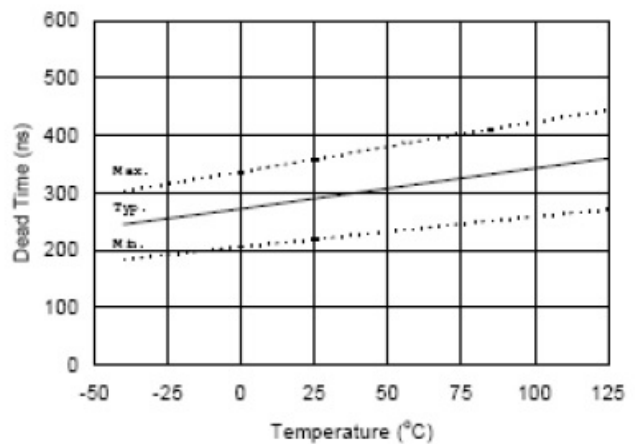
**Figure 12B. ITRIP to FAULT Indication Time vs. Supply Voltage**



**Fig13A. FAULT Clear Time vs. Temperature**



**Figure 13B. FAULT Clear Time vs. Supply Voltage**



**Figure 14A. Dead Time vs. Temperature**

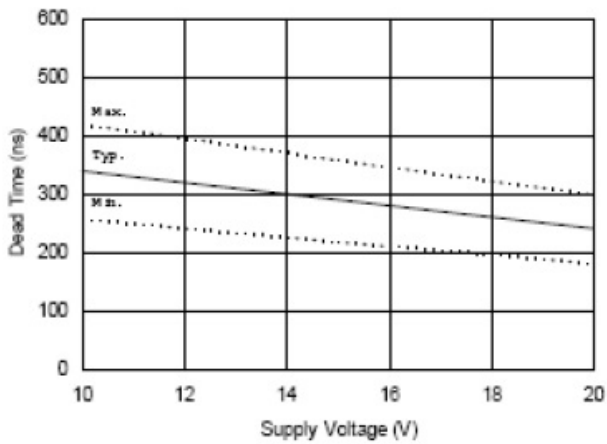


Figure 14B. Dead Time Time vs. Supply Voltage

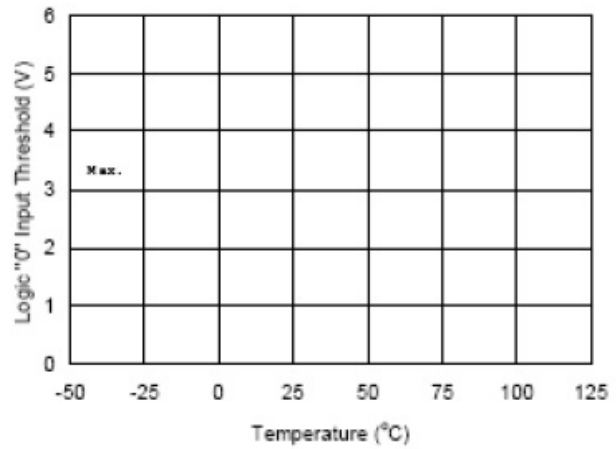


Figure 15A. Logic "0" Input Threshold vs. Temperature

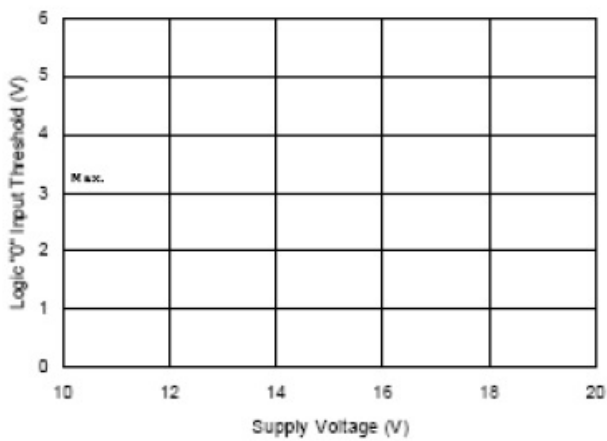


Figure 15B. Logic "0" Input Threshold vs. Supply Voltage

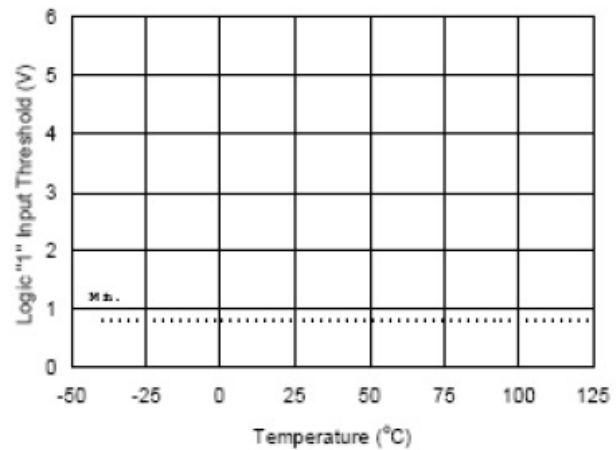
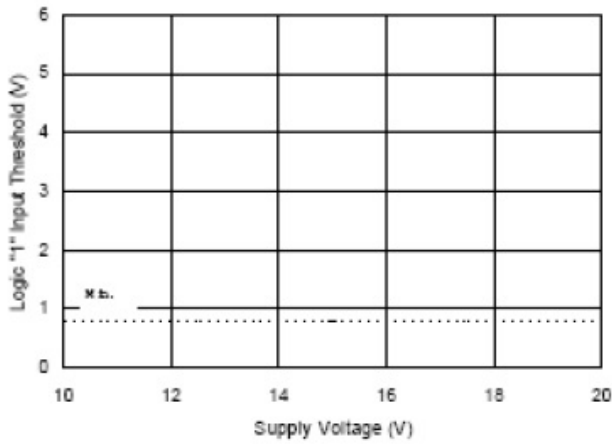
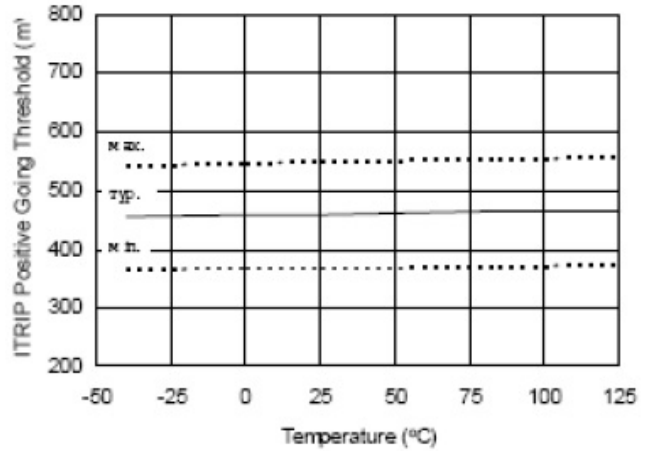


Figure 16A. Logic "1" Input Threshold vs. Temperature

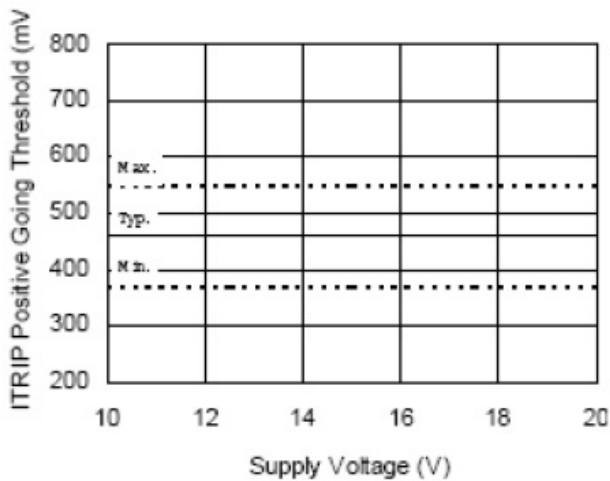




**Figure 16B. Logic "1" Input Threshold vs. Supply Voltage**



**Figure 17A. ITRIP Positive Going Threshold vs. Temperature**



**Figure 17B. ITRIP Positive Going Threshold vs. Supply Voltage**





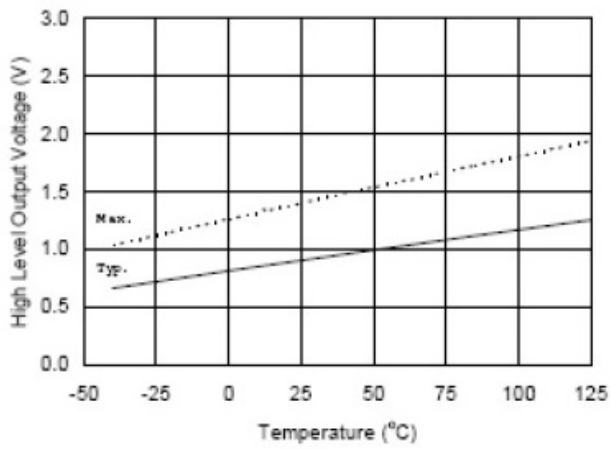


Figure 18A. High Level Output vs. Temperature

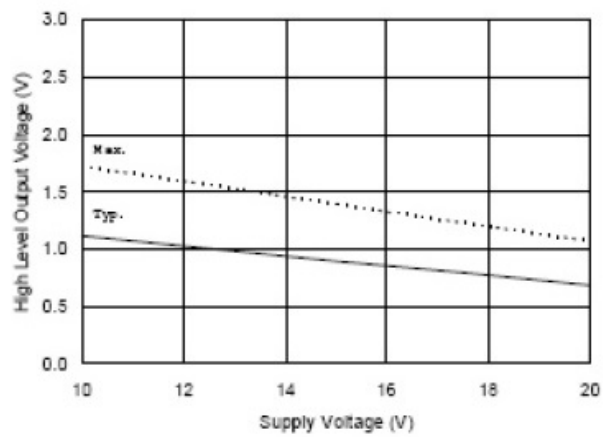


Figure 18B. High Level Output vs. Supply Voltage

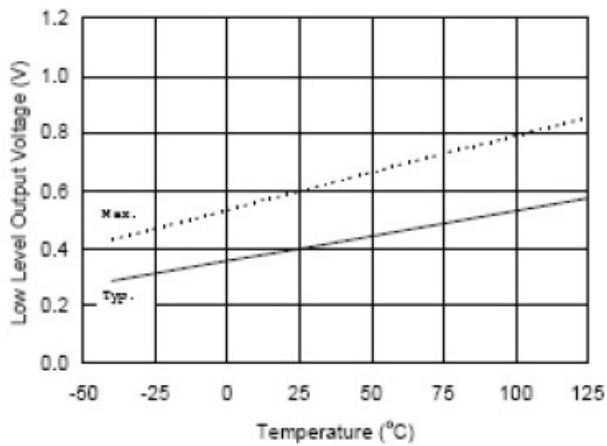


Figure 19A. Low Level Output vs. Temperature

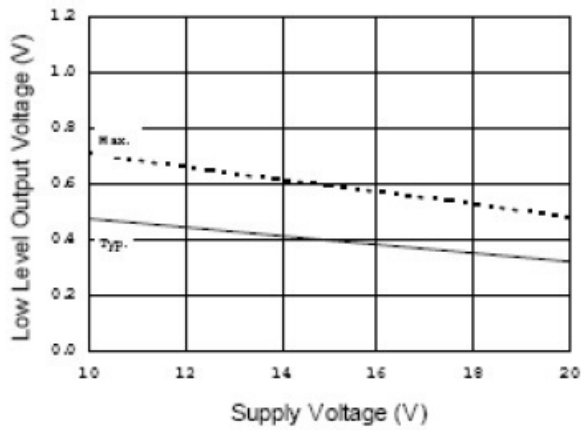


Figure 19B. Low Level Output vs. Supply Voltage

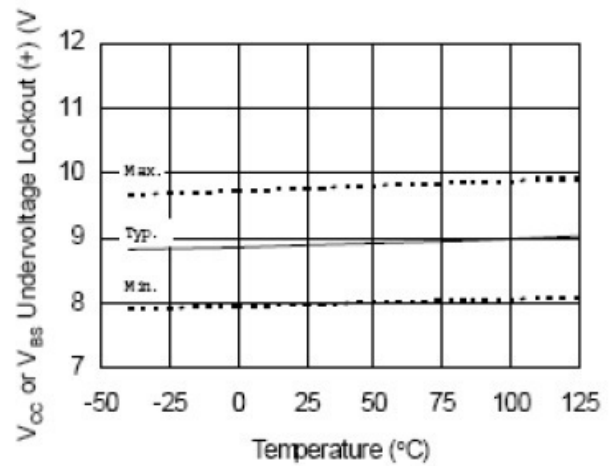


Figure 20.  $V_{CC}$  or  $V_{SS}$  Undervoltage (+) vs. Temperature

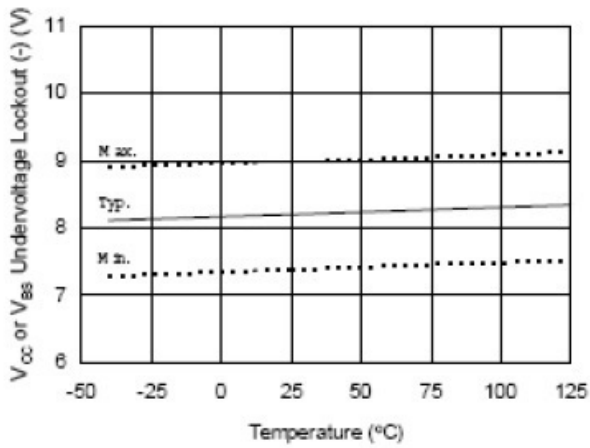


Figure 21.  $V_{CC}$  or  $V_{SS}$  Undervoltage (-) vs. Temperature

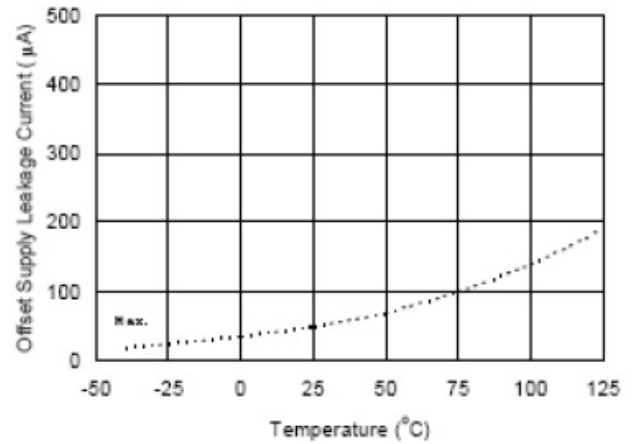


Figure 22. Offset Supply Leakage Current vs. Temperature

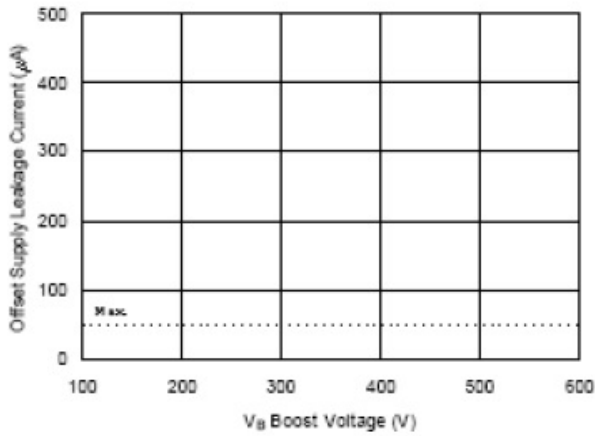


Figure 23. Offset Supply Leakage Current vs.  $V_B$  Boost Voltage

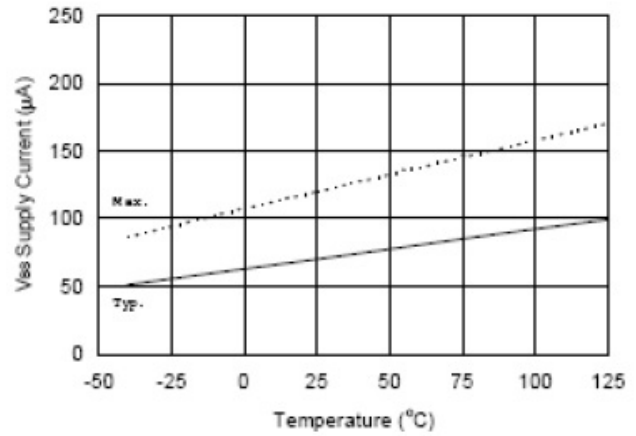


Figure 24.  $V_{Bs}$  Supply Current vs. Temperature

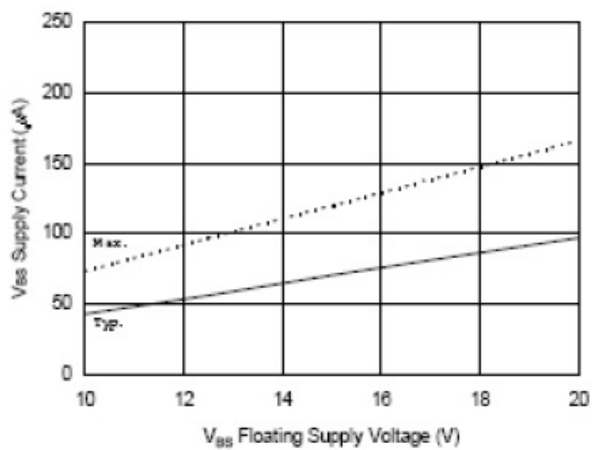


Figure 25.  $V_{Bs}$  Supply Current vs.  $V_{Bs}$  Floating Supply Voltage

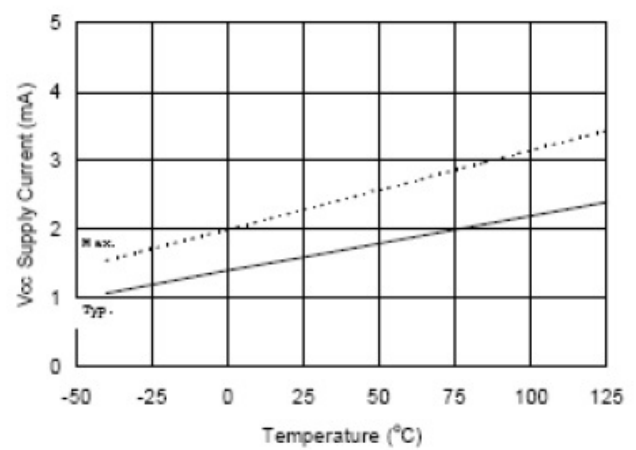
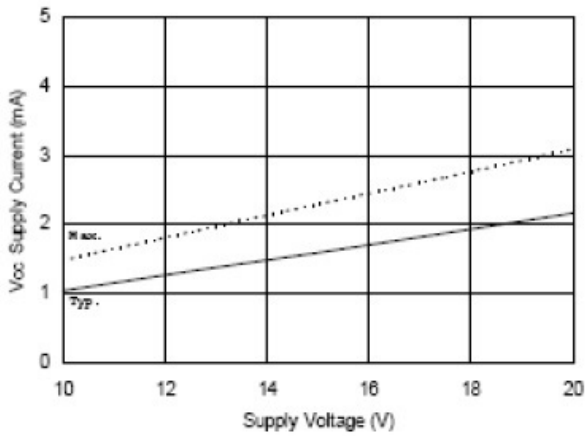
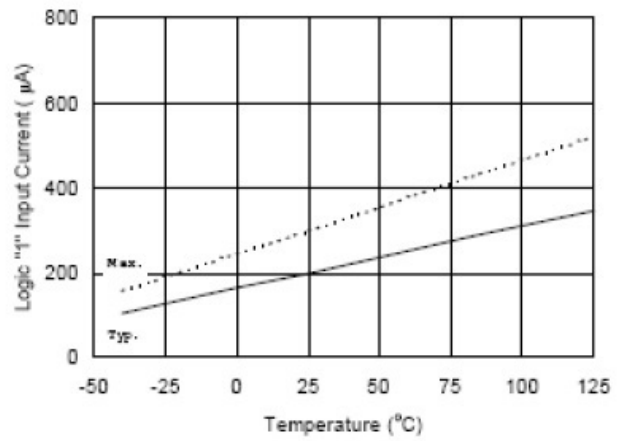


Figure 26.  $V_{Co}$  Supply Current vs. Temperature

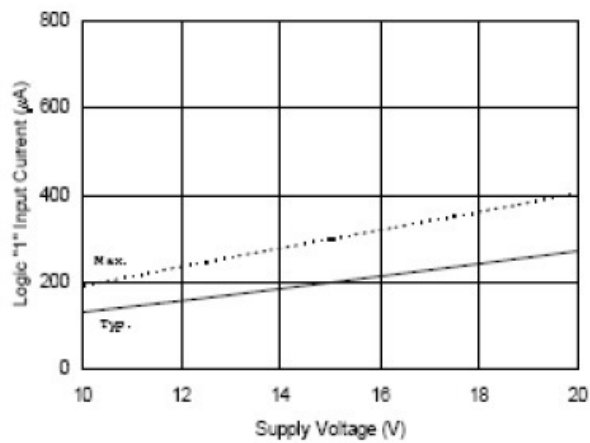
SILL



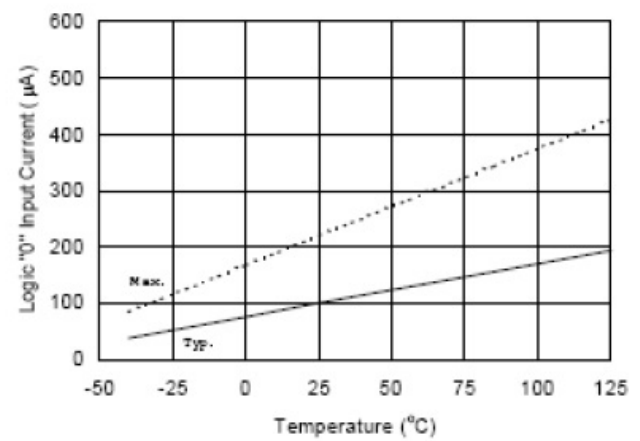
**Figure 27. V<sub>CC</sub> Supply Current vs. V<sub>CC</sub> Supply Voltage**



**Figure 28. Logic "1" Input Current vs. Temperature**



**Figure 29. Logic "1" Input Current vs. Supply Voltage**



**Figure 30A. Logic "0" Input Current vs. Temperature**

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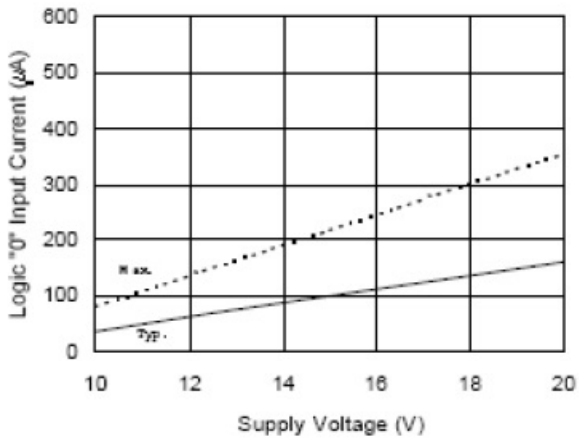


Figure 30B. Logic "0" Input Current vs. Supply

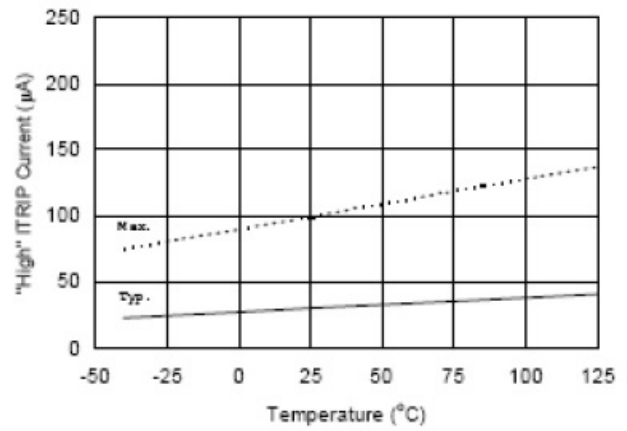


Figure 31A. "High" ITRIP Current vs. Temperature

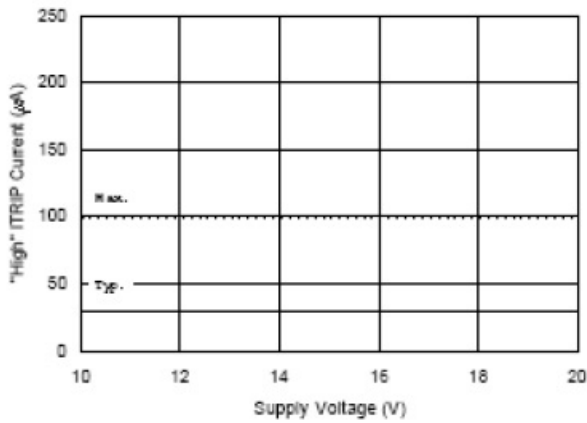


Figure 31B. "High" ITRIP Current vs. Supply Voltage

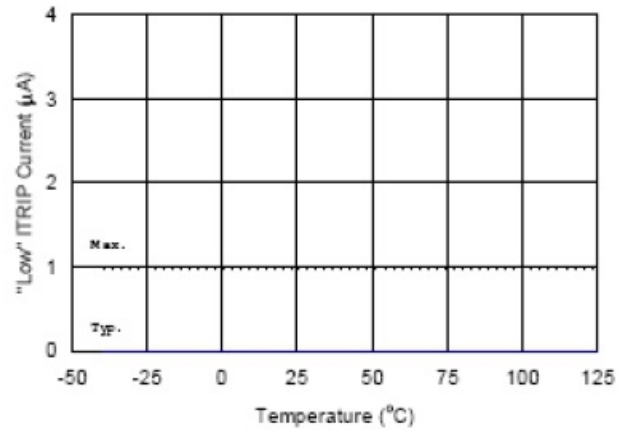


Figure 32A. "Low" ITRIP Current vs. Temperature

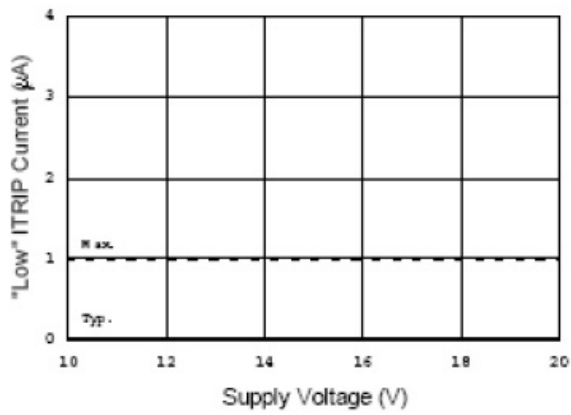


Figure 32B. "Low" ITRIP Current vs. Supply Voltage

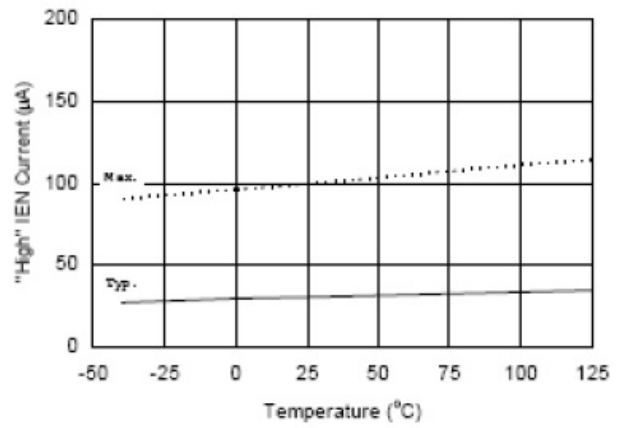


Figure 33A. "High" IEN Current vs. Temperature

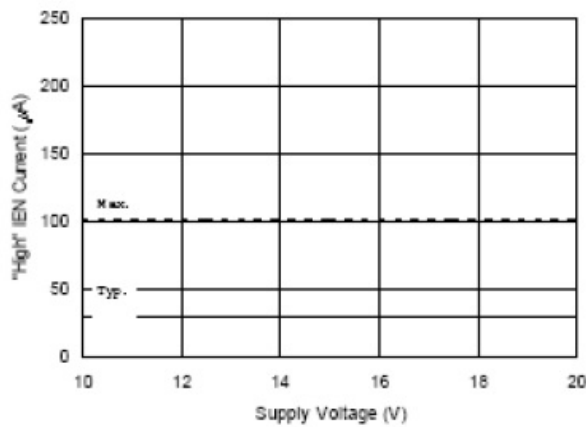


Figure 33B. "High" IEN Current vs. Supply Voltage

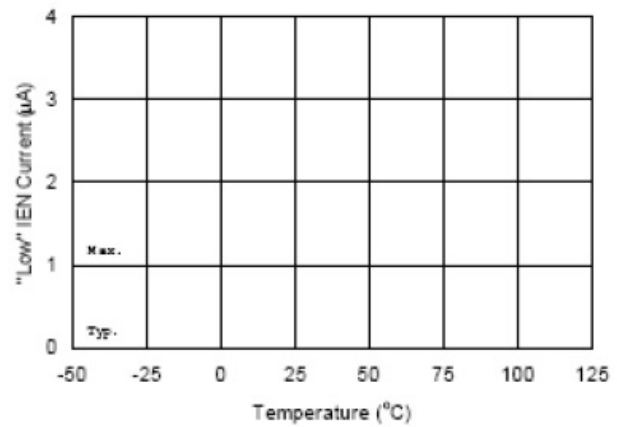


Figure 34A. "Low" IEN Current vs. Temperature

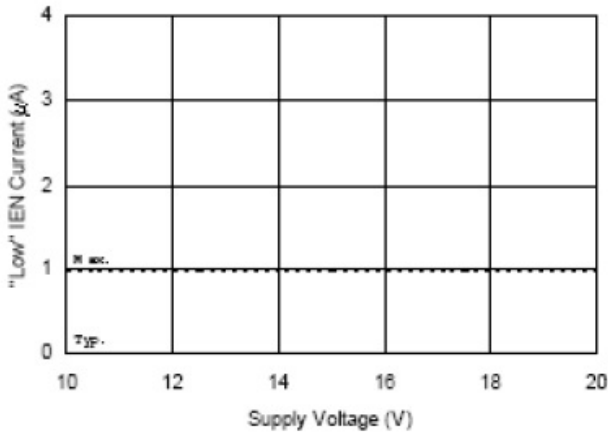


Figure 34B. "Low" IEN Current vs. Supply Voltage

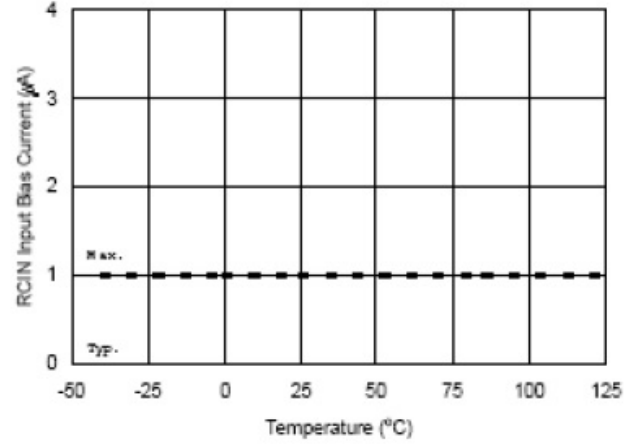


Figure 35A. RCIN Input Bias Current vs. Temperature

Figure 34B. "Low" IEN Current vs. Supply Voltage

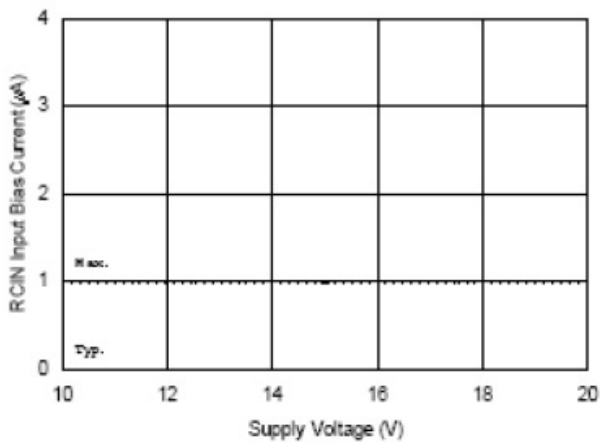


Figure 35B. RCIN Input Bias Current vs. Supply Voltage

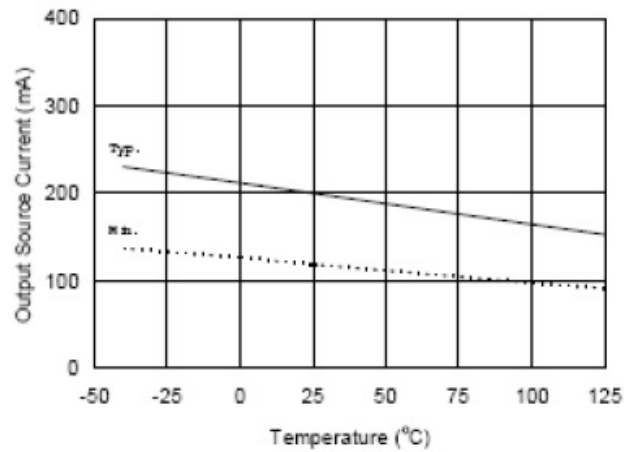
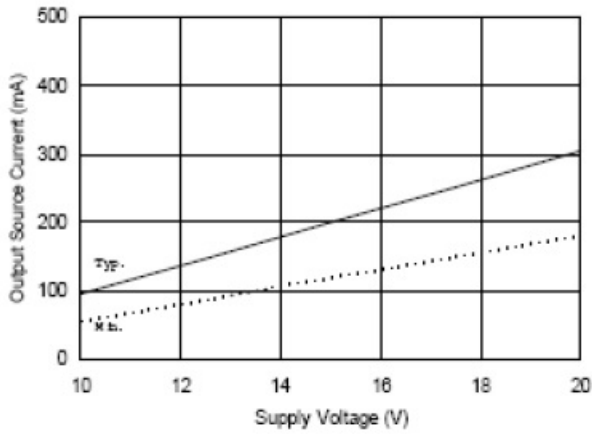
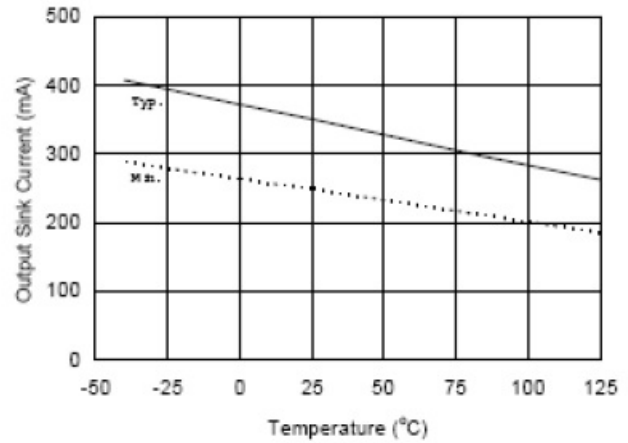


Figure 36A. Output Source Current vs. Temperature

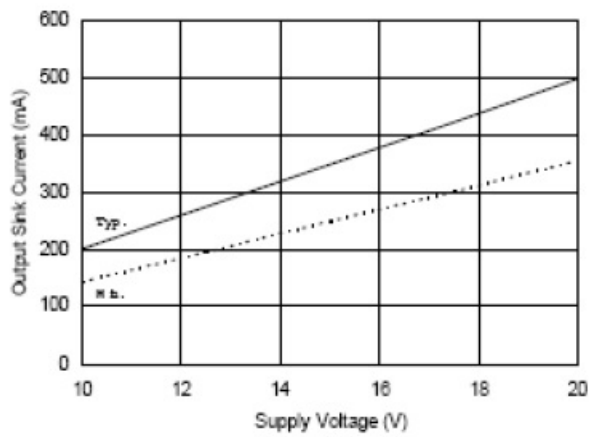




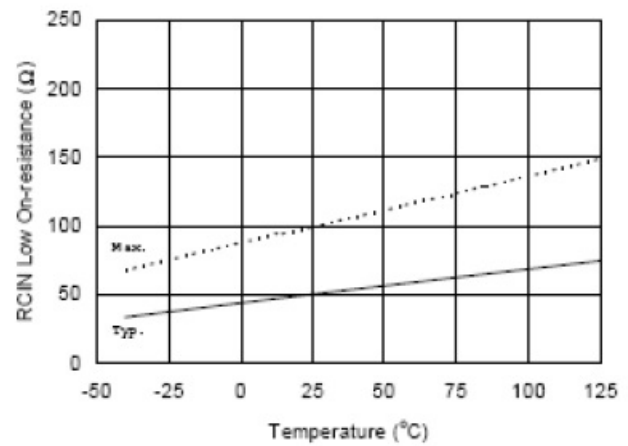
**Figure 36B. Output Source Current vs. Supply Voltage**



**Figure 37A. Output Sink Current vs. Temperature**

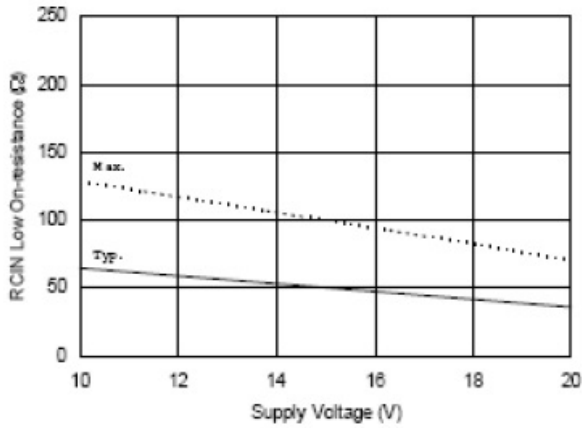


**Figure 37B. Output Sink Current vs. Supply Voltage**

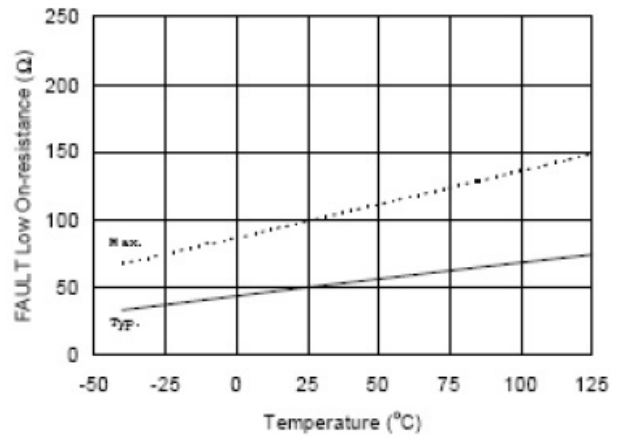


**Figure 38A. RCIN Low On-resistance vs. Temperature**

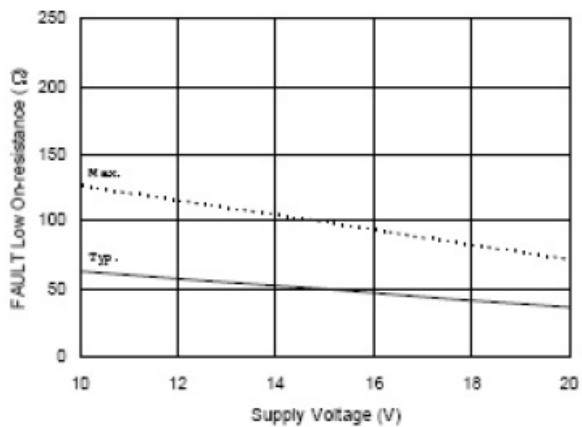




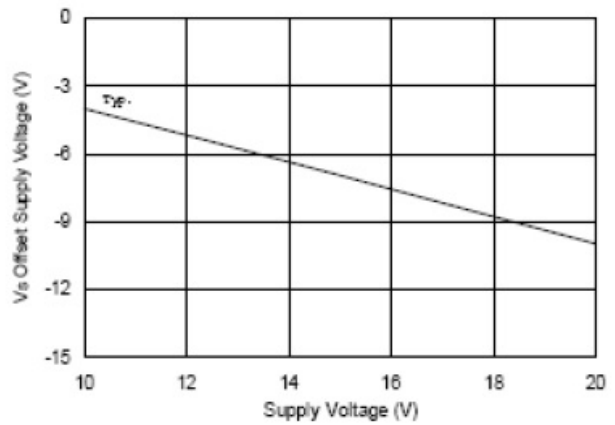
**Figure 38B. RCIN Low On-resistance vs. Supply Voltage**



**Figure 39A. FAULT Low On-resistance vs. Temperature**

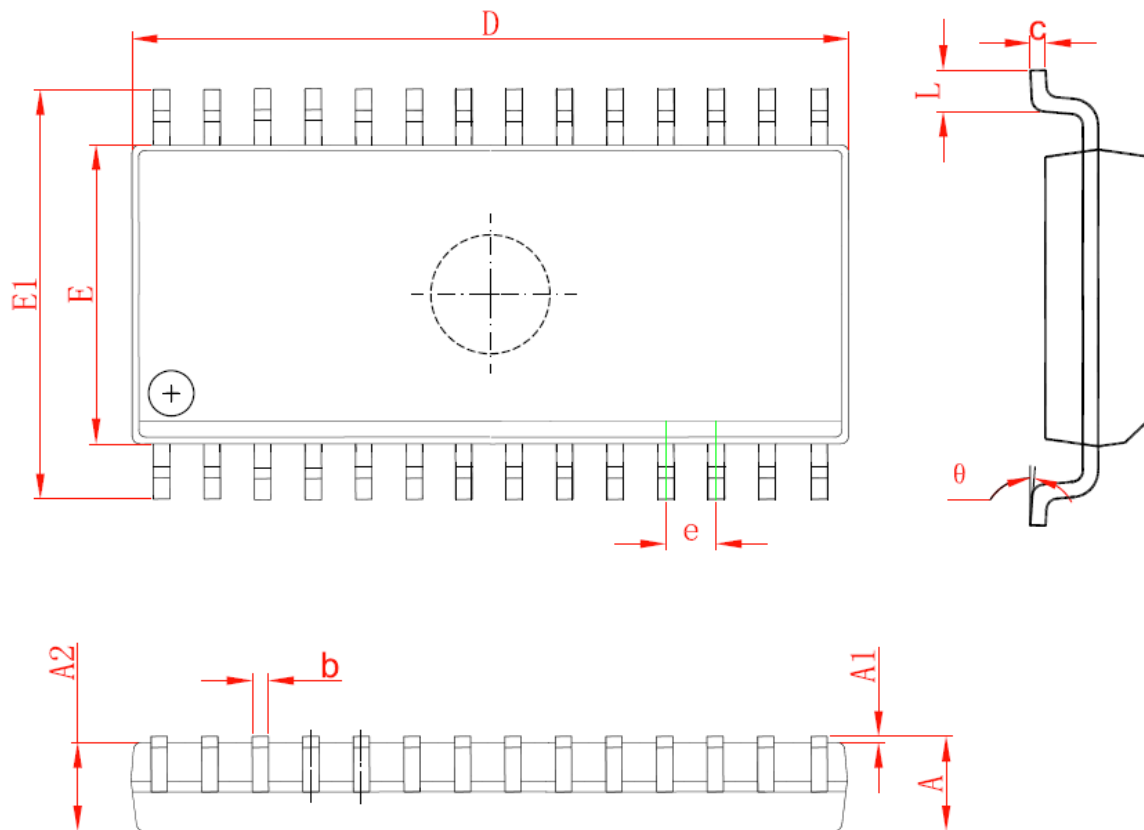


**Figure 39B. FAULT Low On-resistance vs. Supply Voltage**



**Figure 40. Maximum Vs Negative Offset vs. VBS Supply Voltage**

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**SOP28 PACKAGE OUTLINE DIMENSIONS**


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.350	2.650	0.093	0.104
A1	0.100	0.300	0.004	0.012
A2	2.290	2.500	0.09	0.098
b	0.330	0.510	0.013	0.020
c	0.204	0.330	0.008	0.013
D	17.700	18.100	0.697	0.713
E	7.400	7.700	0.291	0.303
E1	10.210	10.610	0.402	0.418
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

**Revision History**

Note: page numbers for previous revisions may differ from page numbers in current version

<b>Page or Item</b>	<b>Subjects (major changes since previous revision)</b>
<b>Rev 1.0 datasheet, 2019-8-27</b>	
Whole document	New company logo released
Page 1	Remove "Figure1" and "June 2019"
Page 6	Revise $V_{RCIN,HYS}$ parameter
<b>Rev 1.0 datasheet, 2019-11-27</b>	
Page 1	Remove a typo
Page 2	Change order information