

**600V Half-Bridge Driver**
**PRODUCT SUMMARY**

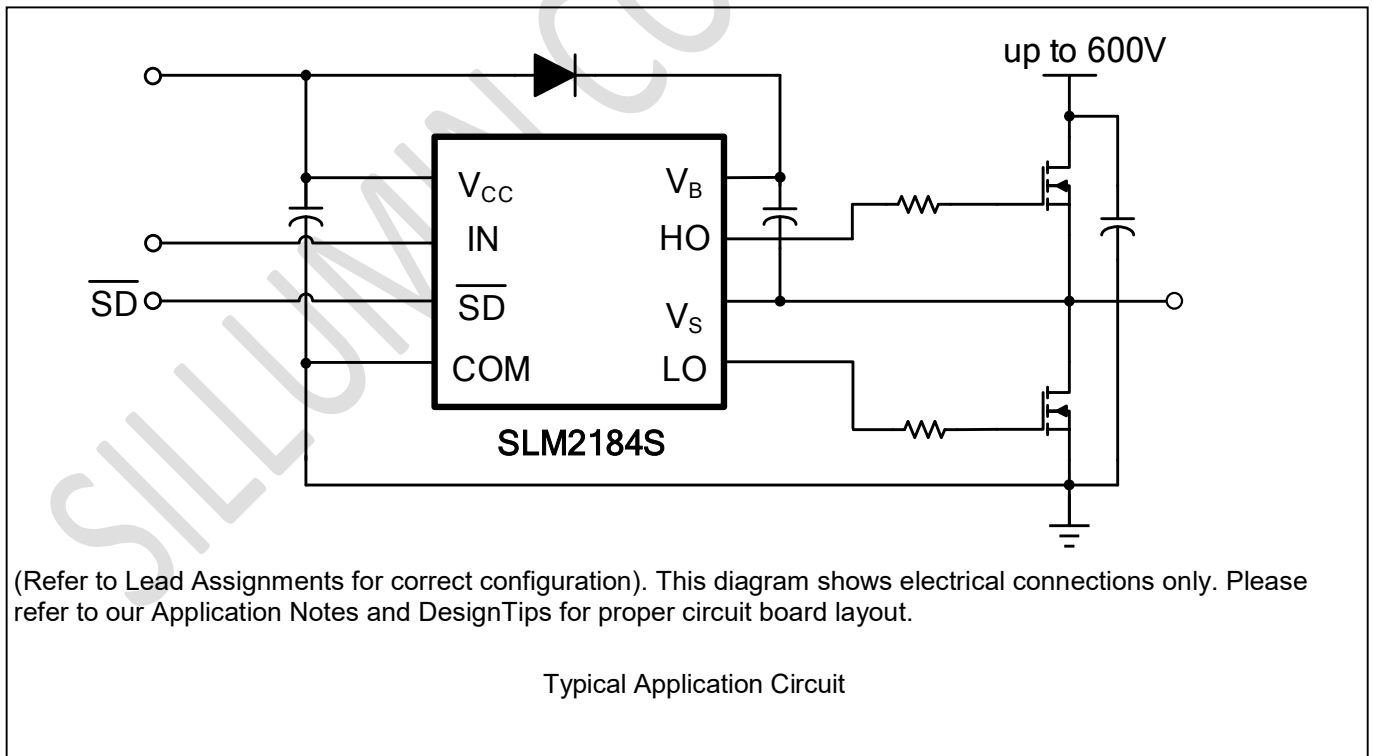
- $V_{\text{OFFSET}}$  600 V max.
- $I_{\text{O}+/-}$  1.4 A/1.8 A
- $V_{\text{OUT}}$  10 V - 20 V
- $t_{\text{on/off}}$  (typ.) 680 ns/270 ns
- **Deadtime** (typ.) 400 ns

**GENERAL DESCRIPTION**

The SLM2184S is a high voltage, high speed power MOSFET and IGBT drivers with dependent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

**FEATURES**

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout
- 3.3 V, 5 V, and 15 V logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Internal set deadtime
- Shutdown input turns off both channels
- RoHS compliant
- SOIC-8 and PDIP-8 package

**TYPICAL APPLICATION CIRCUIT**


**PIN CONFIGURATION**

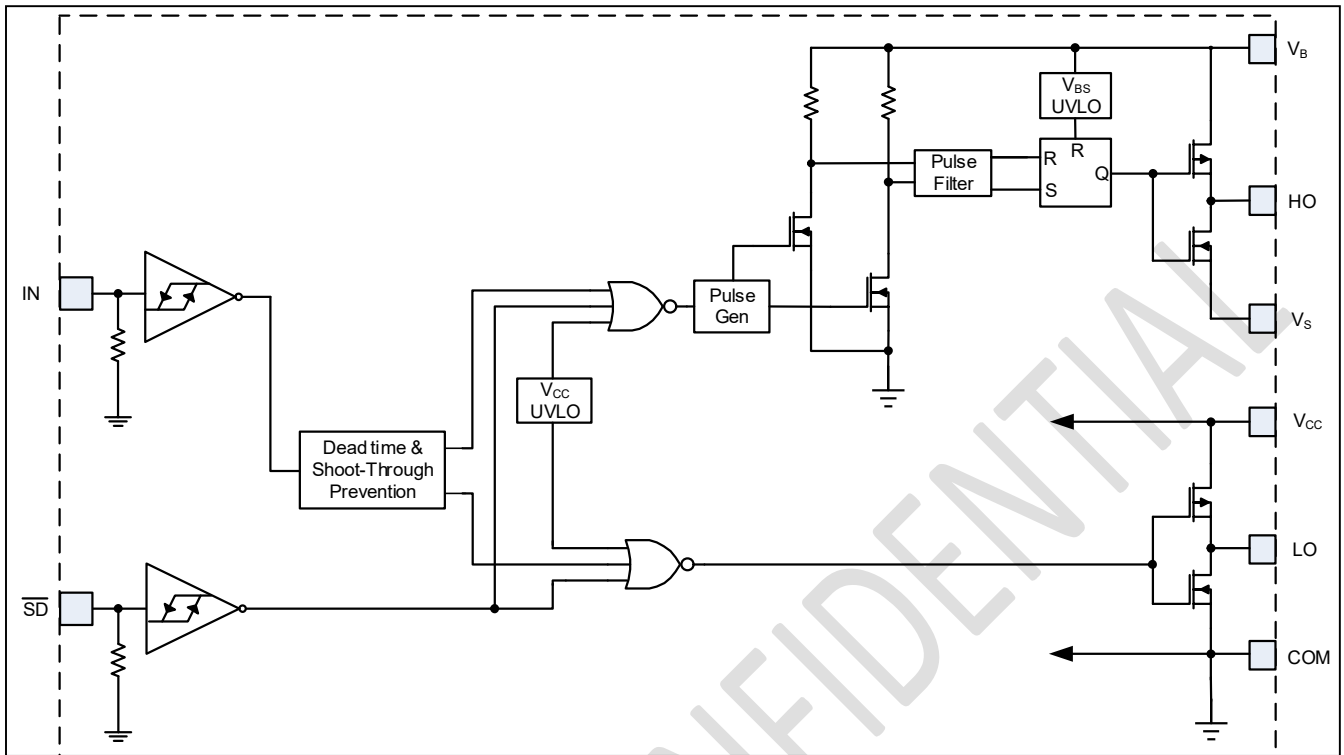
Package	Pin Configuration (Top View)
SOIC-8 and PDIP-8	<p>The diagram shows a top view of the SLM2184S package. It is an 8-pin device. The pins are numbered 1 through 8. Pin 1 is labeled IN, Pin 2 is labeled SD, Pin 3 is labeled COM, Pin 4 is labeled LO, Pin 5 is labeled V<sub>CC</sub>, Pin 6 is labeled V<sub>S</sub>, Pin 7 is labeled HO, and Pin 8 is labeled V<sub>B</sub>. The package has a notch on the top edge.</p>

**PIN DESCRIPTION**

No.	Pin	Description
1	IN	Logic input for high-side and low-side gate driver outputs (HO and LO), in phase with HO
2	$\overline{\text{SD}}$	Logic input for shutdown
3	COM	Low-side return
4	LO	Low-side gate drive output
5	V <sub>CC</sub>	Low-side and logic fixed supply
6	V <sub>S</sub>	High-side floating supply return
7	HO	High-side gate drive output
8	V <sub>B</sub>	High-side floating supply

**ORDERING INFORMATION**
**Industrial Range: -40°C to +125°C**

Order Part No.	Package	QTY
SLM2184SCA-13GTR	SOIC8, Pb-Free	2500/Reel
SLM2184SCA-GT	SOIC8, Pb-Free	100/Tube
SLM2184SDA-GT	PDIP8, Pb-Free	100/Tube

**FUNCTIONAL BLOCK DIAGRAM**


**ABSOLUTE MAXIMUM RATINGS**

Symbol	Definition	Min.	Max.	Units	
$V_B$	High-side floating absolute voltage	-0.3	625	V	
$V_S$	High-side floating supply offset voltage	$V_B - 25$	$V_B + 0.3$		
$V_{HO}$	High-side floating output voltage	$V_S - 0.3$	$V_B + 0.3$		
$V_{CC}$	Low-side and logic fixed supply voltage	-0.3	25		
$V_{LO}$	Low-side output voltage	-0.3	$V_{CC} + 0.3$		
$V_{IN}$	Logic input voltage (IN & SD)	-0.3	$V_{CC} + 0.3$		
$dV_S/dt$	Allowable offset supply voltage transient	---	50	V/ns	
$P_D$	Package power dissipation @ $T_A \leq +25^\circ\text{C}$	PDIP-8	---	1.0	W
		SOIC-8	---	0.625	
$R_{thJA}$	Thermal resistance, junction to ambient	PDIP-8	---	125	$^\circ\text{C/W}$
		SOIC-8	---	200	
$T_J$	Junction temperature	---	150	$^\circ\text{C}$	
$T_S$	Storage temperature	-55	150		
$T_L$	Lead temperature (soldering, 10 seconds)	---	300		

**Note:**

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Definition	Min.	Max.	Units
$V_B$	High-side floating absolute voltage	$V_S + 10$	$V_S + 20$	V
$V_S$	High-side floating supply offset voltage	Note 1	600	
$V_{ST}$	Transient high-side floating supply offset voltage	-40 (within 400ns)	600	
$V_{HO}$	High-side floating output voltage	$V_S$	$V_B$	
$V_{CC}$	Low-side and logic fixed supply voltage	10	20	
$V_{LO}$	Low-side output voltage	0	$V_{CC}$	
$V_{IN}$	Logic input voltage (IN & SD)	0	$V_{CC}$	
$T_A$	Ambient temperature	- 40	125	$^\circ\text{C}$

**Note:**

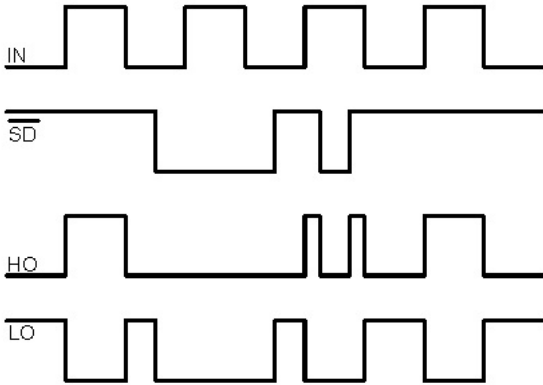
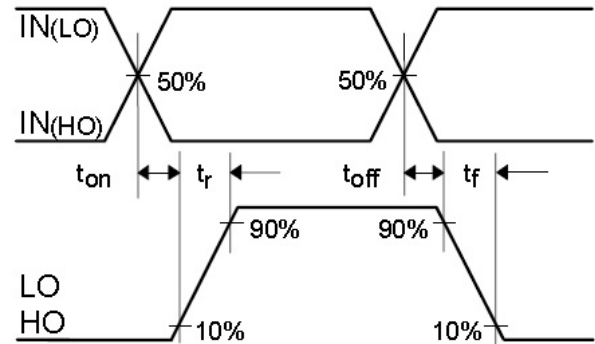
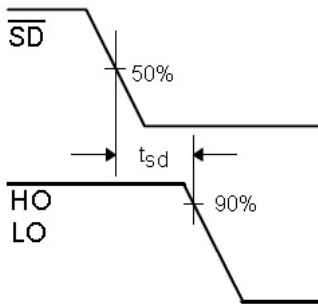
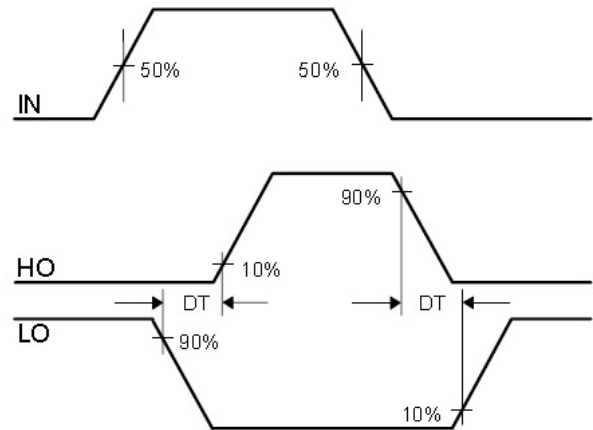
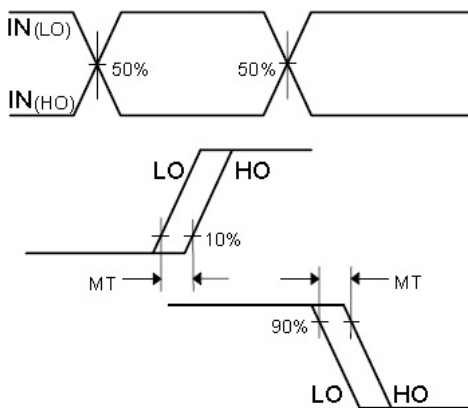
The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The  $V_S$  offset rating is tested with all supplies biased at a 15 V differential.

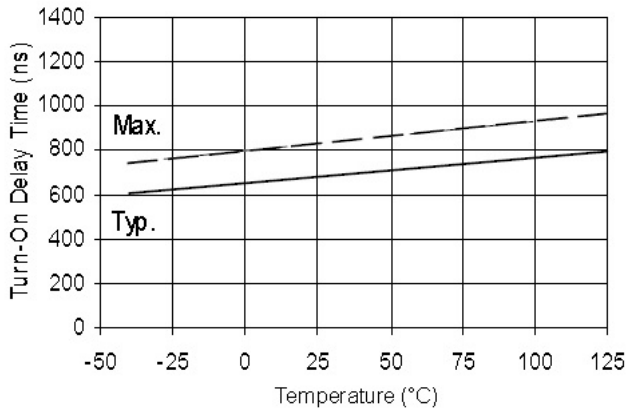
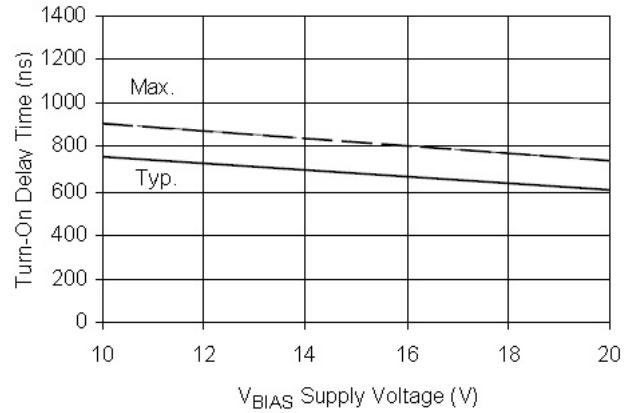
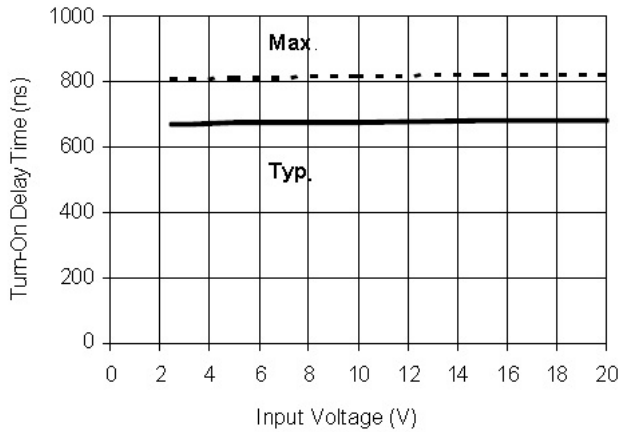
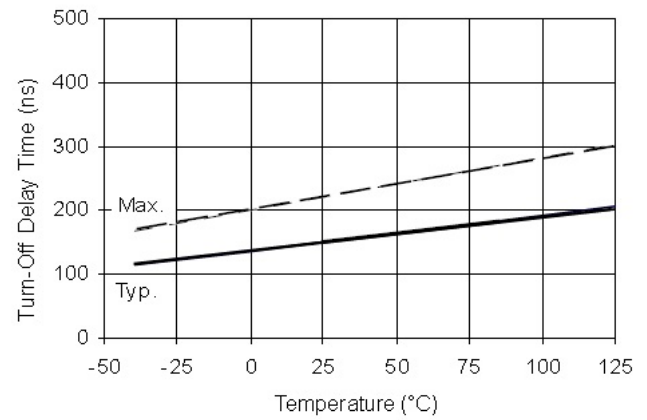
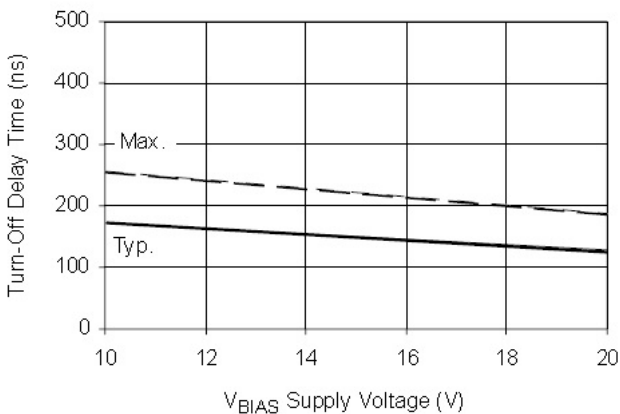
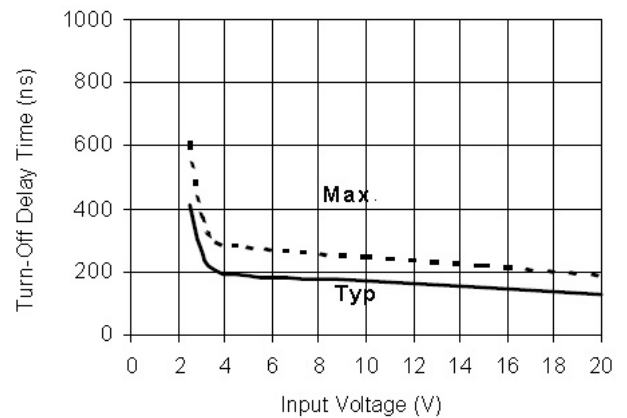
**DYNAMIC ELECTRICAL CHARACTERISTICS**
 $V_{BIAS} (V_{CC}, V_{BS}) = 15\text{ V}$ ,  $C_L = 1000\text{ pF}$  and  $T_A = 25^\circ\text{C}$  unless otherwise specified.

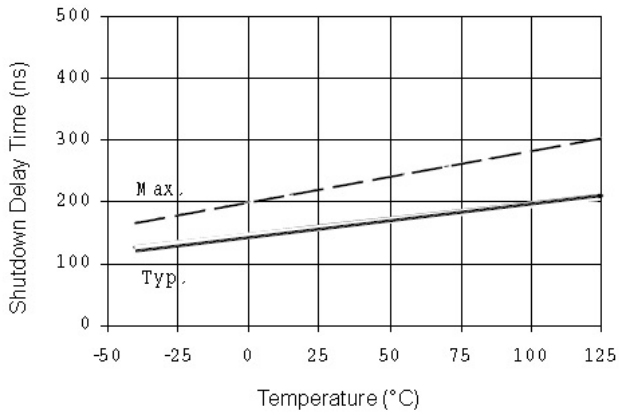
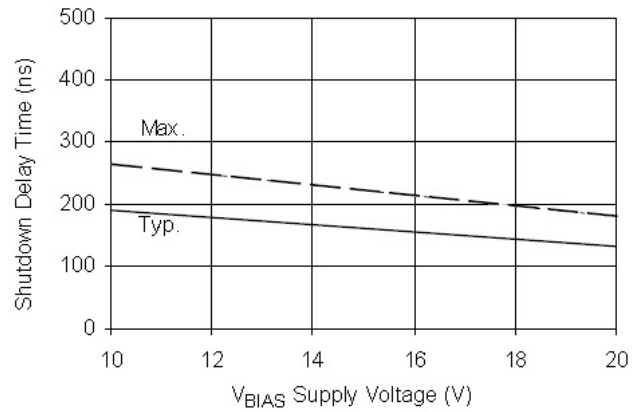
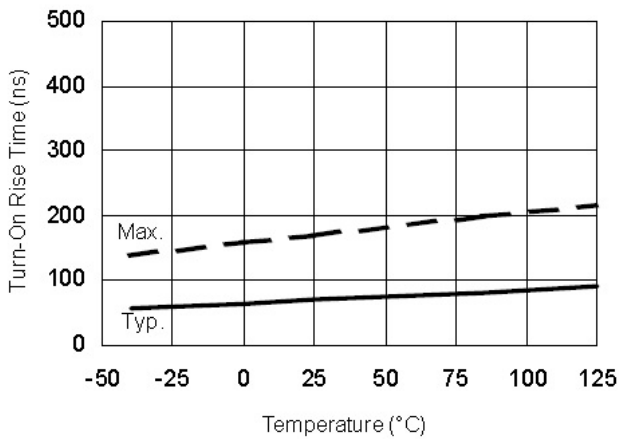
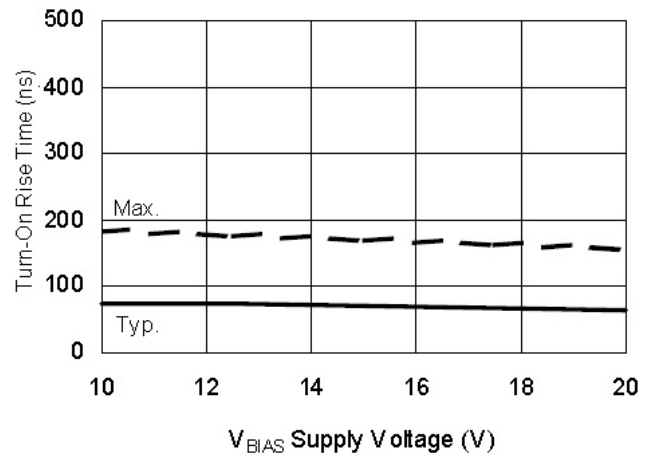
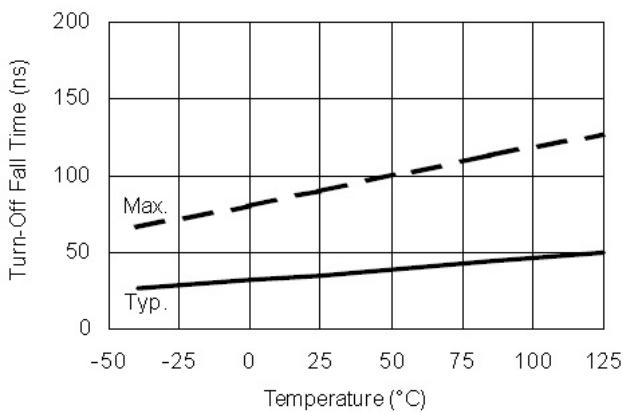
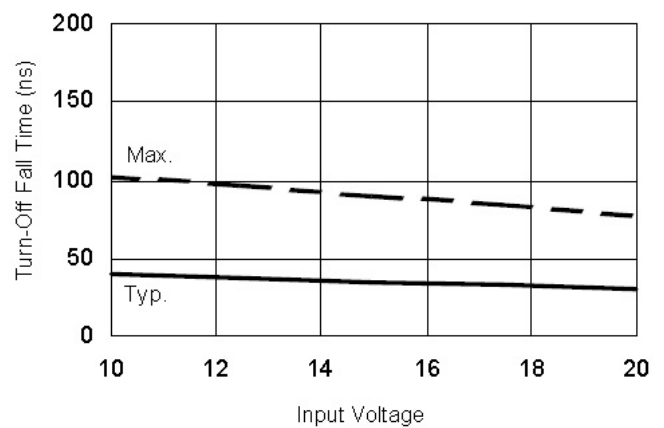
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$t_{on}$	Turn-on propagation delay	$V_S = 0\text{ V}$	---	680	820	ns
$t_{off}$	Turn-off propagation delay	$V_S = 600\text{ V}$	---	270	400	
$t_{sd}$	Shutdown propagation delay		---	160	220	
$t_r$	Turn-on rise time		---	40	80	
$t_f$	Turn-off fall time		---	20	40	
DT	Deadtime, LS turn-off to HS turn-on & HS turn-on to LS turn-off		400	520	650	
MT	Delay matching, HS & LS turn-on/off		---	---	60	

**STATIC ELECTRICAL CHARACTERISTICS**
 $V_{BIAS} (V_{CC}, V_{BS}) = 15\text{ V}$  and  $T_A = 25^\circ\text{C}$  unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$ , and  $I_{IN}$  parameters are referenced to COM. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

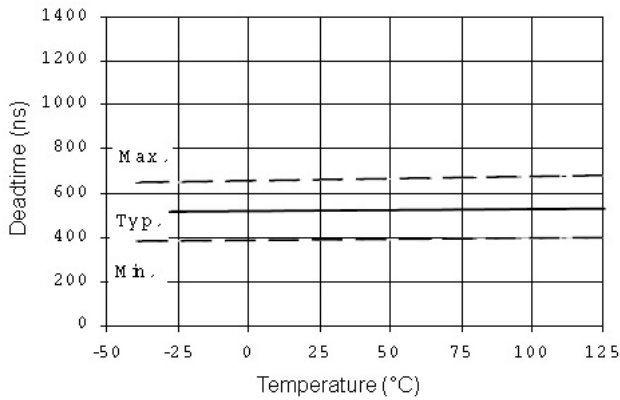
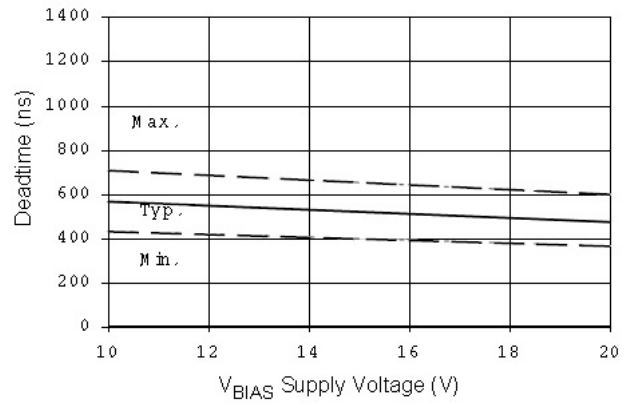
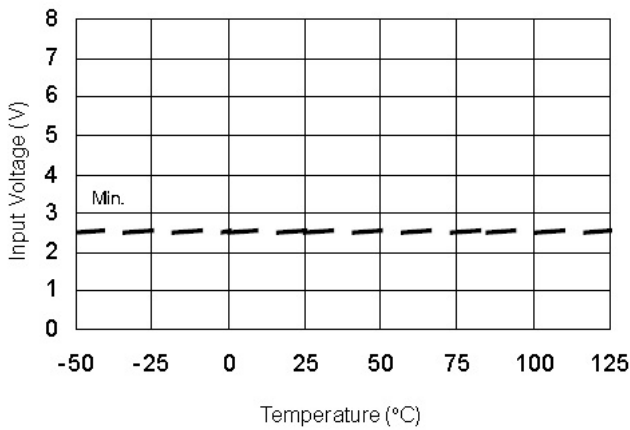
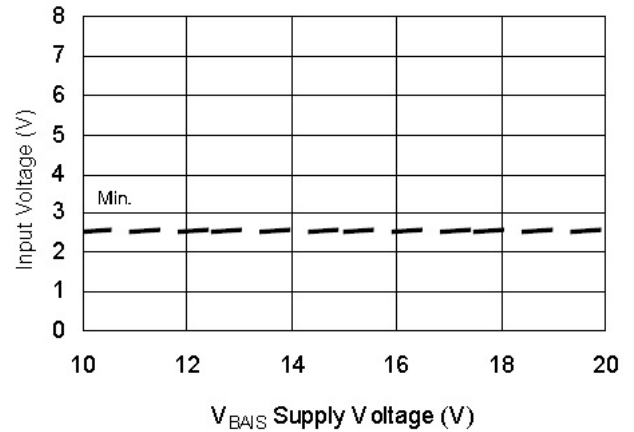
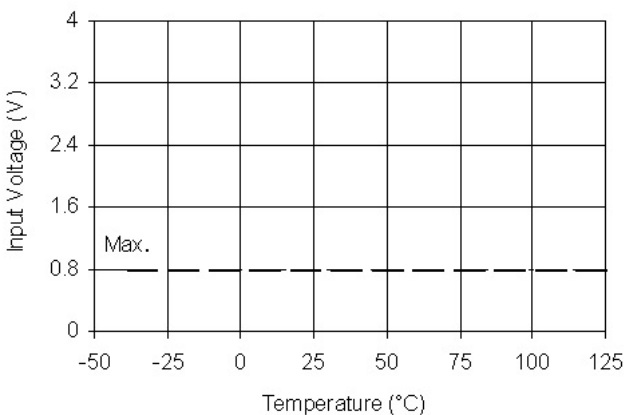
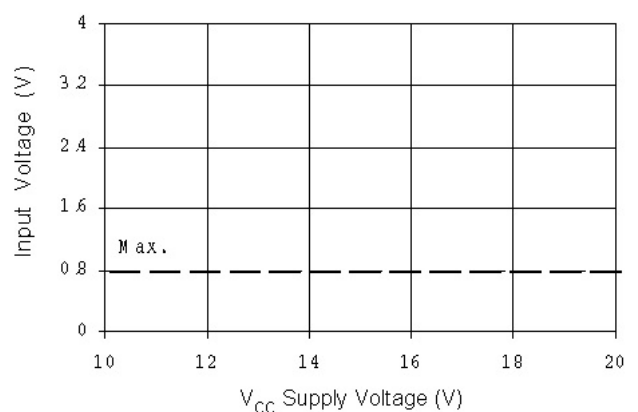
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{IH}$	Logic "1" input voltage	$V_{CC} = 10\text{ V to }20\text{ V}$	2.5	---	---	V
$V_{IL}$	Logic "0" input voltage		---	---	0.8	
VSD, TH+	SD input positive going threshold		2.5	---	---	
VSD, TH-	SD input negative going threshold		---	---	0.8	
$V_{OH}$	High level output voltage, $V_{BIAS} - V_O$	$I_O = 2\text{ mA}$	---	0.05	0.2	
$V_{OL}$	Low level output voltage, $V_O$		---	0.02	0.1	
$I_{LK}$	Offset supply leakage current	$V_B = V_S = 600\text{ V}$	---	---	50	$\mu\text{A}$
$I_{QBS}$	Quiescent $V_{BS}$ supply current	$V_{IN} = 0\text{ V or }5\text{ V}$	---	60	75	
$I_{QCC}$	Quiescent $V_{CC}$ supply current		---	170	270	
$I_{IN+}$	Logic "1" input bias current	$V_{IN} = 5\text{ V}$	---	3	10	
$I_{IN-}$	Logic "0" input bias current	$V_{IN} = 0\text{ V}$	---	---	5	
$V_{CCUV+}$ $V_{BSUV+}$	$V_{CC}$ & $V_{BS}$ supply undervoltage positive going threshold		8	8.9	9.8	V
$V_{CCUV-}$ $V_{BSUV-}$	$V_{CC}$ & $V_{BS}$ supply undervoltage negative going threshold		7.4	8.2	9	
$I_{O+}$	Output high short circuit pulsed current	$V_O = 0\text{ V}$ , $V_{IN} = V_{IH}$ $PW \leq 10\text{ }\mu\text{s}$	1.4	1.9		A
$I_{O-}$	Output low short circuit pulsed current	$V_O = 15\text{ V}$ , $V_{IN} = V_{IL}$ $PW \leq 10\text{ }\mu\text{s}$	1.8	2.3		

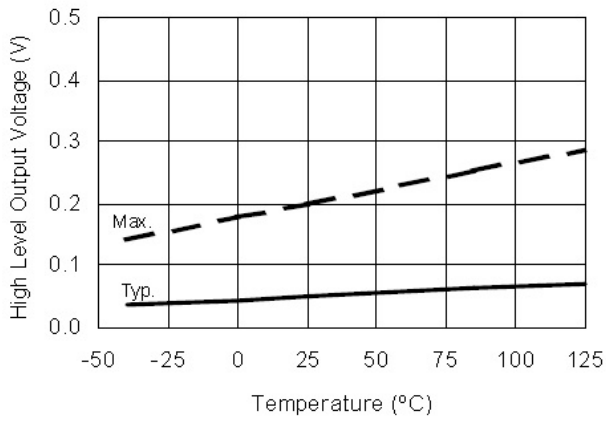

**Figure 1. Input/Output Timing Diagram**

**Figure 2. Switching Time Waveform Definitions**

**Figure 3. Shutdown Waveform Definitions**

**Figure 4. Deadtime Waveform Definitions**

**Figure 5. Delay Matching Waveform Definitions**


**Figure 6A. Turn-On Time vs. Temperature**

**Figure 6B. Turn-On Time vs. Supply Voltage**

**Figure 6C. Turn-On Time vs. Input Voltage**

**Figure 7A. Turn-Off Time vs. Temperature**

**Figure 7B. Turn-Off Time vs. Supply Voltage**

**Figure 7C. Turn-Off Time vs. Input Voltage**

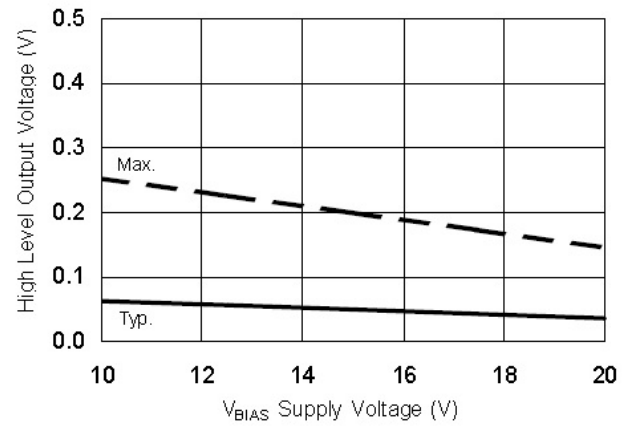

**Figure 8A. Shutdown Time vs. Temperature**

**Figure 8B. Shutdown Time vs. Voltage**

**Figure 9A. Turn-On Rise Time vs. Temperature**

**Figure 9B. Turn-On Rise Time vs. Voltage**

**Figure 10A. Turn-Off Fall Time vs. Temperature**

**Figure 10B. Turn-Off Fall Time vs. Input Voltage**



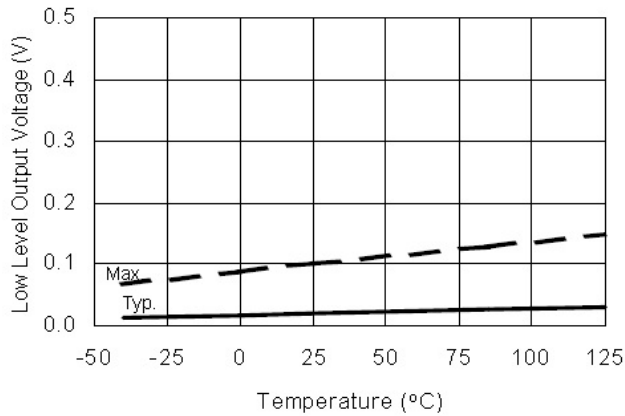

**Figure 11A. Deadtime vs. Temperature**

**Figure 11B. Deadtime vs. Voltage**

**Figure 12A. Logic "1" Input Voltage vs. Temperature**

**Figure 12B. Logic "1" Input Voltage vs. Supply Voltage**

**Figure 13A. Logic "0" (HO) & Logic "1" (LO) & Active SD Input Voltage vs. Temperature**

**Figure 13B. Logic "0" (HO) & Logic "1" (LO) & Active SD Input Voltage vs. Voltage**



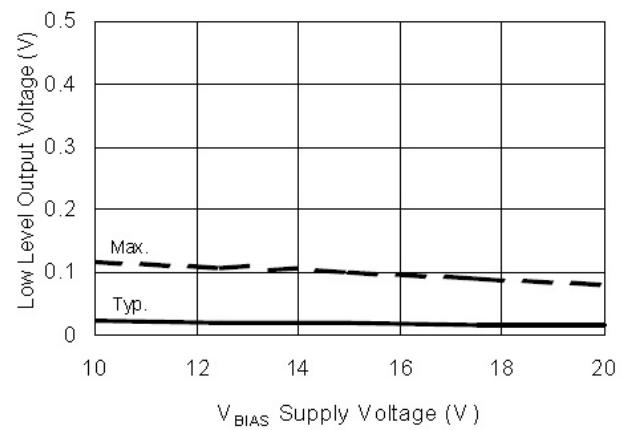
**Figure 14A. High Level Output Voltage vs. Temperature**



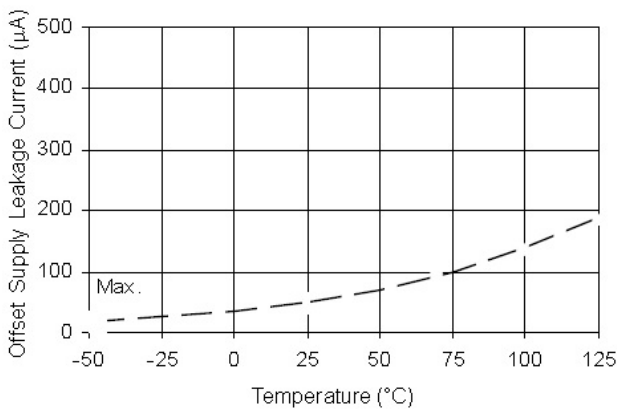
**Figure 14B. High Level Output Voltage vs. Supply Voltage**



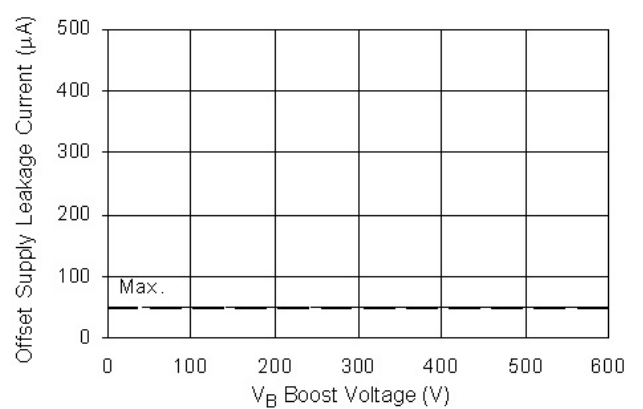
**Figure 15A. Low Level Output Voltage vs. Temperature**



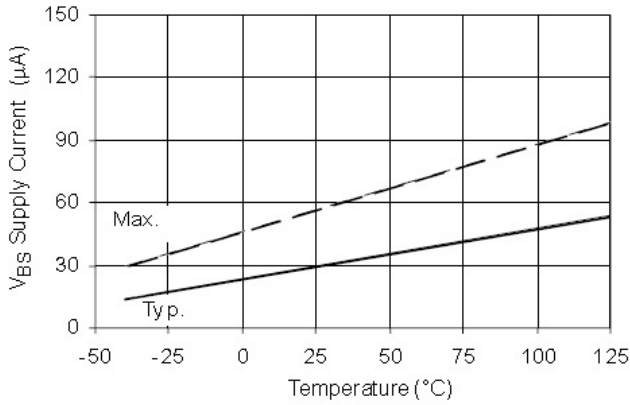
**Figure 15B. Low Level Output Voltage vs. Supply Voltage**



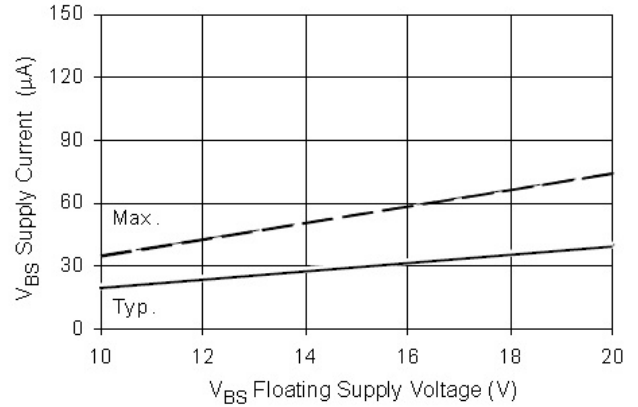
**Figure 16A. Offset Supply Current vs. Temperature**



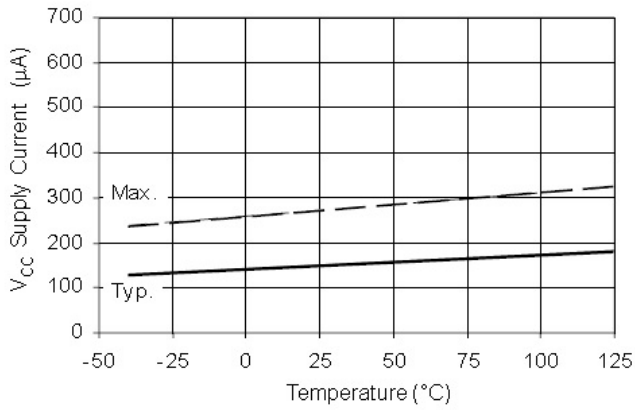
**Figure 16B. Offset Supply Current vs. Voltage**



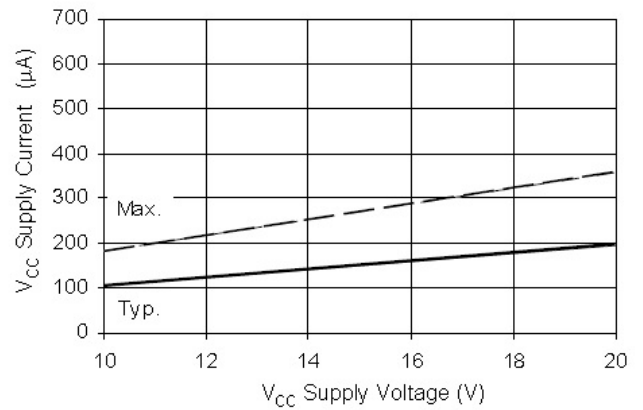
**Figure 17A. V<sub>BS</sub> Supply Current vs. Temperature**



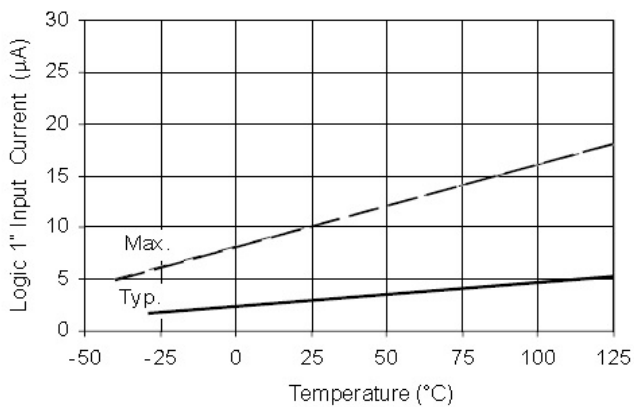
**Figure 17B. V<sub>BS</sub> Supply Current vs. Voltage**



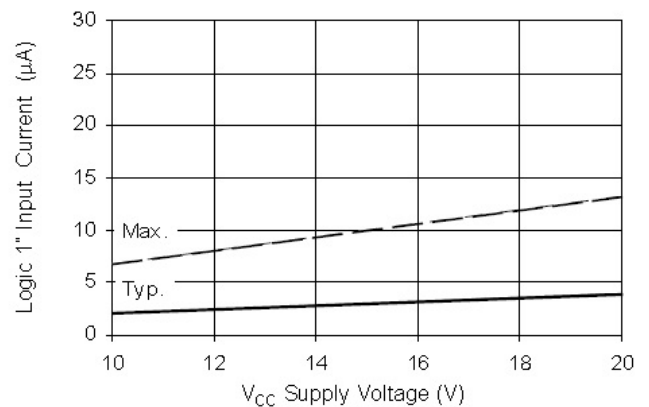
**Figure 18A. V<sub>CC</sub> Supply Current vs. Temperature**



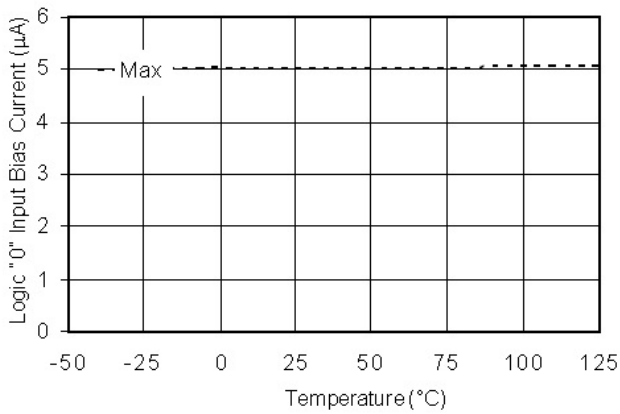
**Figure 18B. V<sub>CC</sub> Supply Current vs. Voltage**



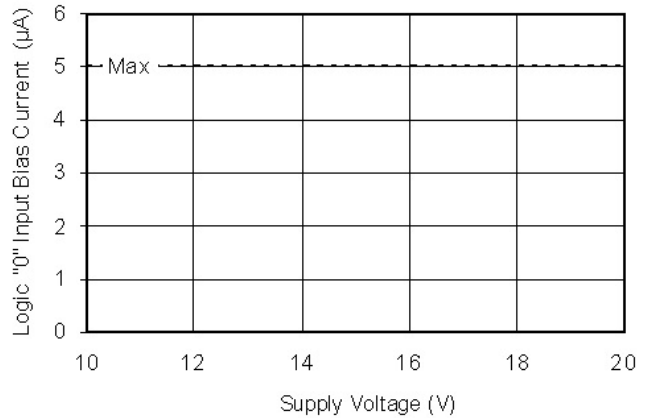
**Figure 19A. Logic "1" Input Current vs. Temperature**



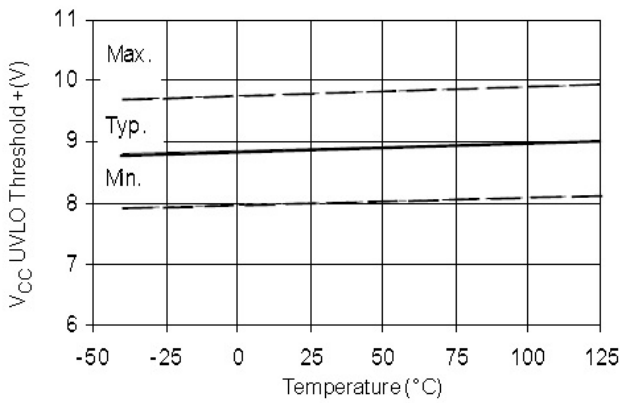
**Figure 19B. Logic "1" Input Current vs. Voltage**



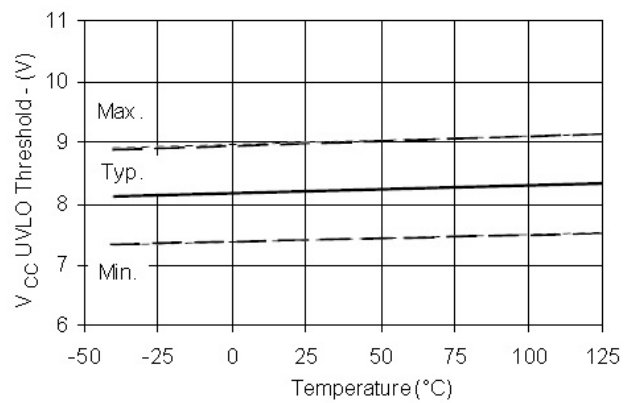
**Figure 20A. Logic "0" Input Bias Current vs. Temperature**



**Figure 20B. Logic "0" Input Bias Current vs. Voltage**

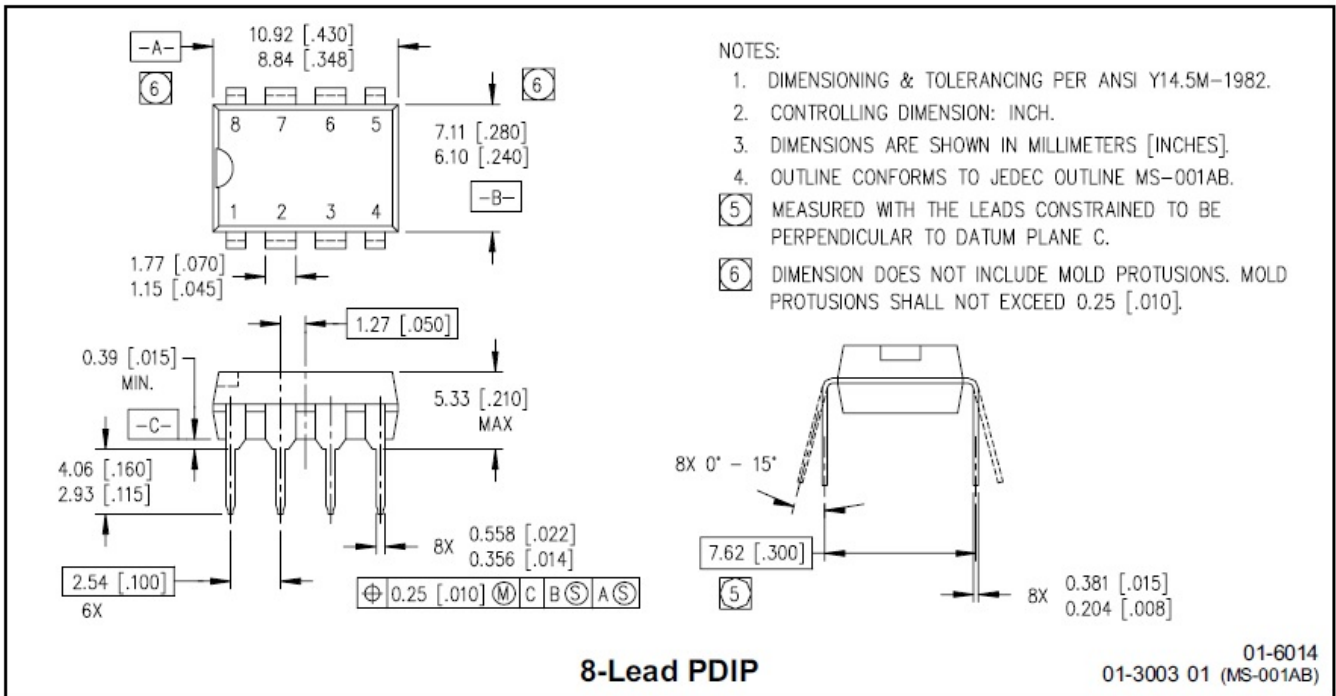


**Figure 21A. V<sub>CC</sub> Undervoltage Threshold(+) vs. Temperature**

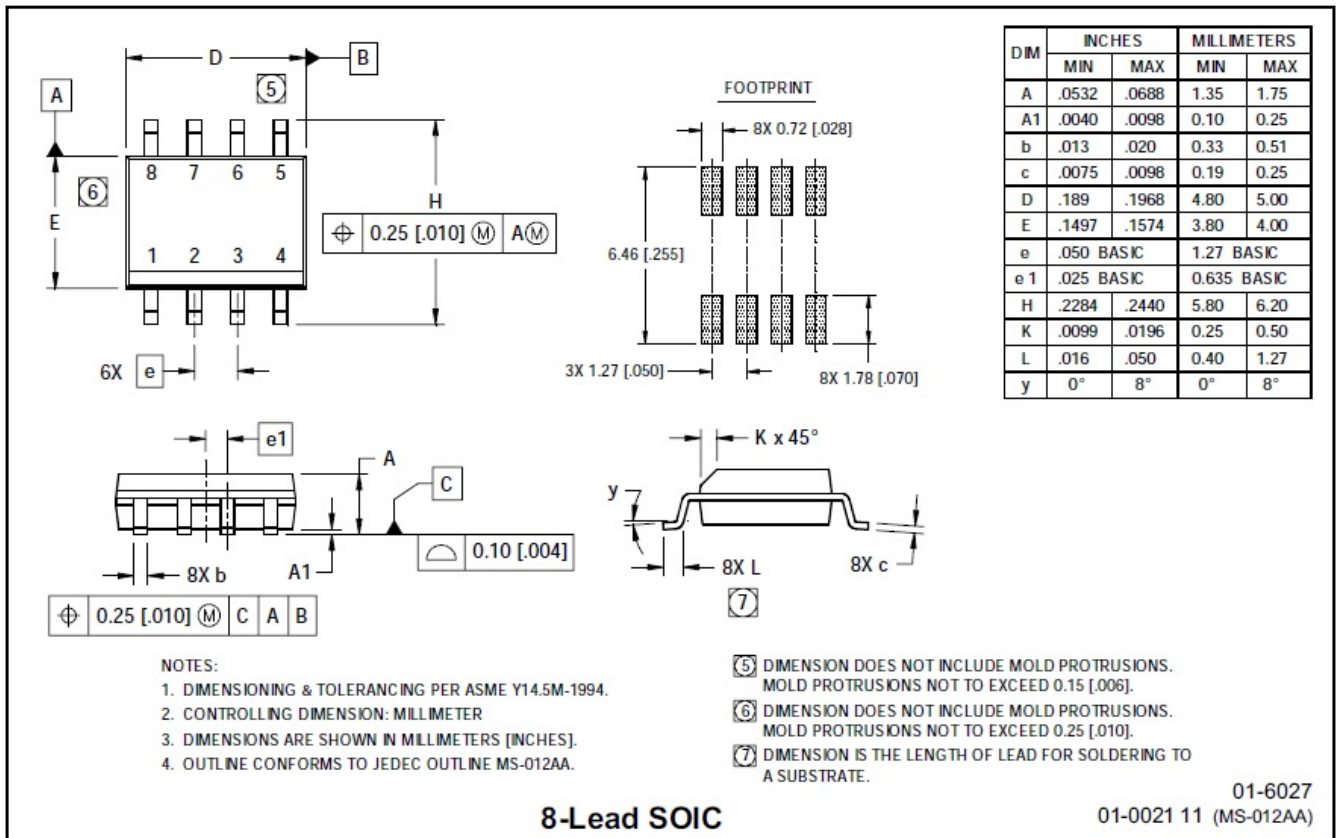


**Figure 21B. V<sub>CC</sub> Undervoltage Threshold(-) vs. Temperature**

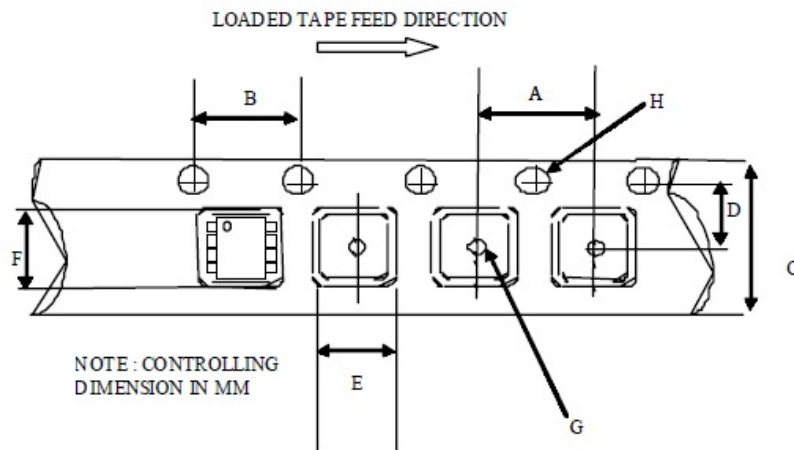
## PACKAGE CASE OUTLINES



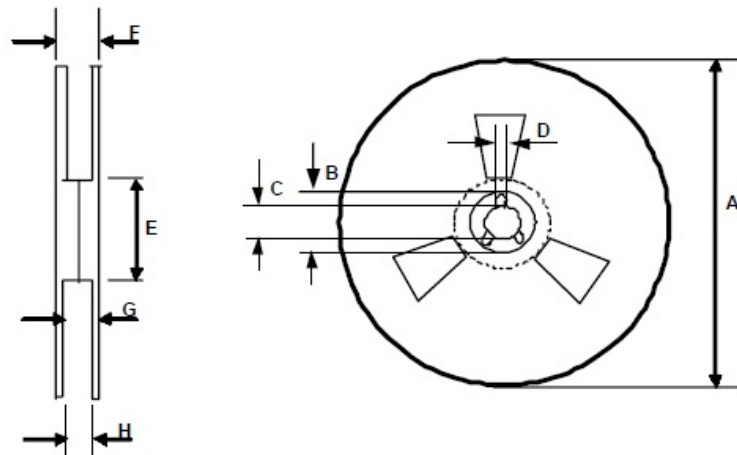
**8-Lead PDIP**



**8-Lead SOIC**

**Tape & Reel  
8-lead SOIC**

**CARRIER TAPE DIMENSION FOR 8SOICN**

Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062


**REEL DIMENSIONS FOR 8SOICN**

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

**Revision History**

Note: page numbers for previous revisions may differ from page numbers in current version

<b>Page or Item</b>	<b>Subjects (major changes since previous revision)</b>
<b>Rev 1.0 datasheet, 2019-8-27</b>	
Whole document	New company logo released
Page 1	Remove "Figure 1." and "June 2019"