Dual Channel 4A, 5.0kV$_{RMS}$ Isolated Gate Driver

GENERAL DESCRIPTION

The SLMi8233/4/5H-AQ isolated driver family is an isolated dual channel gate driver with different configurations. The SLMi8233/4H-AQ are configured as high-side/low-side drivers, while the SLMi8235H-AQ are configured as dual drivers. The peak source output current of SLMi8233/4/5H-AQ is 4.0A. Programmable dead time (DT) feature is available in SLMi8233/4H-AQ. Pulling low the EN pin shuts down both outputs simultaneously, and allows for normal operation when the EN pin is pulled high. As a fail-safe measure, primary-side logic failures force both outputs low.

The VDDA and VDDB supply voltage are up to 40 V. A wide input VDDI range from 3 V to 18 V makes the driver suitable for interfacing with both analog and digital controllers. All the supply voltage pins have under voltage lock-out (UVLO) protection.

The SLMi8233/4/5H-AQ has 5.0kV$_{RMS}$ isolation in SOP16W and SOP14W package per UL1577.

High CMTI, low propagation delay, small size and flexible configuration make the SLMi8233/4/5H-AQ family is suitable for a wide range of isolated MOSFET/IGBT and SiC or GaN FET gate drive applications.

FEATURE

- AEC-Q100 qualified for automotive application
  - Temperature grade 1: –40°C to +125°C, T_A
- 4.0A peak source current
- 40ns (Typ.) propagation delay
- 100kV/us (Min.) common mode transient immunity (CMTI)
- Wide input voltage: 3V to 18V
- Up to 40V driver output voltage
- 5V reverse polarity voltage handling capability on input stage
- 1500V functional isolation between two drivers
- Safety certifications (Planned):
  - 5kVRMS isolation for 1 minute per UL 1577 with SOP16W, SOP14W package
  - CQC certification per GB4943.1-2011
  - DIN VDE 0884-17: 2021-10

APPLICATION

- AC/DC or DC/DC power supplies in server, telecom and industry
- DC/AC solar inverters
- EV battery charging

APPLICATION CIRCUIT

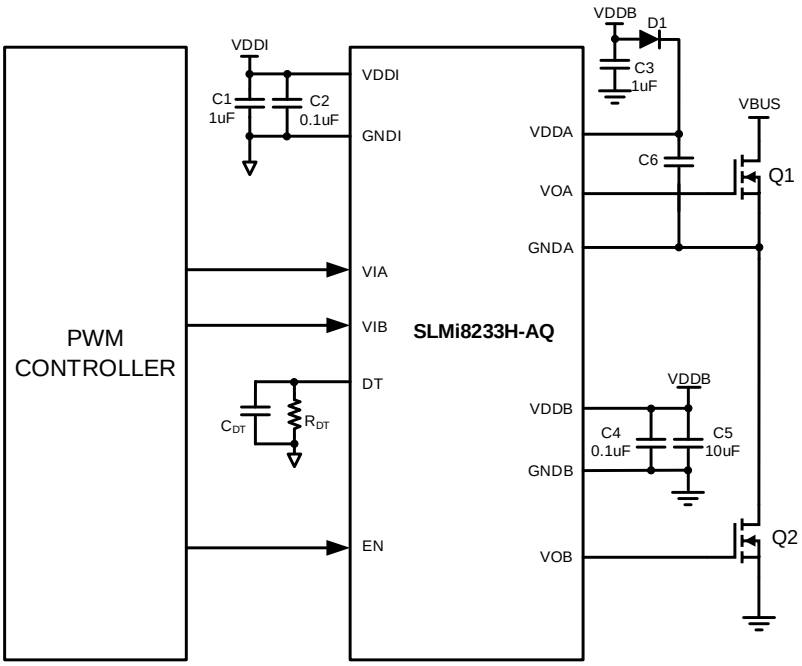


Figure 1. SLMi8233H-AQ Application Circuit

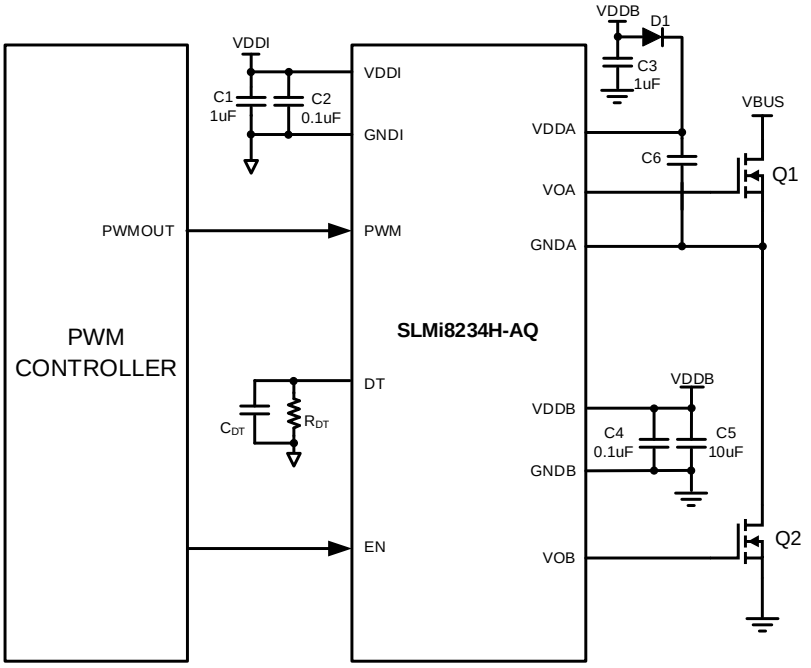


Figure 2. SLMi8234H-AQ Application Circuit

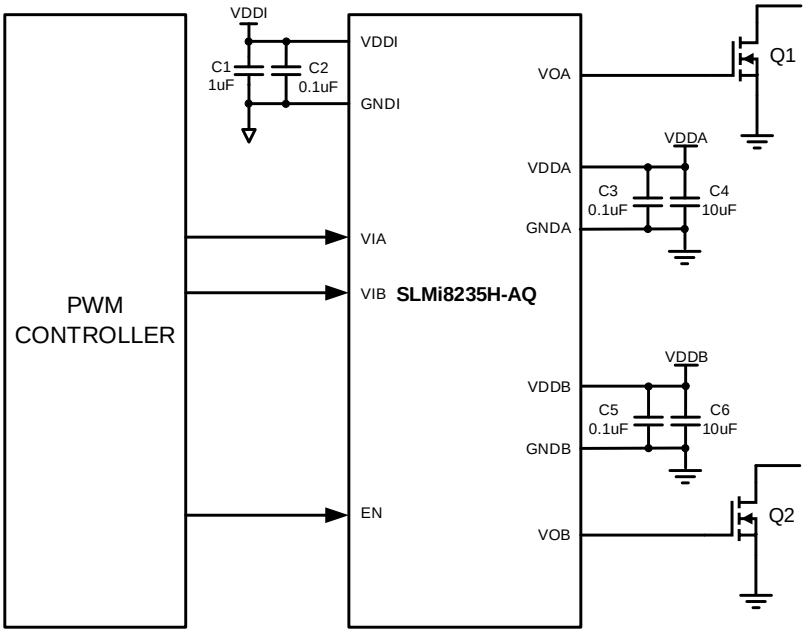
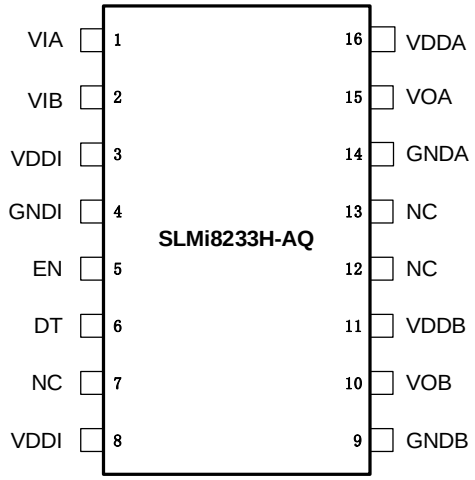
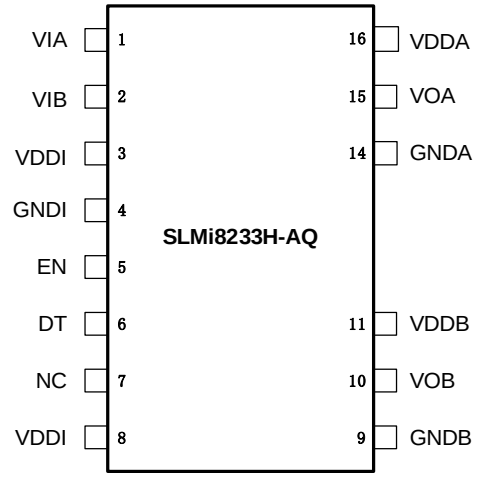
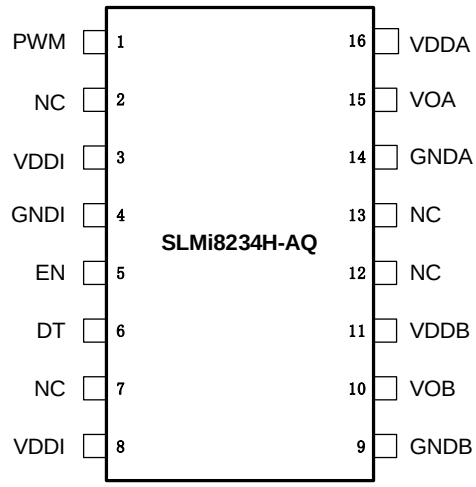
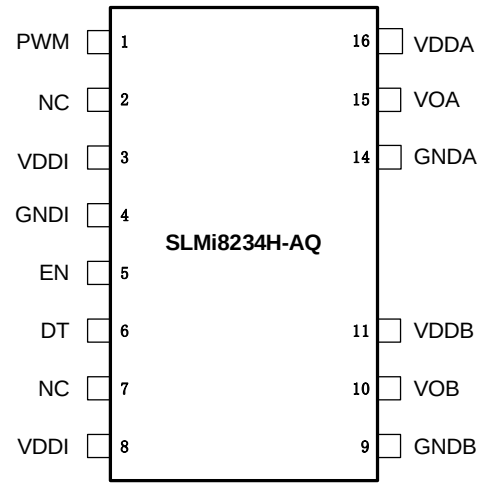
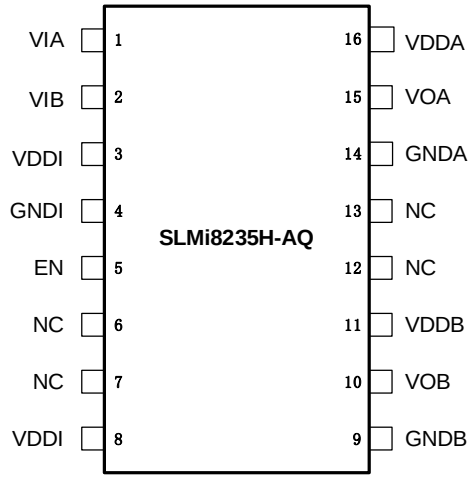
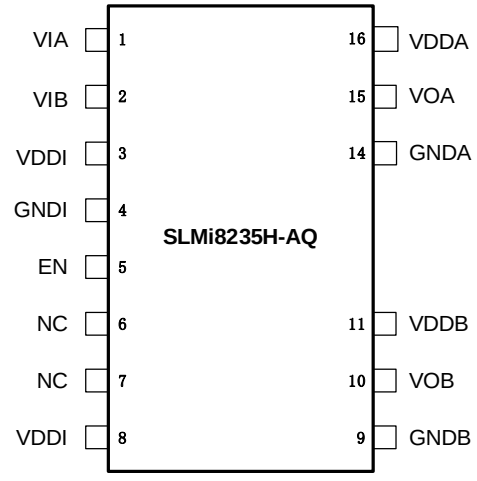


Figure 3. SLMi8235H-AQ Application Circuit

Table of Contents

PIN CONFIGURATION

Part Number	Pin Configuration (Top View)	
	SOP16W	SOP14W
SLMi8233H-AQ		
SLMi8234H-AQ		
SLMi8235H-AQ		

PIN DESCRIPTION

Table 1. SLMi8233H-AQ Pin Description

No.	Pin	Description
1	VIA	Input of driver A. The output of driver A is in phase with the input. This pin is pulled low internally if left open. Recommend to connect this pin to ground if not used for better noise immunity.
2	VIB	Input of driver B. The output of driver B is in phase with the input. This pin is pulled low internally if left open. Recommend to connect this pin to ground if not used for better noise immunity.
3	VDDI	Input power supply. A local low ESR and ESL capacitor should be connected between VDDI and GNDI.
4	GNDI	Input power ground.
5	EN	Device enable input. When EN pin is low, both driver is disabled and driver output is low. When EN pin is high, it allows the device to perform in normal operation.
6	DT	Dead time programming input. Connect a resistor between DT and GNDI to program the dead time. A bypassing capacitor, 2.2nF or greater, is recommended to be put between DT and GNDI to achieve better noise immunity.
7	NC	No connection
8	VDDI	Input power supply. This pin is internally connected to pin3.
9	GNDB	Power ground of driver B.
10	VOB	Output of driver B.
11	VDDB	Power supply of driver B. A local low ESR and ESL capacitor should be connected between VDDB and GNDB.
12	NC	No connection. Pin12 is removed in SOP14W
13	NC	No connection. Pin13 is removed in SOP14W
14	GNDA	Power ground of driver A.
15	VOA	Output of driver A.
16	VDDA	Power supply of driver A. A local low ESR and ESL capacitor should be connected between VDDA and GNDA.

Table 2. SLMi8234H-AQ Pin Description

No.	Pin	Description
1	PWM	PWM input. The output of driver A is in phase with PWM input and the output of driver B is out of phase with PWM input.
2	NC	No connection
3	VDDI	Input power supply. A local low ESR and ESL capacitor should be connected between VDDI and GNDI.
4	GNDI	Input power ground.
5	EN	Device enable input. When EN pin is low, both driver is disabled and driver output is low. When EN pin is high, it allows the device to perform in normal operation.
6	DT	Dead time programming input. Connect a resistor between DT and GNDI to program the dead time. A bypassing capacitor, 2.2nF or greater, is recommended to be put between DT and GNDI to achieve better noise immunity.
7	NC	No connection

No.	Pin	Description
8	VDDI	Input power supply. This pin is internally connected to pin3.
9	GNDB	Power ground of driver B.
10	VOB	Output of driver B.
11	VDDB	Power supply of driver B. A local low ESR and ESL capacitor should be connected between VDDB and GNDB.
12	NC	No connection. Pin12 is removed in SOP14W
13	NC	No connection. Pin13 is removed in SOP14W
14	GNDA	Power ground of driver A.
15	VOA	Output of driver A.
16	VDDA	Power supply of driver A. A local low ESR and ESL capacitor should be connected between VDDA and GNDA.

Table 3. SLMi8235H-AQ Pin Description

No.	Pin	Description
1	VIA	Input of driver A. The output of driver A is in phase with the input. This pin is pulled low internally if left open. Recommend to connect this pin to ground if not used for better noise immunity.
2	VIB	Input of driver B. The output of driver B is in phase with the input. This pin is pulled low internally if left open. Recommend to connect this pin to ground if not used for better noise immunity.
3	VDDI	Input power supply. A local low ESR and ESL capacitor should be connected between VDDI and GNDI.
4	GNDI	Input power ground.
5	EN	Device enable input. When EN pin is low, both driver is disabled and driver output is low. When EN pin is high, it allows the device to perform in normal operation.
6	NC	No connection. Pin12 is removed in SOP14W
7	NC	No connection. Pin13 is removed in SOP14W
8	VDDI	Input power supply. This pin is internally connected to pin3.
9	GNDB	Power ground of driver B.
10	VOB	Output of driver B.
11	VDDB	Power supply of driver B. A local low ESR and ESL capacitor should be connected between VDDB and GNDB.
12	NC	No connection
13	NC	No connection
14	GNDA	Power ground of driver A.
15	VOA	Output of driver A.
16	VDDA	Power supply of driver A. A local low ESR and ESL capacitor should be connected between VDDA and GNDA.

FUNCTIONAL BLOCK DIAGRAM

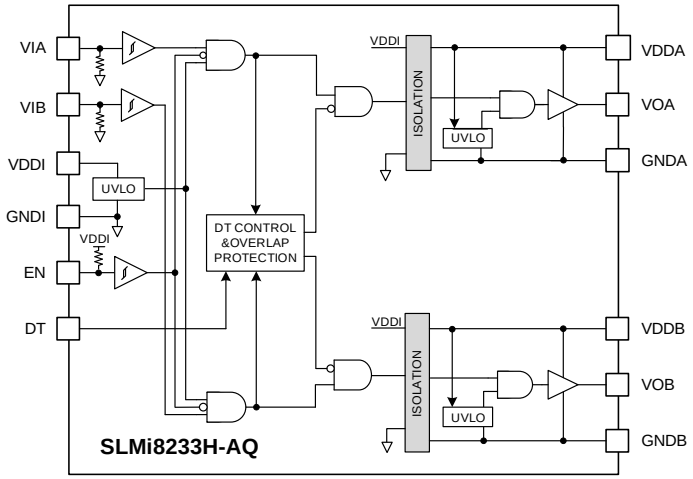


Figure 4. SLMi8233H-AQ Functional Block Diagram

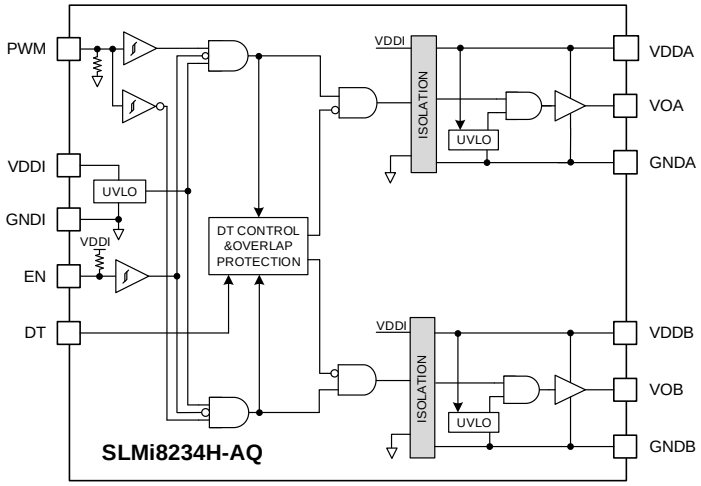


Figure 5. SLMi8234H-AQ Functional Block Diagram

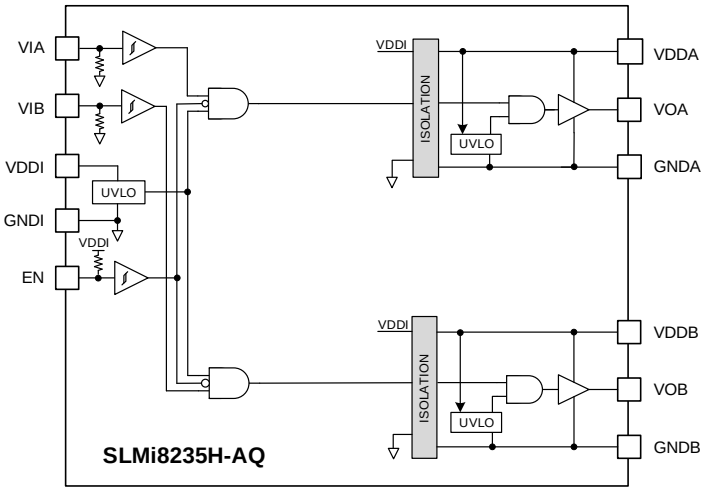


Figure 6. SLMi8235H-AQ Functional Block Diagram

ORDERING INFORMATION

Order Part No.	Package	QTY
SLMi8233HBDCG-AQ	SOP16W, Pb-Free	1500/Reel
SLMi8233HDDCG-AQ	SOP16W, Pb-Free	1500/Reel
SLMi8234HBDCG-AQ	SOP16W, Pb-Free	1500/Reel
SLMi8234HDDCG-AQ	SOP16W, Pb-Free	1500/Reel
SLMi8235HBDCG-AQ	SOP16W, Pb-Free	1500/Reel
SLMi8235HDDCG-AQ	SOP16W, Pb-Free	1500/Reel
SLMi8233HBDCP-AQ	SOP14W, Pb-Free	1500/Reel
SLMi8233HDDCP-AQ	SOP14W, Pb-Free	1500/Reel
SLMi8234HBDCP-AQ	SOP14W, Pb-Free	1500/Reel
SLMi8234HDDCP-AQ	SOP14W, Pb-Free	1500/Reel
SLMi8235HBDCP-AQ	SOP14W, Pb-Free	1500/Reel
SLMi8235HDDCP-AQ	SOP14W, Pb-Free	1500/Reel

FAMILY OVERVIEW

Part Number	Input Configuration	Output Configuration	Programmable Dead Time	Overlap Protection	Peak Output Current	UVLO
SLMi8233HBDCG-AQ, SLMi8233HBDCP-AQ	VIA,VIB	HS/LS	Yes	Yes	4.0 A	8.5V/7.5V
SLMi8233HDDCG-AQ, SLMi8233HDDCP-AQ	VIA,VIB	HS/LS	Yes	Yes	4.0 A	12.5V/11.5V
SLMi8234HBDCG-AQ, SLMi8234HBDCP-AQ	PWM	HS/LS	Yes	Yes	4.0 A	8.5V/7.5V
SLMi8234HDDCG-AQ, SLMi8234HDDCP-AQ	PWM	HS/LS	Yes	Yes	4.0 A	12.5V/11.5V
SLMi8235HBDCG-AQ, SLMi8235HBDCP-AQ	VIA,VIB	Dual Driver	No	No	4.0 A	8.5V/7.5V
SLMi8235HDDCG-AQ, SLMi8235HDDCP-AQ	VIA,VIB	Dual Driver	No	No	4.0 A	12.5V/11.5V

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Definition		Min	Max	Unit
V_{DDI}	Input Power Supply Voltage		-0.3	20	V
V_{IA},V_{IB}, V_{EN},V_{PWM}	Input Signal Voltage		-7	20	V
V_{DDA}, V_{DDB}	Driver Power Supply		-0.3	45	V
V_{OUTA}, V_{OUTB}	Driver Output Voltage		-0.3	45	V
V_{ch2ch}	Channel to Channel Voltage	SOP16W		1500	V
		SOP14W		1850	V
T_J	Junction Temperature		-40	150	°C
T_S	Storage Temperature		-65	150	°C

RECOMMENDED OPERATION CONDITIONS[1]

Symbol	Definition	Min	Max	Unit
V_{DDI}	Input Power Supply Voltage	3	18	V
V_{IA},V_{IB}, V_{EN},V_{PWM}	Input Signal Voltage	-5	18	V
V_{DDA}, V_{DDB}	Driver Power Supply (8.5V UVLO Version)	9	40	V
V_{DDA}, V_{DDB}	Power Supply for Driver (12.5V UVLO Version)	13.5	40	V
T_J	Junction Temperature	-40	150	°C
T_A	Storage Temperature	-40	125	°C

ESD RATINGS

Symbol	Definition	Value	Units
V_{ESD}	HBM	±4000	V
	CDM	±2000	

Note 1: V_{DDI}, V_{IA}, V_{IB}, V_{EN}, V_{PWM} are reference to GNDI; V_{DDA}, V_{OUTA} are referenced to GNDA; V_{DDB}, V_{OUTB} are referenced to GNDB;

THERMAL INFORMATION

Symbol	Definition	Value	Unit
$R_{\theta JA}$	Junction to ambient thermal resistance	100	°C/W
$R_{\theta JC(TOP)}$	Junction to case (top) thermal resistance	40	°C/W

PACKAGE SPECIFICATIONS

Symbol	Definition	Min.	Typ.	Max.	Units
R_{IO}	Resistance (Input Side to Output Side)		10^{12}		Ω
C_{IO}	Capacitance (Input Side to Output Side)		1.8		pF

INSULATION SPECIFICATIONS

Symbol	Definition	Test Condition	Value	Units
CLR	External clearance	Shortest terminal to terminal distance through air	8.0	mm
CPG	External creepage	Shortest terminal to terminal distance across the package surface	8.0	mm
DTI	Distance through the insulation	Minimum internal gap	>16	um
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11), IEC 60112	>600	V
	Material Group		I	
	Overvoltage category	Rated mains voltages ≤150Vrms	I-IV	
		Rated mains voltages ≤300Vrms	I-IV	
		Rated mains voltages ≤600Vrms	I-IV	
		Rated mains voltages ≤1000Vrms	I-III	
DIN V VDE 0884-11(1)				
V_{IORM}	Maximum repetitive peak isolation voltage		1414	V_{PK}
V_{IOWM}	Maximum isolation working voltage		1000	V_{RMS}
V_{IOTM}	Maximum transient isolation voltage	60s	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage	Test method per IEC62368, 1.2/50us waveform, V_{TEST}=1.6 x V_{IOSM}	6250	V_{PK}
q_{pd}	Apparent charge	Method b2: $V_{pd(m)}$=1.875 x V_{IORM}, tm=1 s	≤5	pC
	Climatic Category		40/125/21	
	Pollution Degree		2	
UL1577				
V_{ISO}	Withstand Isolation Voltage	V_{TEST}=V_{ISO}, t=60s (qualification), V_{TEST}=1.2 x V_{ISO}, t=1s (100% production)	5000	V_{RMS}

Note 1: Certification planned

SAFETY RELATED CERTIFICATIONS

VDE（planned）	**UL**	**CQC**
DIN VDE 0884-17: 2021-10	UL 1577 component recognition program	Certified according to GB4943.1-2011
Reinforced Insulation	Single protection, 5000 V_{RMS}	Reinforced insulation, Altitude≤ 5000m, Tropical climate, 400 V_{RMS} maximum working voltage
Certification Planned	Certification Planned	Certification Planned

SAFETY LIMITING VALUES

Symbol	Parameter	Condition	Side	Value	Unit
I_S	Safety output current	V_{DDA}=V_{DDB}=16V, C_{LOAD}=1nF, 2MHz PWM, 50% duty, $R_{\theta JA}$=100°C/W, T_J =150°C, T_A =25°C	Driver A and Driver B	73	mA
P_S	Safety input, output, or total power	V_{DDA}=V_{DDB}=16V, C_{LOAD}=1nF, V_{DDI}=12V, 2MHz PWM, 50% duty, $R_{\theta JA}$=100°C/W, T_J =150°C, T_A =25°C	Input	36	mW
			Driver A	584	
			Driver B	584	
			Total	1204	
T_S	Maximum safety temperature			150	°C

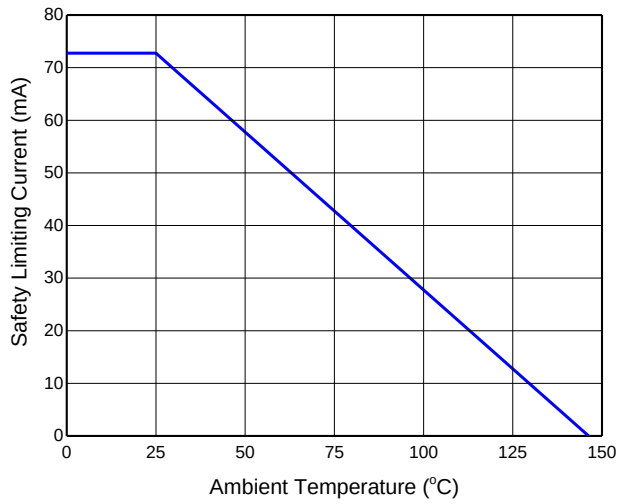


Figure 7. Thermal Derating Curve for Limiting Current per VDE (Current in VDDA and VDDB)

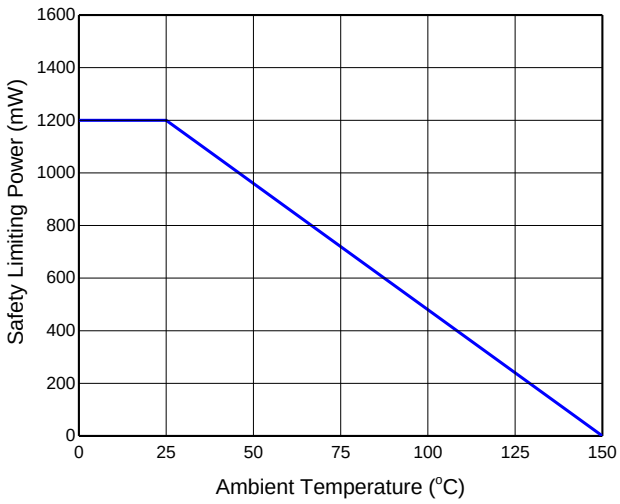


Figure 8. Thermal Derating Curve for Limiting Power per VDE

ELECTRICAL CHARACTERISTICS (DC)

V_{DDI} = 5 V, 0.1μF capacitor from VDDI to GNDI, V_{DDA} = V_{DDB} =15V, 1μF capacitor from VDDA and VDDB to GNDA and GNDB, T_A = –40°C to +125°C, unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Input Power Supply						
V_{DDI}	Input Supply Voltage		3		18	V
$V_{UVLO\_VDDI\_R}$	VDDI UVLO Rising		2.55	2.7	2.85	V
$V_{UVLO\_VDDI\_F}$	VDDI UVLO Falling		2.35	2.5	2.65	V
V_{UVLO_HYS}	VDDI UVLO Hysteresis		1.4	0.2	2.6	V
I_{VDDI}	Quiescent Current	V_{IA} = 0V, V_{IB} = 0V		2		mA
	Operation Current	f_{sw}= 50kHz, (50% Duty Cycle), both channels	2.17	3.1	4.03	mA
Logic Interface						
V_{IH}	High Level Input Threshold Voltage at VIA, VIB, EN and PWM		2			V
V_{IL}	Low Level Input Threshold Voltage at VIA, VIB, EN and PWM				0.8	V
R_{PD}	Pull down Resistance on VIA,VIB and PWM		126	180	235	kΩ
R_{PU}	Pull up Resistance on EN		126	180	235	kΩ
Driver Power Supply						
$V_{UVLO\_VDDA\_R}$, $V_{UVLO\_VDDB\_R}$	VDDA, VDDB UVLO Rising	8.5V UVLO Version	8	8.5	9	V
		12.5V UVLO Version	11.5	12.5	13.5	V
$V_{UVLO\_VDDA\_F}$, $V_{UVLO\_VDDB\_F}$	VDDA, VDDB UVLO Falling	8.5V UVLO Version	7	7.5	8	V
		12.5V UVLO Version	10.5	11.5	12.5	V
$V_{UVLO\_VDDA\_HYS}$, $V_{UVLO\_VDDB\_HYS}$	VDDA, VDDB UVLO Hysteresis	8.5V UVLO Version		1		V
		12.5V UVLO Version		1		V
I_{VDDA}, I_{VDDB}	VDDA/B Quiescent Current, per Channel	V_{IA} = 0V, V_{IB} = 0V	0.8	1.5	2.6	mA
OUTPUT						
I_{OH}	Peak Source Current			4		A
I_{OL}	Peak Sink Current			7		A
V_{OH}	High Level Output Voltage	I_O=-10mA		12	22	mV
V_{OL}	Low Level Output Voltage	I_O=10mA		6.2	11	mV
Dead Time						
R_{DT}	Resistance range on DT		5		220	kΩ

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{DT}	Dead time	R_{DT}=20kΩ	160	200	240	ns
C_{DT}	Capacitance of C_{DT}				10	nF

SWITCHING CHARACTERISTICS (AC)

V_{DDI} = 5 V, 0.1μF capacitor from VDDI to GNDI, V_{DDA} = V_{DDB} =15V, 1μF capacitor from VDDA and VDDB to GNDA and GNDB, T_A = –40°C to +125°C, unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Switching Characteristics						
t_{PLH}	Propagation Delay, Low to High	C_{LOAD}=1nF, f_{sw}=1kHz, (50% Duty Cycle)		40	60	ns
t_{PHL}	Propagation Delay, High to Low			40	60	ns
t_r	Turn on Rise Time			6	15	ns
t_f	Turn off Fall Time			4	10	ns
t_{PWD}	Pulse Width Distortion				18	ns
t_{DM}	Propagation Delay Matching between OUTA and OUTB				18	ns
$t_{UVLO\_REC\_VDDI}$	VDDI UVLO Recovery Delay			15		μs
$t_{UVLO\_REC\_VDDA(B)}$	VDDA, VDDB UVLO Recovery Delay			18		μs
$CMTI_H$	High Level Static Common Mode Transient Immunity	V_{CM}=1000V, T_A=25°C	100			kV/μs
$CMTI_L$	Low Level Static Common Mode Transient Immunity	V_{CM}=1000V, T_A=25°C	100			kV/μs

PARAMETER MEASUREMENT INFORMATION

Propagation Delay and Pulse Width Distortion

Figure 9 shows the timing diagram of the propagation delay t_{PDLH} and t_{PDHL}, pulse distortion t_{PWD} and delay matching t_{DM} from the input V_{IA} and V_{IB}. Short the DT pin to VDDI to disable the dead time function.

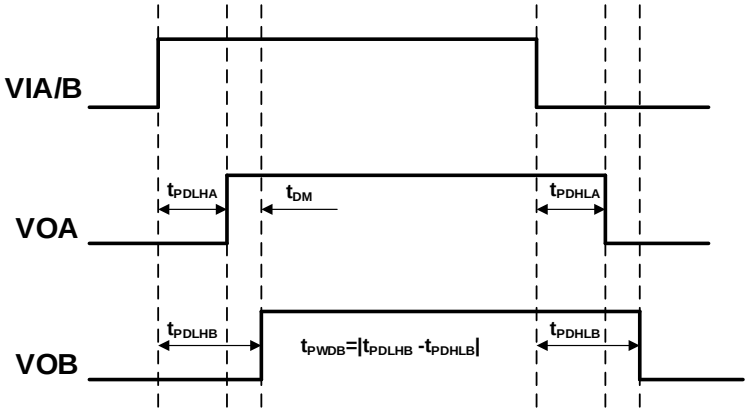


Figure 9. Propagation Delay and Pulse Width Distortion

Rise and Fall Time Testing

Figure 10 shows the criteria for measuring rise time (t_r) and fall time (t_f).

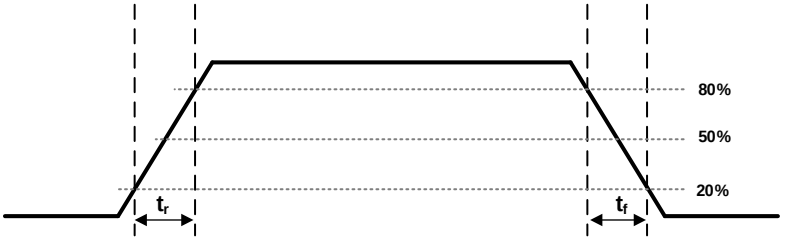


Figure 10. Turn On Rise Time and Turn Off Fall Time

CMTI Testing

Figure 11 is the simplified diagram of the CMTI testing. Common mode voltage is set to 1000V.

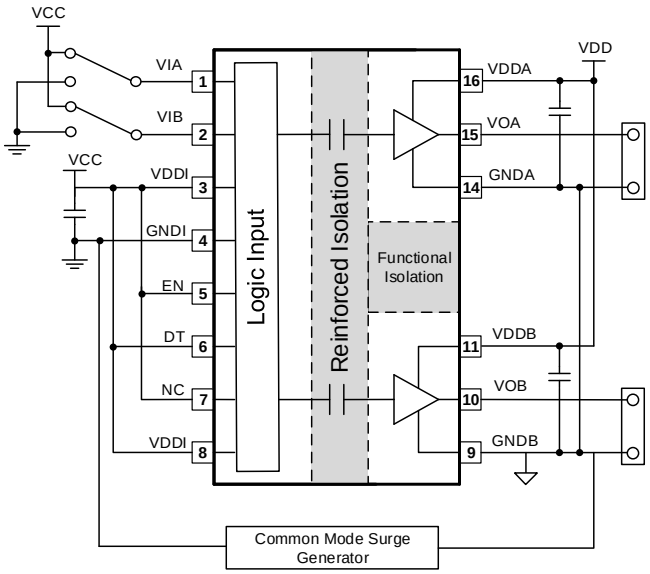


Figure 11. CMTI Test Circuit

FEATURE DESCRIPTION

SLMi8233/4/5H-AQ is a flexible dual channel isolated gate driver that can drive IGBTs and MOSFETs. It has 4.0A peak output current capability with maxim output driver supply voltage of 40V. SLMi8233/4/5H-AQ has many features that allow it to integrate well with control circuitry and protect the gates it drives such as: resistor programmable dead time control, an EN pin, and under voltage lock out (UVLO) for both input and output voltages.

Under Voltage Lockout

The SLMi8233/4/5H-AQ has under voltage lock out (UVLO) protection feature on each driver power supply voltage between the VDDA (VDDB) and GNDA (GNDB) pins. When the VDDx voltage is lower than $V_{UVLO\_VDDX\_R}$, during device start up or lower than $V_{UVLO\_VDDX\_F}$, after start up, the VDDA (VDDB) UVLO feature holds the driver output low, regardless of the status of the input pins. A hysteresis on the UVLO feature prevents glitch when there is noise from the power supply.

The SLMi8233/4/5H-AQ also monitors the input power supply and there is an internal under voltage lock out protection feature on the VDDI. The driver outputs (VOA and VOB) are hold low when the voltage on the VDDI is lower than $V_{UVLO\_VDDI\_R}$ during start up or lower than $V_{UVLO\_VDDI\_F}$ after start up. There is a hysteresis on the VDDI UVLO feature to prevent glitch due the noise on the VDDI power supply.

Enable Input Function

When the EN is pulled low, the VOA and VOB are pulled low regardless of the states of VIA and VIB. When the EN pin is pulled high, the VOA and VOB are allowed for normal operation and controlled by the VIA and VIB.

The EN input has no effect if VDDI is below its UVLO threshold and VOA, VOB remain low. There is an internal pull up resistor on the EN pin.

Control Input and Output Logic

The VIA and VIB input controls the corresponding output channel, VOA and VOB. A logic high signal on VIA (VIB) causes the output of VOA (VOB) to go high. And a logic low on VIA (VIB) causes the output of VOA (VOB) to go low.

For PWM input versions (SLMi8234H-AQ), when the PWM input is high, the VOA is high and VOB is low. And when the PWM input is low, the VOA is low and VOB is high.

The Table 4 and Table 5 show the relationship between VIA,VIB, PWM, EN, UVLO and Output of VOA and VOB.

Table 4. Relationship between Input and Output with VIA, VIB input

VIA	VIB	EN	VDDI UVLO	VDDA UVLO	VDDB UVLO	VOA	VOB	Note
H	L	H	No	No	No	H	L	
L	H	H	No	No	No	L	H	
L	L	H	No	No	No	L	L	
H	H	H	No	No	No	H	H	Dual driver
						L	L	HS/LS
X	X	L	No	No	No	L	L	Device disabled
X	X	X	Yes	No	No	L	L	VDDI UVLO active
H	X	H	No	No	Yes	H	L	VDDB UVLO active
L	X	H	No	No	Yes	L	L	
X	H	H	No	Yes	No	L	H	VDDA UVLO active
X	L	H	No	Yes	No	L	L	

Table 5. Relationship between Input and Output with PWM input

PWM	EN	VDDI UVLO	VDDA UVLO	VDDB UVLO	VOA	VOB	Note
H	H	No	No	No	H	L	
L	H	No	No	No	L	H	
X	L	No	No	No	L	L	Device disabled
X	X	Yes	No	No	L	L	VDDI UVLO active
H	H	No	No	Yes	H	L	VDDB UVLO active
L	H	No	No	Yes	L	L	
H	H	No	Yes	No	L	L	VDDA UVLO active
L	H	No	Yes	No	L	H	

Dead-time Program

For the high side/low side configuration driver, there is a dead-time between VOA and VOB. The dead-time delay (t_{DT}) is programmed by a resistor (R_{DT}) connected from the DT input to ground and it can be calculated with below equation.

$$t_{DT}[\text{ns}] \approx 10\times R_{DT}[\text{k}\Omega]$$

Here, t_{DT} is the dead-time delay, R_{DT} is the resistance value between DT and ground.

The DT pin can be connected to VDDI or left floating to provide a nominal dead time at approximately 400 ps.

A bypassing capacitor is recommended to be put between DT and GNDI to achieve better noise immunity.

A bypassing capacitor, 2.2nF or greater, is recommended to be put between DT and GNDI to achieve better noise immunity.

The Figure 12 shows the input and output logic with dead-time in different condition.

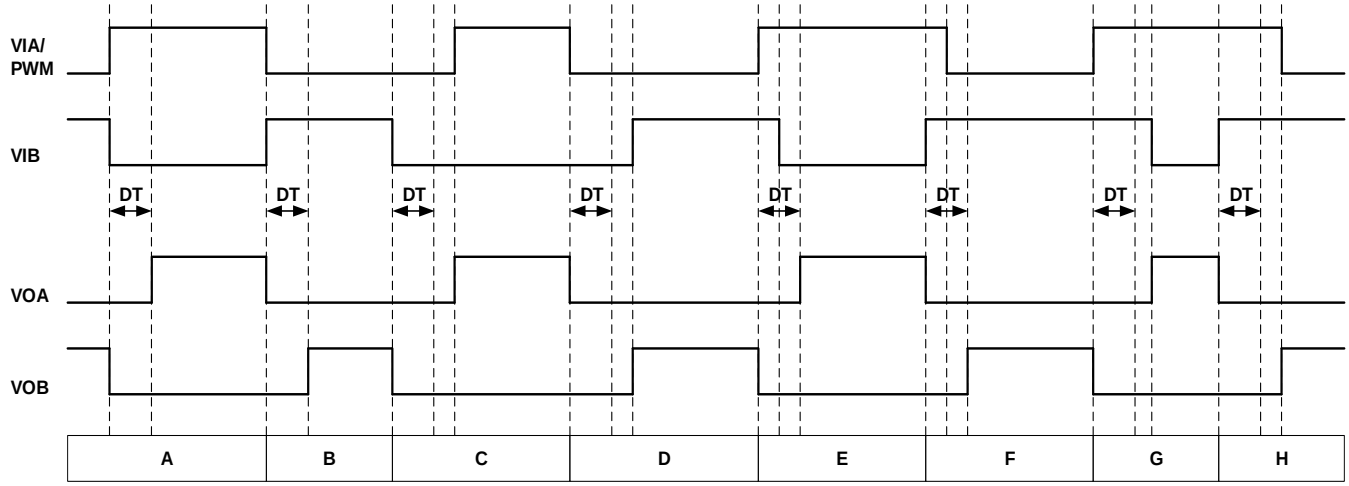


Figure 12. Input and output logic with dead-time

Condition A: VIA goes high and VIB goes low. VOB goes low immediately and VOA goes high after the programmed dead-time.

Condition B: VIA goes low and VIB goes high. VOA goes low immediately and VOB goes high after the programmed dead-time.

Condition C: VIB goes low and VIA still low. VOB goes low immediately. Since the VIA input dead-time is longer than the programmed dead-time, the VOA goes high immediately when the VIA input goes high.

Condition D: VIA goes low and VIB still low. VOA goes low immediately. Since the VIB input dead-time is longer than the programmed dead-time, the VOB goes high immediately when the VIB input goes high.

Condition E: VIA goes high while VIB and VOB are still high, the overlap time is shorter than the programmed dead-time. To avoid overshoot, VOB goes low immediately when the VIA goes high. The VOA goes high after the programmed dead-time.

Condition F: VIB goes high while VIA and VOA are still high, the overlap time is shorter than the programmed dead-time. To avoid overshoot, VOA goes low immediately when the VIB goes high. The VOB goes high after the programmed dead-time.

Condition G: VIA goes high while VIB and VOB are still high, the overlap time is longer than the programmed dead-time. To avoid overshoot, VOB goes low immediately when the VIA goes high. Since the overlap time is longer than the programmed dead-time, the VOA goes high immediately when the VIB goes low.

Condition H: VIB goes high while VIA and VOA are still high, the overlap time is longer than the programmed dead-time. To avoid overshoot, VOA goes low immediately when the VIB goes high. Since the overlap time is longer than the programmed dead-time, the VOB goes high when the VIA goes low.

APPLICATION INFORMATION

The circuit in Figure 13 shows the typical application circuit for SLMi8233H-AQ to driver a typical half bridge configuration which could be used in several popular power converter topologies such as synchronous buck, synchronous boost, half bridge, full bridge, LLC etc. topologies and 3-phase motor drive applications.

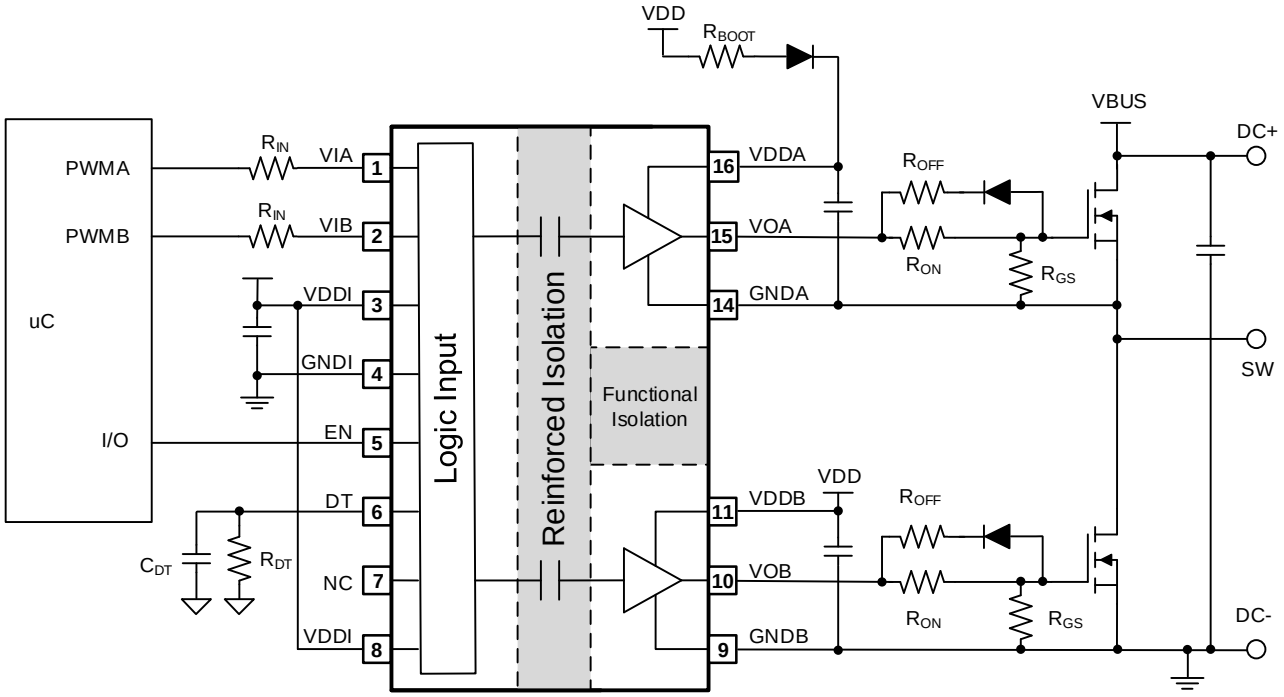
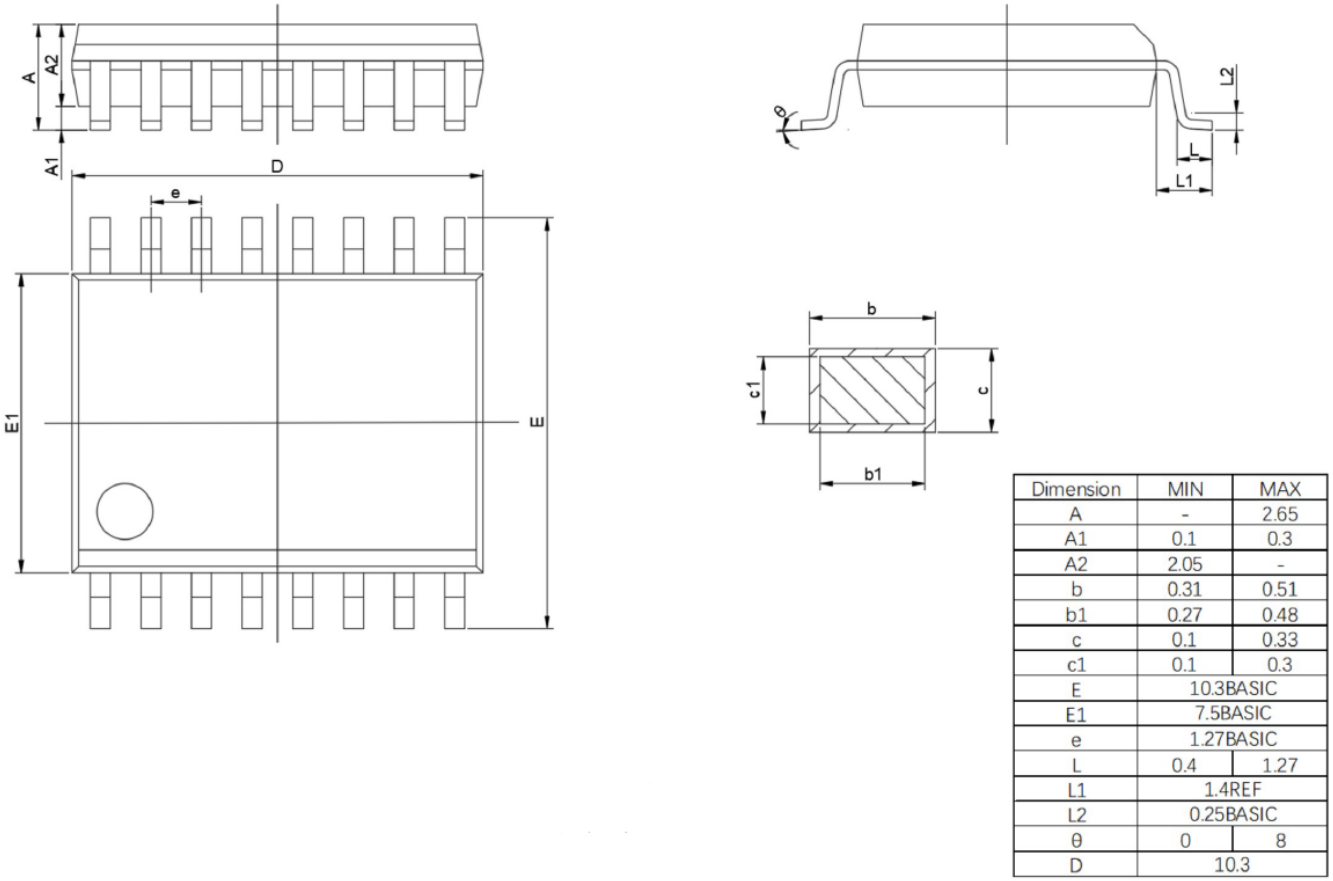


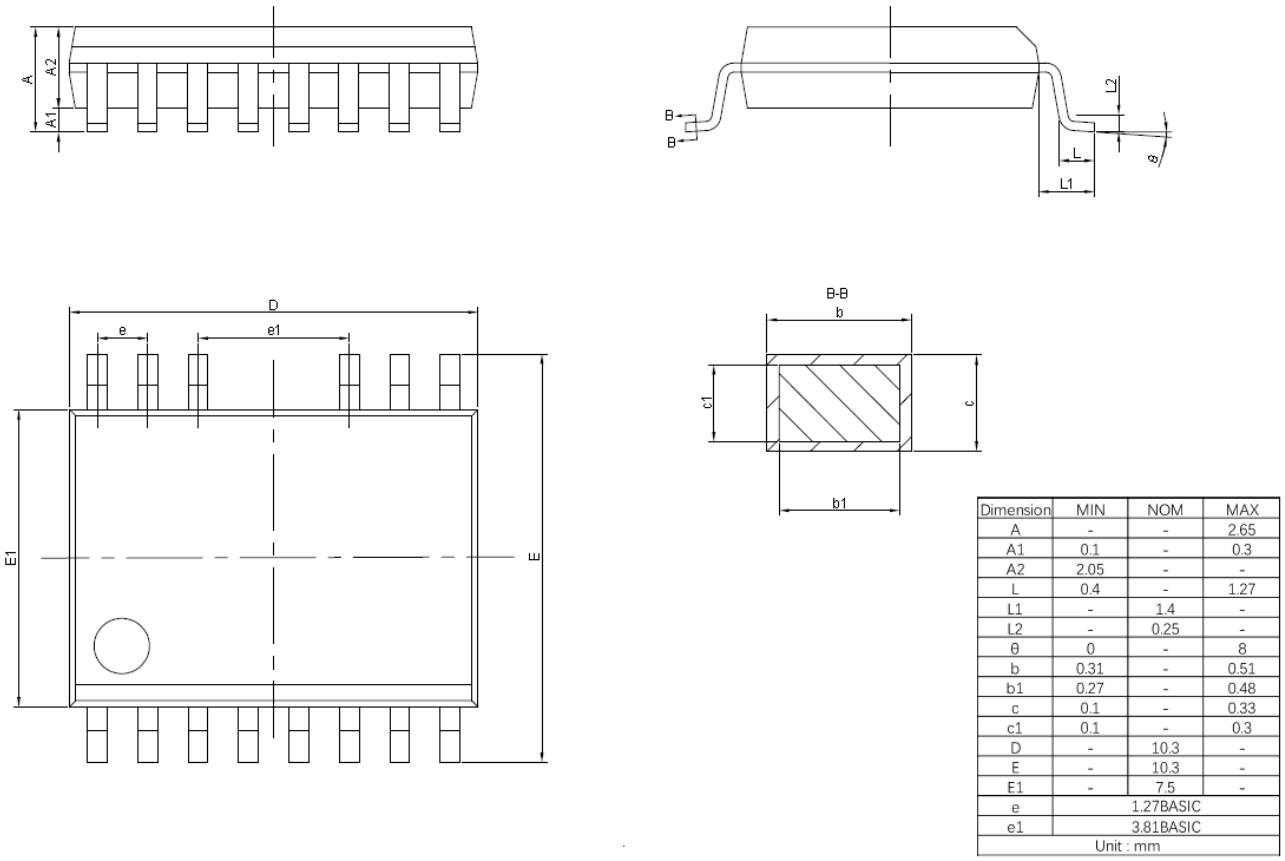
Figure 13. Typical Application Schematic

PACKAGE CASE OUTLINES



Dimension	MIN	MAX
A	-	2.65
A1	0.1	0.3
A2	2.05	-
b	0.31	0.51
b1	0.27	0.48
c	0.1	0.33
c1	0.1	0.3
E	10.3BASIC	
E1	7.5BASIC	
e	1.27BASIC	
L	0.4	1.27
L1	1.4REF	
L2	0.25BASIC	
θ	0	8
D	10.3	

Figure 14. SOP16W Package Outline Dimensions



Dimension	MIN	NOM	MAX
A	-	-	2.65
A1	0.1	-	0.3
A2	2.05	-	-
L	0.4	-	1.27
L1	-	1.4	-
L2	-	0.25	-
θ	0	-	8
b	0.31	-	0.51
b1	0.27	-	0.48
c	0.1	-	0.33
c1	0.1	-	0.3
D	-	10.3	-
E	-	10.3	-
E1	-	7.5	-
e	1.27BASIC		
e1	3.81BASIC		
Unit : mm			

Figure 15. SOP14W Package Outline Dimensions

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Rev 1.0 datasheet: 2022-10-14	
Whole document	Initial version release