



# SLP4N65C / SLF4N65C 650V N-Channel MOSFET

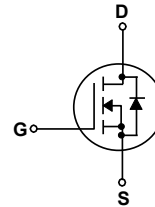
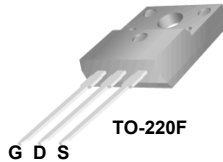
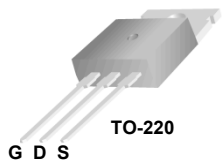
SLP4N65C / SLF4N65C

## General Description

This Power MOSFET is produced using Maple semi's advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

## Features

- 4.0A, 650V,  $R_{DS(on)typ.} = 2.5\Omega @ V_{GS} = 10V$
- Low gate charge ( typical 14nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



## Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted

Symbol	Parameter	SLP4N65C	SLF4N65C	Units
V <sub>DSS</sub>	Drain-Source Voltage	650		V
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C) - Continuous (T <sub>C</sub> = 100°C)	4.0	4.0 *	A
		2.4	2.4 *	A
I <sub>DM</sub>	Drain Current - Pulsed (Note 1)	16	16 *	A
V <sub>GSS</sub>	Gate-Source Voltage	±30		V
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)	100		mJ
I <sub>AR</sub>	Avalanche Current (Note 1)	4.5		A
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)	16.4		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5		V/ns
P <sub>D</sub>	Power Dissipation (T <sub>C</sub> = 25°C) - Derate above 25°C	93	31	W
		0.74	0.25	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +150		°C
T <sub>L</sub>	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		°C

\* Drain current limited by maximum junction temperature.

## Thermal Characteristics

Symbol	Parameter	SLP4N65C	SLF4N65C	Units
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	1.35	4.05	°C/W
R <sub>θJS</sub>	Thermal Resistance, Case-to-Sink Typ.	0.5	--	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	62.5	62.5	°C/W

**Electrical Characteristics**T<sub>C</sub> = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	650	--	--	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	--	0.65	--	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 650 V, V <sub>GS</sub> = 0 V	--	--	1	μA
		V <sub>DS</sub> = 520 V, T <sub>C</sub> = 125°C	--	--	10	μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V	--	--	-100	nA

**On Characteristics**

V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0	--	4.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.0 A	--	2.5	3.0	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 2.0 A (Note 4)	--	4.5	--	S

**Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	--	560	--	pF
C <sub>oss</sub>	Output Capacitance		--	55	--	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	7	--	pF

**Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 325 V, I <sub>D</sub> = 4.0 A, R <sub>G</sub> = 25 Ω (Note 4, 5)	--	10	--	ns
t <sub>r</sub>	Turn-On Rise Time		--	40	--	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	40	--	ns
t <sub>f</sub>	Turn-Off Fall Time		--	50	--	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 520 V, I <sub>D</sub> = 4.0 A, V <sub>GS</sub> = 10 V (Note 4, 5)	--	16	--	nC
Q <sub>gs</sub>	Gate-Source Charge		--	2.5	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	6.5	--	nC

**Drain-Source Diode Characteristics and Maximum Ratings**

I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current	--	--	4.0	A	
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current	--	--	16	A	
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 4.0 A	--	--	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 4.0 A,	--	300	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge	di <sub>F</sub> / dt = 100 A/μs (Note 4)	--	2.0	--	μC

**Notes:**

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 12.5mH, I<sub>AS</sub> = 4.0 A, V<sub>DD</sub> = 50V, R<sub>G</sub> = 25Ω, Starting T<sub>J</sub> = 25°C
3. I<sub>SD</sub> ≤ 4.0 A, di/dt ≤ 200A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, Starting T<sub>J</sub> = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

### Typical Characteristics

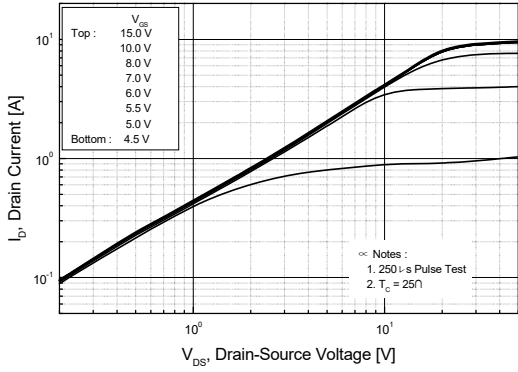


Figure 1. On-Region Characteristics

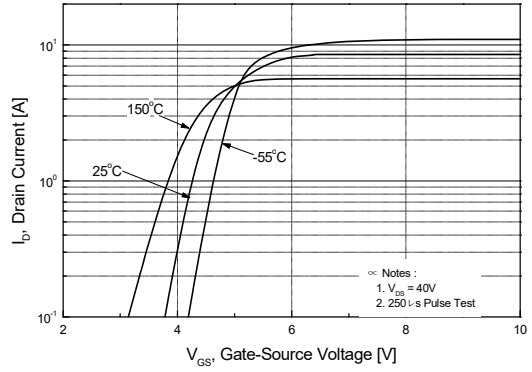


Figure 2. Transfer Characteristics

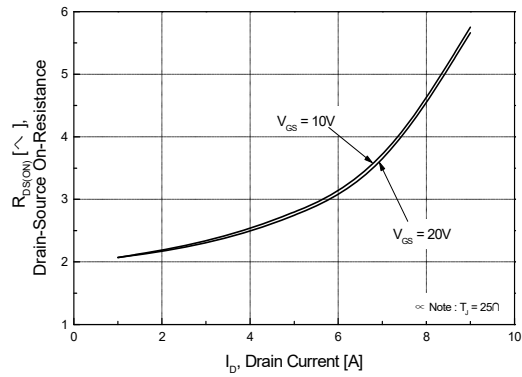


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

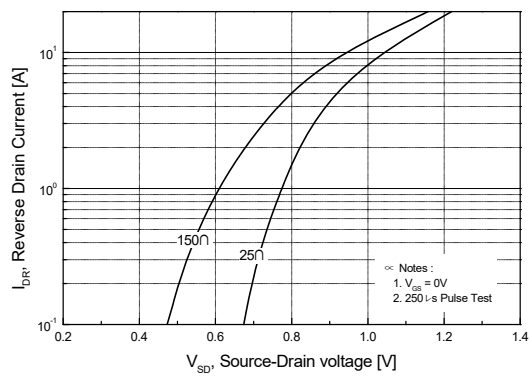


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

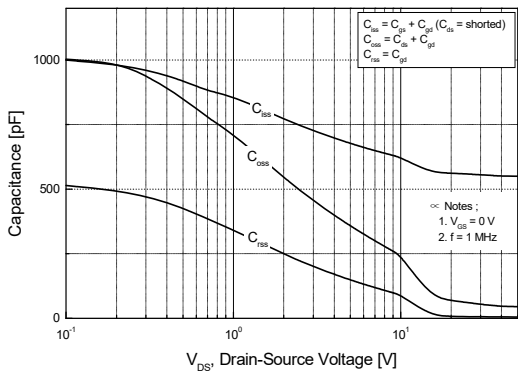


Figure 5. Capacitance Characteristics

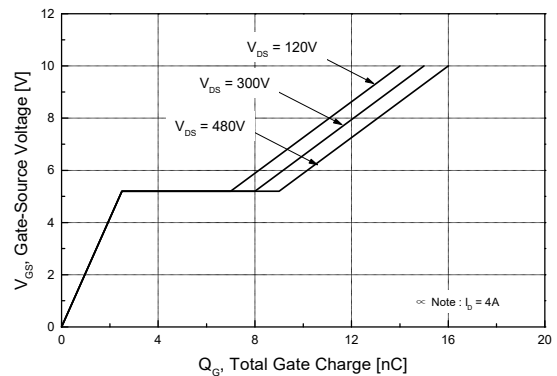


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

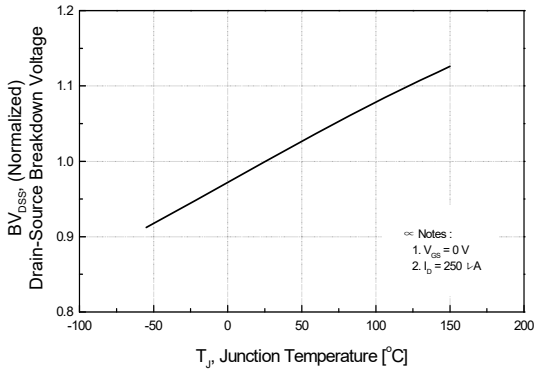


Figure 7. Breakdown Voltage Variation vs Temperature

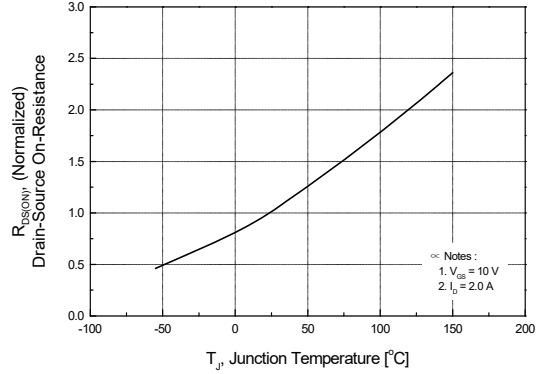


Figure 8. On-Resistance Variation vs Temperature

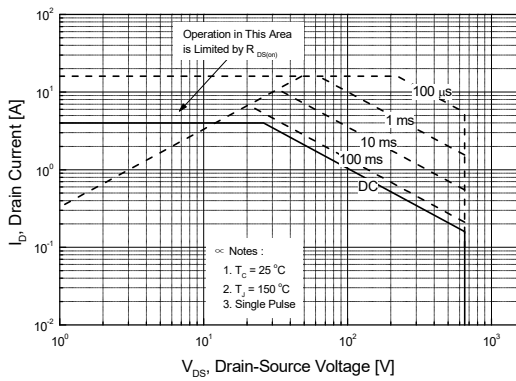


Figure 9-1. Maximum Safe Operating Area for SLP4N65C

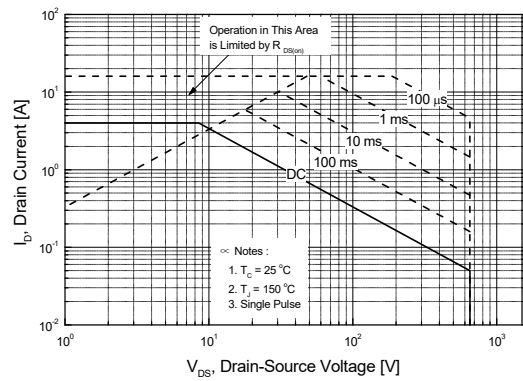


Figure 9-2. Maximum Safe Operating Area for SLF4N65C

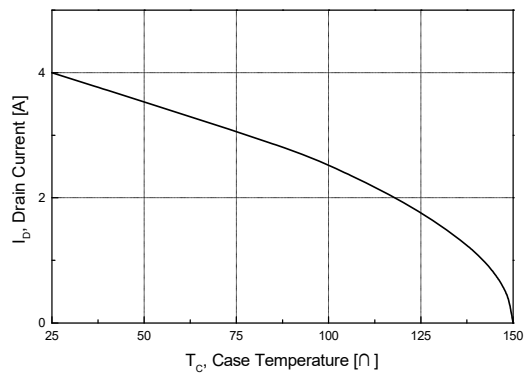


Figure 10. Maximum Drain Current vs Case Temperature

Typical Characteristics (Continued)

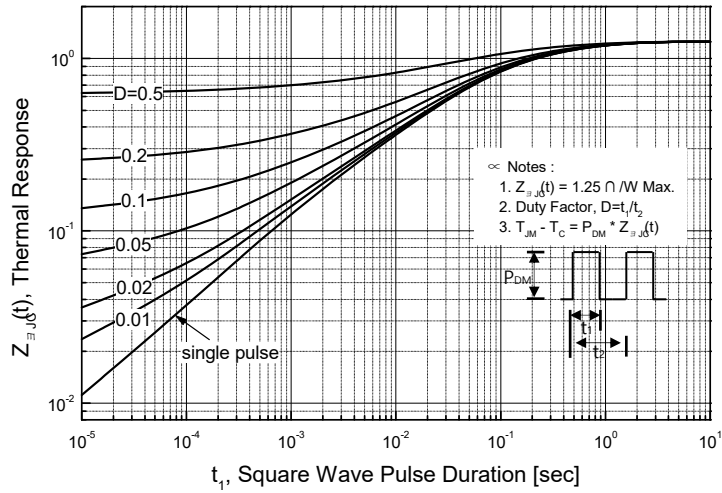


Figure 11-1. Transient Thermal Response Curve for SLP4N65C

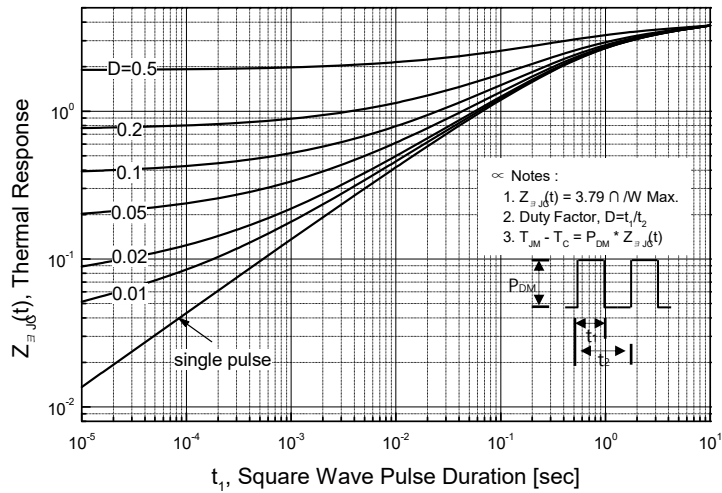
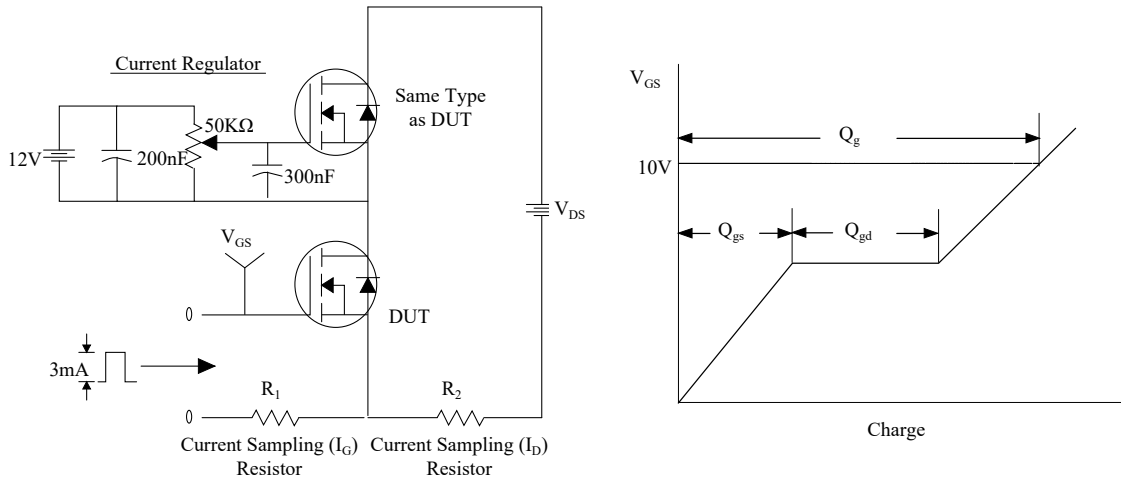
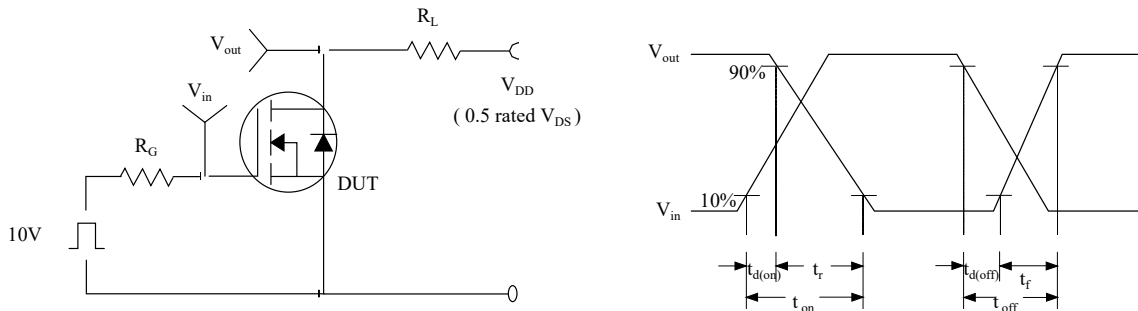


Figure 11-2. Transient Thermal Response Curve for SLF4N65C

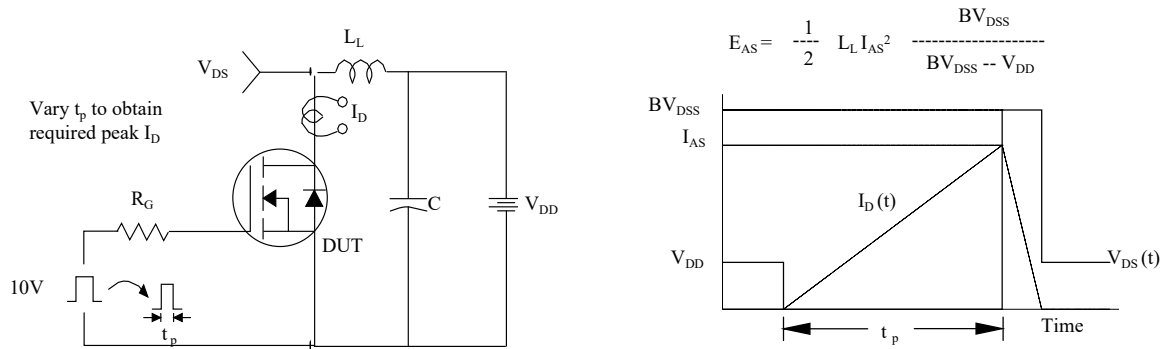
### Gate Charge Test Circuit & Waveform



### Resistive Switching Test Circuit & Waveforms



### Unclamped Inductive Switching Test Circuit & Waveforms



### Peak Diode Recovery dv/dt Test Circuit & Waveforms

