Transient Voltage Suppressors Array for ESD Protection

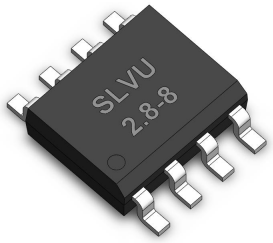
Low Capacitance

SLVU2.8-8

Description

The SLVU2.8-8 is in an SO-08 package and may be used to protect two high-speed line pairs. The “flow-thru” design minimizes trace inductance and reduces voltage overshoot associated with ESD events. The low clamping voltage of the SLVU2.8-8 minimizes the stress on the protected IC.

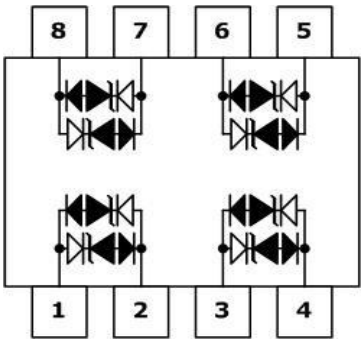
SO-08



Features

- 600 Watts Peak Pulse Power per Line (tp=8/20μs)
- Protects eight lines (four line Pairs)
- Low capacitance
- RoHS Compliant
- IEC61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
- IEC61000-4-4 (EFT) 40A (5/50ηs)
- IEC61000-4-5 (Lightning) 25A (8/20μs)

Pin Configuration



Applications

- 10/100/1000 Ethernet
- WAN/LAN Equipment
- Test & Measurement Equipment
- Switching Systems
- Instrumentation
- DSLAMs
- Base Stations
- Analog Inputs

Mechanical Characteristics

- JEDEC SO-08 Package
- Molding Compound Flammability Rating : UL 94V-0
- Weight 70 Milligrams (Approximate)
- Quantity Per Reel : 2500pcs
- Reel Size : 7 inch
- Lead Finish : Lead Free

Mechanical Characteristics

Symbol	Parameter	Value	Units
P_{PP}	**Peak Pulse Power (tp=8/20μs waveform)**	600	W
T_L	**Lead Soldering Temperature**	260 (10 sec.)	℃
T_{STG}	**Storage Temperature Range**	-55 to +150	℃
T_J	**Operating Temperature Range**	-55 to +150	℃

Transient Voltage Suppressors Array for ESD Protection

Low Capacitance

SLVU2.8-8

Electrical Characteristics (@ 25℃ Unless Otherwise Specified)

Part Number	Device Marking	V_{RWM} (V) (Max.)	V_B (V) (Min.)	I_T (mA)	V_C (V) @5A (Max.)	V_C		I_R (μA) (Max.)	C (pF) (Typ.)
						(V) (Max.)	(@A)		
SLVU2.8-8	SLVU 2.8-8	2.8	3.0	1	8.5	24	25	1	7

Characteristic Curves

Fig1. 8/20μs Pulse Waveform

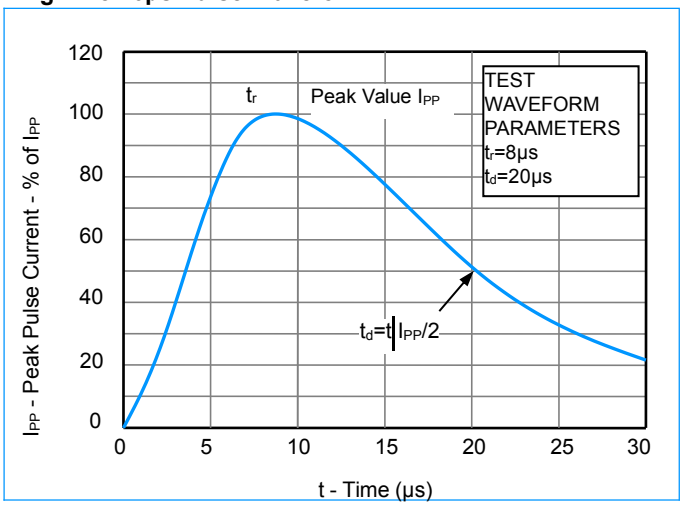


Fig2. ESD Pulse Waveform (according to IEC 61000-4-2)

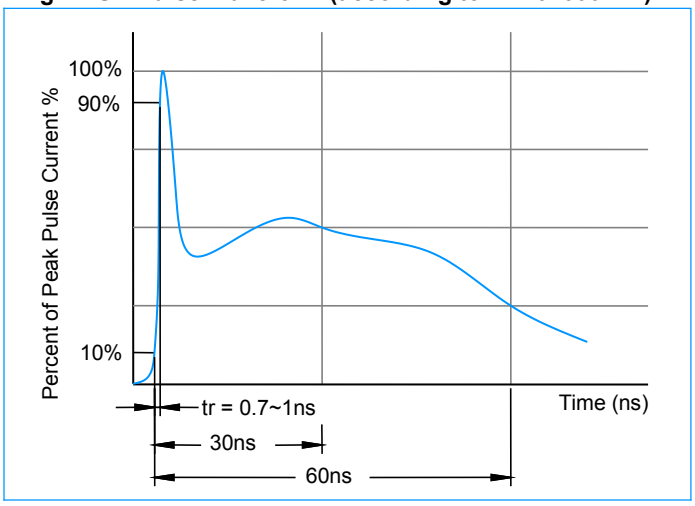


Fig3. Non - Repetitive Peak Pulse Power vs. Pulse Time

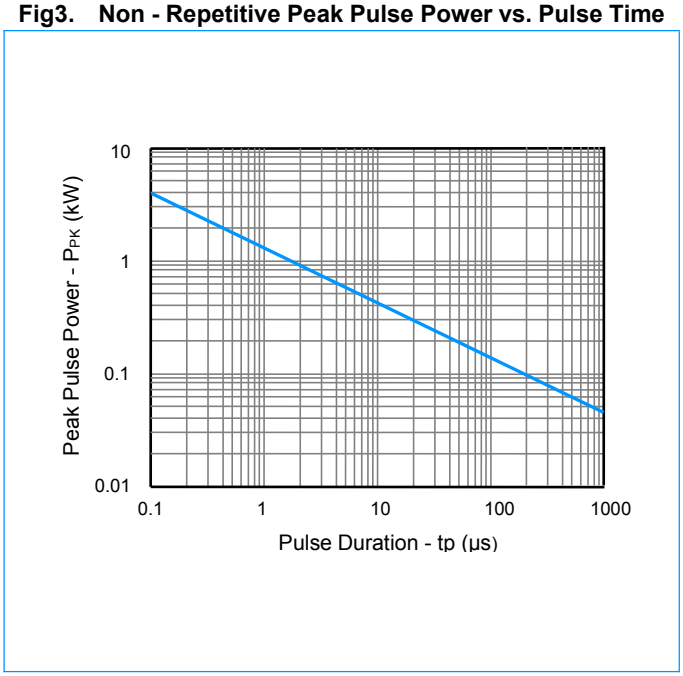
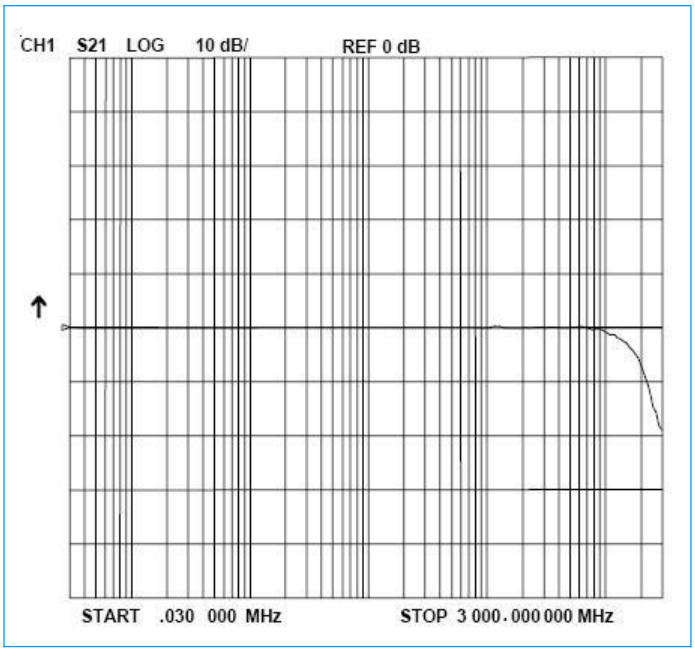


Fig4. Insertion Loss S21

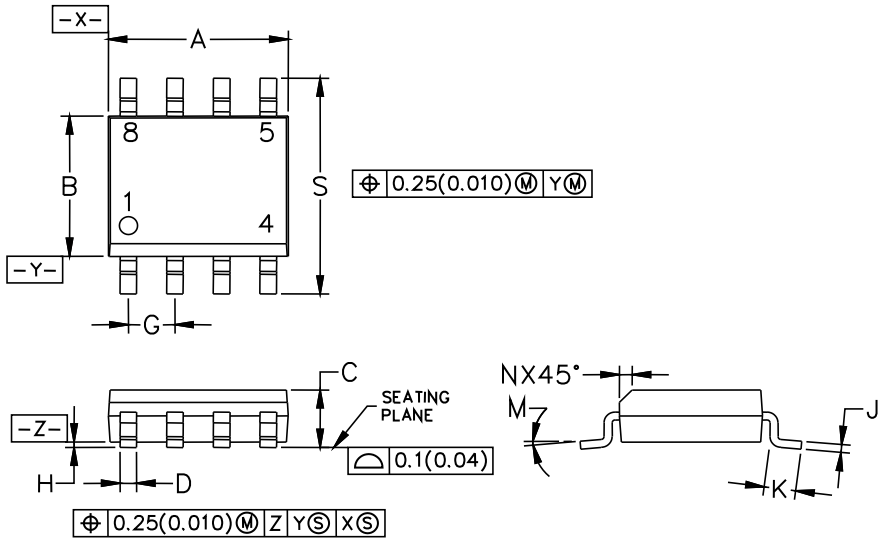


Transient Voltage Suppressors Array for ESD Protection

Low Capacitance

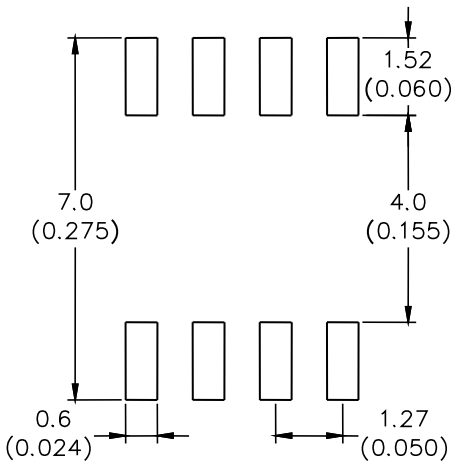
SLVU2.8-8

SO-08 Package Outline & Dimensions



DIM	Millimeters		Inches	
	Min	Max	Min	Max
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27BSC		0.050BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

Soldering Footprint



Applications Note

Electronic equipment is susceptible to damage caused by Electrostatic Discharge (ESD), Electrical Fast Transients (EFT), and tertiary lightning effects. Knowing that equipment can be damaged, the SLVU2.8-8 was designed to provide the level of protection required to safe guard sensitive equipment. This product can be used in different configurations to provide a level of protection to meet unidirectional line requirements as well as bidirectional requirements either in a common-mode or differential-mode configuration.

Figure 1. Unidirectional Common-Mode Protection

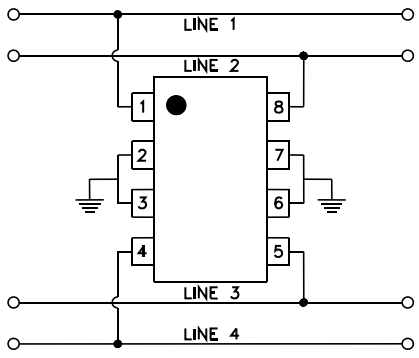
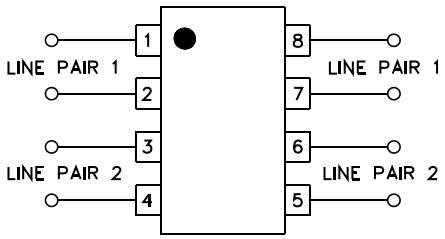


Figure 2. Bidirectional Differential-Mode Protection



Unidirectional Common-Mode Protection (Figure1)

The SLVU2.8-8 provides up to four lines of protection in a common-mode configuration as depicted in figure 1.

Circuit connectivity is as follows:

- Line 1 is connected to Pin 1
- Line 2 is connected to Pin 8
- Line 3 is connected to Pin 5
- Line 4 is connected to Pin 4
- Pins 2, 3, 6 and 7 are connected to ground

Bidirectional Differential-Mode Protection (Figure2)

The SLVU2.8-8 provides up to four lines of protection in a differential-mode configuration as depicted in figure 2.

Circuit connectivity is as follows:

- Line Pair 1 is connected to Pins 1 & 2
- Line Pair 2 is connected to Pins 3 & 4
- Line Pair 3 is connected to Pins 7 & 8
- Line Pair 4 is connected to Pins 5 & 6

Circuit Board Layout Recommendations

Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:

- The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.
- The path length between the TVS device and the protected line should be minimized.
- All conductive loops including power and ground loops should be minimized.
- The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.
- Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.