SM2400

SM2400 N-PLC Transceiver

Multi-Standard Narrowband Power Line Communication Modem

DATA SHEET

Communication Technology by:
Semitech Semiconductor

Features

- Dual core architecture with custom N-PLC optimized DSP and Data Link Layer 32-bit controller
  - Supports a multitude of communication schemes via firmware loads
- High performing custom DSP engine with embedded turnkey firmware featuring:
  - Configurable operational band within 5 - 500 kHz range - compliant with CENELEC, FCC and ARIB
  - OFDM and FSK modulations
  - PHY firmware options compliant with IEEE 1901.2, PRIME, G3-PLC
  - Proprietary operating modes: XR, XXR
  - Selectable differential and coherent BPSK, QPSK, 8PSK and coherent 16QAM modulations
  - Configurable data rate up to (or over) 600 kbps depending on communication mode
  - Programmable frequency notching to improve coexistence
  - Jammer cancellation
  - Adaptive tone mapping (on/off sub-band bit loading)
  - FEC - Convolutional, Reed-Salomon and Viterbi coding
  - CRC16
  - Carrier RSSI, SNR and LQI indicators for best channel adaptation and L2/L3 metrics
  - Zero-crossing detector
- Programmable 32-bit RISC protocol engine featuring:
  - Data Link Layer firmware options compliant with IEEE 1901.2, G3-PLC, PRIME, IEC61334-4-32 and others
  - IP adaptation layers - IPv4, 6LoWPAN
  - Carrier Sense Multiple Access/Collision Avoidance (CSMA/CA) channel access
  - Automatic Repeat Request (ARQ)
  - Meshing and self discovery mechanisms
- CCM* with AES128 / AES256 encryption core
- On-chip Peripheral Interfaces:
  - SPI (slave) / UART host interface
  - Up to two additional SPI slaves for metering, wireless transceiver or other devices
  - SPI master for external Flash
  - 5 GPIO's (additional GPIO's can be made available if other interfaces are unused)
  - Special purpose control signals: Data Rx LED (PHYLED), External AGC (RXRANGE1), External Power Amp. (TXEN), External AFE (AFEEN)
  - JTAG
- Seamless interface to an external line driver for optimal system performance:
  - Integrated A/D and D/A
  - Integrated OpAmp's for Rx and Tx
  - Integrated Programmable Gain Amplifier (PGA)
- Low power operation modes
  - Off-line mode
  - Listen mode
  - Receive mode
  - Transmit mode
- 3.3V (5V tolerant) digital I/O
- Receiver sensitivity of -80 dBV
- -40 °C to +105 °C temperature range
- LQFP64 package

1. Introduction

The SM2400 is the ultimate Narrow-band Power Line Communication (N-PLC) modem that combines cost-effective design optimized for PLC applications with high level of programmability to address multitude of communications schemes and evolving standards. Extremely flexible the SM2400 system-on-chip (SoC) features a dual core architecture for dedicated PHY signal processing and MAC layer functionality to guarantee superior communication performance while maintaining very high levels of flexibility and programmability for OFDM based and other open standards and fully customized implementations. It contains a high-speed 256-bit AES-CCM* engine to ensure standard compliance and secure communication, and all the necessary mixed signal components, such as A/D, D/A, OpAmp's, PGA to yield a cost-effective N-PLC system design for any IoT application.

The SM2400 is a highly programmable OFDM based N-PLC modem combining PHY and MAC with mixed signal components for optimal system cost and performance. The SM2400 combines the benefits of programmable architecture with power and cost efficiency by utilizing a DSP core configured specifically for N-PLC modulations and a dedicated 32-bit core that runs protocols. With its high level of programmability, the SM2400 addresses multitude of communications schemes and can accommodate application specific communication schemes and evolving standards.

The SM2400 comes with a set of firmware options implementing IEEE 1901.2 compliant PHY and MAC layers, a 6LoWPAN data link layer as well as PRIME, G3-PLC and other special modes tailored for Industrial IoT applications.

Proprietary and patented modes (XXR and XR) enable robust communication in harsh conditions for applications where standards compliance is not required. The SM2400 can achieve data rates of up to 500 kbps over 500 kHz frequency band.

The SM2400 enables secure communication featuring a 256-bit AES encryption core with CCM* mode support. Integrated analog front end featuring ADC, DAC, gain control and two OpAmp's allows for a very efficient system design with a low cost BOM.

The SM2400 executes its firmware from internal memory. The code is loaded at the boot time. The SM2400 can boot either from an external SPI flash or from a host MCU, if such is present in the system, via UART or SPI, with the host MCU being the master.

The SM2400 offers the following benefits:

- Single-chip integrating Physical Layer (PHY) and Media Access Controller (MAC)
- Multitude of operating modes addressing all common OFDM-based standards including full compliance with: IEEE 1901.2, G3-PLC, PRIME
- Extremely robust proprietary modes of communication optimized for noisy power line environment
- High flexibility to address standard evolution, new standards and special proprietary modes
- Cost optimized system solution with integrated A/D, D/A, two OpAmp's, and PGA
- Low power consumption

For a definition of acronyms used throughout this document, refer to Section 10., Glossary of Terms.

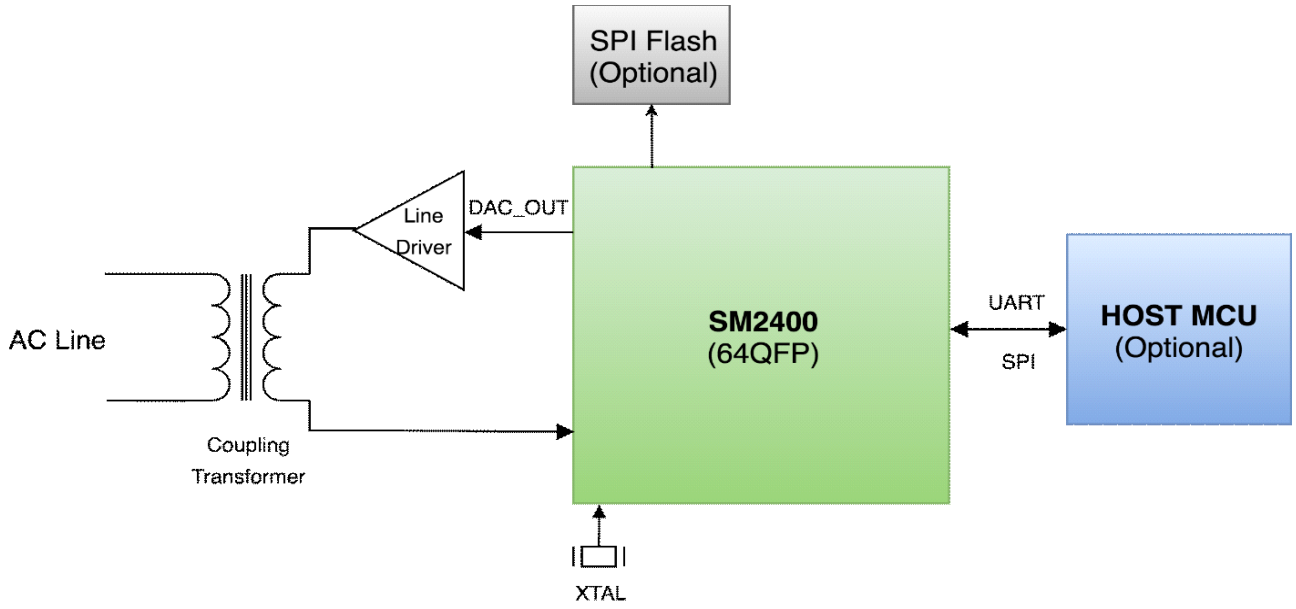
2. System Applications

Typical applications for the SM2400 device include:

- Smart grid communication
- Advanced Metering Infrastructure (AMI)
- Automated Meter Reading (AMR)
- Street lighting control and smart ballasts
- Solar and alternative energy management
- Smart home energy monitoring
- Factory and Building Automation (BA)
- Supervisory Control And Data Acquisition (SCADA)

Figure 2-1 shows a PLC communications module application using the SM2400 device.

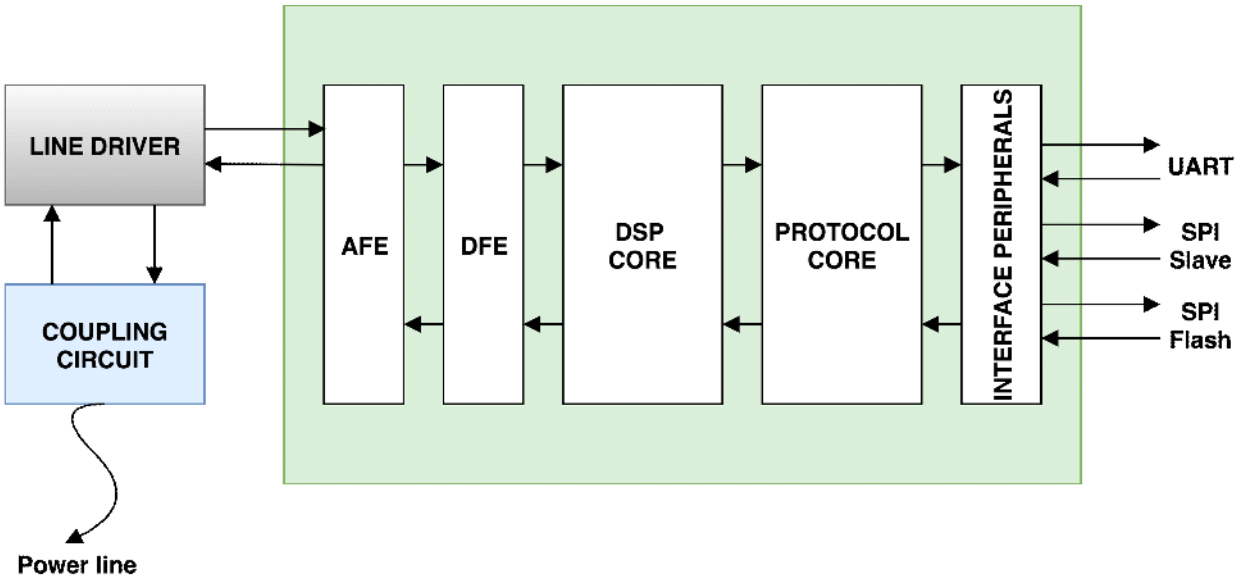
Figure 2-1.PLC Communications Module Application Using the SM2400



3. Block Diagram

Figure 3-1 shows a block diagram of the SM2400 device.

Figure 3-1.SM2400 Block Diagram



3.1 Analog Front-End

The SM2400 integrates an Analog Front-End (AFE) optimized for N-PLC communication. The AFE includes ADC, DAC, PGA and two OpAmp's to achieve the best signal power with minimum external BOM. External components include coupling circuitry and high voltage line driver that can vary for different applications and for different operational bands.

To enable most cost-effective system design, the SM2400 includes an internal voltage regulator. To achieve best power efficiency, external power regulation is recommended.

3.1.1 LDO Voltage Regulator

The LDO voltage regulator integrated in the SM2400 AFE outputs a 1.8V voltage from a 3.3V power supply. It can drive 250mA maximum current load. The output needs external decoupling capacitor to make the regulator stable. A power down signal "LDO_PD" (Pin 56) is used to power on the regulator. When "LDO_PD" is low, the regulator is enabled, and the output is used for the whole chip. When "LDO_PD" is high, a 1.8V external voltage is applied directly and the regulator is bypassed.

3.1.2 Analog to Digital Converter (ADC)

Table 3-1 shows the analog to digital converter specifications for the SM2400 transceiver.

Table 3-1. Analog to Digital Converter Specifications

Parameters	Value
Input	Single Ended
Number of Inputs	1
Sample Rate	Up to 2.5MSPS
Resolution	12 bit

Table 3-1. Analog to Digital Converter Specifications *(continued)*

Parameters	Value
Input Bandwidth	≤ 600 kHz
Input Impedance	> 1kΩ
Input Signal Range	0V ~ AVDD_RX
Supply Voltage	3.0V ~ 3.6V
Standby Power	< 10 µA
INL	0.92 LSB
DNL	0.65 LSB
SNDR	> 70 dB

3.1.3 Digital to Analog Converter (DAC)

Table 3-2 shows the digital to analog converter specifications for the SM2400 transceiver.

Table 3-2. Digital to Analog Converter Specifications

Parameter	Value
Output Bandwidth	1.06 MHz (0 dB)
Output Signal Range	0.3 ~ (AVDD_TX - 0.30) V
Supply Voltage	3.00 ~ 3.60 V
Standby Power	7.5 µA
SNDR	74 dB
INL	< 1.0 LSB
DNL	< 0.5 LSB
Recovery From PD	< 10 µs (No Filter)
Attenuation Range	-21 ~ 0 dB
Attenuation Step	3 dB

3.1.4 Operational Amplifiers (OpAmps)

Table 3-3 shows the operational amplifier specifications for the SM2400 transceiver.

Table 3-3. Operational Amplifier Specifications

Parameter	Value
Open loop gain	> 100,000
Slew rate	23 V/µs
Input Noise (5kHz ~ 1GHz)	8 µV
Phase Margin	68°
Supply Current	0.88 mA

Table 3-3. Operational Amplifier Specifications *(continued)*

Parameter	Value
Power Down Current	< 0.5 µA
Supply voltage	3.0V ~ 3.6V
Output	Rail-to-Rail

3.1.5 Programmable Gain Amplifier (PGA)

Table 3-4 shows the programmable gain amplifier specifications for the SM2400 transceiver.

Table 3-4. Programmable Gain Amplifier Specifications

Parameter	Value
Supply Voltage	3.0 ~ 3.6 V
Standby Current	< 1 µA
Input Voltage Range	Rail-to-Rail
Gain Range	0 ~ 30 dB
Gain Step	3 dB
Output	Rail-to-Rail

3.2 Digital Front-End

The SM2400 integrates a Digital Front End (DFE) which includes dedicated hardware accelerators such as Preamble Detector, Decimation and Interpolation Filtering, Tone cancelers and Zero Crossing Detector to provide performance and flexibility without compromising cost or power.

3.2.1 Preamble Detector

The preamble detector is a specialized circuit to efficiently detect PLC packet preambles without any support from the DSP core. This allows preamble detection while the DSP core is kept in a low-power mode. The preamble detector can be programmed to detect a variety of preamble types including G3-PLC and PRIME 1.3.6 and 1.4.

3.2.2 Decimation and Interpolation Filtering

The DFE includes configurable digital interpolation filters for transmit signal processing and digital decimation filters for receive signals.

3.2.3 Tone Cancelers

The DFE includes a set of tone cancelers to block out narrow band noise interference.

3.2.4 Zero Crossing Detector

The SM2400 includes a zero-crossing input pin which is typically connected to an external zero-crossing detector that generates a pulse signal based on the transition through zero volts of a 50Hz (or 60Hz) sinusoidal on the power line. The SM2400 provides a phase detection feature allowing the transmission to begin at an arbitrary phase offset and measuring the phase offset of the received packet.

3.3 DSP Core

The DSP Core implements the PHY function of the various PLC communication modes and standards. It is fully programmable and is designed specifically to accommodate a variety of OFDM based (and similar) N-PLC PHY's to optimize performance and power consumption. The DSP core is generally not available for customer programming. Some key functions implemented in the DSP core are listed below

3.3.1 Selectable Modes and Modulations

By using different firmware images, the SM2400 can be configured to operate in one of several modes, such as: G3-PLC-FCC, G3-PLC-CENELEC A, PRIME, IEEE 1901.2, XR, XXR, etc. Different modes may imply different operational frequency bands (such as FCC, CEN-A/B/C) with a different number of carriers.

The SM2400 with its OFDM engine allows for configurable modulations per carrier. While in the case of standard based modes of operation (such as. G3-PLC-FCC) the configurations are implied by the standard, the SM2400 offers a number of proprietary modes tunes for best performance or specific application needs. As an example, XXR mode offers unique robustness in the presence noise with relatively low data rates 1-4kbps), while FullBand-PLC mode is similar to G3-PLC, but utilizes the entire 30 - 500 kHz band to achieve much higher bit rates in similar channel conditions.

In general, the following modulations are available: Differential and coherent BPSK, QPSK, 8PSK and coherent 16QAM. From time to time, additional modes are created depending on customer requirements.

Note that using different frequency bands (such as FCC or CENELEC) may require different passive components on the board.

3.3.2 Forward Error Correction (FEC)

The SM2400 supports a number of FEC schemes: Reed-Solomon (255,239) and (255,247); rate half Convolutional coding with constraint length 7 (generator polynomial is [133,171]). In G3 and IEEE 1901.2 modes Convolutional coding is concatenated with RS to achieve the best reliability. As with modulations, special FEC modes that include extra repetition coding for increased robustness and puncturing for increased data rate on capable channels are added from time to time based on customer requirements.

3.3.3 Communication Medium Metrics

The SM2400 provides several metrics to assist L2 and L3 channel adaptation and routing. These metrics are: RSSI, SNR and LQI, which is a measure of the data rate. The RSSI is an estimate of received signal strength. Each packet received can be interrogated for its estimated signal strength. This is very useful to determine the signal to noise ratio of different nodes on the network. It may be that the noise in a particular band is low but the signal is also attenuated significantly making data transmission unreliable. Network management systems can also interrogate each node for signal to noise ratios to create a database of all transmission path conditions. This produces a deterministic way of finding where repeaters are needed in a difficult environment even if they are dynamic.

3.4 Protocol Core

The Protocol Core is designed to implement the MAC and routing functions of the various PLC protocols along with general control functions. It is based on a 32-bit RISC CPU with some customized hardware blocks (e.g. CRC accelerator). The Protocol Core includes dedicated Watchdog timer and high-performance program and data memory.

The Protocol Core includes a dedicates Advanced Encryption Standard (AES) engine which conforms to FIPS 197 standard. It is used for efficiently implement data encryption and authentication protocols. Key sizes of up to 256 bits are supported. The AES engine supports the following modes:

- Electronic Code Book (ECB) encryption
- Cipher Block Chaining (CBC) encryption
- AES Counter with CBC-MAC (CCM*) authenticated encryption

- Counter (CTR) encryption mode

3.5 Interface Peripherals

The SM2400 peripherals are accessed by the system bus. The SM2400 peripherals includes the following:

- UART — Serves as the main host interface
- SPI Slave — Connects to host MCU (alternative to UART)
- SPI Master — Flash and general purpose. Extends to two additional devices that can be used for telemetry or to interface to a wireless transceiver
- Special purpose control signals
- GPIO's
- JTAG

3.5.1 Universal Asynchronous Receiver Transmitter (UART)

The UART interface serves as the main interface to a host, which can be an MCU or a converter, such as serial-to-USB. Apart from two data signals (in and out), the UART interface includes two handshake signals for peripherals that include hardware handshake. These signals are optional.

Table 3-5. UART Specifications

Parameter	Value
Tx FIFO	16 bytes (one byte per entry)
Rx FIFO	16 bytes (one byte per entry)
Baud Rate	300 kbps ~ 1 Mbps
Data Bits	5, 6, 7, 8
Start Bits	1
Stop Bits	1, 1.5, 2
Parity	None, Odd, Even, Sticky
Auto Flow Control	Configurable for Tx and Rx
Break Detection	Yes

3.5.2 Serial Peripheral Interface (SPI) Slave

The SPI slave is used as an alternative to UART to connect to a host MCU. When using the SPI Slave interface, apart from the standard four SPI signals, the SM2400 uses the HOSTREQ signal to interrupt the host whenever data is available.

Table 3-6. SPI Slave Specifications

Parameter	Value
Mode	Slave
Tx FIFO	16 bytes (one byte per entry)
Rx FIFO	16 bytes (one byte per entry)
Data Width	4 ~ 16 bit

Table 3-6. SPI Slave Specifications *(continued)*

Parameter	Value
SCK Freq Max	6 MHz
CPOL	0, 1
CPHA	0, 1
Number of Data Frames	0 ~ 65535 (Allows for automatic reception and transmit)

Table 3-9 lists the SPI slave timing parameters shown in Figure 3-2 and Figure 3-3.

Table 3-7. SPI Slave Interface Timing

Parameter	Description	Min	Max	Units
F_{MCLOCK}	SPI master clock frequency		6	MHz
t_{DS}	Data in setup time	2		ns
t_{DH}	Data in hold time	2		ns
t_V	Data out valid time		7	ns

3.5.3 Serial Peripheral Interface (SPI) Master

The SM2400 supports up to three SPI peripherals which are selected by the SPI Select pins — SS0b, SS1b and SS2b. The SPI boot Flash must be connected to SS0b. The other SPI slave selects (i.e. SS1b and SS2b) are available for customers running their application in the Protocol Core to connect and communicate with other peripherals, such as telemetry sensors or a wireless transceiver.

Table 3-8 shows the SPI Master specifications for the SM2400 transceiver.

Table 3-8. SPI Master Specifications

Parameter	Value
Mode	Dedicated Master (boot flash)
Tx FIFO	16 bytes (one byte per entry)
Rx FIFO	16 bytes (one byte per entry)
Data Width	4 ~ 16 bit
SCK Freq Max	15 MHz
CPOL	0, 1
CPHA	0, 1
Num, Data Frames	0 ~ 65535 (Allows for automatic reception and transmit)

Figure 3-2.SPI Master Bus Timing Diagram — Write Operation

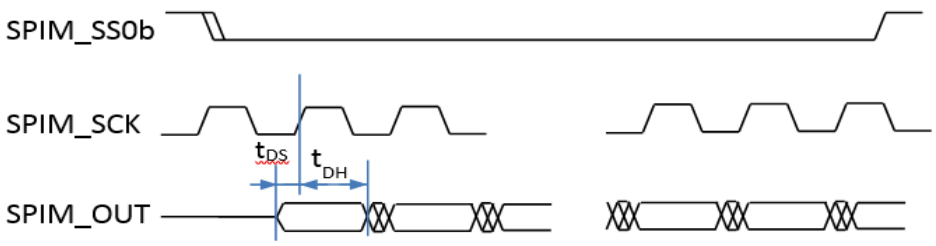


Figure 3-3.SPI Master Bus Timing Diagram — Read Operation

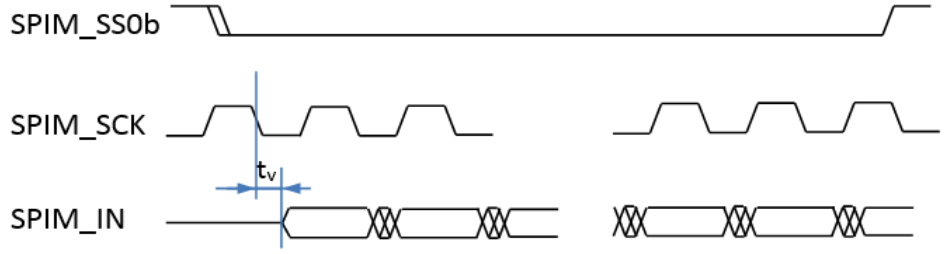


Table 3-9 lists the SPI Master timing parameters shown in Figure 3-2 and Figure 3-3.

Table 3-9. SPI Master Interface Timing

Parameter	Description	Min	Max	Units
F_{MCLOCK}	SPI master clock frequency		15	MHz
t_{DS}	Data in setup time	2		ns
t_{DH}	Data in hold time	2		ns
t_V	Data out valid time		7	ns

3.5.4 Special Purpose Control Signals

There are a number of output signals that are used by the modem firmware to enable specific peripherals, if those are available in the system.

Table 3-10 summarizes the Special Purpose Control signals of the SM2400.

Table 3-10.Special Purpose Control Signals

Signal Name	Description
RXRANGE1	Enables external AGC; -12db when asserted.
PHYLED	Asserted when incoming packet is detected. Can be connected to an LED.
TXEN	Enables external line driver (PA) when transmitting.
AFEEN	Enables the power supply to the external AFE circuit, if available (optional).

Additionally, the SM2400 has a PHYERR input signal that can be used to indicate error conditions, such as over-current or over-heating reported by the line driver.

3.5.5 GPIO's

The SM2400 supports five General Purpose IO's (GPIO's): GPIO0, GPIO9, GPIO12, GPIO13, GPIO14. Those GPIO's are available for use by customer application running on the Protocol Core.

3.5.6 JTAG

JTAG interface for software development. Boundary scan is not supported.

3.6 Crystal Oscillator

The SM2400 device requires an external crystal oscillator that operates in parallel mode of oscillation at its fundamental frequency. The recommended oscillator circuit for the SM2400 is shown in Figure 3-4, the values of the Rd, C1 and C2 are determined by the PCB design and the crystal oscillator properties.

Figure 3-4.Crystal Oscillator Circuit

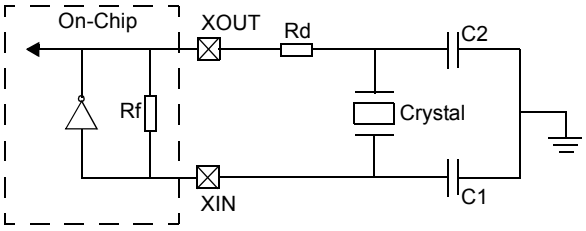


Table 3-11 lists the crystal oscillator AC characteristics.

Table 3-11.Crystal Oscillator AC Characteristics

Parameter	Description	Prime	G3	IEEE	XXR	Units
$XTAL_{TYPE}$	Crystal type	Parallel				
$XTAL_{FREQ}$	Crystal frequency (fundamental)	12,000				MHz
$XTAL_{TOL}$	Frequency total requirement (1)	±50	±25	±25	±25	ppm

1. Including frequency tolerance plus frequency stability plus aging.

Table 3-12 lists the crystal oscillator DC characteristics.

Table 3-12.Crystal Oscillator AC Characteristics

Parameter	Description	Min	Typ	Max	Units
ESR	Equivalent series resistance			150	Ω
C_{XIN}	XTAL_XIN pin capacitance		3		pF
C_{XOUT}	XTAL_XOUT pin capacitance		3		pF

To calculate the input capacitance, the above information can be consolidated into the following formula.

```
CXIN(C1) = CXOUT(C2) = 2 * (CLOAD - CS)
```

In this formula, C_{XIN} and C_{XOUT} are determined by the load capacitance of a crystal and the stray capacitance of the printed circuit board and connections (C_{STRAY}).

The role of Rd in Figure 3-4 is to limit the drive level of the crystal and manufacturers provide different measurement methods to calculate this external resistor but the recommended way of optimizing Rd is to first choose C_{XIN} and C_{XOUT} then connect a potentiometer in the place of the Rd to adjust a value until an acceptable output and crystal drive level are obtained.

4. Boot Options

The SM2400 can be configured to boot in one of four ways using the 3-bit mode control bus.

Boot Mode	MODE[2:0] (1)	Description
SPI Master	000	Boot from SPI Master SSb0 (i.e. external SPI Flash).
CI SPI Slave	001	Boot-loader over SPI interface allows directly download firmware (boot from HOST) or in-system programming of an attached SPI Flash.
CI UART	010	Boot-loader over UART interface allows directly download firmware (boot from HOST) or in-system programming of an attached SPI Flash.
Reserved	011	Reserved.
Reserved	1xx	Reserved.

1. It is recommended that the MODE[2:0] pins are pulled to the desired state via pull-up and/or pull-down resistors rather than tied directly to VDDIO or VSSIO.

5. Power Modes

Table 5-1 shows the typical modes of operation and associated power consumption in milliwatts for the SM2400 when operating in G3-PLC mode. The Listen, Receive, and Transmit modes are the operational modes of the device. The Reset mode indicates that the reset pin has been asserted and the device is booting up.

Table 5-1. Modes of Operation and Associated Power Consumption

Mode	Device Power @1.8V (mW)	Note
Reset	16	Reset pin is asserted, device is to be bootstrapped. PLC communication is disabled in this mode.
Listen	≤ 55	Synchronizer preamble search/detect (waiting for packets).
Receive	≤ 85	Preamble is detected, header and payload being processed.
Transmit	≤ 70	Packet being transmitted.

6. Pinout

The SM2400 is offered in 64-pin package.

6.1 SM2400 Package Pinout

Figure 6-1 shows the package pinout of the SM2400 transceiver.

Figure 6-1.SM2400 Device Package Pinout

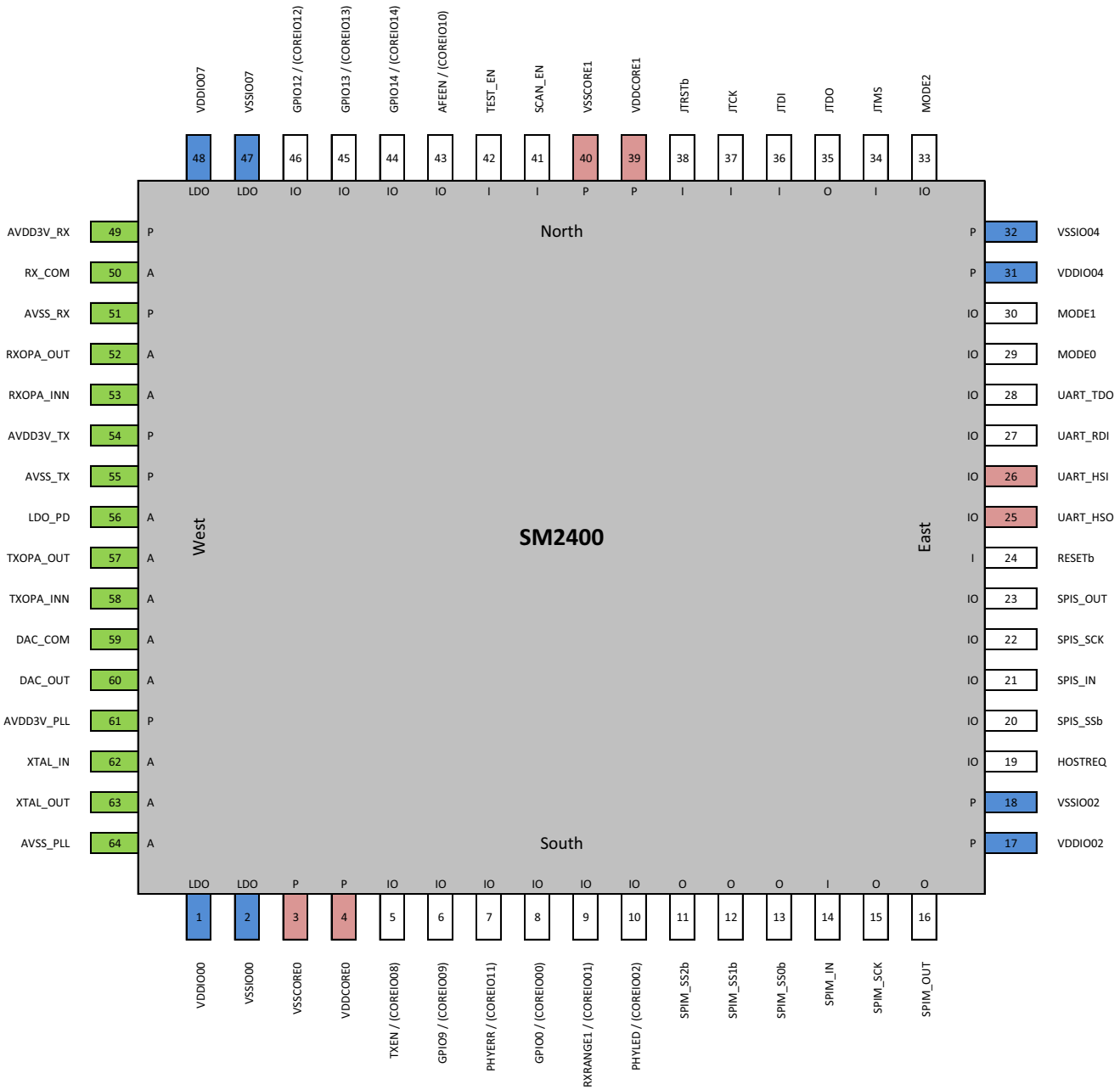


Table 6-1 shows a numerical pin listing for the SM24000 transceiver.

Table 6-1. SM2400 Transceiver Numerical Pin Listing

Pin #	Pin Name	Pin Direction	Pin Description
1	VDDIO00	LDO	VDDIO Supply (3.3V). Note: Recommended power supply with minimum current of 150 mA, if internal 1.8V regulator is used.
2	VSSIO00	LDO	VSSIO (0V). Note: Can be tied to digital ground.
3	VSSCORE0	P	VSSCORE (0V). Note: Can be tied to digital ground.
4	VDDCORE0	P	VDDCORE Supply (1.8V). Note: Minimum current should be 60 mA.
5	TXEN (COREIO08)	O	Enables external line driver (PA) when transmitting.
6	GPIO9 (COREIO09)	IO	GPIO pin available for customer application running on the Protocol Core
7	PHYERR (COREIO11)	O	Asserted (typically by the Line Driver) when and operational error occurs, such as when an over-current or over-heat condition is detected.
8	GPIO0 (COREIO00)	IO	GPIO pin available for customer application running on the Protocol Core
9	RXRANGE1 (COREIO01)	O	External AGC control. -12db when asserted.
10	PHYLED (COREIO02)	O	Asserted when incoming packet is detected.
11	SPIM_SS2b	O	SPI Master Interface (Boot). Hardware slave select pin that works in conjunction with SPIM_SS1b and SPIM_SS0b to provide access to up to three slave devices. One device per pin. Only one device can be active at a time.
12	SPIM_SS1b	O	SPI Master Interface (Boot). Hardware slave select pin that works in conjunction with SPIM_SS2b and SPIM_SS0b to provide access to up to three slave devices. One device per pin. Only one device can be active at a time.
13	SPIM_SS0b	O	SPI Master Interface (Boot). Hardware slave select pin that works in conjunction with SPIM_SS2b and SPIM_SS1b to provide access to up to three slave devices. One device per pin. Only one device can be active at a time.
14	SPIM_IN	I	SPI master interface input data pin.
15	SPIM_SCK	O	SPI master interface clock pin. Supports frequencies up to 15 MHz.

Table 6-1. SM2400 Transceiver Numerical Pin Listing *(continued)*

Pin #	Pin Name	Pin Direction	Pin Description
16	SPIM_OUT	O	SPI master interface output data pin.
17	VDDIO02	P	VDDIO (3.3V)
18	VSSIO02	P	VSSIO (0V)
19	HOSTREQ	IO	Enabled by the firmware using Host SPI Slave Interface. This is an interrupt request to the Host.
20	SPIS_SSb	IO	Host SPI slave interface select. Enabled by the firmware using the Host SPI Slave Interface.
21	SPIS_IN	IO	Host SPI slave interface data in. Enabled by the firmware using the Host SPI Slave Interface.
22	SPIS_SCK	IO	Host SPI slave interface clock. Enabled by the firmware using the Host SPI Slave Interface.
23	SPIS_OUT	IO	Host SPI slave interface data out. Enabled by the firmware using the Host SPI Slave Interface.
24	RESETb	I	System Reset Pin, active low synchronous reset signal with glitch filtering. This pin should be held low until the power rail stabilized and the external oscillator has started. Asserting this pin causes full chip reset and reboot.
25	UART_HSO	IO	Host UART handshake out. Enabled by the firmware using the Host UART Interface.
26	UART_HSI	IO	Host UART handshake in. Enabled by the firmware using the Host UART Interface.
27	UART_RDI	IO	Host UART receive data in. Enabled by the firmware using the Host UART Interface.
28	UART_TDO	IO	Host UART transmit data out. Enabled by the firmware using the Host UART Interface.
29	MODE0	IO	Boot mode pin latched on reset. This pin works in conjunction with the MODE1 and MODE2 pins to select the boot mode as described in Section 4., Boot Options.
30	MODE1	IO	Boot Mode Pin latched on reset. This pin works in conjunction with the MODE0 and MODE2 pins to select the boot mode as described in Section 4., Boot Options.
31	VDDIO04	P	VDDIO (3.3V)

Table 6-1. SM2400 Transceiver Numerical Pin Listing *(continued)*

Pin #	Pin Name	Pin Direction	Pin Description
32	VSSIO04	P	VSSIO (0V)
33	MODE2	IO	Boot Mode Pin latched on reset. This pin works in conjunction with the MODE0 and MODE1 pins to select the boot mode as described in Section 4., Boot Options.
34	JTMS	I	JTAG test mode select pin. This pin is used to determine the JTAG test mode.
35	JTDO	O	JTAG test data out pin.
36	JTDI	I	JTAG test data in pin.
37	JTCK	I	JTAG test clock pin.
38	JTRSTb	I	JTAG test reset pin.
39	VDDCORE1	P	VDDCORE Supply (1.8V)
40	VSSCORE1	P	VSSCORE (0V)
41	SCAN_EN	I	Scan Enable, used for manufacturing test. This pin should be tied low.
42	TEST_EN	I	Test Mode Enable, used for manufacturing test. This pin should be tied low.
43	AFEEN (COREIO10)	O	Enables the power supply to the external AFE circuit, if available (optional).
44	GPIO14 (COREIO14)	IO	I/O pin available for customer application running on the Protocol Core.
45	GPIO13 (COREIO13)	IO	I/O pin available for customer application running on the Protocol Core.
46	GPIO12 (COREIO12)	IO	I/O pin available for customer application running on the Protocol Core. Must be connected to an external Zero Crossing detector circuit if zero crossing detection is required by the firmware.
47	VSSIO07	LDO	VSSIO (0V)
48	VDDIO07	LDO	VDDIO (3.3V)
49	AVDD3V_RX	P	Analog 3.3V power supply, receive.
50	RX_COM	A	Analog 3.3V mid rail bias.
51	AVSS_RX	P	Analog ground, receive.
52	RXOPA_OUT	A	Rx OpAmp output.
53	RXOPA_INN	A	Rx OpAmp inverting input.
54	AVDD3V_TX	P	Analog 3.3V power supply, transmit.
55	AVSS_TX	P	Analog ground, transmit.
56	LDO_PD	A	LDO power down.

Table 6-1. SM2400 Transceiver Numerical Pin Listing *(continued)*

Pin #	Pin Name	Pin Direction	Pin Description
57	TXOPA_OUT	A	Tx OpAmp output
58	TXOPA_INN	A	Tx OpAmp input
59	DAC_COM	A	DAC 3.3V mid-rail bias.
60	DAC_OUT	A	DAC output.
61	AVDD3V_PLL	P	Analog 3.3V power supply, PLL.
62	XTAL_IN	A	Oscillator input. Refer to Section 3.6,
63	XTAL_OUT	A	Oscillator output. Refer to Section 3.6,
64	AVSS_PLL	P	PLL VSS.

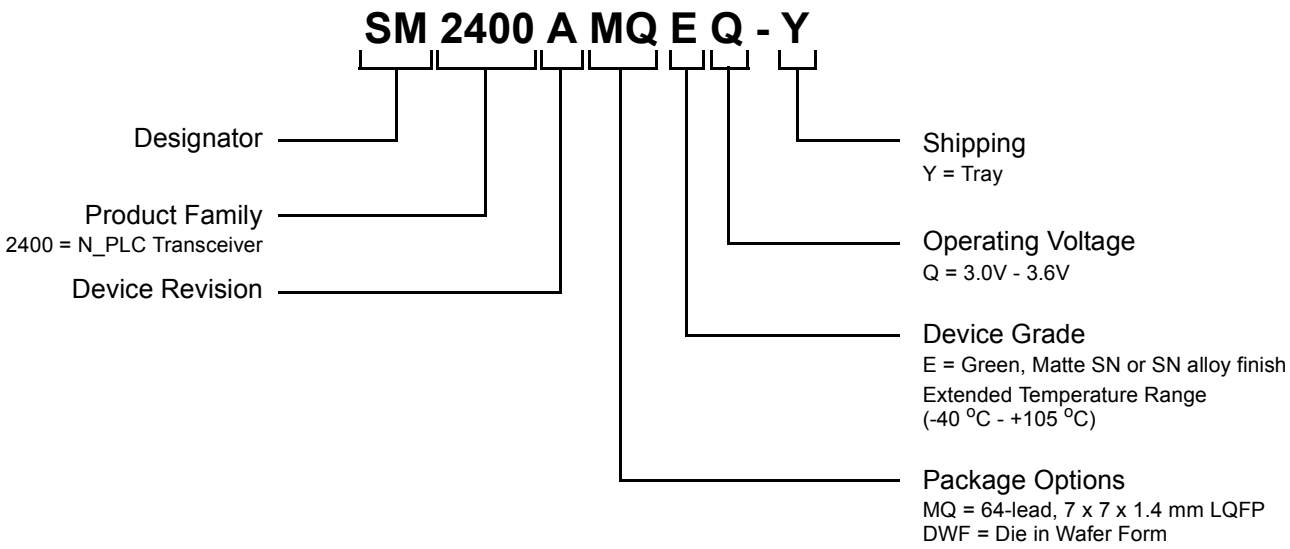
7. DC Characteristics

Table 6-1 shows recommended operating conditions for the SM24000 transceiver.

Table 7-1. Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Units
V_{DDIO}	VDDIO Supply Voltage		3.00	3.30	3.60	V
V_{DDCORE}	VDDCORE Supply Voltage		1.62	1.80	1.98	V
AV_{DD_RX}	Analog Receive Voltage		3.00	3.30	3.60	V
AV_{DD_TX}	Analog Transmit Voltage		3.00	3.30	3.60	V
AV_{DD_PLL}	Analog PLL Voltage		3.00	3.30	3.60	V
AV_{DD_AOUT}	Analog Output Voltage		0.00	3.30	3.60	V
AV_{DD_AIN}	Analog Input Voltage		0.00	3.30	3.60	V
T_{OPT}	Ambient Operating Temperature		-40		+105	°C
T_J	Junction Temperature		0	25	125	ºC
V_{IL}	Input Low Voltage		-0.3		0.8	V
V_{IN}	Input High Voltage		2.0		5.5	V
V_T	Threshold point		1.32	1.38	1.45	V
V_{T+}	Schmitt Trigger Low to High Threshold point		1.48	1.55	1.71	V
V_{T-}	Schmitt Trigger High to Low Threshold point		1.13	1.21	1.27	V
V_{TPU}	Threshold Point with Pull-up Resistor		1.29	1.35	1.41	V
V_{TPD}	Threshold Point with Pull-down Resistor		1.33	1.41	1.48	V
V_{TPU+}	Schmitt Trigger Low to High Threshold Point with Pull-up		1.44	1.51	1.56	V
V_{TPU-}	Schmitt Trigger High to Low Threshold Point with Pull- up		1.11	1.18	1.23	V
V_{TPD+}	Schmitt Trigger Low to High Threshold Point with Pull-down		1.51	1.58	1.64	V
V_{TPD-}	Schmitt Trigger High to Low Threshold Point with Pull-down		1.15	1.23	1.31	V
I_L	Input Leakage Current @ V_I = 3.3V or 0V				±1	µA
I_{OZ}	Tri-state Output Leakage Current @ V_o = 3.3V or 0V				±1	µA
R_{PU}	Pull-up resistor		36	51	75	kΩ
R_{PD}	Pull-down resistor		33	55	102	kΩ
V_{OL}	Output Low Voltage				0.4	V
V_{OH}	Ouput High Voltage		2.4			V
I_{OL}	Low Level Output Current @ VOL(MAX)	12mA	13.7	22.5	31.6	mA
		16mA	17.1	28.1	39.6	mA
I_{OH}	High level output current@ VOH(MAX)	12mA	19.7	38.0	61.7	mA
		16mA	24.1	46.4	75.4	mA

8. Ordering Information

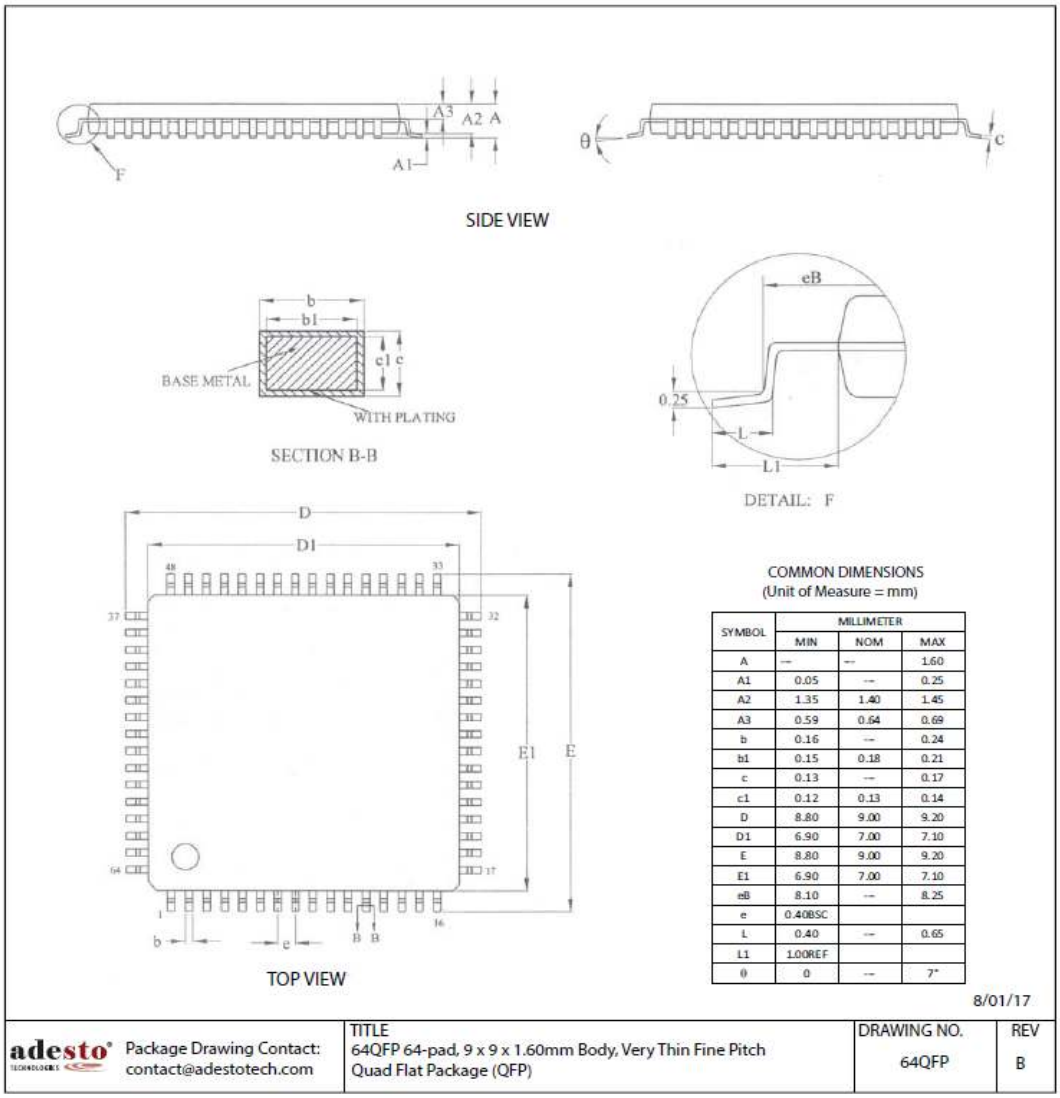


Ordering Code [1]	Package	Lead Finish	Operating Voltage (VDDCore)	Operating Voltage (VDDIO)	Data Rate	Operation Range
SM2400A-MQEQ-Y	64QFP	NnAgCu	1.62V to 1.98V (1.8V nominal)	3.0V to 3.6V (3.3V nominal)	Up to 500 kbps	Industrial (-40°C to +105°C)
SM2400A-DWF [2]	Wafer					

1. The shipping carrier option code is not marked on the device.
2. Contact Adesto for bond diagrams and other ordering information.

Package	Description
64QFP	64-lead, 7 x 7 x 0.1.4mm Body, 0.5 mm Pad Pitch, Very Thin Fine Pitch Quad Flat Package (QFP)
DWF	Die in Wafer Form

9. Packaging Information



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.60
A1	0.05	--	0.25
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.16	--	0.24
b1	0.15	0.18	0.21
c	0.13	--	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	--	8.25
e	0.40BSC		
L	0.40	--	0.65
L1	1.00REF		
θ	0	--	7°

8/01/17

adesto TECHNOLOGIES Package Drawing Contact: contact@adestotech.com	TITLE 64QFP 64-pad, 9 x 9 x 1.60mm Body, Very Thin Fine Pitch Quad Flat Package (QFP)	DRAWING NO. 64QFP	REV B

9.1 Compliance

The SM2400 is designed to be compliant with FCC, Industry Canada, Japan MPT, and CENELEC specification for low voltage signaling (EN50065), as well as with the European Directive 2002/95EC on Restriction of Hazardous Substances (RoHS) in electrical and electronic equipment.

9.2 Contact Information

For more information regarding the SM2400 including technical data sheets, application notes, sample enquiries, demonstration modules, pricing and ordering, please contact:

Adesto Technologies

http://www.adestotech.com

SM2400 Product Technical Support provided by:

Semitech Semiconductor Pty. Ltd.

http://www.semitechsemi.com

10. Glossary of Terms

Table 10-1. Glossary of Terms

Acrynom	Definition		Acrynom	Definition
16QAM	Quadrature Amplitude Modulation		FSK	Frequency Shift Keying
8PSK	High order Phase Shift Keying		GPIO	General Purpose Input/Output
ADC	Analog to Digital Converter		IEEE	Institute of Electrical and Electronics Engineers
AES	Advanced Encryption Standard		JTAG	Joint Test Action Group
AMI	Advanced Metering Infrastructure		LPC	Low Pin Count
AMR	Automatic Meter Reading		LQFP	Low Quad Flat Pack
ARIB	Association of Radio Industries and Businesses		MAC	Media Access Controller
ARQ	Automatic Repeat-Request		MCU	Microcontroller Unit
BA	Building Automation		OFDM	Orthogonal Frequency-Division Multiplexing
BPSK	Binary Phase Shift Keying		PGA	Programmable Gain Amplifier
CBC	Cipher Block Chaining		PHY	Physical layer device
CCM	Counter with CBC MAC		PLC	Power Line Controller
CENELEC	European Committee for Electro-technical Standardization		PLL	Phase Locked Loop
CRC	Cyclic Redundancy Check		QPSK	Quadrature Phase Shift Keying
CTIA	Cellular Telecommunications Industry Association		RAM	Random Access Memory
CTR	Counter mode		RISC	Reduced Instruction Set Computer
DAC	Digital to Analog Converter		ROM	Read Only Memory
DSP	Digital Signal Processor		RSSI	Received Signal Strength Indicator
ECB	Electronic Code Book		SCADA	Supervisor Control and Data Acquisition
FCC	Federal Communications Commission		SNR	Signal to Noise Ratio
FEC	Forward Error Correction		SRAM	Synchronous Random Access Memory
FFT	Fast Fourier Transforms		UART	Universal Asynchronous Receiver Transmitter
FIR	Finite Impulse Response		XOR	Exclusive OR logical function

11. Revision History

Revision Number	Date	Tasks
A	May 1, 2016	Initial release.
B	July 5, 2017	Added DWF package to ordering tables.
C	August 15, 2017	Updated QFT package outline drawing.
D	August 12, 2018	Thorough technical edit of existing material. Added new material or clarified existing material where necessary. Updated Application and Device block diagrams in Sections 2 and 3. Updated pinout drawing in Figure 6-1. Updated AC/DC tables. Updated Pin Descriptions table. Updated Ordering Information diagram in Section 8. Change data sheet status from Advanced to Complete.

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