SM2480

Integrated N-PLC SCADA Controller for Solar Micro-inverters and Smart Ballasts

ADVANCE DATASHEET

Communication technology by: Semitech Semiconductor

Features

- Dual core architecture with custom N-PLC optimized DSP and Data Link Layer 32bit controller
- High speed PWM with 6 channels of outputs with programmable pairing modes and independent settings
- 4 comparators with independent references and programmable fault detection
- 16 channel Signal Monitoring ADC with simultaneous sampling of voltage/current pairs
- High performing custom N-PLC DSP engine with embedded turnkey firmware featuring:
  - Configurable operational band within 5-500KHz range – compliant with CENELEC, FCC and ARIB bands operation
  - OFDM and FSK modulations
  - Compliant with IEEE 1901.2, PRIME, G3-PLC, CTIA/EIA709.2, G.hnem
  - Proprietary operation modes: NOFDM
  - Selectable differential and coherent BPSK, QPSK, 8PSK and coherent 16QAM modulations
  - Configurable data rate up to 500kbps
  - Programmable frequency notching to improve coexistence
  - Jammer cancellation
  - Adaptive tone mapping (on-off sub-band bit loading)
  - FEC – Convolutional, Reed-Salomon and Viterbi coding
  - CRC16
  - Carrier RSSI, SNR and LQI indicators for best channel adaptation and L2/L3 metrics
  - Zero-crossing detector
- Programmable 32bit RISC protocol engine featuring:
  - Data Link Layer firmware options compliant with IEEE 1901.2, G3-PLC, PRIME, IEC61334-4-32 and others
  - Direct access to Signal Monitoring ADC for SCADA algorithms implementation - Solar micro-inverter, Arc detection, LED control, etc.
  - Carrier Sense Multiple Access/Collision Avoidance (CSMA/CA) channel access
  - Automatic Repeat Request (ARQ)
  - Meshing and self discovery mechanisms
- CCM* with AES128 / AES256 encryption core
- On-chip Peripheral Interfaces:
  - UART
  - 5 GPIO's
  - JTAG
  - SPI master for external flash
  - Up to 2 additional SPI slaves for metering, wireless transceiver or other devices
- Seamless interface to an external line driver for optimal system performance:
  - Integrated A/D and D/A
  - Integrated OpAmp's for RX and TX
  - Integrated PGA
- Low power operation modes
  - Offline mode
  - Listen mode
  - Receive mode
  - Transmit mode

- 3.3V (5V tolerant) digital I/O
- Receiver sensitivity of -80dBV
- -40 °C to +105 °C temperature range
- LQFP128 pin package

Benefits

- Single-chip grid connected signal controller ideal for solar inverters, smart lighting ballasts and other SCADA applications reducing cost and simplifying the design
- Flexible high-speed PWM and high precision dual ADC allowing simultaneous sampling of I/V values as well as fast and flexible signal adjustments ideal for power-conversion applications
- Programmable comparator triggered events for fault detection and handling
- High speed, flexible and reliable communication through integrated programmable multi-mode N-PLC modem supporting all common OFDM standards including full compliance with: IEEE 1901.2, G3-PLC, PRIME, G.hnem as well as FSK/S-FSK and proprietary communication schemes
- Low latency communication schemes
- Cost optimized system solution with integrated A/D's, D/A's, OpAmp's, PGA

Overview

The SM2480 is a member of the SM24xx family that expands the SM2400 Narrowband Power Line Communication (N-PLC) modem to a fully integrated Analog Controller with Grid connectivity. It is specifically targeted for applications such as solar panel micro-inverters, smart LED controllers and other Grid-connected devices. For easy and cost effective system design the SM2480 combines N-PLC connectivity with analog signal monitoring and control required by such applications. As all the members of the SM24xx family, the SM2480 features a dual core architecture, dedicating one core to the system control application and a second core to guarantee superior communication performance, while maintaining flexibility and programmability for OFDM based standards and proprietary communication schemes. Both cores are supported by full development systems to facilitate implementation of proprietary application specific control and monitoring algorithms.

Applications

- Solar micro-inverters and alternative energy management
- Smart lighting control
- Building automation (BA)
- SCADA (Supervisory Control And Data Acquisition)

Figure 0-1. SM2480 N-PLC SCADA Controller

1. Description

The SM2480 is single chip "grid connected" that combines the most advanced N-PLC connectivity with high speed PWM control logic and featuring extensive computational power to enable complete and flexible implementation of solar-microinverter, Arc detection, LED control and similar algorithms. The SM2480 combines the benefits of programmable architecture with power and cost efficiency by utilizing two 32bit cores designed specifically for N-PLC modulations, voltage/current signal monitoring and M2M protocols.

To efficiently address applications, such as solar micro-inverters, the SM2480 features a high speed flexible PWM controller with individually programmable 8 pairs of outputs with independent timing, and a number of analog interfaces that include 16 12-bit ADC channels and 4 comparators for high speed monitoring of I/V and other sensors.

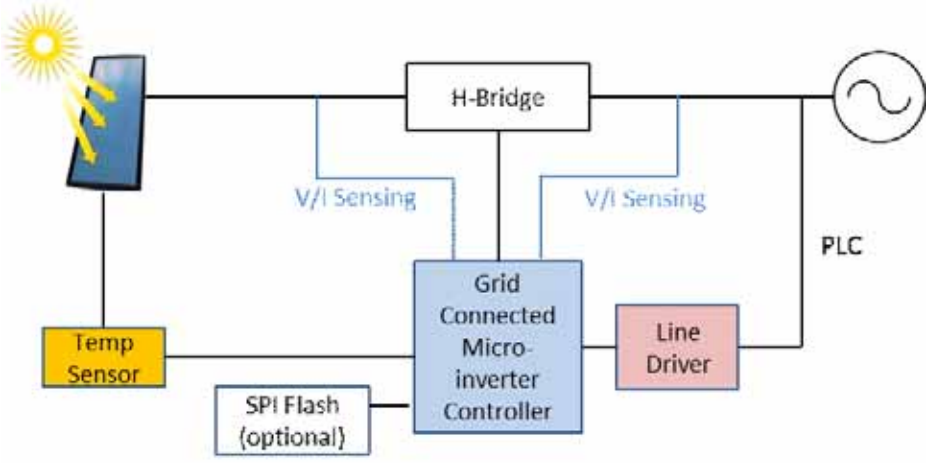
As a member of the SM24xx family the SM2480 features programmable OFDM based N-PLC modem including PHY, MAC and AFE featuring ADC, DAC, gain control and two OpAmp's for optimal system cost and performance.

The SM2480 comes with a number of firmware versions implementing various N-PLC schemes, such as IEEE 1901.2, PRIME, G3-PLC, and other special modes tailored for SCADA and smart grid applications.

The SM2480 enables secure communication with its 256-bit AES encryption core with CCM* mode support.

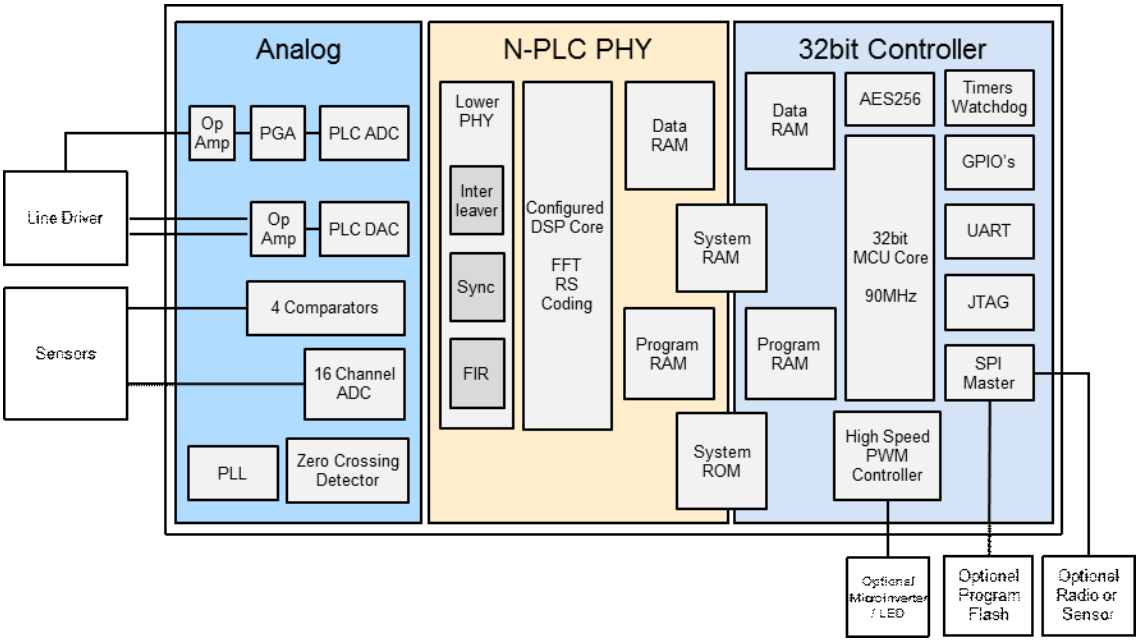
2. Typical Application Diagram

Figure 2-1. SM2480 Based Grid Connected Solar Micro-inverter



3. Block Diagram

Figure 3-1. SM2480 Block Diagram



4. Signal Control

Additionally to its high computational and DSP performance, the SM2480 integrates advanced features necessary for implementing a complete analog control system. Those include High Speed PWM, Monitoring ADC, DAC and 4 analog comparators as well as triggering logic for fast fault detection.

4.1 High Speed PWM

The high speed PWM is designed to control analog peripherals with high short response time and high degree of accuracy such as power inverters and LED lighting.

- 6 PWM channels
- Each PWM channel consists of PWMLx and PWMHx pins programmable to any of the following modes:
  - Complementary
  - Mirrored
  - Dual Duty Cycle
  - Pulsed
- PWMLx and PWMHx instant output pin swapping
- Chopper clock with conditional gating by the PWMH/PWML pins
- External reset mode to support terminating (short cycling) the current PWM cycle in two modes;
  - Constant period
  - Variable period
- Accuracy of up to T=11.1ns (1/90MHz)
- Individual and independent parameter setting for each output:
  - Duty cycle
  - Dead time
  - Phase offset

- Period
- Two “Group Settings” allowing to manipulate multiple grouped outputs simultaneously (via a single configuration instruction) to trigger simultaneous changes in PWM frequency, duty cycle, and phase shift
- New setting can be applied immediately or at the end of the current period via configuration option
- Individual and independent fault and current-limit inputs selectable either from a comparator or an external source
- Two triggers per PWM period (falling and rising edges) from PWM to ADC to initiate sampling at T resolution with 8bit programmable leading edge blanking.

4.2 Signal Monitoring Dual ADC

Signal monitoring is possible using the Simultaneous Sampling Dual ADC which is designed to sample a multitude of sensors and in particular simultaneously sample current-voltage pairs.

Input	Single Ended
Architecture	SAR
Number of Inputs	1
Sample Rate	Up to 1.0 MSPS
Resolution	12 bits
Input Impedance	>kΩ
Input Setting Tiime	< 1 µs
Operational Power	≤ 1.86 mA
Supply Voltage	3.0 ~ 3.6 V
Standby Power	<10 µA
INL	0.92 LSB
DNL	0.65 LSB
SNDR	>70 dB

Conversions can be independently triggered by the PWM module or by a timer.

Configurable simultaneous or independent modes are supported.

Each channel has its own data output buffer plus each ADC has a FIFO for burst acquisitions.

4.3 Timer Capture

Three timer capture modules are available for mains synchronisation and detection.

Time Base	11.1ns
Prescaler	8 bit
Resolution	16 bit
Capture Modes	Rising → Rising Falling → Falling

4.4 Analog Comparators & DAC's

The SM2480 incorporates four high-speed analog comparators with individual reference DAC's and individual multi-level hysteresis control.

Comparators	
Output	Single Ended
Input Voltage Range	0 ~ AVDD_AIN
Input Offset	≤ 5 mV
Output Delay	≤ 20 ns
Output Voltage Range	0 ~ AVDD_AIN
Supply Voltage	3.0 ~ 3.6 V
Operational Power	< 100 µA
Standby Power	< 1 µA
RDAC Resolution	10 bits
External RDAC Reference	Yes (AOUT_REF)

DAC's	
Output	Single Ended
Number of Inputs	1
Resolution	10 bits
External Reference	Yes (AOUT_REF)
Reference Voltage	1V ~ AVDD_AOUT
Output Signal Range	0V ~ AOUT_REF
INL	0.88 LSB Max
DNL	0.22 LSB Max
Gain Error	< 0.1 LSB
Operational Power	< 100 µA
Supply Voltage	3.0 ~ 3.6 V
Standby Power	< 1 µA

5. N-PLC MODEM

Both the SM2400 and the SM2480 support all common N-PLC standards in addition to several proprietary modes of operation. This enables maximum flexibility to the designer in implementing closed or grid connected SCADA systems utilizing analog control functions.

5.1 Selectable Modes and Modulations

The SM2480 can be configured to operate in one of several modes, such as: 1901.2, G3-PLC, PRIME, ITU1901/2, G.hnem, S-FSK, Lon, NOFDM, etc. Different modes require different firmware images and imply different operational frequency bands with a varying number of carriers.

The SM2480 allows for configurable modulations per carrier. While most configurations are implied by the different standards, special modes can be created using specific combinations of carriers and modulations to achieve best performance in given channel conditions. The following modulations are available: Differential and coherent BPSK, QPSK and 8PSK and coherent 16QAM.

5.2 Forward Error Correction

The SM2480 supports Reed-Solomon (255,239) and (255,247), and rate half Convolutional coding with constraint length 7 (generator polynomial is [133,171]). In G3 and IEEE modes Convolutional coding is concatenated with RS to achieve the best reliability. Special error correction modes include extra repetition coding for increased robustness and puncturing for increased data rate on capable channels.

5.3 Communication Medium Metrics

The SM2480 provides several metrics to assist L2 and L3 channel adaptation and routing. These metrics are: RSSI, SNR and LQI, which is a measure of the data rate. The RSSI is an estimate of received signal strength. Each packet received can be interrogated for its estimated signal strength. This is very useful to determine the signal to noise ratio of different nodes on the network. It may be that the noise in a particular band is low but the signal is also attenuated significantly making data transmission unreliable. Network management systems can also interrogate each node for signal to noise ratios to create a database of all transmission path conditions. This produces a deterministic way of finding where repeaters are needed in a difficult environment even if they are dynamic.

5.4 Security

AES encryption engine conforms to FIPS 197 standard featuring CCM*, ECB, CBC, CTR modes and of up to 256 bit key size.

5.5 Zero-crossing Detector

The SM2480 has a zero-crossing input pin which takes signals generated by an external zero-crossing detector based on the transition through zero volts of a 50Hz (or 60Hz) sinusoidal on the power line. The SM2480 provides a phase detection feature allowing the transmission beginning at an arbitrary phase offset and measuring the phase offset of the received packet.

6. Analog Front End (AFE)

The SM2480 integrates an AFE optimized for N-PLC communication, which includes ADC, DAC, PGA and 2 OpAmp's to achieve the best signal power with minimum external BOM. External components include coupling circuitry and high voltage line driver that can vary for different applications and for different operational bands.

Table 6-1. ADC

ADC	
Input	Single Ended
Number of Inputs	1
Sample Rate	Up to 2.5MSPS
Resolution	12 bit

ADC	
Input Bandwidth	≤ 600 kHz
Input Impedance	> 1kΩ
Input Signal Range	0V ~ AVDD_RX
Supply Voltage	3.0V ~ 3.6V
Standby Power	< 10 µA
INL	0.92 LSB
DNL	0.65 LSB
SNDR	> 70 dB

Table 6-2. Main DAC

DAC	
Output Bandwidth	1.06 MHz (0 dB)
Signal Range	0.3 ~ (AVDD_TX - 0.30) V
Supply Voltage	3.00 ~ 3.60 V
Standby Power	7.5 µA
SNDR	74 dB
INL	< 1.0 LSB
DNL	< 0.5 LSB
Recovery From PD	< 10 µs (No Filter)
Attenuation Range	-21 ~ 0 dB
Attenuation Step	3 dB

Table 6-3. OpAmps

OpAmps	
Open loop gain	> 100,000
Slew rate	23 V/µs
GBP (Gain Bandwidth Product)	101 MHz
Input Noise (5kHz ~ 1GHz)	8 µV
Phase Margin	68°
Supply Current	0.88 mA

OpAmps	
Power Down Current	< 0.5 µA
Supply voltage	3.0V ~ 3.6V
Output	Rail-to-Rail

Table 6-4. PGA

PGA	
Supply Voltage	3.0 ~ 3.6 V
Standby Current	< 1µA
Input Voltage Range	Rail-to-Rail
Gain Range	0 ~ 30 dB
Gain Step	3 dB
Output	Rail-to-Rail

7. Peripheral Interfaces

The *SM2480* includes several peripheral interfaces for adding optional components. Those interfaces include UART, SPI master for external flash interface and JTAG. The second SPI extends to two additional devices that can be used for telemetry or to interface to a wireless transceiver.

Table 7-1. UART

UART	
TX Fifo	Yes
RX Fifo	Yes
Baud Rate	300 ~ 1Mbps
Data Bits	5, 6, 7, 8
Start Bits	1
Stop Bits	1, 1.5, 2
Parity	None, Odd, Even, Sticky
Auto Flow Control	Configurable for Tx & Rx
Break Detection	Yes

Table 7-2. SPI0

SPI0	
Mode	Dedicated Master (boot flash)
TX Fifo	Yes
RX Fifo	Yes
Data Width	4 ~ 16 bit
SCK Freq	Max15MHz
CPOL	0, 1
CPHA	0, 1
Num, Data Frames	0~ 65376 (Allows for automatic reception and transmit)

Table 7-3. SPI1

SPIS	
Mode	Slave
TX Fifo	Yes
RX Fifo	Yes
Data Width	4 ~ 16 bit
SCK Freq Max	6MHz
CPOL	0, 1
CPHA	0, 1
Num, Data Frames	0~ 65376 (Allows for automatic reception and transmit)

Table 7-4. JTAG

JTAG
JTAG interface for software development.

8. Boot Options

The SM2480 can be configured to boot in one of four ways:

Table 8-1. Boot Options

Boot Mode	MODE[2:0] (1)	Description
SPI Master	"000"	Read and process valid bootsector from SPI Master SSb0
CI SPI Slave	"001"	Wait on Command Interface via SPI Slave
CI UART	"010"	Wait on Command Interface via UART
Parallel Memory	"011"	Read and process valid bootsector from Parallel Memory
Reserved	"1xx"	Reserved

1. It is recommended that the MODE[2:0] pins are pulled to the desired state via pull-up and/or pull-down resistors rather than tied directly to VDDIO or VSSIO.

9. Pinout

The SM2480 is offered in a 128pin LQFP package.

Figure 9-1. SM2480 - 128 pin configuration

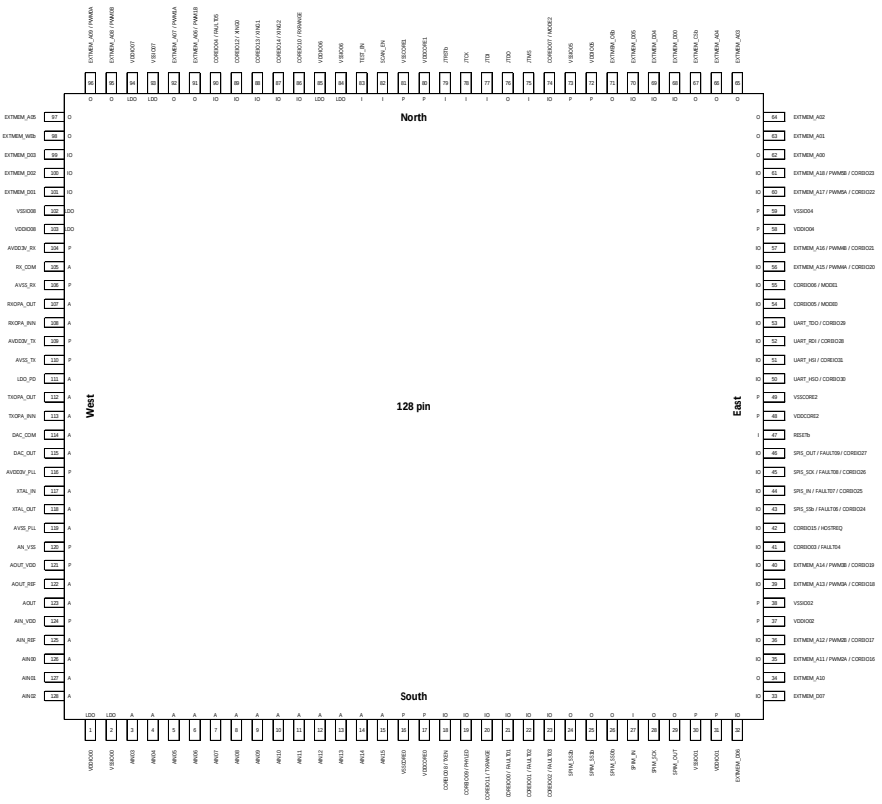


Table 9-1. Pin Assignments

Pin #	Pin Name	Pin Type	Description
1	VDDIO00	LDO	VDDIO Suplpy (3.3V)
2	VSSIO00	LDO	VSSIO (0V)
3	AIN03	A	ADC Input
4	AIN04	A	ADC Input
5	AIN05	A	ADC Input
6	AIN06	A	ADC Input
7	AIN07	A	ADC Input
8	AIN08	A	ADC Input
9	AIN09	A	ADC Input
10	AIN10	A	ADC Input
11	AIN11	A	ADC Input
12	AIN12	A	ADC Input
13	AIN13	A	ADC Input
14	AIN14	A	ADC Input
15	AIN15	A	ADC Input
16	VSSCORE0	P	VSSCORE (0V)
17	VDDCORE0	P	VDDCORE Supply (1.8V)
18	COREIO08 / TXEN	IO	Firmware defined functionality
19	COREIO09 / PHYLED	IO	Firmware defined functionality
20	COREIO11 / TXRANGE	IO	Firmware defined functionality
21	COREIO00 / FAULT01	IO	User IO
22	COREIO01 / FAULT02	IO	User IO
23	COREIO02 / FAULT03	IO	User IO
24	SPIM_SS2b	O	SPI Master Interface (Boot)
25	SPIM_SS1b	O	SPI Master Interface (Boot)
26	SPIM_SS0b	O	SPI Master Interface (Boot)
27	SPIM_IN	I	SPI Master Interface (Boot)
28	SPIM_SCK	O	SPI Master Interface (Boot)
29	SPIM_OUT	O	SPI Master Interface (Boot)
30	VSSIO01	P	VSSIO (0V)
31	VDDIO01	P	VDDIO (3.3V)
32	EXTMEM_D06	IO	Dedicated external memory interface pins

33	EXTMEM_D07	IO	Dedicated external memory interface pins
34	EXTMEM_A10	O	Dedicated external memory interface pins
35	EXTMEM_A11 / PWM2A / COREIO16	IO	PWM interface
36	EXTMEM_A12 / PWM2B / COREIO17	IO	PWM interface
37	VDDIO02	P	VDDIO (3.3V)
38	VSSIO02	P	VSSIO (0V)
39	EXTMEM_A13 / PWM3A / COREIO18	IO	PWM interface
40	EXTMEM_A14 / PWM3B / COREIO19	IO	PWM interface
41	COREIO03 / FAULT04	IO	User IO
42	COREIO15 / HOSTREQ	IO	Firmware defined functionality
43	SPIS_SSb / FAULT06 / COREIO24	IO	Host SPI Slave Interface
44	SPIS_IN / FAULT07 / COREIO25	IO	Host SPI Slave Interface
45	SPIS_SCK / FAULT08 / COREIO26	IO	Host SPI Slave Interface
46	SPIS_OUT / FAULT09 / COREIO27	IO	Host SPI Slave Interface
47	RESETb	I	System Reset Pin
48	VDDCORE2	P	VDDCORE Supply (1.8V)
49	VSSCORE2	P	VSSCORE (0V)
50	UART_HSO / COREIO30	IO	Host UART Interface
51	UART_HSI / COREIO31	IO	Host UART Interface
52	UART_RDI / COREIO28	IO	Host UART Interface
53	UART_TDO / COREIO29	IO	Host UART Interface
54	COREIO05 / MODE0	IO	Boot Mode Pin latched on reset
55	COREIO06 / MODE1	IO	Boot Mode Pin latched on reset
56	EXTMEM_A15 / PWM4A / COREIO20	IO	PWM interface
57	EXTMEM_A16 / PWM4B / COREIO21	IO	PWM interface
58	VDDIO04	P	VDDIO (3.3V)
59	VSSIO04	P	VSSIO (0V)

60	EXTMEM_A17 / PWM5A / COREIO22	IO	PWM interface
61	EXTMEM_A18 / PWM5B / COREIO23	IO	PWM interface
62	EXTMEM_A00	O	Dedicated external memory interface pins
63	EXTMEM_A01	O	Dedicated external memory interface pins
64	EXTMEM_A02	O	Dedicated external memory interface pins
65	EXTMEM_A03	O	Dedicated external memory interface pins
66	EXTMEM_A04	O	Dedicated external memory interface pins
67	EXTMEM_CSb	O	Dedicated external memory interface pins
68	EXTMEM_D00	IO	Dedicated external memory interface pins
69	EXTMEM_D04	IO	Dedicated external memory interface pins
70	EXTMEM_D05	IO	Dedicated external memory interface pins
71	EXTMEM_Oeb	O	Dedicated external memory interface pins
72	VDDIO05	P	VDDIO (3.3V)
73	VSSIO05	P	VSSIO (0V)
74	COREIO07 / MODE2	IO	Boot Mode Pin latched on reset
75	JTMS	I	JTAG Interface
76	JTDO	O	JTAG Interface
77	JTDI	I	JTAG Interface
78	JTCK	I	JTAG Interface
79	JTRSTb	I	JTAG Interface
80	VDDCORE1	P	VDDCORE Supply (1.8V)
81	VSSCORE1	P	VSSCORE (0V)
82	SCAN_EN	I	Scan Enable
83	TEST_EN	I	Test Mode Enable
84	VSSIO06	LDO	VSSIO (0V)
85	VDDIO06	LDO	VDDIO (3.3V)
86	COREIO10 / RXRANGE	IO	Firmware defined functionality

87	COREIO14 / XING2	IO	Firmware defined functionality
88	COREIO13 / XING1	IO	Firmware defined functionality
89	COREIO12 / XING0	IO	Firmware defined functionality
90	COREIO04 / FAULT05	IO	User IO
91	EXTMEM_A06 / PWM1B	O	PWM interface
92	EXTMEM_A07 / PWM1A	O	PWM interface
93	VSSIO07	LDO	VSSIO (0V)
94	VDDIO07	LDO	VDDIO (3.3V)
95	EXTMEM_A08 / PWM0B	O	PWM interface
96	EXTMEM_A09 / PWM0A	O	PWM interface
97	EXTMEM_A05	O	Dedicated external memory interface pins
98	EXTMEM_Web	O	Dedicated external memory interface pins
99	EXTMEM_D03	IO	Dedicated external memory interface pins
100	EXTMEM_D02	IO	Dedicated external memory interface pins
101	EXTMEM_D01	IO	Dedicated external memory interface pins
102	VSSIO08	LDO	VSSIO (0V)
103	VDDIO08	LDO	VDDIO (3.3V)
104	AVDD3V_RX	P	PLC Interface
105	RX_COM	A	PLC Analog
106	AVSS_RX	P	PLC Interface
107	RXOPA_OUT	A	PLC Analog
108	RXOPA_INN	A	PLC Analog
109	AVDD3V_TX	P	PLC Interface
110	AVSS_TX	P	PLC Interface
111	LDO_PD	A	LDO powerdown
112	TXOPA_OUT	A	PLC Interface
113	TXOPA_INN	A	PLC Interface
114	DAC_COM	A	PLC Interface
115	DAC_OUT	A	PLC Interface
116	AVDD3V_PLL	P	PLL VDD
117	XTAL_IN	A	Oscillator Input
118	XTAL_OUT	A	Oscillator Output

119	AVSS_PLL	A	PLL VSS
120	AN_VSS	P	ADC/DAC VSS
121	AOUT_VDD	P	DAC VDD
122	AOUT_REF	A	DAC Reference
123	AOUT	A	DAC Output
124	AIN_VDD	P	ADC VDD
125	AIN_REF	A	ADC Reference
126	AIN00	A	ADC Input
127	AIN01	A	ADC Input
128	AIN02	A	ADC Input

10. Operating Conditions

Table 10-1. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DDIO}	VDDIO Supply Voltage	3	3.3	3.6	V
V_{DDCORE}	VDDCORE Supply Voltage	1.62	1.8	1.98	V
AV_{DD_RX}		3	3.3	3.6	V
AV_{DD_TX}		3	3.3	3.6	V
AV_{DD_PLL}		3	3.3	3.6	V
AV_{DD_AOUT}		0	3.3	3.6	V
AV_{DD_AIN}		0	3.3	3.6	V
T_{OPT}	Ambient Operating Temperature	-40		105	°C
T_J	Junction Temperature	0	25	125	ºC
V_{IL}	Input Low Voltage	-0.3		0.8	V
V_{IN}	Input High Voltage	2		5.5	V
V_T	Threshold point	1.32	1.38	1.45	V
V_T^+	Schmitt Trigger Low to High Threshold point	1.48	1.55	1.71	V
V_T^-	Schmitt Trigger High to Low Threshold point	1.13	1.21	1.27	V

Symbol	Parameter		Min	Typ	Max	Units
V_{TPU}	Threshold Point with Pull-up Resistor		1.29	1.35	1.41	V
V_{TPD}	Threshold Point with Pull-down Resistor		1.33	1.41	1.48	V
V_{TPU+}	Schmitt Trigger Low to High Threshold Point with Pull-up		1.44	1.51	1.56	V
V_{TPU-}	Schmitt Trigger High to Low Threshold Point with Pull- up		1.11	1.18	1.23	V
V_{TPD+}	Schmitt Trigger Low to High Threshold Point with Pull-down		1.51	1.58	1.64	V
V_{TPD-}	Schmitt Trigger High to Low Threshold Point with Pull-down		1.15	1.23	1.31	V
I_L	Input Leakage Current @ V_I = 3.3V or 0V				±1	µA
I_{OZ}	Tri-state Output Leakage Current @ V_o = 3.3V or 0V				±1	µA
R_{PU}	Pull-up resistor		36	51	75	kΩ
R_{PD}	Pull-down resistor		33	55	102	kΩ
V_{OL}					0.4	V
V_{OH}			2.4			V
I_{OL}	Low Level Output Current @ $V_{OL(MAX)}$	12mA	13.7	22.5	31.6	mA
		16mA	17.1	28.1	39.6	mA
I_{OH}	High level output current@ $V_{OH(MAX)}$	12mA	19.7	38	61.7	mA
		16mA	24.1	46.4	75.4	mA

11. Power Usage

Table 11-1. Power Usage Specifications

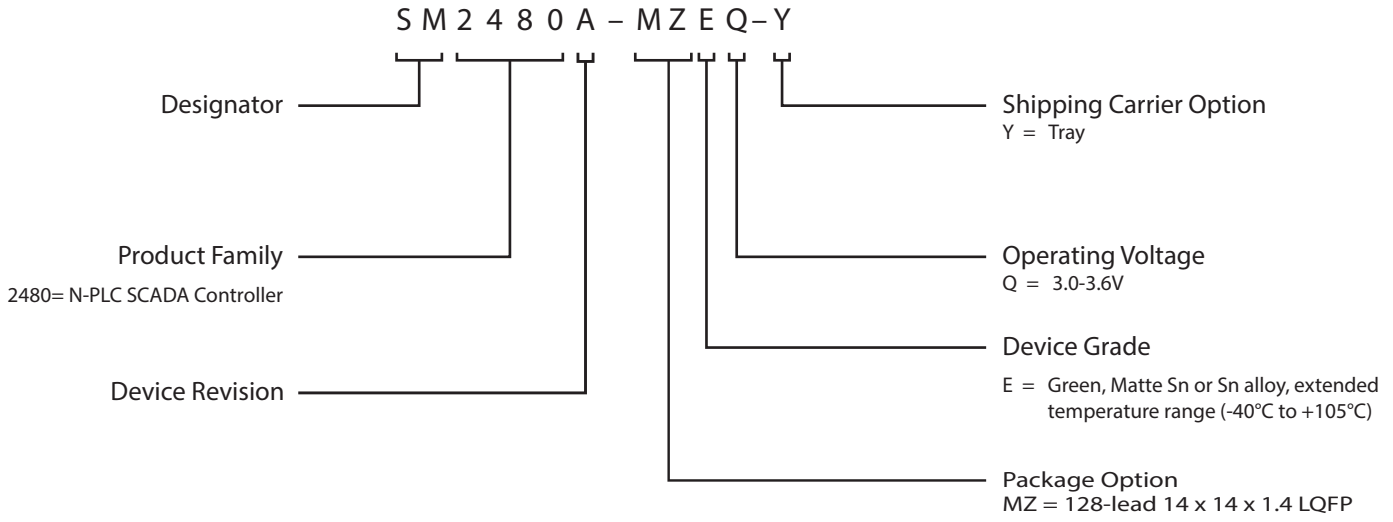
Mode	Device Power @1.8V (mW)	Note
Reset	16	Reset pin is asserted, device is to be bootstrapped, no comms.
Offline	22	Bootstrapped, but disabled, fast recovery, no comms.

Mode	Device Power @1.8V (mW)	Note
Listen	≤ 55*	Synchroniser preamble search/detect; PWM is active
Receive	≤ 85*	Preamble is detected, header and pay-load being processed
Transmit	≤ 70*	Packet being transmitted.

* Close estimate. The actual numbers may vary depending on the tracking/control algorithm(s) running

12. Ordering Information

12.1 Ordering Code Detail



Ordering Code [1]	Package	Lead Finish	Operating Voltage (VDDCore)	Operating Voltage (VDDIO)	Data Rate	Operation Range
SM2480-MZEQ-T	128QFP	SnAgCu	1.62V to 1.98V (1.8V nominal)	3.0V to 3.6V (3.3 nominal)	Up to 500kbps	Extended Industrial (-40°C to +105°C)
SM2480-MZEQ-Y	128QFP					

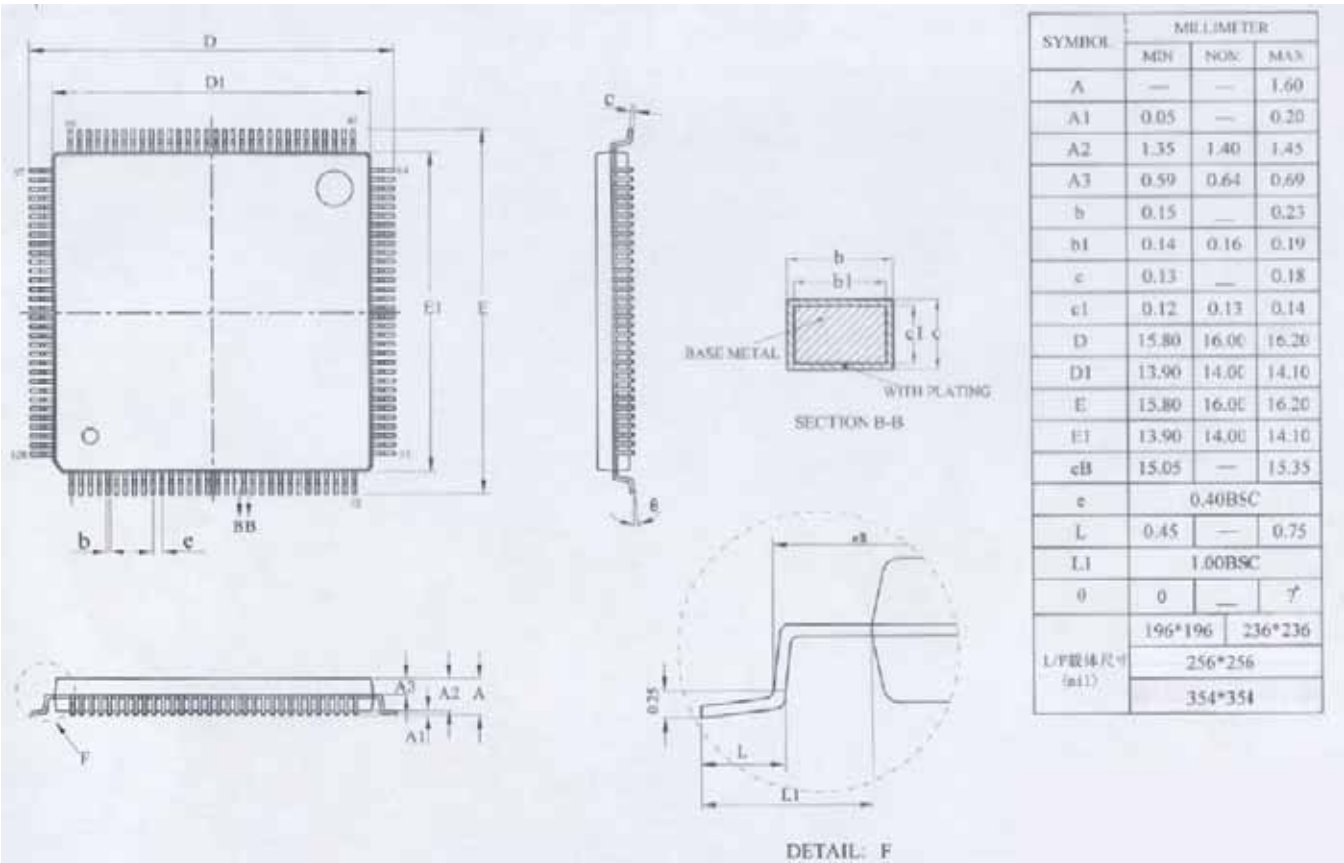
1. The shipping carrier option code is not marked on the device.

Package Type	
128QFP	128-lead, 14 x 14 x 0.1.4mm Body, 0.5 mm Pad Pitch, Very Thin Fine Pitch Quad Flat Package (QFP)

Compliance: SM2480 is designed to be compliant with FCC, Industry Canada, Japan MPT, and CENELEC specification for low voltage signaling (EN50065). SM2480 is designed to be compliant with European Directive 2002/95EC on Restriction of Hazardous Substances (RoHS) in electrical and electronic equipment.

13. Packaging Information

Figure 13-1. 128QFP - 128 lead QFP



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.20
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.15	—	0.23
b1	0.14	0.16	0.19
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
cB	15.05	—	15.35
e	0.40BSC		
L	0.45	—	0.75
L1	1.00BSC		
θ	0	—	7°
L/F最体尺寸 (mil)	196*196		236*236
	256*256		
	354*354		

14. Contact Information

For more information regarding the SM2480 including application notes, product samples, demonstration modules, pricing and ordering please contact:

Adesto Technologies
http://www.adestotech.com

SM2480 Product Technical Support provided by:
Semitech Semiconductor Pty. Ltd.
http://www.semitechsemi.com

15. Revision History

Revision Level – Release Date	History
A – June 2016	Initial release.

Corporate Office

California | USA
Adesto Headquarters
1250 Borregas Avenue
Sunnyvale, CA 94089
Phone: (+1) 408.400.0578
Email: contact@adestotech.com