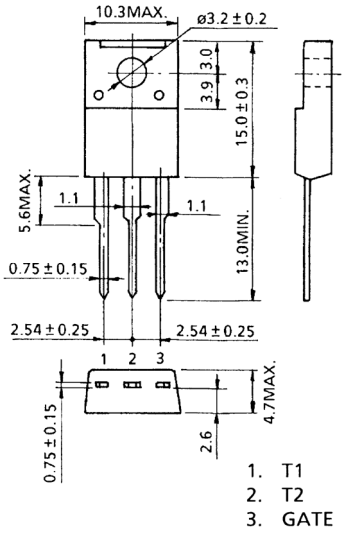
TOSHIBA BI−DIRECTIONAL TRIODE THYRISTOR SILICON PLANAR TYPE

SM2GZ47, SM2GZ47A, SM2JZ47, SM2JZ47A

AC POWER CONTROL APPLICATIONS

- $I_{T\ (RMS)}$ = 1A (Ta = 65°C without radiator)
- Gate Trigger Current: I_{GT} = 5mA Max. (TYPE "A")
- Repetitive Peak Off−State Voltage: V_{DRM} = 400V, 600V
- R.M.S On−State Current: $I_{T\ (RMS)}$ = 2A (Tc = 110°C)
- Isolation Voltage: V_{ISOL} = 1500V (AC, t = 60s)

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	13-10H1A

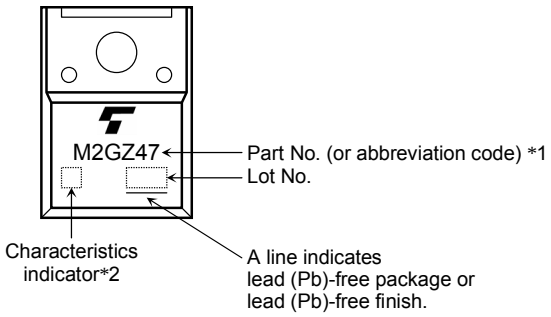
Weight: 1.7 g (typ.)

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC		SYMBOL	RATING	UNIT
Repetitive Peak Off−State Voltage and Repetitive Peak Reverse Voltage	SM2GZ47 SM2GZ47A	V_{DRM}	400	V
	SM2JZ47 SM2JZ47A		600	
R.M.S On−State Current (Full Sine Waveform)	Tc = 110°C	$I_{T\ (RMS)}$	2	A
	Ta = 65°C		1	
Peak One Cycle Surge On−State Current (Non−Repetitive)		I_{TSM}	8 (50Hz)	A
			8.8 (60Hz)	
I2t Limit Value		I2t	0.32	A2s
Peak Gate Power Dissipation		P_{GM}	3	W
Average Gate Power Dissipation		$P_{G\ (AV)}$	0.3	W
Peak Gate Voltage		V_{FGM}	10	V
Peak Gate Current		I_{GM}	1.6	A
Junction Temperature		T_j	−40~125	°C
Storage Temperature Range		T_{stg}	−40~125	°C
Isolation Voltage (AC, t = 1min.)		V_{ISOL}	1500	V

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

MARKING

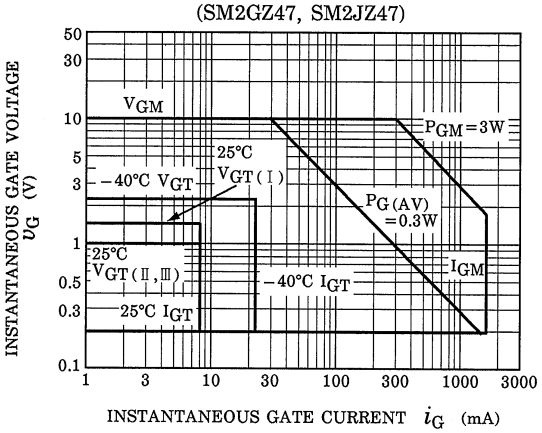


	Part No. (or abbreviation code)	Part No.
*1	M2GZ47	SM2GZ47, SM2GZ47A
	M2JZ47	SM2JZ47, SM2JZ47A
*2	Nothing	SM2GZ47, SM2JZ47
	A	SM2GZ47A, SM2JZ47A

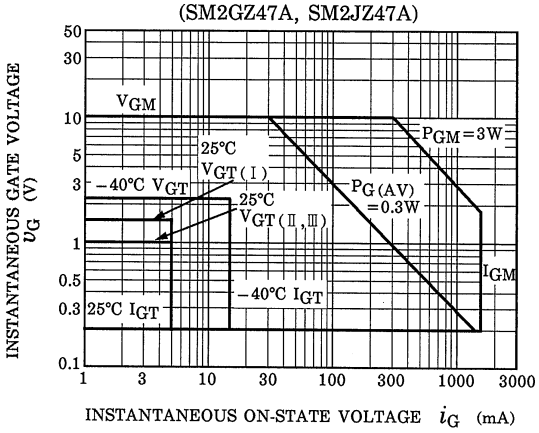
ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC			SYMBOL	TEST CONDITION		MIN	TYP.	MAX	UNIT
Repetitive Peak Off−State Current			I_{DRM}	V_{DRM} = Rated		—	—	20	μA
Gate Trigger Voltage		I	V_{GT}	V_D = 12V R_L = 20Ω	T2 (+) , Gate (+)	—	—	1.5	V
		II			T2 (+) , Gate (−)	—	—	1	
		III			T2 (−) , Gate (−)	—	—	1	
		IV			T2 (−) , Gate (+)	—	—	—	
Gate Trigger Current	SM2GZ47 SM2JZ47	I	I_{GT}	V_D = 12V R_L = 20Ω	T2 (+) , Gate (+)	—	—	8	mA
		II			T2 (+) , Gate (−)	—	—	8	
		III			T2 (−) , Gate (−)	—	—	8	
		IV			T2 (−) , Gate (+)	—	—	—	
	SM2GZ47A SM2JZ47A	I			T2 (+) , Gate (+)	—	—	5	
		II			T2 (+) , Gate (−)	—	—	5	
		III			T2 (−) , Gate (−)	—	—	5	
		IV			T2 (−) , Gate (+)	—	—	—	
Peak On−State Voltage			V_{TM}	I_{TM} = 3A		—	—	1.7	V
Gate Non−Trigger Voltage			V_{GD}	V_D = Rated, Tc = 125°C		0.2	—	—	V
Holding Current			I_H	R_L = 100Ω		—	—	10	mA
Thermal Resistance			$R_{th\ (j-a)}$	Junction to Ambient, AC		—	—	55	°C / W

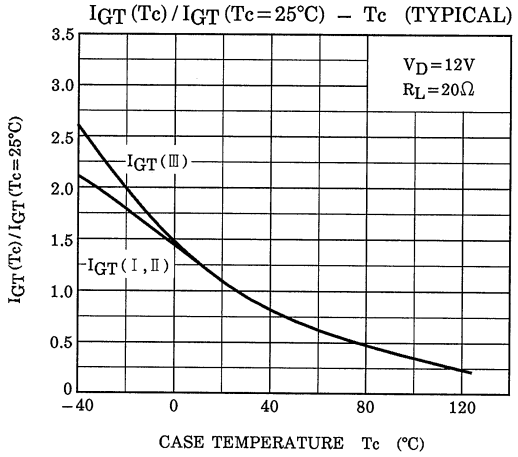
GATE TRIGGER CHARACTERISTIC
(SM2GZ47, SM2JZ47)



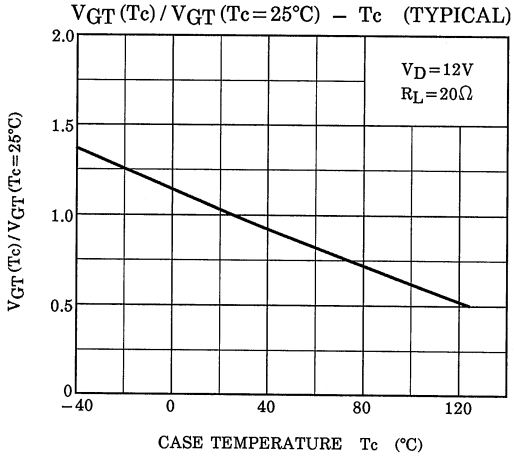
GATE TRIGGER CHARACTERISTIC
(SM2GZ47A, SM2JZ47A)



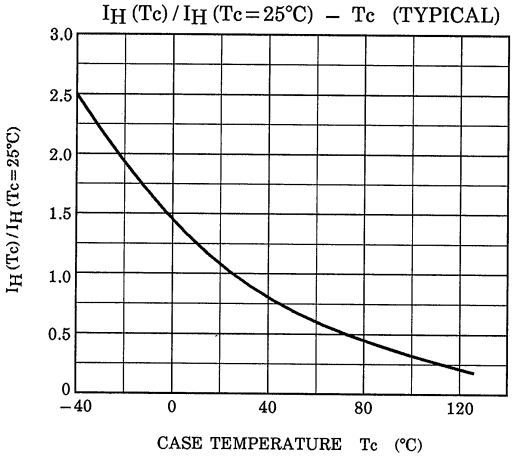
I_{GT} (Tc) / I_{GT} (Tc = 25°C) – Tc (TYPICAL)



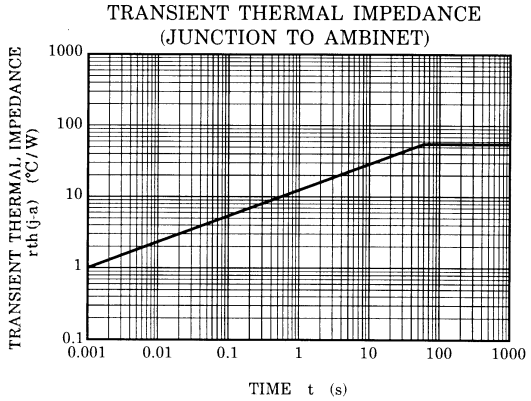
V_{GT} (Tc) / V_{GT} (Tc = 25°C) – Tc (TYPICAL)



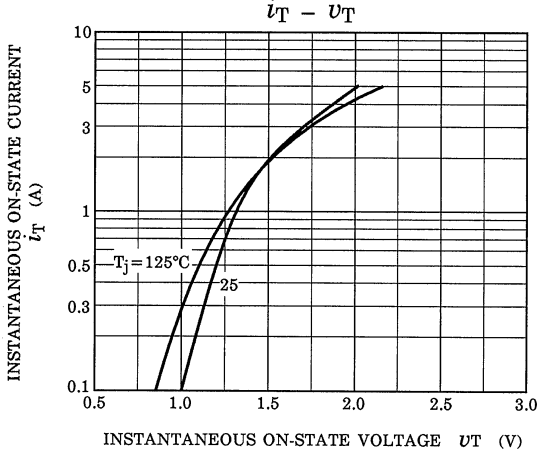
I_H (Tc) / I_H (Tc = 25°C) – Tc (TYPICAL)



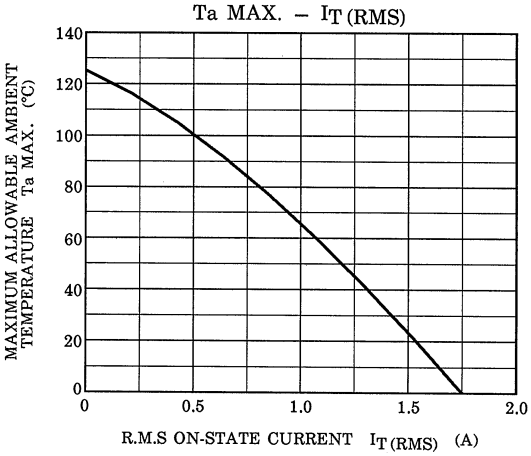
TRANSIENT THERMAL IMPEDANCE
(JUNCTION TO AMBINET)



$i_T - v_T$



Ta MAX. – $I_{T\,(RMS)}$



<CONDITION>

- NO HEAT SINK
- LEAD FORMING : LB182
- PRINT BOARD
  (t=1.6mm
  SOLDER LAND : 2mmϕ)

RESTRICTIONS ON PRODUCT USE

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