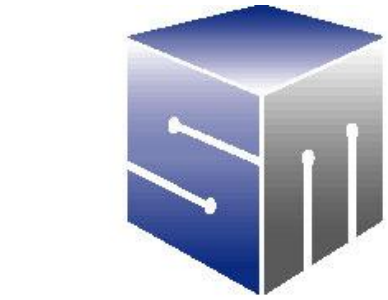

Silicon Motion, Inc.

# SM324

**High Speed USB2.0 Flash Memory Controller**

# SM324 DATABOOK

**Version 1.03**

**Confidential**

# Silicon Motion®, Inc.

## SM324 DataBook

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**Revision History**

| Reversion No | Draft Date | Notes |
|---|---|---|
| 0.9 | 2005/08 | Initial draft |
| 0.91 | 2005/08 | Update Pin Definition |
| 0.92 | 2005/11 | Correct Pin #47 and Pin #52 |
| 0.93 | 2005/11 | Add PCB Layout Guideline and Correct Pin Definitions |
| 0.94 | 2006/01 | Correct the Pin#13 name to PIO04 |
| 1.00 | 2006/05 | Add the AC/DC, Regulators, Voltage Detector Characteristics |
| 1.01 | 2006/08 | 5V regulator input min. voltage to 4.2V |
| 1.02 | 2006/09 | Add the TQFP package option |
| 1.03 | 2007/04/ | Add the LGA package option |

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# 1. INTRODUCTION

## 1.1 General Description

The SM324 is a highly compatible, and best performance USB2.0 Flash Disk controller intended for supporting NAND type Flash memory and SPI interface on one chip.

The SM324 integrates high-speed USB2.0 Transceiver Macro-cell Interface (UTMI) transceiver and Serial Interface Engine (SIE) and an enhanced 80C51 compatible 8-bit microprocessor.

By complies with USB specification ver.2.0 and USB Mass Storage Class specification ver.1.0, the SM324 can be supported by Windows XP/2000/Me default driver. Also it is supported in Windows 98/98SE, Mac and Linux operating system.

For the power consumption consideration, the SM324 complies with USB power specification ver.2.0 for bus-powered devices. And for the USB2.0 Flash Disk application, the SM324 supports up to 8 data Flash banks, “Write Protect” security function, and PC boot up from USB2.0 Flash Disk.

The SM324 is designed specifically for high-speed performance and high capacity USB2.0 Flash Disks. These USB2.0 Flash Disks can be used as removable storage disk for data exchange applications. With SM324’s complete software support, users can easily use USB2.0 Flash Disks for backup, and security.

The objective of the SM324 controller is to drastically increase the USB Flash memory data transfer rate as well as reduce the overall system cost by offering a manufacturing-ready turnkey solution to customers. The SM324 is available in 64-pin LQFP package.

## 1.2 Features

- Completes USB specification ver.2.0 compatibility
- Complies with USB Mass Storage Class specification ver.1.0
- Bulk Only transport protocol
- Complies with USB power specifications for bus-powered devices
- Operating system supported: Windows XP/2000/Me/98/98SE, Mac OS 9.x and above, Linux Kernel 2.4 and above.
- Master & Slave SPI (Serial Peripheral Interface) for flexible applications.
- ISP (In System Programming) firmware update capability.
- Supports dual channel for Flash memory, averaged data transfer rate up to 32* MB/sec
- Compatible with SLC NAND type Flash and up to 8 banks
- Supports MLC Flash Memory with 4 symbols (bytes) ECC engine.
- Supports VID, PID, serial number & vender information update
- Provides LED indicator when USB Flash Disk is in Ready/Working mode
- Supports “Write Protect” security function to protect data in UFD
- Supports suspend and wake-up resume
- Integrated 80C51 compatible 8-bit microprocessor with enhanced feature
- 12MHz crystal driver circuit
- Fabricated in 0.16um CMOS process
- 1.8 Volts low power core operation
- Operates on a single power supply (Vdd = 5.0V)
- Available in LQFP 64-pin (9x9mm including pads) package

*This figure may vary on different platform.

## 1.3 Function Block Diagram

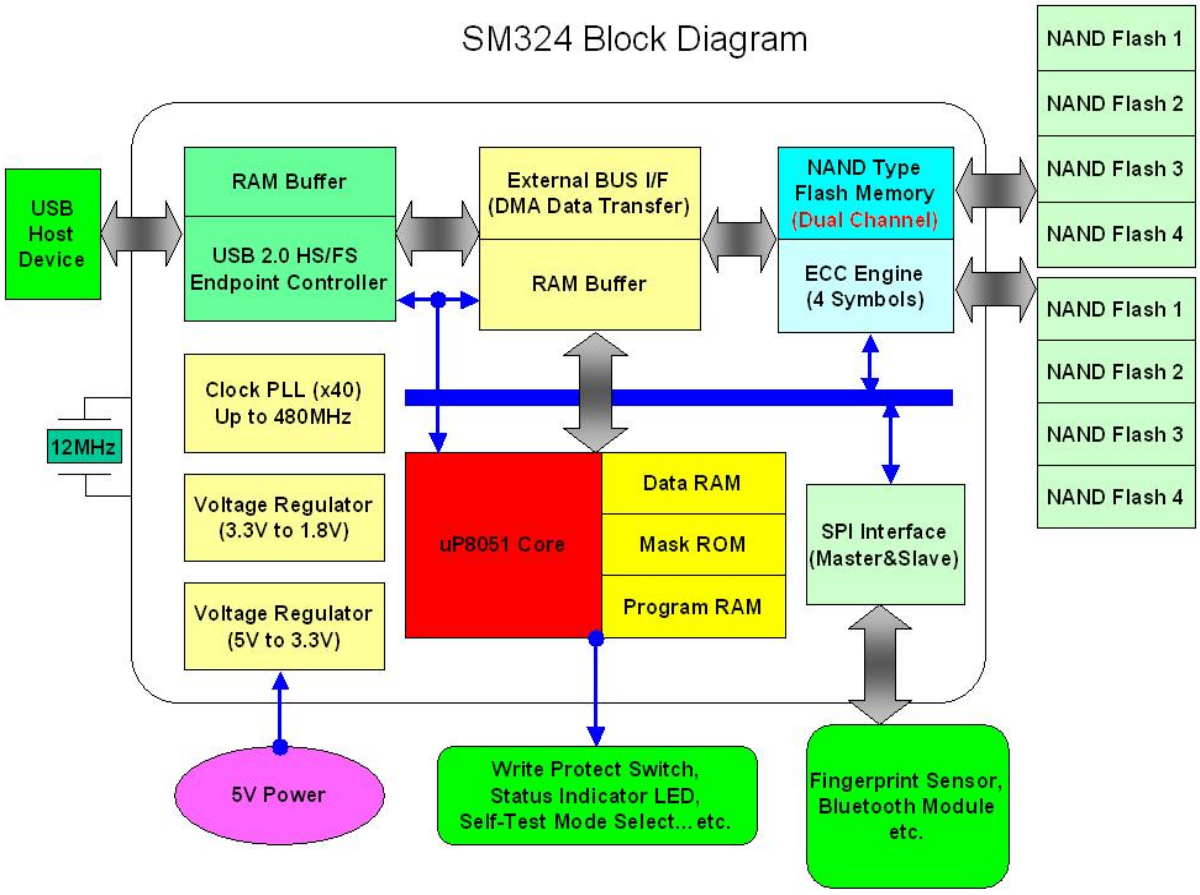



Figure 1.1 Function Block Diagram

## 2. PIN Description

### 2.1 QFP Pin-out Diagram

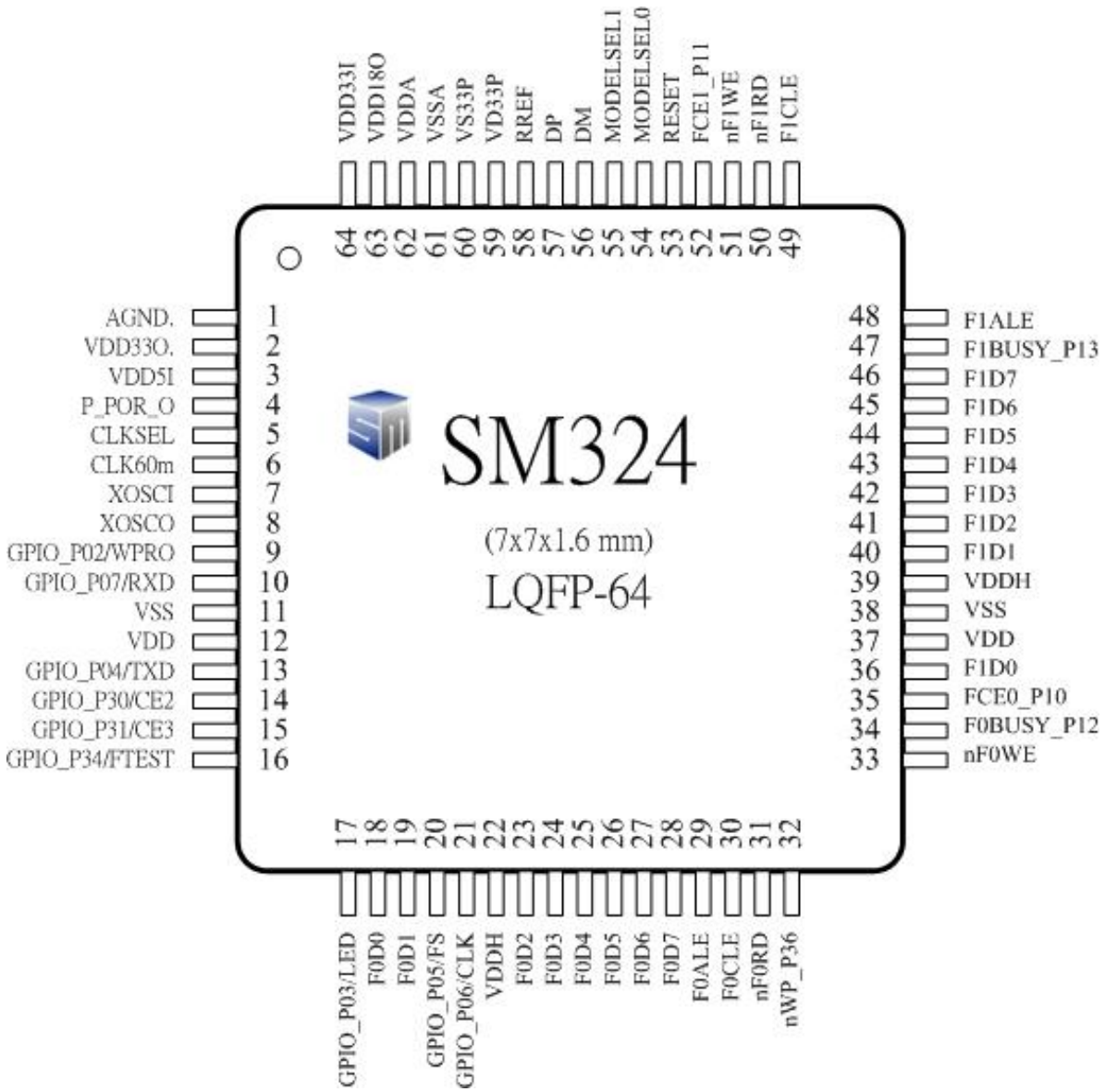



Figure 2.1 SM324 64-pin LQFP Pin-out Diagram

## 2.2 LGA Pin-out Diagram

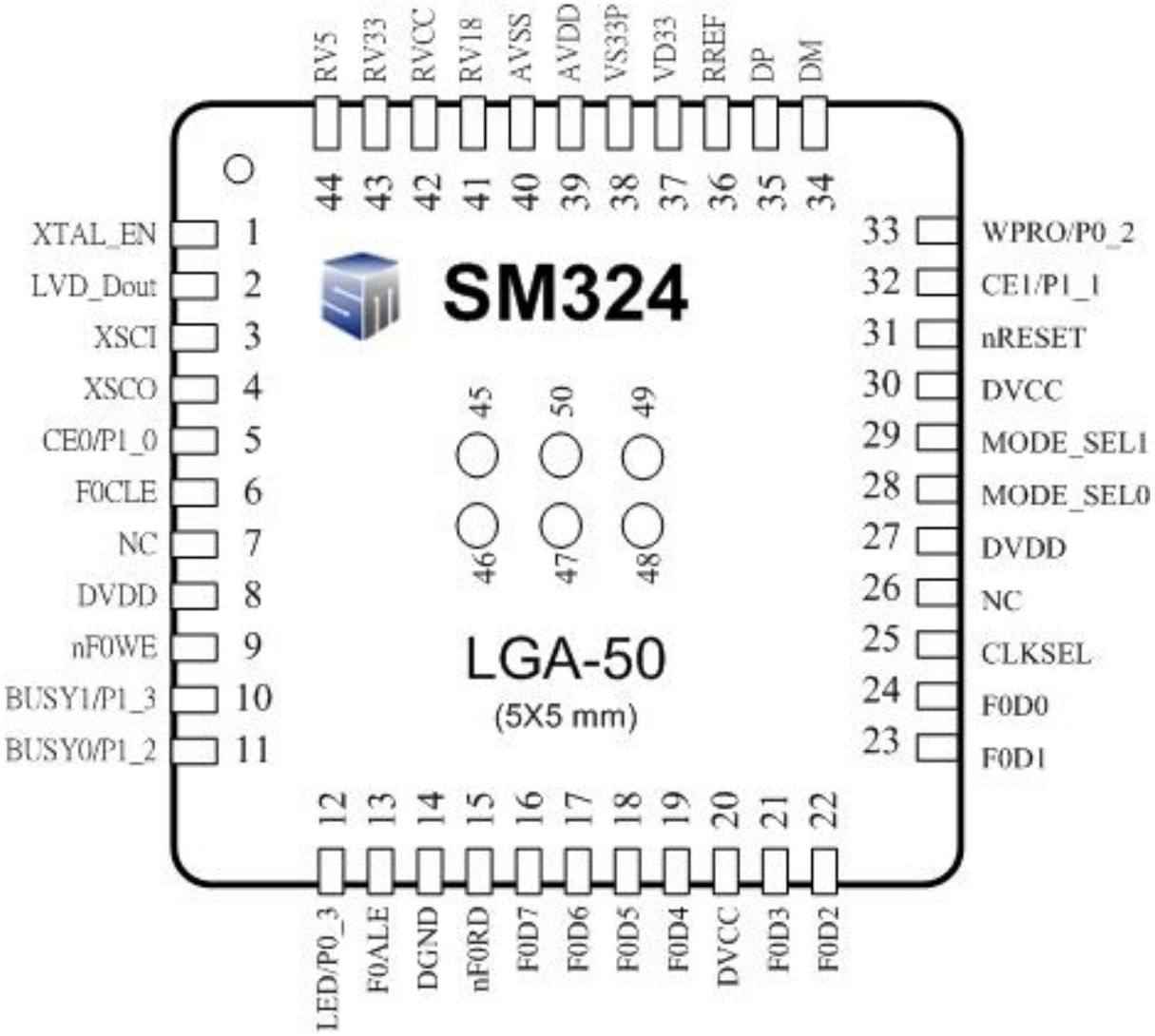



Figure 2.2 SM324 50-pin LGA Pin-out Diagram

Note: the 6 pads in the bottom of the LGA package is for the testing used, which Pin#45~50 should be no connected

## 2.3 Pin Descriptions

| PIN# | | Symbols | Type | Description |
|---|---|---|---|---|
| QFP | LGA | | | |
| 1 | | AGND | Power | Analog Ground (VSS of regulator) Connect to ground with as short a path as possible. |
| 2 | 43 | VDD33O | Power | Analog Power 3.3V Output (Regulator 3.3V Output). This signal provides power to the analog section of the chip. |
| 3 | 44 | VDD5I | Power | Regulator 5.0V Input (VBUS) |
| 4 | 2 | P_POR_O | O | Voltage (2.7V) output |
| 5 | 25 | CLKSEL. | Test | Internal Test Pin |
| 6 | 1 | CLK60in | Test | Internal Test Pin |
| 7 | 3 | XOSC_I | I | Crystal Input. Connect this signal to a 12-MHz parallel-resonant, fundamental mode crystal and 20pF capacitor to GND. |
| 8 | 4 | XOSC_O | O | Crystal Output. Connect this signal to a 12-MHz parallel-resonant, fundamental mode crystal and 20pF capacitor to GND. |
| 9 | 33 | GPIO_P02/WPRO | I/O | General Purpose I/O (UFD Write Protect: Active Low) |
| 10 | | GPIO_P07/RXD | I/O | General Purpose I/O (SPI_RX) |
| 11 | 14 | VSS | Power | Digital/Logic Ground |
| 12 | 8 | VDD | Power | Digital/Logic Power 1.8V |
| 13 | | GPIO_P04/TXD | I/O | General Purpose I/O (SPI_TX) |
| 14 | | GPIO_P30/CE2 | I/O | General Purpose I/O (CE2: Flash Chip Enable 2) |
| 15 | | GPIO_P31/CE3 | I/O | General Purpose I/O (CE3: Flash Chip Enable 3) |
| 16 | | GPIO_P34/FTEST | I/O | General Purpose I/O (nFIDSK: Reset, Active: Low) |
| 17 | 12 | GPIO_P03/LED | I/O | General Purpose I/O (nLED: UFD LED) |

| | | | | |
|---|---|---|---|---|
| **18** | **24** | **F0_D0** | I/O | Channel 0 Flash Data Bus 0 |
| **19** | **23** | **F0_D1** | I/O | Channel 0 Flash Data Bus 1 |
| **20** | | **GPIO_P05/FS** | I/O | General Purpose I/O (SPI_Frame Select) |
| **21** | | **GPIO_P06/CLK** | I/O | General Purpose I/O (SPI_CLK) |
| **22** | **20** | **VDDH** | Power | Digital/Logic Power 3.3V |
| **23** | **22** | **F0_D2** | I/O | Channel 0 Flash Data Bus 2 |
| **24** | **21** | **F0_D3** | I/O | Channel 0 Flash Data Bus 3 |
| **25** | **19** | **F0_D4** | I/O | Channel 0 Flash Data Bus 4 |
| **26** | **18** | **F0_D5** | I/O | Channel 0 Flash Data Bus 5 |
| **27** | **17** | **F0_D6** | I/O | Channel 0 Flash Data Bus 6 |
| **28** | **16** | **F0_D7** | I/O | Channel 0 Flash Data Bus 7 |
| **29** | **13** | **F0_ALE** | O | Channel 0 Flash Address Latch Enable |
| **30** | **6** | **F0_CLE** | O | Channel 0 Flash Command Latch Enable |
| **31** | **15** | **nF0_RD** | O | Channel 0 Flash Read Enable (Active: Low) |
| **32** | | **GPIO_P36/nWP** | I/O | General Purpose I/O (nWP: Flash Write Protect: Active Low) |
| **33** | **9** | **nF0_WE** | O | Channel 0 Flash Write Enable (Active: Low) |
| **34** | **11** | **F0BUSY_P12** | O | Channel 0 Flash Busy Signal |
| **35** | **5** | **FCE0_P10** | O | Channel 0 Flash Chip Select |
| **36** | **24** | **F1_D0** | I/O | Channel 1 Flash Data Bus 0 |
| **37** | **27** | **VDD** | Power | Digital/Logic Power 1.8V |
| **38** | | **VSS** | Power | Digital/Logic Ground |
| **39** | **30** | **VDDH** | Power | Digital/Logic Power 3.3V |
| **40** | | **F1_D1** | I/O | Channel 1 Flash Data Bus 1 |
| **41** | | **F1_D2** | I/O | Channel 1 Flash Data Bus 2 |
| **42** | | **F1_D3** | I/O | Channel 1 Flash Data Bus 3 |
| **43** | | **F1_D4** | I/O | Channel 1 Flash Data Bus 4 |
| **44** | | **F1_D5** | I/O | Channel 1 Flash Data Bus 5 |
| **45** | | **F1_D6** | I/O | Channel 1 Flash Data Bus 6 |
| **46** | | **F1_D7** | I/O | Channel 1 Flash Data Bus 7 |
| **47** | **10** | **F1BUSY_P13** | O | Channel 1 Flash Busy Signal |
| **48** | | **F1_ALE** | O | Channel 1 Flash Address Latch Enable |

| | | | | |
|---|---|---|---|---|
| **49** | | **F1_CLE** | O | Channel 1 Flash Command Latch Enable |
| **50** | | **nF1_RD** | O | Channel 1 Flash Read Enable (Active: Low) |
| **51** | | **nF1_WE** | O | Channel 1 Flash Write Enable (Active: Low) |
| **52** | **32** | **FCE1_P11** | O | Channel 1 Flash Chip Select |
| **53** | **31** | **RESET** | I | Chip Reset (Active: Low) |
| **54** | **28** | **Model_SEL0** | I | Tie to Digital/Logic 3.3V |
| **55** | **29** | **Model_SEL1** | I | Tie to Digital/Logic 3.3V |
| **56** | **34** | **DM** | I/O | USB2.0 Data Negative Pin |
| **57** | **35** | **DP** | I/O | USB2.0 Data Positive Pin |
| **58** | **36** | **RREF** | I | Reference Resistor (330Ω ±1%) to AGND |
| **59** | **37** | **VDD33P** | Power | Analog 3.3V |
| **60** | **38** | **VS33P** | Power | Analog PLL Ground |
| **61** | **40** | **VSSA** | Power | Analog Ground |
| **62** | **39** | **VDDA** | Power | Analog 1.8V |
| **63** | **41** | **VDD18O** | Power | Analog 1.8V Power Output (Regulator 1.8V Output) |
| **64** | **42** | **VDD33I** | Power | Analog 3.3V Power Input (Regulator 3.3V Input) |

Table 2-1. SM324 Pin Descriptions

# 3. Electrical Characteristics

## 3.1 Absolute Maximum Ratings

| | |
|---|---|
| Operating Temperature Range …… | 0℃ to +70℃ |
| Storage Temperature Range …….. | -55o to +150℃ |
| Lead Temperature Range (soldering, 10 seconds) ……. | +325℃ |
| Positive Voltage on any pin, with respect to Ground …… | +5.5V |
| Negative Voltage on any pin, with respect to Ground ……. | -0.3V |
| Maximum AVDD, DVDD ……..…….. | +2.0V |
| Maximum AVCC, DVCC ……..…….. | +3.6V |

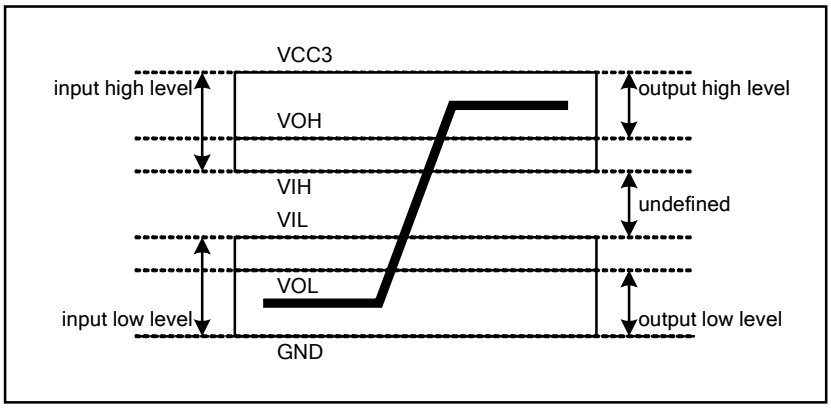
*Stresses above the specified parameters could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

## 3.2 AC/DC characteristics

**General DC Characteristics**

| Parameter | Symbol | Min. | Max. | Unit | Remark |
|---|---|---|---|---|---|
| Peak voltage on all lines | | -0.5 | 3.6 | V | Except VCC5V input |
| All input leakage current | | -10 | 10 | uA | |
| All output leakage current | | -10 | 10 | uA | |
| Supply voltage | VCC3 | 2.7 | 3.6 | V | |

**Bus Signal Level**




| Parameter | Symbol | Min. | Max. | Unit | Remark |
|---|---|---|---|---|---|
| Output High voltage | $V_{OH}$ | 2.4 | | V | |
| Output Low voltage | $V_{OL}$ | | 0.4 | V | |
| Input High voltage | $V_{IH}$ | 2.0 | | V | |
| Input Low voltage | $V_{IL}$ | | 0.8 | V | |

**Bus Signal Line Loading**

| Parameter | Symbol | Min. | Max. | Unit | Remark |
|---|---|---|---|---|---|
| Bus line capacitance | $C_L$ | | 20 | pF | |

### 3.3 Internal Regulator (5.0V to 3.3V ):

## Electrical characteristics:

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| VDD5I | Analog supply voltage | | 4.2 | 5.0 | 5.5 | V |
| VDD33O | Regulated output voltage | VBUS=5.0V | 2.9 | 3.3 | 3.6 | V |
| $I_{STB}$ | Stand-by current | No Load | | 25 | 35 | µA |
| Ioutput | Output driving current | | | 200 | 250 | mA |

**Note: The regulator output is @100mA condition.**

### 3.4 Internal Regulator (3.3V to 1.8V ):

## Electrical characteristics:

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| VDD33I | Analog supply voltage | | 2.4 | 3.3 | 3.6 | V |
| VDD18O | Regulated output voltage | V33=3.3V Cload=4.7uF | 1.6 | 1.8 | 2.0 | V |
| $I_{STB}$ | Stand-by current | No Load | | 25 | 35 | µA |
| Ioutput | Output driving current | | | 70 | 100 | mA |

### 3.5 Voltage Detector (2.7V ):

## Electrical characteristics:

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VDD33I | Power Supply Voltage | 2 | 3.3 | 3.6 | V |
| P_POR_RR | Reference High Voltage | 2.4 | 2.5 | 2.6 | V |
| P_POR_FR | Reference Low Voltage | 2.2 | 2.3 | 2.4 | V |
| VHYS | Hysterisis Width | 0.1 | 0.2 | 0.3 | V |

## 4. Layout Guideline

### PCB Layer Stack-up

In USB 2.0 applications, a PCB with a minimum of 4 layers is required. Because it needs to control the impedance of the USB 2.0 differential signal pair and supply a clear power and ground. The 4 layers are typically configured as described as below.

| Layer | Description | Signification Features |
|---|---|---|
| 1 | Component Side(Top) | Contains differential signal pair and other signal routing and primary surface-mounted components. |
| 2 | Ground Layer | Ground plane (include AGND and DGND). Also, is reference layer for differential signal pair. |
| 3 | Power Layer | Power plane (include AVCC and DVCC). |
| 4 | Solder Side(Bottom) | Contains signal routing and secondary surface-mounted components. |

The PCB designer should use an impedance calculator to determine the differential trace impedance of USB 2.0 differential signal pair. Note that the calculations to determine the differential impedance are somewhat different from those used to calculate the impedance of a signal trance. The appropriate software should be selected.

Using 8-mil wide traces with 12-mil spacing between differential signal pair to obtain 90Ω differential impedance is recommended by SMI. The specific printed circuit board stackup is as follows:

W = 8 mils
S = 12 mils
D > 12 mils
H = 4 ~ 5 mils (prepreg)
T = 1 ounce copper
Er = 4.5 (FR4 material)
Board thickness = 0.8 ~ 1.0 mm

### Reference

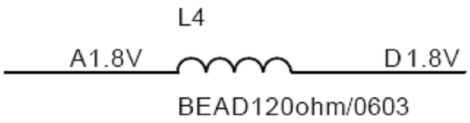
*" High Speed USB Platform Design Guidelines " by Intel Corporation.*

## Stability

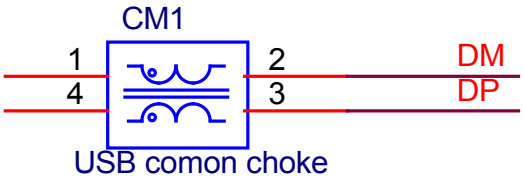
To improve the stability of Flash Memory support, please review the detailed description and updated circuit hereunder to revise your current layout.

1. **The bypass capacitances should be placed as close to the SM32X as possible, especially AVDD 1.8 voltage. The distance between 0.1uF and controller should be under 3mm.**

2. **Please also separate the AVDD(1.8V) and DVDD(1.8V) by the ferret bead.**




3. **Please add a common choke between DM and DP to enhance the EMI.**



## 5. Packaging Specification

### 5.1 QFP 64-pin Packaging Dimension

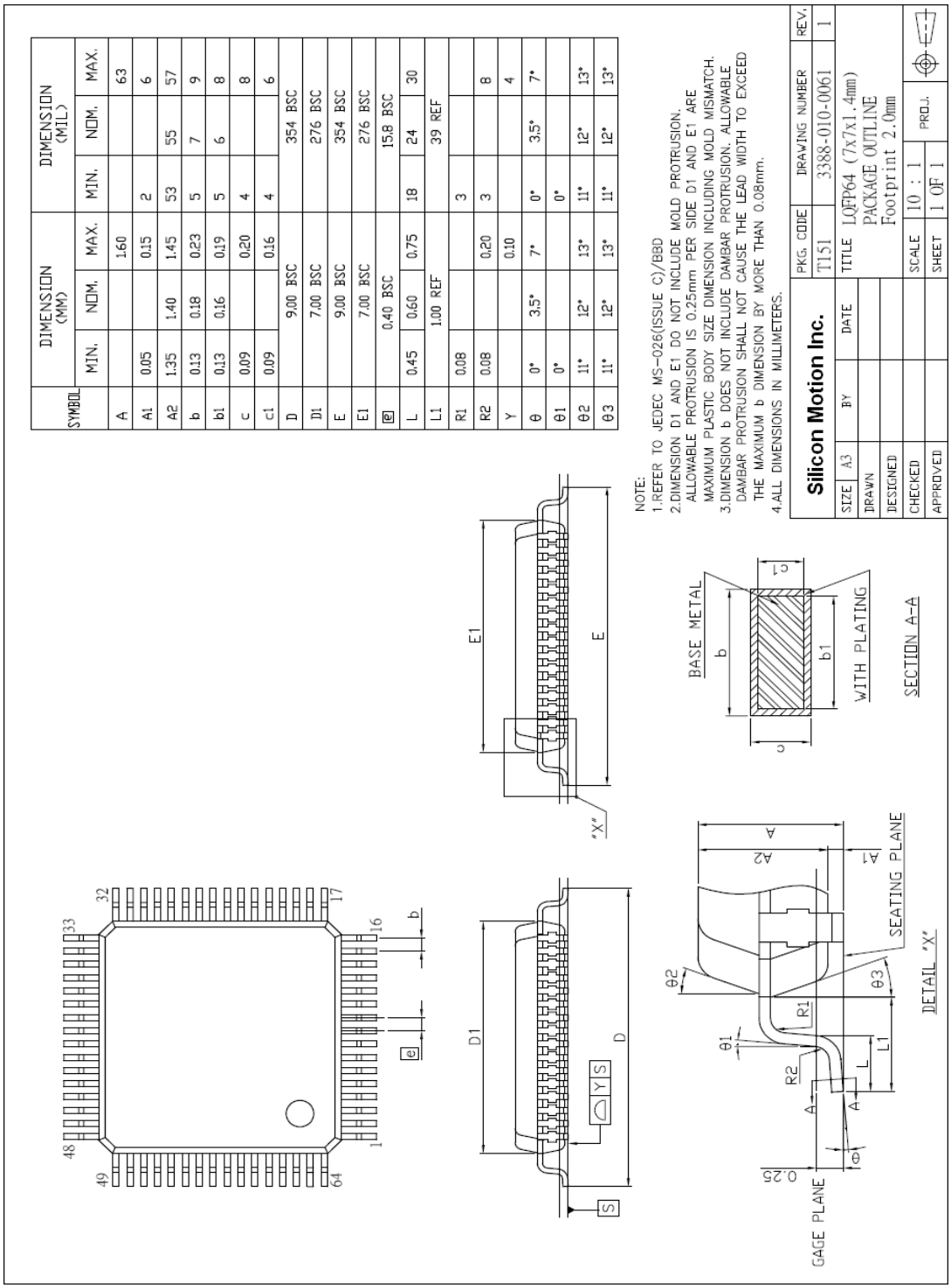



Figure 5.1 LQFP 64-pin Packaging Dimension

## 5.2 TQFP 64-pin Packaging Dimension

| SYMBOL | DIMENSION (MM) | | | DIMENSION (MIL) | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | | | 1.20 | | | 47 |
| A1 | 0.05 | | 0.15 | 2 | | 6 |
| A2 | 0.95 | 1.00 | 1.05 | 37 | 39 | 41 |
| b | 0.13 | 0.18 | 0.23 | 5 | 7 | 9 |
| b1 | 0.13 | 0.16 | 0.19 | 5 | 6 | 8 |
| c | 0.09 | | 0.20 | 4 | | 8 |
| c1 | 0.09 | | 0.16 | 4 | | 6 |
| D | 9.00 BSC | | | 354 BSC | | |
| D1 | 7.00 BSC | | | 276 BSC | | |
| E | 9.00 BSC | | | 354 BSC | | |
| E1 | 7.00 BSC | | | 276 BSC | | |
| e | 0.40 BSC | | | 16 BSC | | |
| L | 0.45 | 0.60 | 0.75 | 18 | 24 | 30 |
| L1 | 1.00 REF | | | 39 REF | | |
| R1 | 0.08 | | | 3 | | |
| R2 | 0.08 | | 0.20 | 3 | | 8 |
| Y | | | 0.075 | | | 3 |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| θ1 | 0° | | | 0° | | |
| θ2 | 11° | 12° | 13° | 11° | 12° | 13° |
| θ3 | 11° | 12° | 13° | 11° | 12° | 13° |

NOTE:
1.REFER TO JEDEC MS-026/ABD
2.DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
ALLOWABLE PROTRUSION IS 0.25mm PER SIDE D1 AND E1 ARE
MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE
DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED
THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
4.ALL DIMENSIONS IN MILLIMETERS.

TQFP64 (7x7x1.0mm)
PACKAGE OUTLINE
Footprint 2.0mm

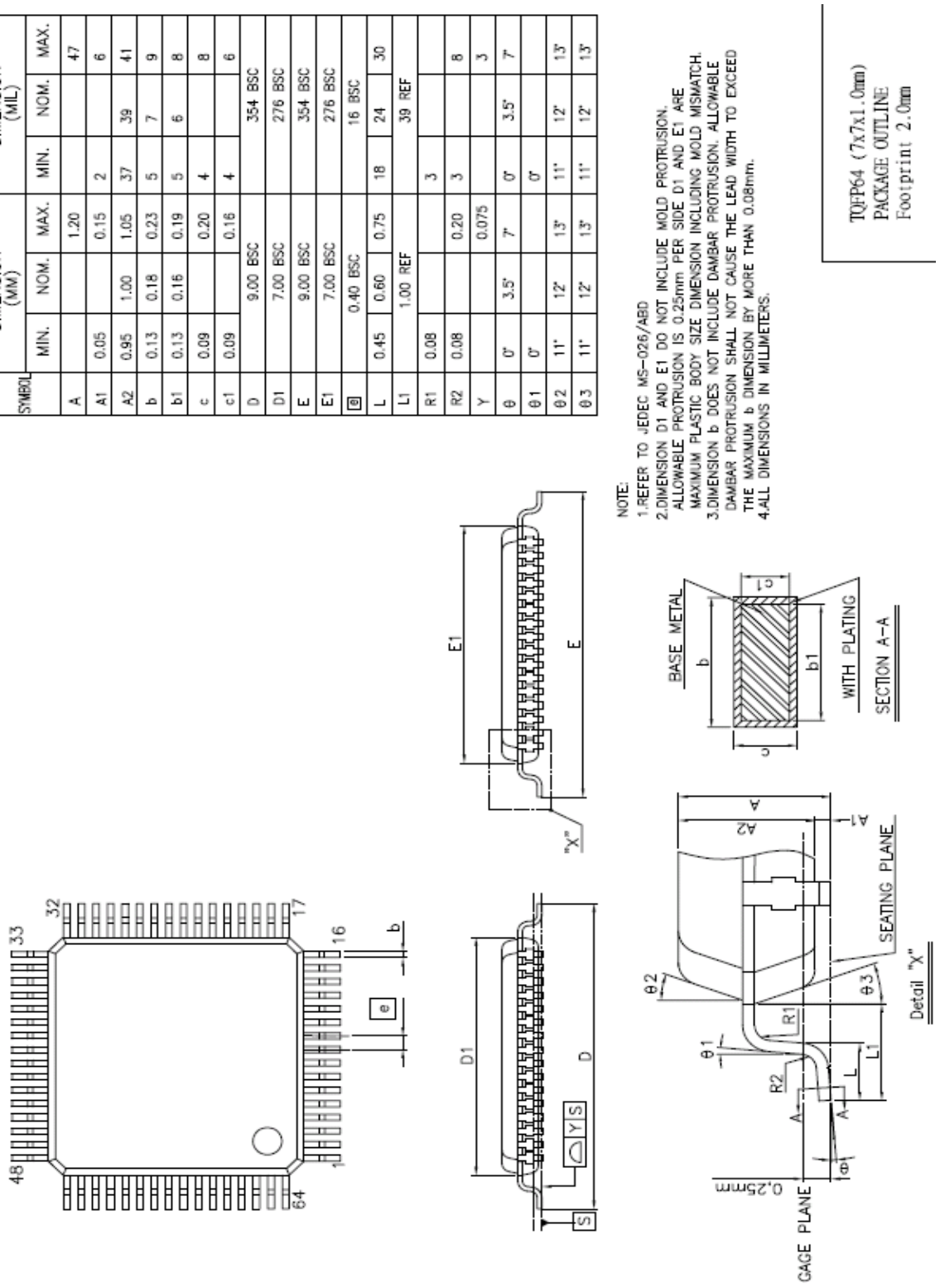
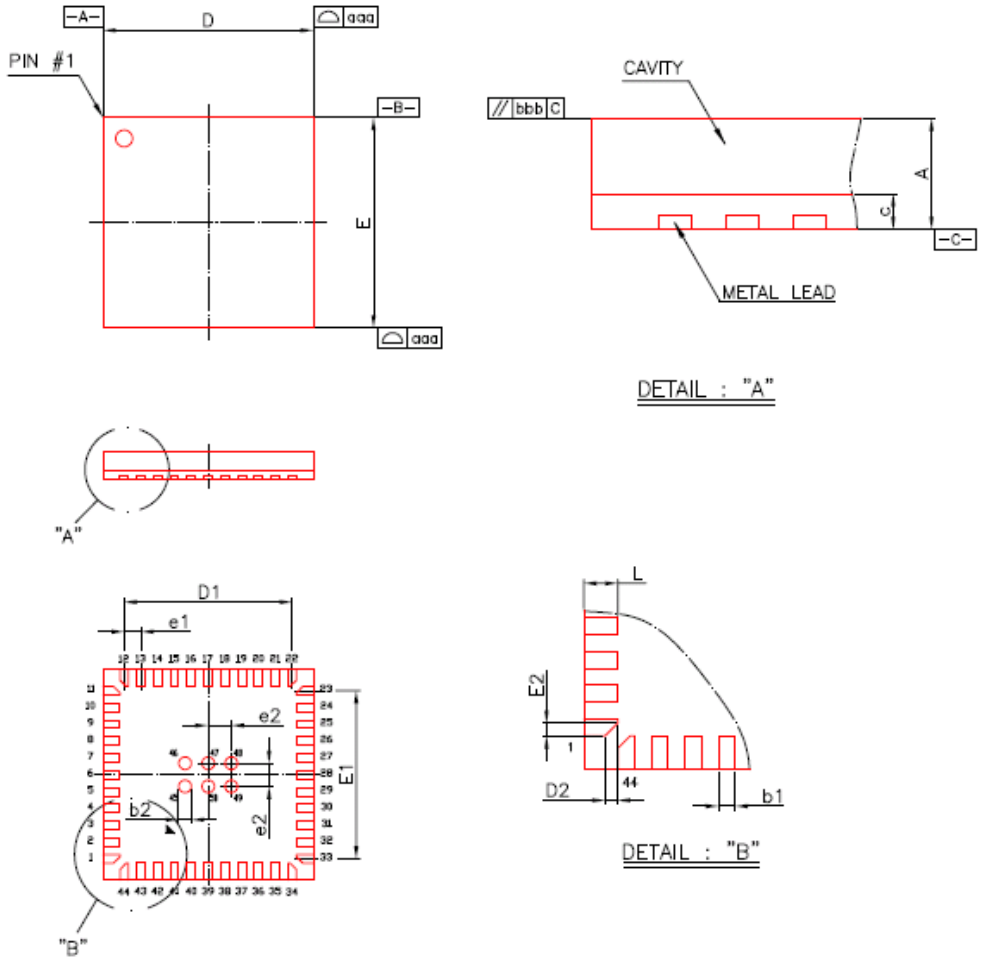



Figure 5.2 TQFP 64-pin Packaging Dimension

## 5.3 LGA 50-pin Packaging Dimension




| Symbol | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | --- | --- | 0.70 | --- | --- | 0.028 |
| c | 0.17 | 0.21 | 0.25 | 0.007 | 0.008 | 0.010 |
| D | 4.90 | 5.00 | 5.10 | 0.193 | 0.197 | 0.201 |
| D1 | --- | 4.00 | --- | --- | 0.157 | --- |
| D2 | --- | 0.15 | --- | --- | 0.006 | --- |
| E | 4.90 | 5.00 | 5.10 | 0.193 | 0.197 | 0.201 |
| E1 | --- | 4.00 | --- | --- | 0.157 | --- |
| E2 | --- | 0.15 | --- | --- | 0.006 | --- |
| e1 | --- | 0.40 | --- | --- | 0.016 | --- |
| e2 | --- | 0.55 | --- | --- | 0.022 | --- |
| b1 | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| b2 | 0.25 | 0.30 | 0.35 | 0.010 | 0.012 | 0.014 |
| L | 0.30 | 0.40 | 0.50 | 0.012 | 0.016 | 0.020 |
| aaa | 0.10 | | | 0.004 | | |
| bbb | 0.10 | | | 0.004 | | |