OVERVIEW

The SM3470B is an interpolation IC for encoders. It accepts displacement detection, 2-phase analog signals (A and B phases) and a zero point detection analog signal (Z phase) from an encoder, interpolates the signals by a specified interpolation factor, and outputs corresponding 2-phase digital signals (A and B phases) and a zero point detection digital signal (Z phase). It incorporates a built-in EEPROM for interpolation switching and input signal adjustment functions, providing support for system miniaturization and high-speed input/output signal operation.

FEATURES

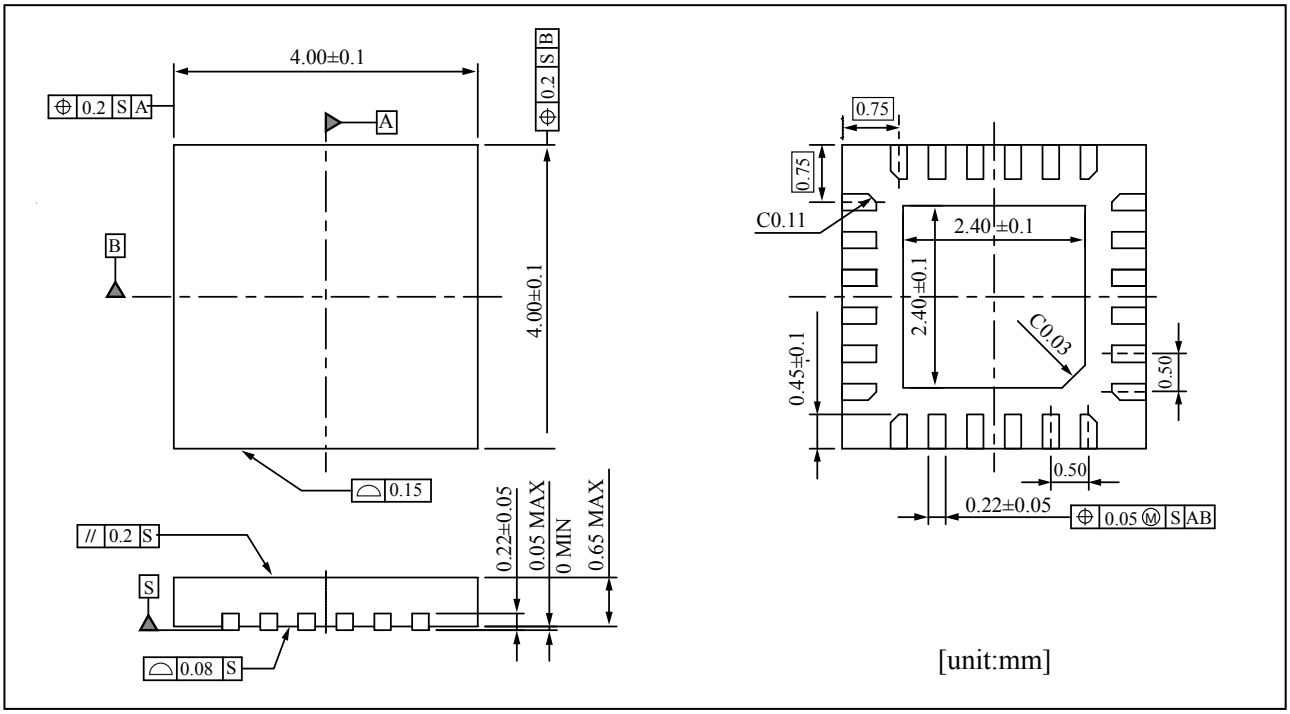
- Interpolation switching function: ×1, 2, 4, 8, 16, 32, 5, 10, 20 (selectable)
- Adjustment function: Offset adjustment
- Supply voltage: 2.7 to 5.5V
- Operating temperature range: –40 to +125°C
- Input frequency: 500kHz (max)
- Output frequency: 2.5MHz (max)
- Package: QFN24 (size: 4mm × 4mm)

ORDERING INFORMATION

Device	Package
SM3470BB-G*1	24 pin QFN

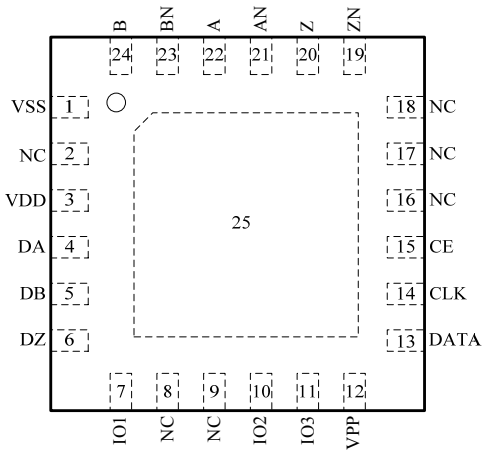
*1. "-G" option code lead-free package

PACKAGE DIMENSIONS



PINOUT

QFN24 package
(Top view)

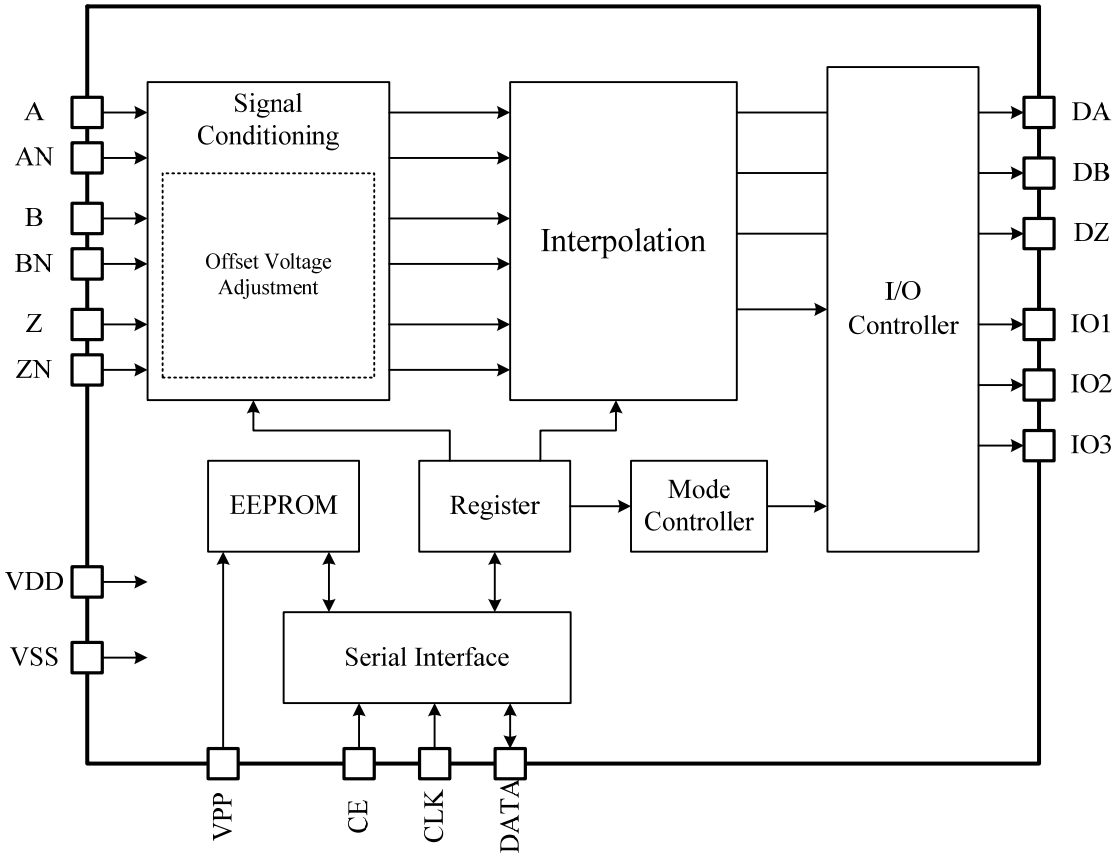


PIN DESCRIPTION

Pin No.	Name	I/O	Function
1	VSS	-	Ground
2	NC	-	No connection
3	VDD	-	Power supply
4	DA	O	Displacement detector signal output (A)
5	DB	O	Displacement detector signal output (B)
6	DZ	O	Zero point detector signal output (Z)
7	IO1	O	General-purpose output 1
8	NC	-	No connection
9	NC	-	No connection
10	IO2	O	General-purpose output 2
11	IO3	O	General-purpose output 3
12	VPP	-	EEPROM access high-voltage pulse
13	DATA	I/O	Serial interface data input/output with pull-down resistor
14	CLK	I	Serial interface clock input with pull-down resistor
15	CE	I	Serial interface enable input with pull-down resistor
16	NC	-	No connection
17	NC	-	No connection
18	NC	-	No connection
19	ZN	I	Zero point detector inverse-phase signal input
20	Z	I	Zero point detector signal input
21	AN	I	Displacement detector signal (–cos) input
22	A	I	Displacement detector signal (cos) input
23	BN	I	Displacement detector signal (–sin) input
24	B	I	Displacement detector signal (sin) input
25	TP	-	Thermal pad. Connect to VSS or leave OPEN.

*. I: Input pin O: Output pin I/O: Input/Output pin

BLOCK DIAGRAM



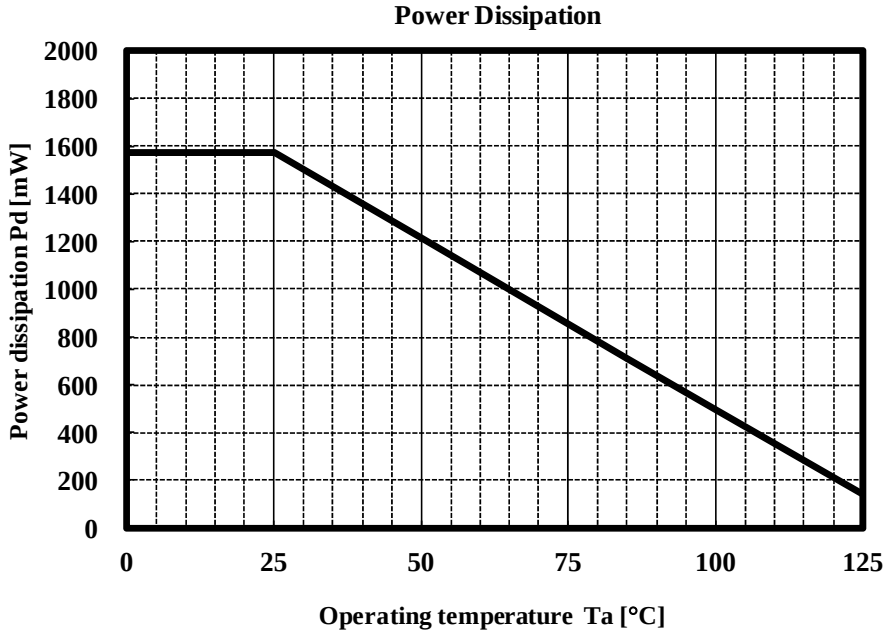
SPECIFICATIONS

Absolute Maximum Ratings

V_{SS}=0V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage 1*1	V_{DD}	VDD pin	–0.3 to +6.5	V
Supply voltage 2*1	V_{PP}	VPP pin	V_{DD} to +20.0	V
Input voltage*1,*3	V_{IN}	Input pins*5	–0.3 to V_{DD}+0.3	V
Output voltage*1,*3	V_{OUT}	Output pins*6	–0.3 to V_{DD}+0.3	V
Junction temperature*2	T_j		+150	°C
Power dissipation*1	P_D	T_a=25°C*7	1570	mW
Storage temperature*4	T_{stg1}		–40 to +125	°C
EEPROM data retention temperature	T_{stg2}		+125	°C
EEPROM rewrite cycles	N_W		10	cycles

*1. Parameters must not exceed ratings, not even momentarily. If a rating is exceeded, there is a risk of IC failure, deterioration in characteristics, and decrease in reliability.
*2. Parameters should not exceed ratings. If a rating is exceeded, there is a risk of deterioration in characteristics and decrease in reliability.
*3. V_{DD} value is the recommended operating voltage rating.
*4. Stored separately without packing material in Nitrogen or vacuum atmosphere.
*5. CE, CLK, DATA, A, AN, B, BN, Z, and ZN terminals.
*6. DATA, DA, DB, DZ, IO1, IO2, and IO3 terminals.
*7. 114.3×76.2×1.6mm, 150% wiring ratio, FR-4 4-layer board (with thermal pad connections). Dissipation will vary due to differences in board specifications and footprint pattern.



Recommended Operating Conditions

The recommended operating conditions are the conditions for which the electrical characteristics are guaranteed.

V_{SS}=0V

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Supply voltage 1	V_{DD}	VDD pin	2.7		5.5	V
Supply voltage 2	V_{PP}	VPP pin, when writing to EEPROM*1	19		19.5	V
Input voltage	V_{IN}		V_{SS}		V_{DD}	V
Operating temperature range	T_a		–40		+125	°C

*1. Use with the VPP terminal open-circuit when not accessing EEPROM.

Note. Operation outside the recommended operating conditions may adversely affect reliability. Use only within specified ratings.

Electrical Characteristics

DC Electrical Characteristics

Recommended operating conditions using reference circuit, unless otherwise noted

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Current consumption	I_{DD}	V_{DD}, No load		25*1	36	mA
Logic input voltage	V_{IH}	CE, CLK, DATA	$0.7V_{DD}$		V_{DD}	V
	V_{IL}		V_{SS}		$0.3V_{DD}$	
Logic input current	I_{IH}	CE, CLK, DATA	20		200	µA
	I_{IL}		–1			
Logic output voltage	V_{OH}	DATA, I_{out} = +1mA	V_{DD}–0.4			V
	V_{OL}	DATA, I_{out} = –1mA			0.3	

*1. Typical conditions: V_{DD}=5V, Ta=25°C, 16x interpolation, no output load

Analog Circuit Electrical Characteristics

V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=–40 to +125°C unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage range*1	V_{inHL}		1		V_{DD}–1	V
Output voltage*2	V_{outH}	I_{out} = +1.5mA, digital output	V_{DD}–0.4			V
	V_{outL}	I_{out} = –1.5mA, digital output			0.3	V
Input frequency	f_{in}				500	kHz
Output frequency	f_{out}				2.5	MHz
Angular error*3 (max – min)	A_{RAL}	V_{DD}=5.0V, 16x interpolation, 10kHz input frequency, single-ended input, 3.0Vpp input amplitude			3	Degrees
Rise/Fall time	t_{rf}	0.1V_{DD} to 0.9V_{DD}, CL=20pF			10	ns

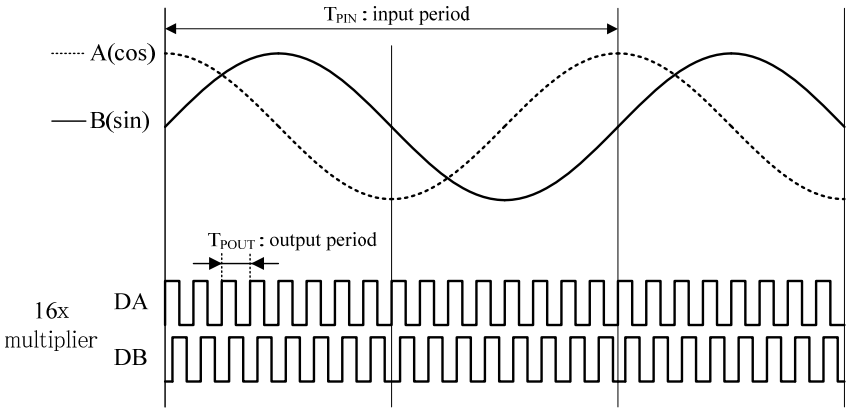
*1. A, AN, B, BN, Z, and ZN terminals.

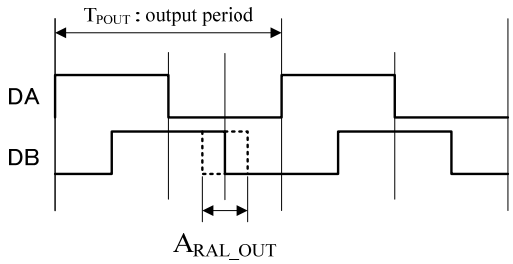
*2. DA, DB, DZ, IO1, IO2, and IO3 terminals.

*3. The angular error expresses the variation from the ideal phase difference of interpolation outputs DA and DB as a phase difference of the input period. Converting 3° and expressing as a percentage of the output period gives 13.3% using equation (1) below.

$$\frac{3\,\text{deg} \times 16x}{360\,\text{deg}} = 13.3\% \qquad (1)$$

(where 16x is the interpolation factor)





Conversion to output period reference

* $T_{POUT}=T_{PIN}/\text{Multiplier}=360\text{deg}$

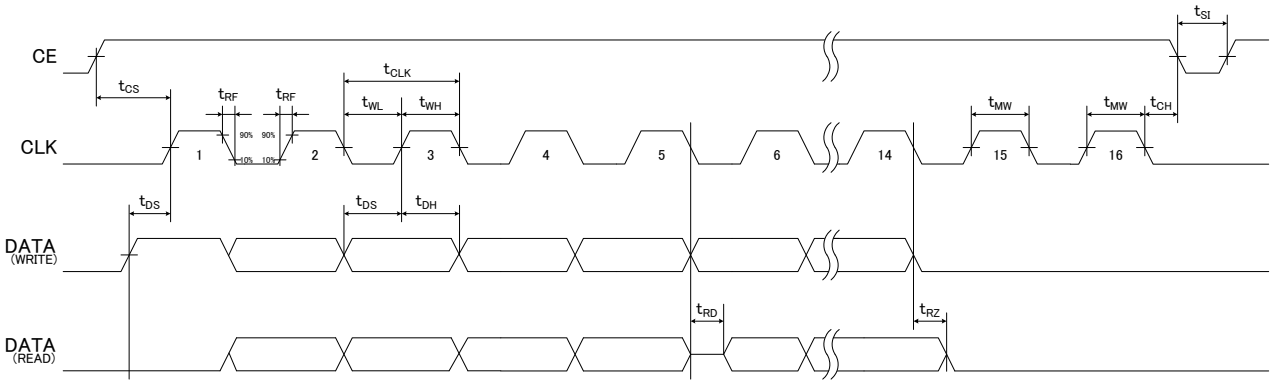
$$A_{RAL\_OUT} = 3\text{deg} \times 16 = 48\text{deg}$$

$$= \frac{3\text{deg} \times 16}{360\text{deg}} = 13.3\%$$

Serial Interface AC Characteristics

V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=–40 to +125°C unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CLK cycle	t_{CLK}		1000			ns
CLK HIGH pulse width	t_{WH}		400			ns
CLK LOW pulse width	t_{WL}		400			ns
CLK rise/fall time	t_{RF}				100	ns
CE setup time	t_{CS}		200			ns
CE hold time	t_{CH}		200			ns
Write data setup time	t_{DS}	Write mode, DATA pin	100			ns
Write data hold time	t_{DH}	Write mode, DATA pin	100			ns
Data propagation delay	t_{RD}	Read mode, CL=20pF			200	ns
Output disable time	t_{RZ}	CL=20pF, DATA pin			200	ns
Interface waiting time	t_{SI}		500			ns
EEPROM write time	t_{MW}		25			ms



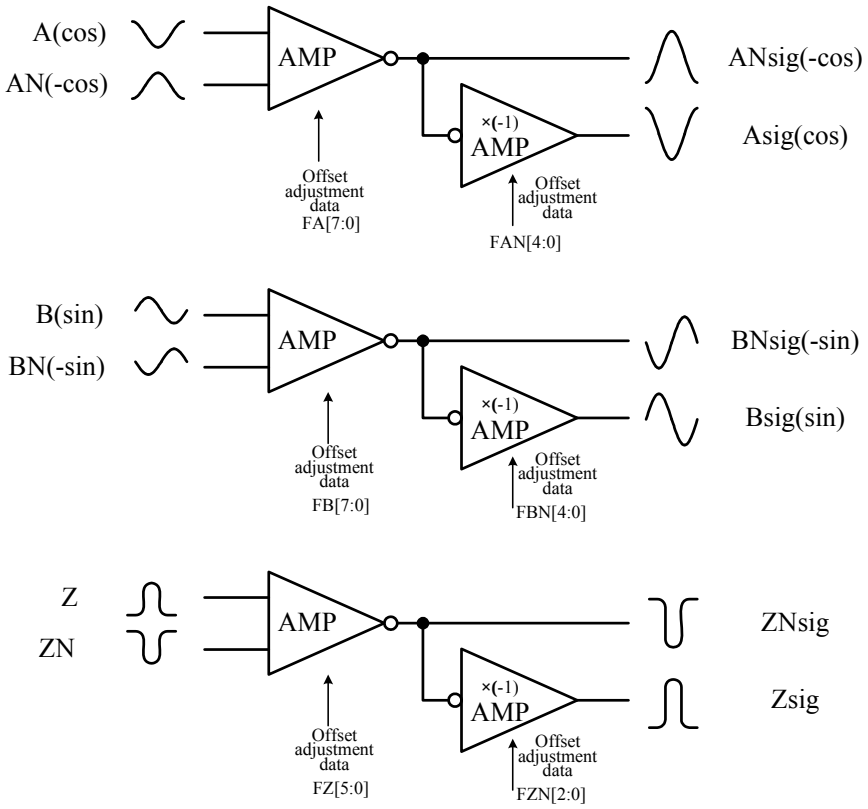
FUNCTIONAL DESCRIPTION

Adjustment Circuit

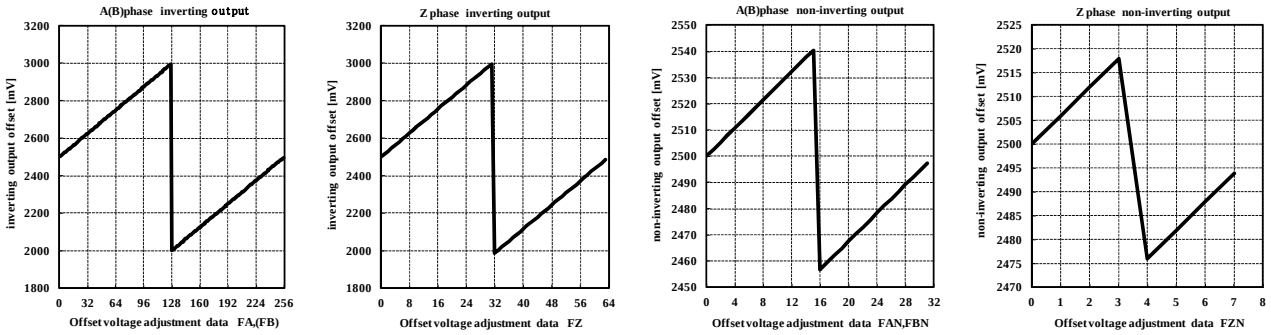
The adjustment circuit block accepts displacement detection 2-phase analog signals from the encoder (A-phase and B-phase) and the zero-point detection analog signal (Z-phase) and perform offset adjustment.
The offset adjustment is set according to register data. For details, see "Analog Adjustment Bit Assignment."

In the offset adjustment sequence, first adjust the internal reference voltage (V_{DD}/2) offsets (FA, FB, FZ) for the inverting output amplifier (monitoring IO1, IO2, IO3), then adjust the offsets (FAN, FBN, FZN) for the non-inverting output amplifier (monitoring DA, DB, DZ).

If the A/B/Z-phase inputs are used as single-ended inputs, the AN, BN, and ZN inputs can be set to V_{DD}/2 level according to the operating mode.



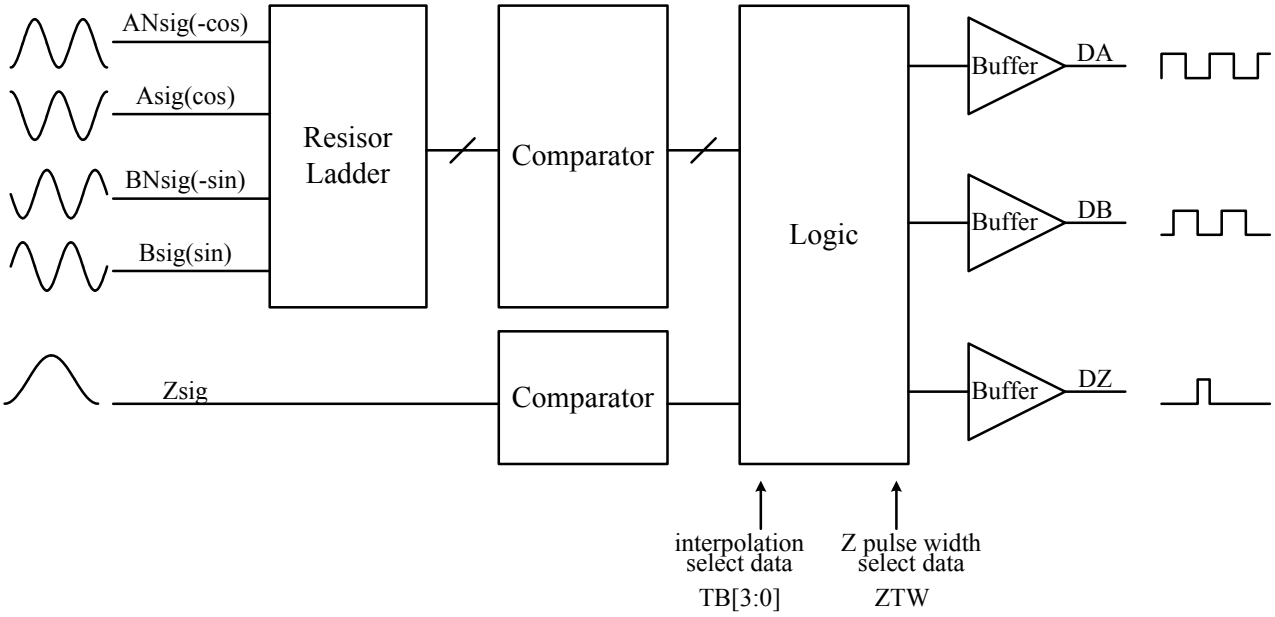
Offset adjustment example (V_{DD}=5.0V)



Interpolation Circuit

The interpolation circuit passes the input signals, with offset correction by the adjustment circuit, through a resistance network divider, converts the signals to binary using comparators, and outputs 2-phase digital signals corresponding to the interpolation factor selected by register data using logical operation processing.

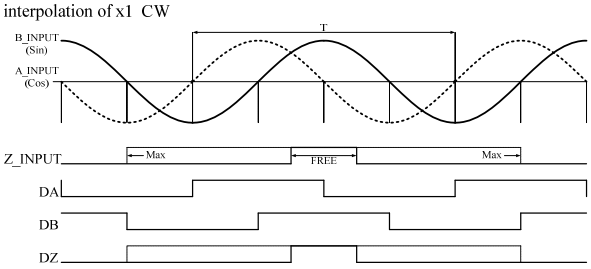
The interpolation factor can be set to one of nine values: ×1, 2, 4, 8, 16, 32, 5, 10, or 20. The interpolation factor is set using 4-bit (TB[3:0]) data written to the register.



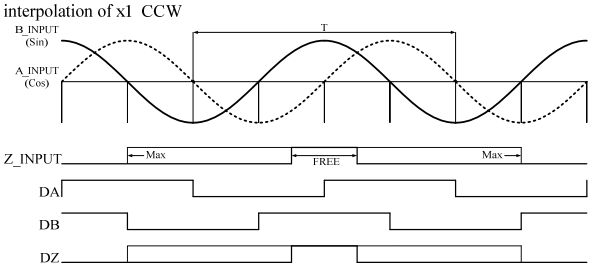
Timing Diagrams

Interpolation Function and Z-phase Input/Output Timing

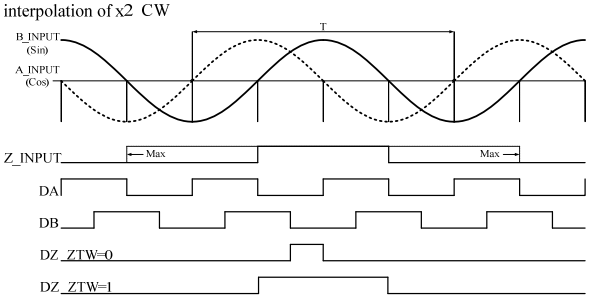
interpolation of x1 CW



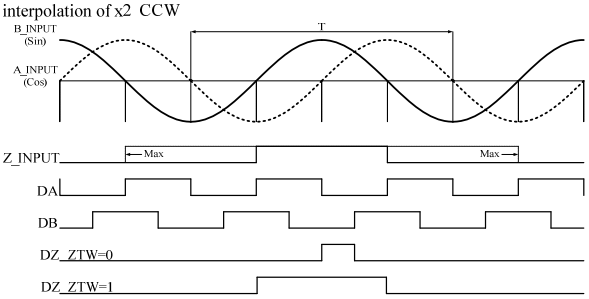
interpolation of x1 CCW



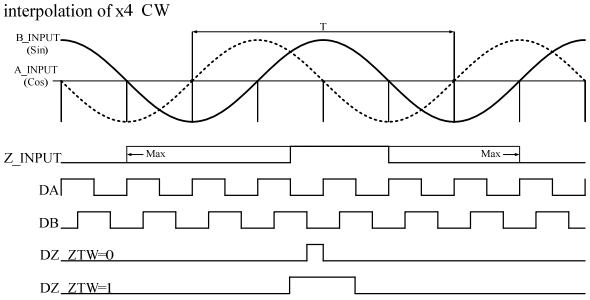
interpolation of x2 CW



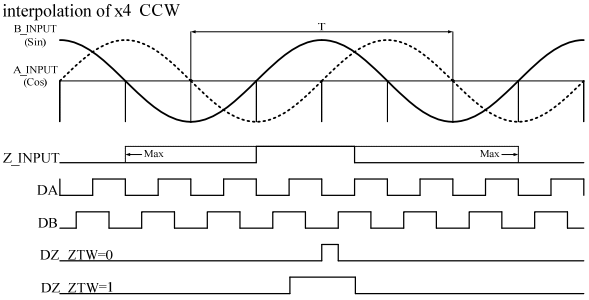
interpolation of x2 CCW



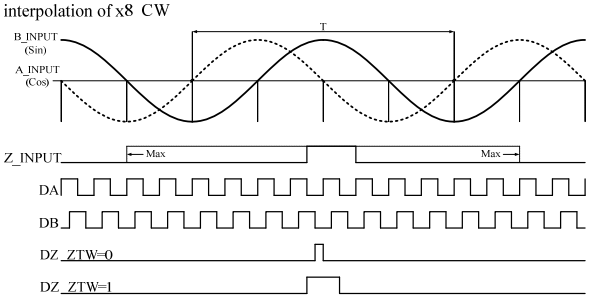
interpolation of x4 CW



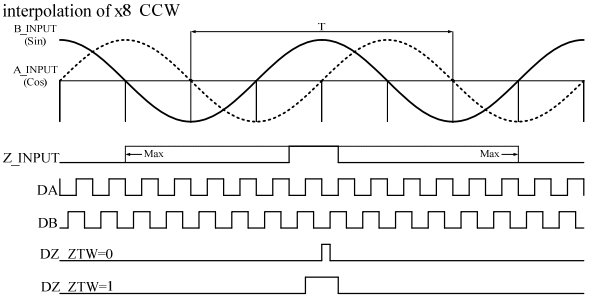
interpolation of x4 CCW



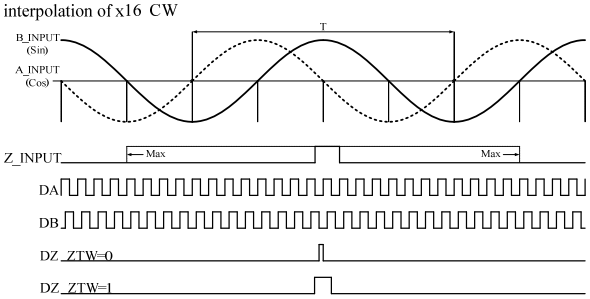
interpolation of x8 CW



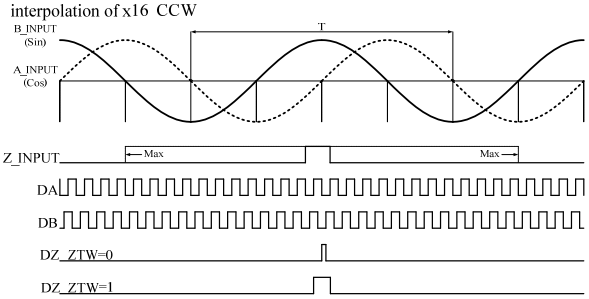
interpolation of x8 CCW



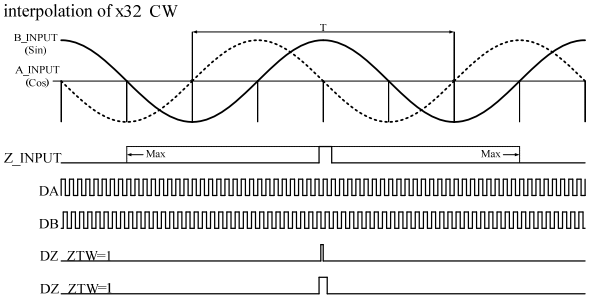
interpolation of x16 CW



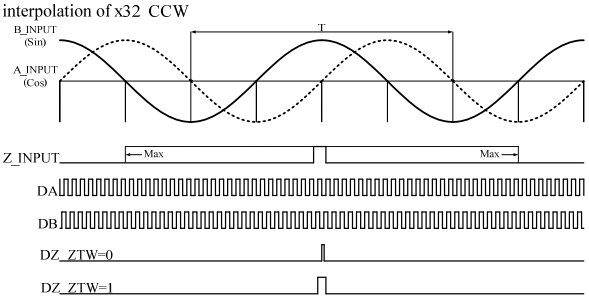
interpolation of x16 CCW



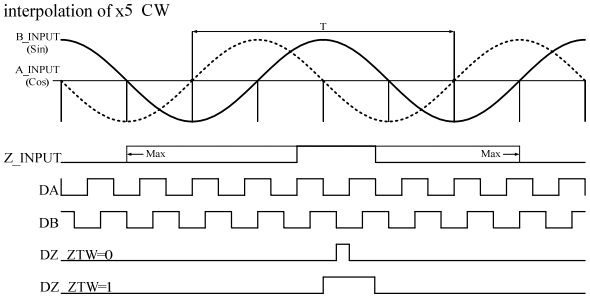
interpolation of x32 CW



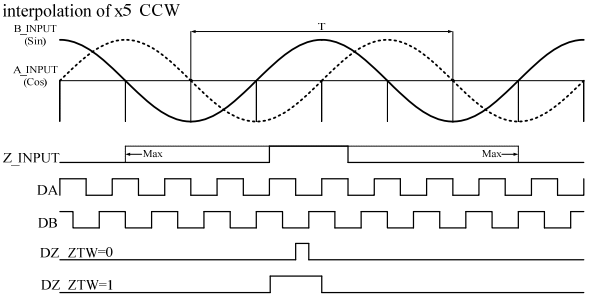
interpolation of x32 CCW



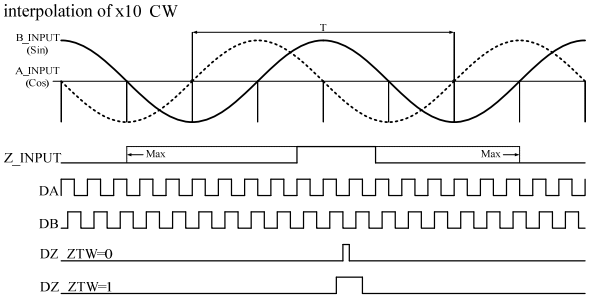
interpolation of x5 CW



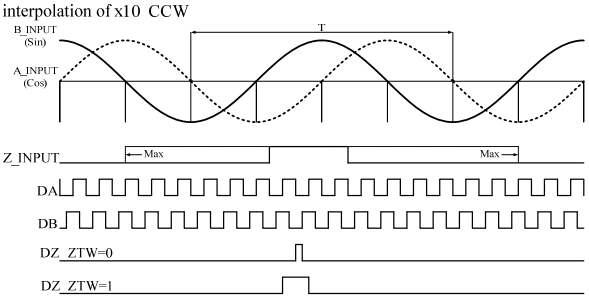
interpolation of x5 CCW



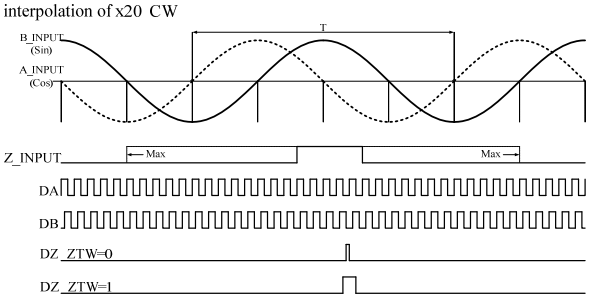
interpolation of x10 CW



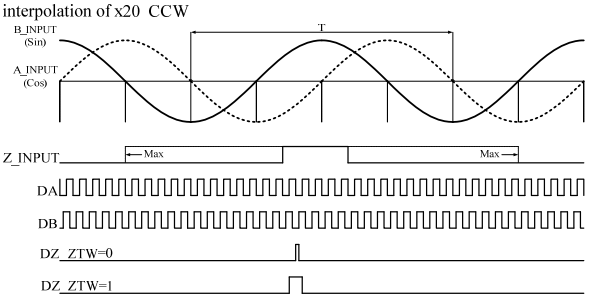
interpolation of x10 CCW



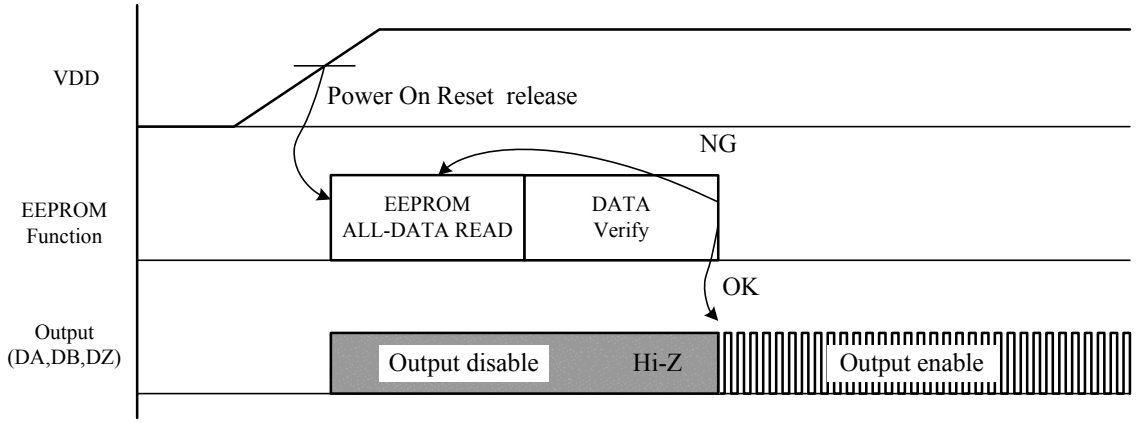
interpolation of x20 CW



interpolation of x20 CCW



Power-ON Timing



When power is applied, the settings written in EEPROM and the adjustment data are automatically transferred to the register. During this interval, the outputs are disabled (Hi-Z). If there is a discrepancy between the data written to the resister and the EEPROM data after data verification, the EEPROM settings are automatically transferred again and then the outputs are enabled if the data matches. The automatic transfer time is 200µs or less. During this interval, the VPP terminal should be left open. If a voltage is applied to VPP, the automatic transfer of settings is aborted.

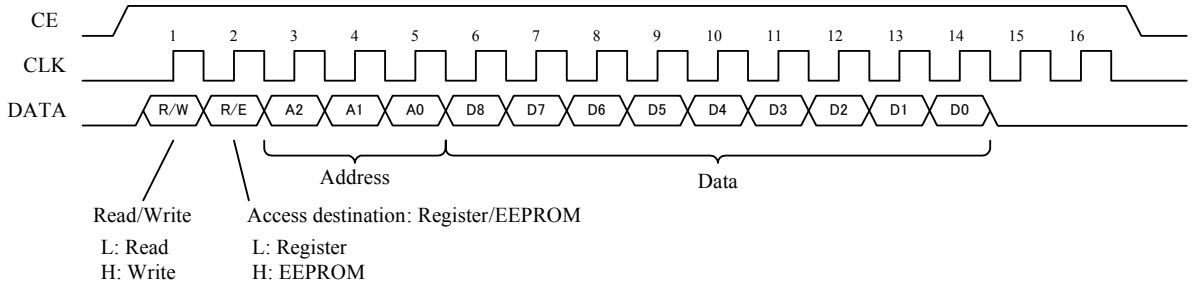
Serial Interface

The IC has a built-in EEPROM for the register for the analog circuit adjustment and operating mode settings, and for data retention. The EEPROM is accessed using a 3-wire serial interface.

The CE, CLK, and DATA signal inputs are used only when writing and reading data, and should not be modified at other times to prevent incorrect operation.

The serial interface is disabled during the interval while the settings are automatically transferred from EEPROM to the register after power is applied.

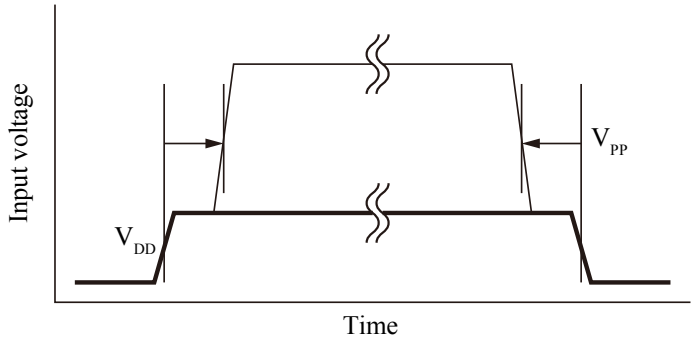
Data Format



* The read and write data are not guaranteed if there are too many or too few CLK pulses.
* Control the EEPROM data write time using the HIGH-level pulse time of the 15th and 16th pulses on CLK.
* The operating mode setting is ignored when writing to EEPROM. The mode is set when writing to the register.

VPP Terminal

Apply the high-voltage write-pulse voltage (V_{PP}) to the EEPROM program terminal VPP only after the voltage (V_{DD}) rising edge on VDD. Also, the falling edge of V_{PP} should precede the falling edge of V_{DD}.



Address Structure

Mode	Address			Data								
	A2	A1	A0	D8	D7	D6	D5	D4	D3	D2	D1	D0
Input, interpolation factor, operating mode settings	0	0	0	ZI	ABI	TB[3:0]				MC[2:0]		
-*1	0	0	1	-	-	-	-	-	-	-	-	-
Offset voltage adjustment (A-phase inverting output amplifier)	0	1	0	-	FA[7:0]							
Offset voltage adjustment (B-phase inverting output amplifier)	0	1	1	-	FB[7:0]							
Offset voltage adjustment (Z-phase non-inverting/inverting output amplifier)	1	0	0	FZN[2:0]			FZ[5:0]					
Offset voltage adjustment (A-phase non-inverting output amplifier)	1	0	1	-	-	-	-	FAN[4:0]				
Z-phase output pulse setting, Offset voltage adjustment (B-phase non-inverting output amplifier)	1	1	0	ZTW	0*2	-	-	FBN[4:0]				
-*1	1	1	1	-	-	-	-	-	-	-	-	-

*1. Address 001 and 111 are prohibited for use.
*2. This bit should be set to 0.
*3. All EEPROM data is set to 0 when shipped from the factory.

Analog Adjustment Bit Assignment

■ Analog input setting

Z	ABI	Analog input setting
0	0	A-phase, B-phase Z-phase differential input
0	1	A-phase, B-phase single-ended input Z-phase differential input
1	0	A-phase, B-phase differential input Z-phase single-ended input
1	1	A-phase, B-phase Z-phase single-ended input

* Single-ended inputs AN, BN, ZN = V_{DD}/2 level.

■ Interpolation factor setting TB[3:0]

TB3	TB2	TB1	TB0	Interpolation factor
0	0	0	0	1
-	0	0	1	2
-	0	1	0	4
-	0	1	1	8
-	1	0	0	16
-	1	0	1	32
-	1	1	0	5
-	1	1	1	20
1	0	0	0	10

■Operating mode setting (output terminal setting)

MC2	MC1	MC0	DA pin	DB pin	DZ pin	IO1 pin	IO2 pin	IO3 pin	Notes
0	0	0	A-phase interpolation output	B-phase interpolation output	Z-phase output	Hi-Z	Hi-Z	Hi-Z	Digital single-ended output
0	0	1	A-phase interpolation output	B-phase interpolation output	Z-phase output	A-phase interpolation inverting output (DA inverse)	A-phase interpolation inverting output (DB inverse)	Z-phase inverting output (DZ inverse)	Digital differential output
0	1	0	A-phase amplifier non-inverting output	B-phase amplifier non-inverting output	Z-phase amplifier non-inverting output	Hi-Z	Hi-Z	Hi-Z	Analog single-ended output
0	1	1	A-phase amplifier non-inverting output	B-phase amplifier non-inverting output	Z-phase amplifier non-inverting output	A-phase amplifier inverting output	B-phase amplifier inverting output	Z-phase amplifier inverting output	Analog differential output
1	0	0	Not used						
1	0	1							
1	1	0							
1	1	1							

■ Offset voltage adjustment 1 (FA[7:0], FB[7:0])

F7	F6	F5	F4	F3	F2	F1	F0	Offset [mV]	Tolerance [mV]
0	1	1	1	1	1	1	1	2995	3.9
0	1	1	1	1	1	1	0	2991	3.9
0	1	1	1	1	1	0	1	2988	3.9
0	1	1	1	1	1	0	0	2984	3.9
0	1	1	1	1	0	1	1	2980	3.9
0	1	1	1	1	0	1	0	2976	3.9
0	1	1	1	1	0	0	1	2972	3.9
0	1	1	1	1	0	0	0	2968	3.9
0	1	1	1	0	1	1	1	2964	3.9
0	1	1	1	0	1	1	0	2960	3.9
0	1	1	1	0	1	0	1	2956	3.9
0	1	1	1	0	1	0	0	2952	3.9
0	1	1	1	0	0	1	1	2949	3.9
0	1	1	1	0	0	1	0	2945	3.9
0	1	1	1	0	0	0	1	2941	3.9
0	1	1	1	0	0	0	0	2937	3.9
0	1	1	0	1	1	1	1	2933	3.9
0	1	1	0	1	1	1	0	2929	3.9
0	1	1	0	1	1	0	1	2925	3.9
0	1	1	0	1	1	0	0	2921	3.9
0	1	1	0	1	0	1	1	2917	3.9
0	1	1	0	1	0	1	0	2913	3.9
0	1	1	0	1	0	0	1	2910	3.9
0	1	1	0	1	0	0	0	2906	3.9
0	1	1	0	0	1	1	1	2902	3.9
0	1	1	0	0	1	1	0	2898	3.9
0	1	1	0	0	1	0	1	2894	3.9
0	1	1	0	0	1	0	0	2890	3.9
0	1	1	0	0	0	1	1	2886	3.9
0	1	1	0	0	0	1	0	2882	3.9
0	1	1	0	0	0	0	1	2878	3.9
0	1	1	0	0	0	0	0	2874	3.9
0	1	0	1	1	1	1	1	2871	3.9
0	1	0	1	1	1	1	0	2867	3.9
0	1	0	1	1	1	0	1	2863	3.9
0	1	0	1	1	1	0	0	2859	3.9
0	1	0	1	1	0	1	1	2855	3.9
0	1	0	1	1	0	1	0	2851	3.9
0	1	0	1	1	0	0	1	2847	3.9
0	1	0	1	1	0	0	0	2843	3.9
0	1	0	1	0	1	1	1	2839	3.9
0	1	0	1	0	1	1	0	2835	3.9
0	1	0	1	0	1	0	1	2832	3.9
0	1	0	1	0	1	0	0	2828	3.9
0	1	0	1	0	0	1	1	2824	3.9
0	1	0	1	0	0	1	0	2820	3.9
0	1	0	1	0	0	0	1	2816	3.9
0	1	0	1	0	0	0	0	2812	3.9
0	1	0	0	1	1	1	1	2808	3.9
0	1	0	0	1	1	1	0	2804	3.9
0	1	0	0	1	1	0	1	2800	3.9
0	1	0	0	1	1	0	0	2796	3.9
0	1	0	0	1	0	1	1	2793	3.9
0	1	0	0	1	0	1	0	2789	3.9
0	1	0	0	1	0	0	1	2785	3.9
0	1	0	0	1	0	0	0	2781	3.9
0	1	0	0	0	1	1	1	2777	3.9
0	1	0	0	0	1	1	0	2773	3.9
0	1	0	0	0	1	0	1	2769	3.9
0	1	0	0	0	1	0	0	2765	3.9
0	1	0	0	0	0	1	1	2761	3.9
0	1	0	0	0	0	1	0	2757	3.9
0	1	0	0	0	0	0	1	2754	3.9
0	1	0	0	0	0	0	0	2750	3.9

F7	F6	F5	F4	F3	F2	F1	F0	Offset [mV]	Tolerance [mV]
0	0	1	1	1	1	1	1	2746	3.9
0	0	1	1	1	1	1	0	2742	3.9
0	0	1	1	1	1	0	1	2738	3.9
0	0	1	1	1	1	0	0	2734	3.9
0	0	1	1	1	0	1	1	2730	3.9
0	0	1	1	1	0	1	0	2726	3.9
0	0	1	1	1	0	0	1	2722	3.9
0	0	1	1	1	0	0	0	2718	3.9
0	0	1	1	0	1	1	1	2715	3.9
0	0	1	1	0	1	1	0	2711	3.9
0	0	1	1	0	1	0	1	2707	3.9
0	0	1	1	0	1	0	0	2703	3.9
0	0	1	1	0	0	1	1	2699	3.9
0	0	1	1	0	0	1	0	2695	3.9
0	0	1	1	0	0	0	1	2691	3.9
0	0	1	1	0	0	0	0	2687	3.9
0	0	1	0	1	1	1	1	2683	3.9
0	0	1	0	1	1	1	0	2679	3.9
0	0	1	0	1	1	0	1	2676	3.9
0	0	1	0	1	1	0	0	2672	3.9
0	0	1	0	1	0	1	1	2668	3.9
0	0	1	0	1	0	1	0	2664	3.9
0	0	1	0	1	0	0	1	2660	3.9
0	0	1	0	1	0	0	0	2656	3.9
0	0	1	0	0	1	1	1	2652	3.9
0	0	1	0	0	1	1	0	2648	3.9
0	0	1	0	0	1	0	1	2644	3.9
0	0	1	0	0	1	0	0	2640	3.9
0	0	1	0	0	0	1	1	2637	3.9
0	0	1	0	0	0	1	0	2633	3.9
0	0	1	0	0	0	0	1	2629	3.9
0	0	1	0	0	0	0	0	2625	3.9
0	0	0	1	1	1	1	1	2621	3.9
0	0	0	1	1	1	1	0	2617	3.9
0	0	0	1	1	1	0	1	2613	3.9
0	0	0	1	1	1	0	0	2609	3.9
0	0	0	1	1	0	1	1	2605	3.9
0	0	0	1	1	0	1	0	2601	3.9
0	0	0	1	1	0	0	1	2598	3.9
0	0	0	1	1	0	0	0	2594	3.9
0	0	0	1	0	1	1	1	2590	3.9
0	0	0	1	0	1	1	0	2586	3.9
0	0	0	1	0	1	0	1	2582	3.9
0	0	0	1	0	1	0	0	2578	3.9
0	0	0	1	0	0	1	1	2574	3.9
0	0	0	1	0	0	1	0	2570	3.9
0	0	0	1	0	0	0	1	2566	3.9
0	0	0	1	0	0	0	0	2562	3.9
0	0	0	0	1	1	1	1	2559	3.9
0	0	0	0	1	1	1	0	2555	3.9
0	0	0	0	1	1	0	1	2551	3.9
0	0	0	0	1	1	0	0	2547	3.9
0	0	0	0	1	0	1	1	2543	3.9
0	0	0	0	1	0	1	0	2539	3.9
0	0	0	0	1	0	0	1	2535	3.9
0	0	0	0	1	0	0	0	2531	3.9
0	0	0	0	0	1	1	1	2527	3.9
0	0	0	0	0	1	1	0	2523	3.9
0	0	0	0	0	1	0	1	2520	3.9
0	0	0	0	0	1	0	0	2516	3.9
0	0	0	0	0	0	1	1	2512	3.9
0	0	0	0	0	0	1	0	2508	3.9
0	0	0	0	0	0	0	1	2504	3.9
0	0	0	0	0	0	0	0	2500	-

Offset voltage example at V_{DD}=5.0V.

■ Offset voltage adjustment 2 (FA[7:0], FB[7:0])

F7	F6	F5	F4	F3	F2	F1	F0	Offset [mV]	Tolerance [mV]
1	1	1	1	1	1	1	1	2496	3.9
1	1	1	1	1	1	1	0	2492	3.9
1	1	1	1	1	1	0	1	2488	3.9
1	1	1	1	1	1	0	0	2484	3.9
1	1	1	1	1	0	1	1	2481	3.9
1	1	1	1	1	0	1	0	2477	3.9
1	1	1	1	1	0	0	1	2473	3.9
1	1	1	1	1	0	0	0	2469	3.9
1	1	1	1	0	1	1	1	2465	3.9
1	1	1	1	0	1	1	0	2461	3.9
1	1	1	1	0	1	0	1	2457	3.9
1	1	1	1	0	1	0	0	2453	3.9
1	1	1	1	0	0	1	1	2449	3.9
1	1	1	1	0	0	1	0	2445	3.9
1	1	1	1	0	0	0	1	2442	3.9
1	1	1	1	0	0	0	0	2438	3.9
1	1	1	0	1	1	1	1	2434	3.9
1	1	1	0	1	1	1	0	2430	3.9
1	1	1	0	1	1	0	1	2426	3.9
1	1	1	0	1	1	0	0	2422	3.9
1	1	1	0	1	0	1	1	2418	3.9
1	1	1	0	1	0	1	0	2414	3.9
1	1	1	0	1	0	0	1	2410	3.9
1	1	1	0	1	0	0	0	2406	3.9
1	1	1	0	0	1	1	1	2403	3.9
1	1	1	0	0	1	1	0	2399	3.9
1	1	1	0	0	1	0	1	2395	3.9
1	1	1	0	0	1	0	0	2391	3.9
1	1	1	0	0	0	1	1	2387	3.9
1	1	1	0	0	0	1	0	2383	3.9
1	1	1	0	0	0	0	1	2379	3.9
1	1	1	0	0	0	0	0	2375	3.9
1	1	0	1	1	1	1	1	2371	3.9
1	1	0	1	1	1	1	0	2367	3.9
1	1	0	1	1	1	0	1	2364	3.9
1	1	0	1	1	1	0	0	2360	3.9
1	1	0	1	1	0	1	1	2356	3.9
1	1	0	1	1	0	1	0	2352	3.9
1	1	0	1	1	0	0	1	2348	3.9
1	1	0	1	1	0	0	0	2344	3.9
1	1	0	1	0	1	1	1	2340	3.9
1	1	0	1	0	1	1	0	2336	3.9
1	1	0	1	0	1	0	1	2332	3.9
1	1	0	1	0	1	0	0	2328	3.9
1	1	0	1	0	0	1	1	2325	3.9
1	1	0	1	0	0	1	0	2321	3.9
1	1	0	1	0	0	0	1	2317	3.9
1	1	0	1	0	0	0	0	2313	3.9
1	1	0	0	1	1	1	1	2309	3.9
1	1	0	0	1	1	1	0	2305	3.9
1	1	0	0	1	1	0	1	2301	3.9
1	1	0	0	1	1	0	0	2297	3.9
1	1	0	0	1	0	1	1	2293	3.9
1	1	0	0	1	0	1	0	2289	3.9
1	1	0	0	1	0	0	1	2286	3.9
1	1	0	0	1	0	0	0	2282	3.9
1	1	0	0	0	1	1	1	2278	3.9
1	1	0	0	0	1	1	0	2274	3.9
1	1	0	0	0	1	0	1	2270	3.9
1	1	0	0	0	1	0	0	2266	3.9
1	1	0	0	0	0	1	1	2262	3.9
1	1	0	0	0	0	1	0	2258	3.9
1	1	0	0	0	0	0	1	2254	3.9
1	1	0	0	0	0	0	0	2250	3.9

F7	F6	F5	F4	F3	F2	F1	F0	Offset [mV]	Tolerance [mV]
1	0	1	1	1	1	1	1	2247	3.9
1	0	1	1	1	1	1	0	2243	3.9
1	0	1	1	1	1	0	1	2239	3.9
1	0	1	1	1	1	0	0	2235	3.9
1	0	1	1	1	0	1	1	2231	3.9
1	0	1	1	1	0	1	0	2227	3.9
1	0	1	1	1	0	0	1	2223	3.9
1	0	1	1	1	0	0	0	2219	3.9
1	0	1	1	0	1	1	1	2215	3.9
1	0	1	1	0	1	1	0	2211	3.9
1	0	1	1	0	1	0	1	2208	3.9
1	0	1	1	0	1	0	0	2204	3.9
1	0	1	1	0	0	1	1	2200	3.9
1	0	1	1	0	0	1	0	2196	3.9
1	0	1	1	0	0	0	1	2192	3.9
1	0	1	1	0	0	0	0	2188	3.9
1	0	1	0	1	1	1	1	2184	3.9
1	0	1	0	1	1	1	0	2180	3.9
1	0	1	0	1	1	0	1	2176	3.9
1	0	1	0	1	1	0	0	2172	3.9
1	0	1	0	1	0	1	1	2169	3.9
1	0	1	0	1	0	1	0	2165	3.9
1	0	1	0	1	0	0	1	2161	3.9
1	0	1	0	1	0	0	0	2157	3.9
1	0	1	0	0	1	1	1	2153	3.9
1	0	1	0	0	1	1	0	2149	3.9
1	0	1	0	0	1	0	1	2145	3.9
1	0	1	0	0	1	0	0	2141	3.9
1	0	1	0	0	0	1	1	2137	3.9
1	0	1	0	0	0	1	0	2133	3.9
1	0	1	0	0	0	0	1	2130	3.9
1	0	1	0	0	0	0	0	2126	3.9
1	0	0	1	1	1	1	1	2122	3.9
1	0	0	1	1	1	1	0	2118	3.9
1	0	0	1	1	1	0	1	2114	3.9
1	0	0	1	1	1	0	0	2110	3.9
1	0	0	1	1	0	1	1	2106	3.9
1	0	0	1	1	0	1	0	2102	3.9
1	0	0	1	1	0	0	1	2098	3.9
1	0	0	1	1	0	0	0	2094	3.9
1	0	0	1	0	1	1	1	2091	3.9
1	0	0	1	0	1	1	0	2087	3.9
1	0	0	1	0	1	0	1	2083	3.9
1	0	0	1	0	1	0	0	2079	3.9
1	0	0	1	0	0	1	1	2075	3.9
1	0	0	1	0	0	1	0	2071	3.9
1	0	0	1	0	0	0	1	2067	3.9
1	0	0	1	0	0	0	0	2063	3.9
1	0	0	0	1	1	1	1	2059	3.9
1	0	0	0	1	1	1	0	2055	3.9
1	0	0	0	1	1	0	1	2052	3.9
1	0	0	0	1	1	0	0	2048	3.9
1	0	0	0	1	0	1	1	2044	3.9
1	0	0	0	1	0	1	0	2040	3.9
1	0	0	0	1	0	0	1	2036	3.9
1	0	0	0	1	0	0	0	2032	3.9
1	0	0	0	0	1	1	1	2028	3.9
1	0	0	0	0	1	1	0	2024	3.9
1	0	0	0	0	1	0	1	2020	3.9
1	0	0	0	0	1	0	0	2016	3.9
1	0	0	0	0	0	1	1	2013	3.9
1	0	0	0	0	0	1	0	2009	3.9
1	0	0	0	0	0	0	1	2005	3.9
1	0	0	0	0	0	0	0	2001	3.9

* Offset voltage example at V_{DD}=5.0V.

■ Offset voltage adjustment (FZ[5:0])

F5	F4	F3	F2	F1	F0	Offset [mV]	Tolerance [mV]
0	1	1	1	1	1	2996	16
0	1	1	1	1	0	2980	16
0	1	1	1	0	1	2964	16
0	1	1	1	0	0	2948	16
0	1	1	0	1	1	2932	16
0	1	1	0	1	0	2916	16
0	1	1	0	0	1	2900	16
0	1	1	0	0	0	2884	16
0	1	0	1	1	1	2868	16
0	1	0	1	1	0	2852	16
0	1	0	1	0	1	2836	16
0	1	0	1	0	0	2820	16
0	1	0	0	1	1	2804	16
0	1	0	0	1	0	2788	16
0	1	0	0	0	1	2772	16
0	1	0	0	0	0	2756	16
0	0	1	1	1	1	2740	16
0	0	1	1	1	0	2724	16
0	0	1	1	0	1	2708	16
0	0	1	1	0	0	2692	16
0	0	1	0	1	1	2676	16
0	0	1	0	1	0	2660	16
0	0	1	0	0	1	2644	16
0	0	1	0	0	0	2628	16
0	0	0	1	1	1	2612	16
0	0	0	1	1	0	2596	16
0	0	0	1	0	1	2580	16
0	0	0	1	0	0	2564	16
0	0	0	0	1	1	2548	16
0	0	0	0	1	0	2532	16
0	0	0	0	0	1	2516	16
0	0	0	0	0	0	2500	-

F5	F4	F3	F2	F1	F0	Offset [mV]	Tolerance [mV]
1	1	1	1	1	1	2484	16
1	1	1	1	1	0	2468	16
1	1	1	1	0	1	2452	16
1	1	1	1	0	0	2436	16
1	1	1	0	1	1	2420	16
1	1	1	0	1	0	2404	16
1	1	1	0	0	1	2388	16
1	1	1	0	0	0	2372	16
1	1	0	1	1	1	2356	16
1	1	0	1	1	0	2340	16
1	1	0	1	0	1	2324	16
1	1	0	1	0	0	2308	16
1	1	0	0	1	1	2292	16
1	1	0	0	1	0	2276	16
1	1	0	0	0	1	2260	16
1	1	0	0	0	0	2244	16
1	0	1	1	1	1	2228	16
1	0	1	1	1	0	2212	16
1	0	1	1	0	1	2196	16
1	0	1	1	0	0	2180	16
1	0	1	0	1	1	2164	16
1	0	1	0	1	0	2148	16
1	0	1	0	0	1	2132	16
1	0	1	0	0	0	2116	16
1	0	0	1	1	1	2100	16
1	0	0	1	1	0	2084	16
1	0	0	1	0	1	2068	16
1	0	0	1	0	0	2052	16
1	0	0	0	1	1	2036	16
1	0	0	0	1	0	2020	16
1	0	0	0	0	1	2004	16
1	0	0	0	0	0	1988	16

* Offset voltage example at V_{DD}=5.0V.

■ A/B-phase non-inverting output amplifier offset Voltage adjustment (FAN[4:0], FBN[4:0])

FN4	FN3	FN2	FN1	FN0	Offset [mV]	Tolerance [mV]
0	1	1	1	1	2541	2.7
0	1	1	1	0	2538	2.7
0	1	1	0	1	2535	2.7
0	1	1	0	0	2532	2.7
0	1	0	1	1	2530	2.7
0	1	0	1	0	2527	2.7
0	1	0	0	1	2524	2.7
0	1	0	0	0	2522	2.7
0	0	1	1	1	2519	2.7
0	0	1	1	0	2516	2.7
0	0	1	0	1	2514	2.7
0	0	1	0	0	2511	2.7
0	0	0	1	1	2508	2.7
0	0	0	1	0	2505	2.7
0	0	0	0	1	2503	2.7
0	0	0	0	0	2500	-

FN4	FN3	FN2	FN1	FN0	Offset [mV]	Tolerance [mV]
1	1	1	1	1	2497	2.7
1	1	1	1	0	2495	2.7
1	1	1	0	1	2492	2.7
1	1	1	0	0	2489	2.7
1	1	0	1	1	2487	2.7
1	1	0	1	0	2484	2.7
1	1	0	0	1	2481	2.7
1	1	0	0	0	2478	2.7
1	0	1	1	1	2476	2.7
1	0	1	1	0	2473	2.7
1	0	1	0	1	2470	2.7
1	0	1	0	0	2468	2.7
1	0	0	1	1	2465	2.7
1	0	0	1	0	2462	2.7
1	0	0	0	1	2460	2.7
1	0	0	0	0	2457	2.7

* Offset voltage example at V_{DD}=5.0V.

■ Z-phase non-inverting output amplifier offset Voltage adjustment (FZN[2:0])

FN2	FN1	FN0	Offset [mV]	Tolerance [mV]
0	1	1	2518	6.0
0	1	0	2512	6.0
0	0	1	2506	6.0
0	0	0	2500	-
1	1	1	2494	6.0
1	1	0	2488	6.0
1	0	1	2482	6.0
1	0	0	2476	6.0

Offset voltage example at V_{DD}=5.0V.

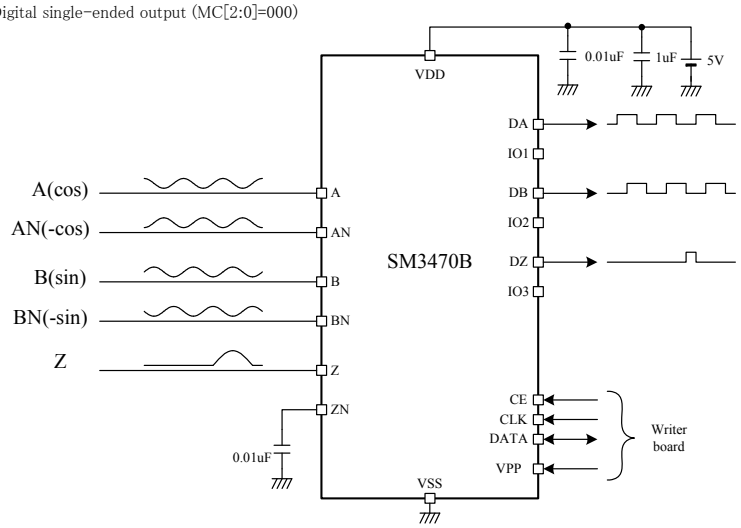
■ Z-phase output pulsewidth setting
See "Z-phase Output Timing" on Page 9-10

ZTW	Pulse width (T=output period)
0	T/4 (DA=LOW, DB=LOW)
1	T (clockwise direction, sync on DA falling edge)

TYPICAL APPLICATION CIRCUITS

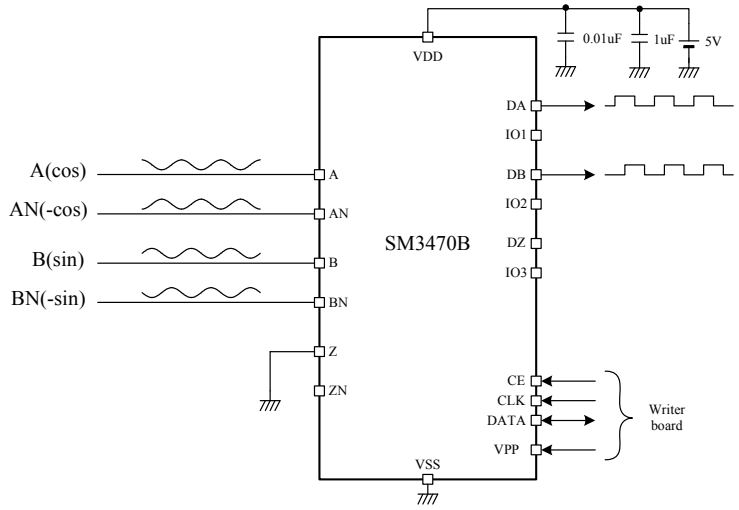
Typical Application Circuit 1

Operating condition: A/B-phase differential input (ABI=0)
(Register setting) Z-phase single-ended input (ZI=1)
Digital single-ended output (MC[2:0]=000)



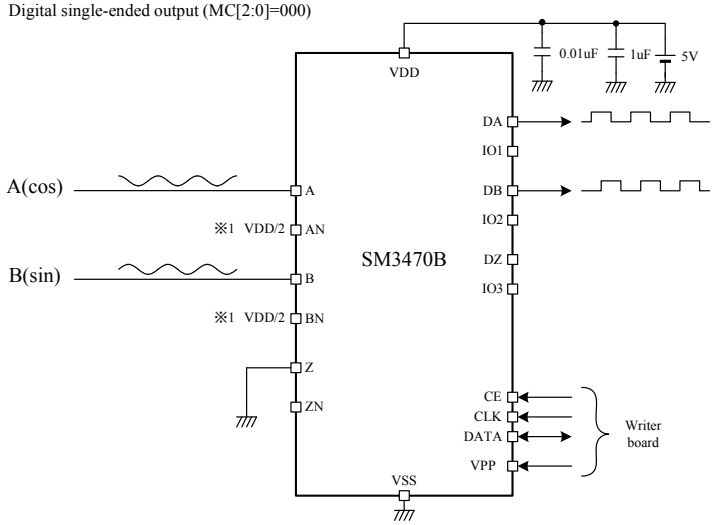
Typical Application Circuit 2

Operating condition: A/B-phase differential input (ABI=0)
(Register setting): Z-phase not used, single-ended input setting (ZI=1)
Digital single-ended output (MC[2:0]=000)



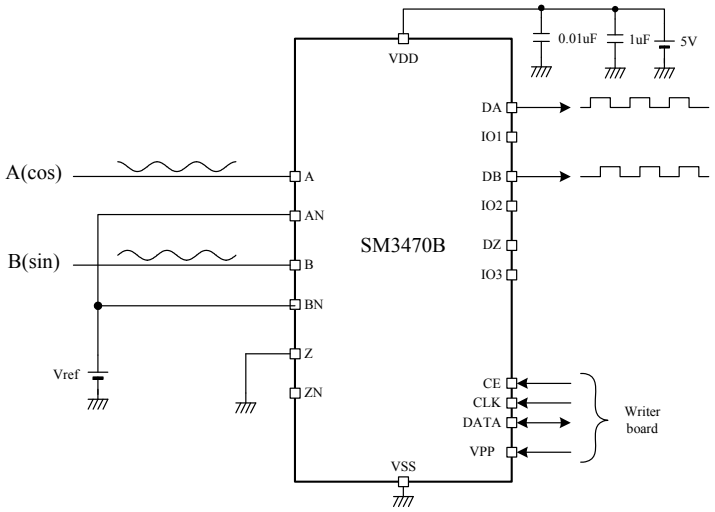
Typical Application Circuit 3

Operating condition: A/B-phase single-ended input (ABI=1)
*1: AN and BN are set to $V_{DD}/2$ internally.
(Register setting): Z-phase not used, single-ended input setting (ZI=1)
Digital single-ended output (MC[2:0]=000)



Typical Application Circuit 4

Operating condition: A/B-phase differential input (ABI=0)
(Register setting): Z-phase not used, single-ended input setting (ZI=1)
Digital single-ended output (MC[2:0]=000)



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