## OVERVIEW

The SM3471 is an interpolation IC for encoders. It accepts displacement detection, 2-phase analog signals (A and B phases) and a zero point detection analog signal (Z phase) from an encoder, interpolates the signals by a specified interpolation factor, and outputs corresponding 2-phase digital signals (A and B phases) and a zero point detection digital signal (Z phase).

## FEATURES

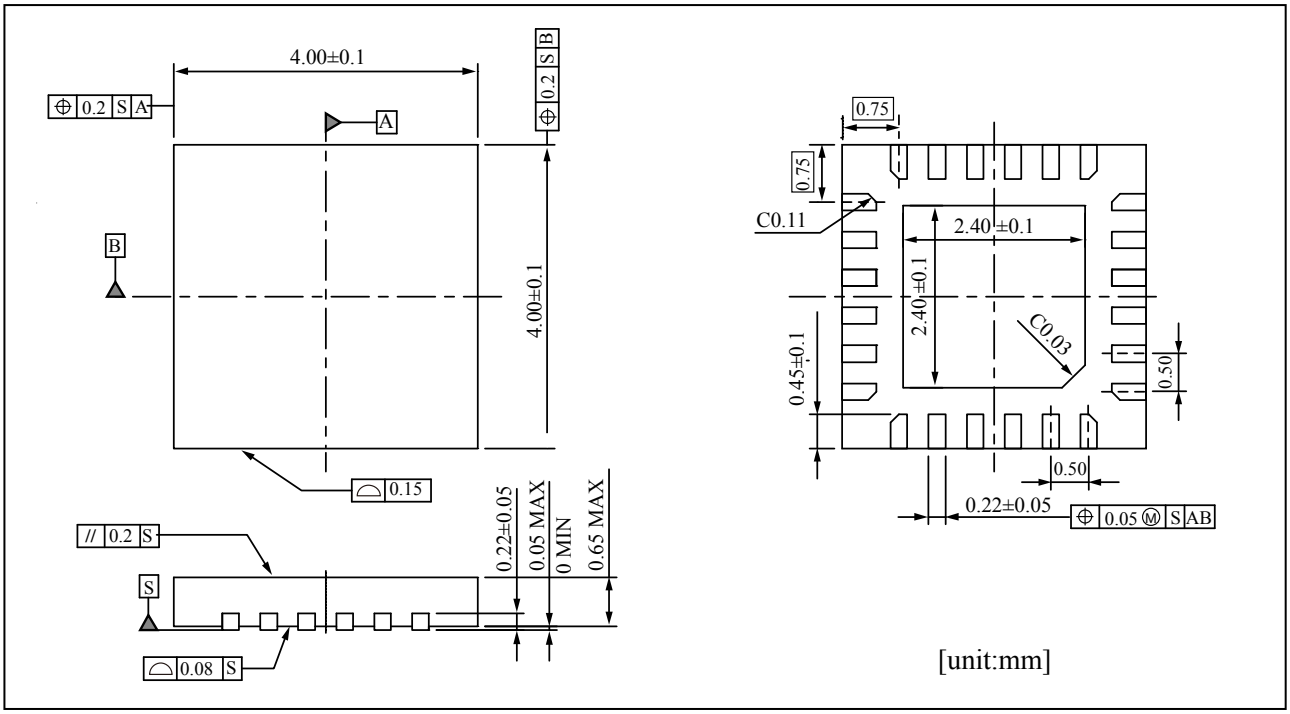
- Interpolation switching function: ×2, 4, 8, 16 (selectable)
- Input frequency: 300kHz (max)
- Output frequency: 2.5MHz (max)
- Supply voltage: 2.7 to 5.5V
- Operating temperature range: –40 to +125°C
- Package: QFN24 (size: 4mm × 4mm)

## ORDERING INFORMATION

| Device | Package |
|---|---|
| SM3471AB-G*1 | 24 pin QFN |

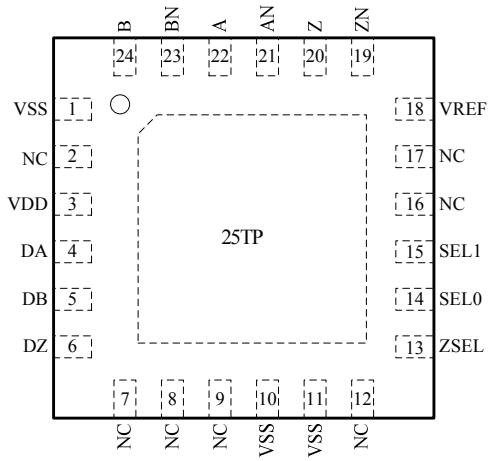
*1. "-G" option code lead-free package

## PACKAGE DIMENSIONS



## PINOUT

QFN24 package
(Top view)

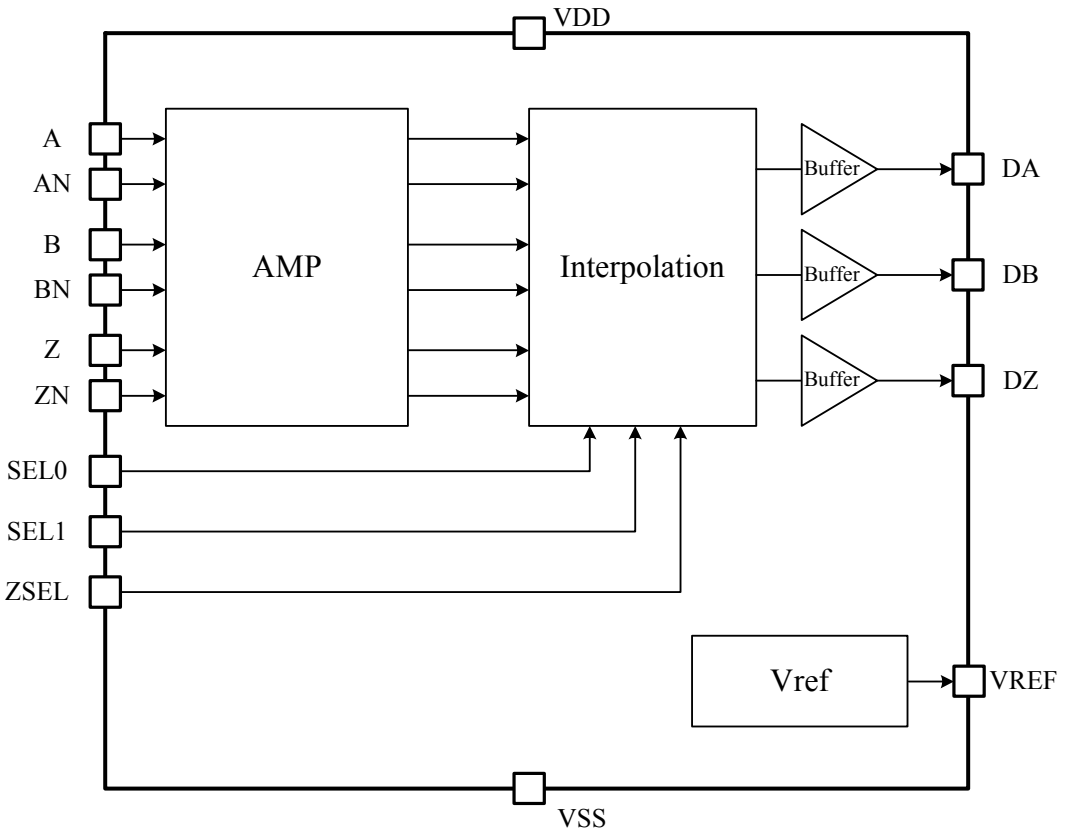



## PIN DESCRIPTION

| Pin No. | Name | I/O[*1] | Description |
|---|---|---|---|
| 1 | VSS | - | Ground |
| 2 | NC | - | No connection |
| 3 | VDD | - | Power supply |
| 4 | DA | O | Displacement detector signal output (A) |
| 5 | DB | O | Displacement detector signal output (B) |
| 6 | DZ | O | Zero point detector signal output (Z) |
| 7 | NC | - | No connection |
| 8 | NC | - | No connection |
| 9 | NC | - | No connection |
| 10 | VSS | - | Ground |
| 11 | VSS | - | Ground |
| 12 | NC | - | No connection |
| 13 | ZSEL | I | Z-phase output timing setting input with pull-down resistor |
| 14 | SEL0 | I | Interpolation setting input with pull-down resistor |
| 15 | SEL1 | I | Interpolation setting input with pull-down resistor |
| 16 | NC | - | No connection |
| 17 | NC | - | No connection |
| 18 | VREF | O | $V_{DD}$/2 level voltage output |
| 19 | ZN | I | Zero point detector inverse-phase signal input |
| 20 | Z | I | Zero point detector signal input |
| 21 | AN | I | Displacement detector signal (–cos) input |
| 22 | A | I | Displacement detector signal (cos) input |
| 23 | BN | I | Displacement detector signal (–sin) input |
| 24 | B | I | Displacement detector signal (sin) input |
| 25 | TP | - | Thermal pad. Connect to VSS or leave OPEN. |

*1. I: Input pin O: Output pin I/O: Input/Output pin
VSS terminals number 1, 10 and 11 must be connected to the ground on the mounting board.

## BLOCK DIAGRAM




## SPECIFICATIONS

### Absolute Maximum Ratings

$V_{SS}$=0V

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Supply voltage 1[*1] | $V_{DD}$ | VDD pin | –0.3 to +6.5 | V |
| Input voltage[*1,*4] | $V_{IN}$ | Input pins[*6] | –0.3 to $V_{DD}$+0.3 | V |
| Output voltage[*1,*4] | $V_{OUT}$ | Output pins[*7] | –0.3 to $V_{DD}$+0.3 | V |
| Output current[*2] | $I_{OUT}$ | Output pins[*7] | -1.8 to 1.8 | mA |
| Junction temperature[*3] | $T_j$ | | +150 | °C |
| Power dissipation[*1] | $P_D$ | $T_a$=25°C[*8] | 1570 | mW |
| Storage temperature[*5] | $T_{stg1}$ | | –40 to +125 | °C |

*1. Parameters must not exceed the ratings, not even momentarily. If the rating is exceeded, there is a risk of IC failure, deterioration in characteristics, and decrease in reliability.

*2. Parameter must not exceed the rating on average. If the rating is exceeded, there is a risk of IC failure, deterioration in characteristics and decrease in reliability.

*3. Parameter should not exceed the rating. If the rating is exceeded, there is a risk of deterioration in characteristics and decrease in reliability.

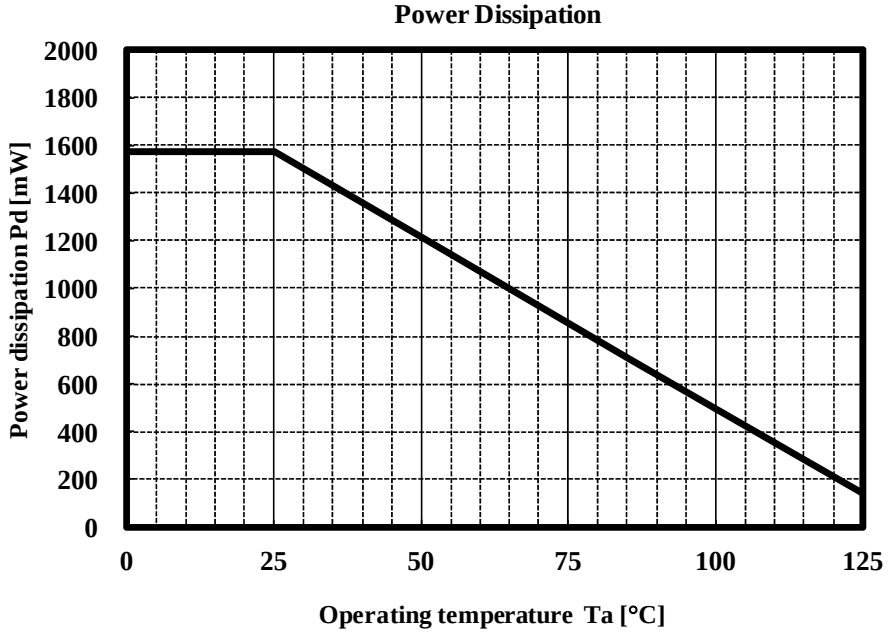
*4. $V_{DD}$ value is the recommended operating voltage rating.

*5. Stored separately without packing material in Nitrogen or vacuum atmosphere.

*6. SEL0, SEL1, ZSEL, A, AN, B, BN, Z, and ZN terminals.

*7. DA, DB, and DZ terminals.

*8. 114.3×76.2×1.6mm, 150% wiring ratio, FR-4 4-layer board (with thermal pad connections). Dissipation will vary due to differences in board specifications and footprint pattern.




## Recommended Operating Conditions

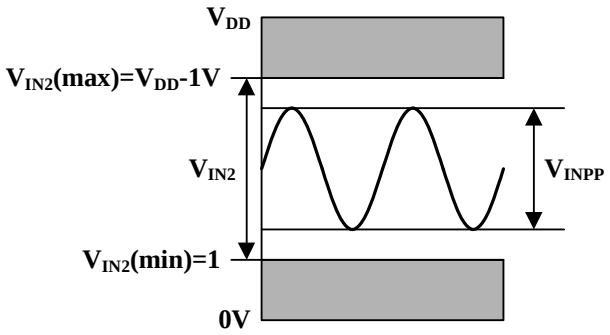
The recommended operating conditions are the conditions for which the electrical characteristics are guaranteed.

$V_{SS}$=0V

| Parameter | Symbol | Condition | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | VDD pin | 2.7 | - | 5.5 | V |
| Logic input voltage | $V_{IN1}$ | SEL0, SEL1, ZSEL pins | $V_{SS}$ | - | $V_{DD}$ | V |
| Analog Input voltage range*1 | $V_{IN2}$ | A, AN, B, BN, Z, and ZN pins | 1 | - | $V_{DD}$–1 | V |
| Input signal amplitude*1 | $V_{INPP}$ | A, AN, B, BN, Z, and ZN pins | 0.6 | - | - | Vpp |
| Input offset voltage*2 | $V_{OFFSET}$ | A-AN center offset<br>B-BN center offset<br>$V_{DD}$=5.0V, 25°C | -25 | - | 25 | mV |
| Input signal frequency | $F_{IN}$ | A, AN, B, BN, Z, and ZN pins | - | - | 300 | kHz |
| Operating temperature range | $T_a$ | | –40 | - | +125 | °C |

Note. Operation outside the recommended operating conditions may adversely affect reliability. Use only within specified ratings.

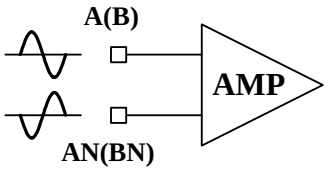
### *1 Definition $V_{IN2}$ and $V_{INPP}$




* Higher accuracy is obtained by increasing signal amplitude $V_{INPP}$, so largest value within the input voltage range is recommended.

### *2 Definition $V_{OFFSET}$

**A, AN(B, BN) each ±12.5mV**
**⇒Absolute value:25mV**



## Electrical Characteristics

$V_{DD}$=2.7 to 5.5V, $V_{SS}$=0V, Ta=–40 to +125°C unless otherwise noted

| Parameter | Symbol | Condition | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| Current consumption*1 | $I_{DD}$ | No load | - | 15 | 25 | mA |
| Logic input voltage*2 | $V_{IH}$ | | 0.7$V_{DD}$ | - | $V_{DD}$ | V |
| | $V_{IL}$ | | $V_{SS}$ | - | 0.3$V_{DD}$ | |
| Logic input current*2 | $I_{IH}$ | $V_{IN}$=$V_{DD}$, $T_a$=25°C | 20 | - | 200 | µA |
| | $I_{IL}$ | $V_{IN}$=$V_{SS}$, $T_a$=25°C | –1 | - | - | |
| Output voltage*3 | $V_{outH}$ | $I_{out}$ = +1.5mA | $V_{DD}$–0.4 | - | - | V |
| | $V_{outL}$ | $I_{out}$ = –1.5mA | - | - | 0.3 | |
| Output frequency | $f_{out}$ | | - | - | 2.5 | MHz |
| Angular error*4 (max – min) | $A_{RAL}$ | $V_{DD}$=5.0V, 16x interpolation, Input ideal sin(cos) wave, 10kHz input frequency, 3.0Vppinput amplitude | - | - | 6 | Degrees |
| Rise/Fall time | $t_{rf}$ | 0.1$V_{DD}$ to 0.9$V_{DD}$, CL=20pF | - | - | 10 | ns |

*1. Typical conditions: $V_{DD}$=5V, Ta=25°C, 8x interpolation, $F_{IN}$=10kHz

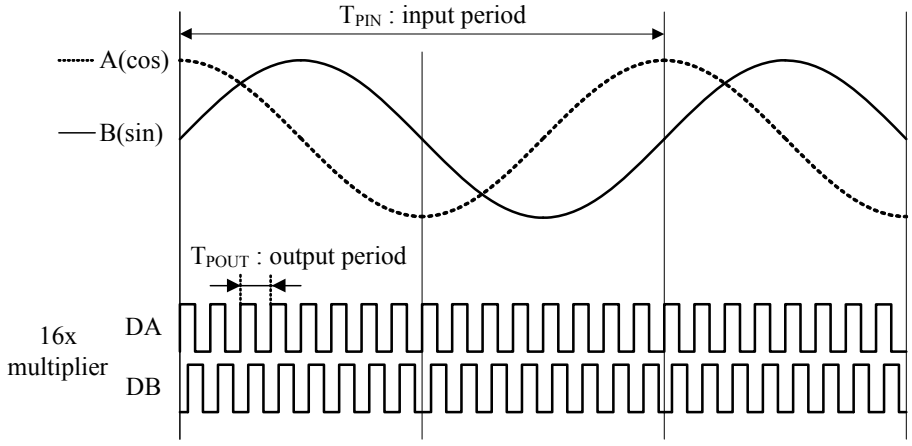
*2. SEL0, SEL1, and ZSEL terminals.

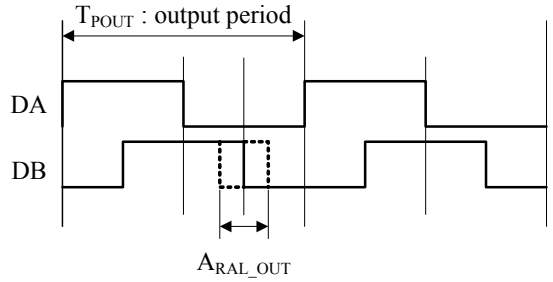
*3. DA, DB, and DZ terminals.

*4. The angular error expresses the variation from the ideal phase difference of interpolation outputs DA and DB as a phase difference of the input period. Converting 6° and expressing as a percentage of the output period gives 26.6% using equation (1) below.

$$\frac{6\,\text{deg} \times 16x}{360\,\text{deg}} = 26.6\% \qquad (1)$$

(where 16x is the interpolation factor)




### Conversion to output period reference

$T_{POUT} = T_{PIN} / \text{Multiplier} = 360\text{deg}$

$A_{RAL\_OUT} = 6\text{deg} \times 16 = 96\text{deg}$

$$= \frac{6\text{deg} \times 16}{360\text{deg}} = 26.6\%$$

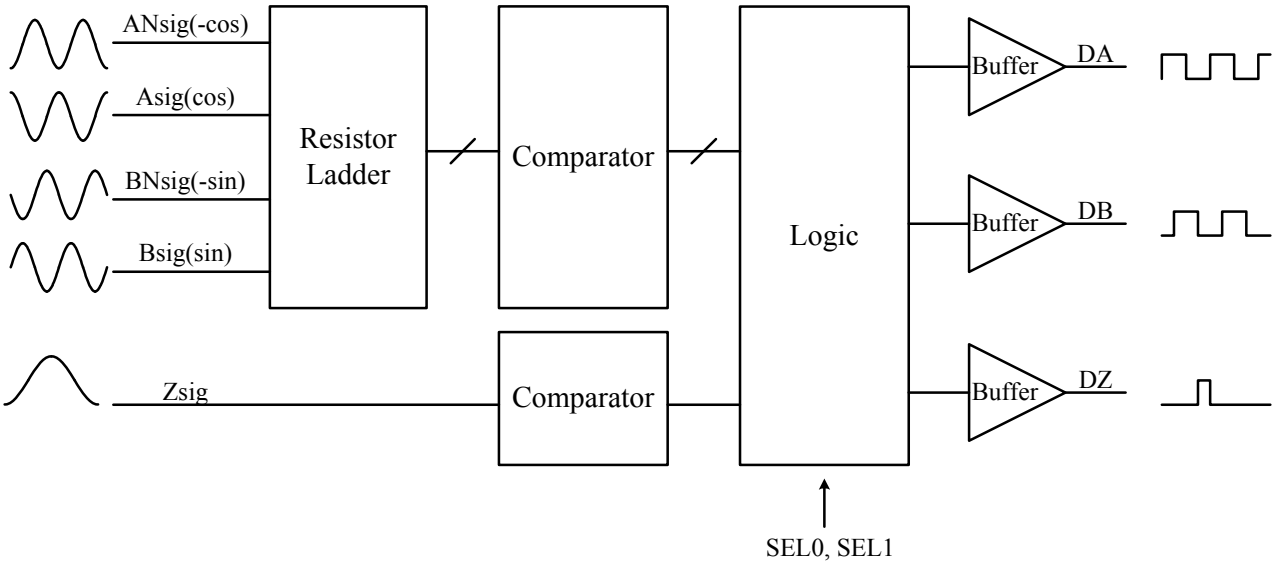
# FUNCTIONAL DESCRIPTION

## Interpolation Circuit

The interpolation circuit passes the input signals, through a resistance network divider, converts the signals to binary using comparators, and outputs 2-phase digital signals corresponding to the interpolation factor selected by register data using logical operation processing.

The interpolation factor is set using input level of SEL0 and SEL1 terminals.

| SEL1 | SEL0 | Interpolation factor |
|---|---|---|
| L | L | 2 |
| L | H | 4 |
| H | L | 8 |
| H | H | 16 |




## Output Reference voltage

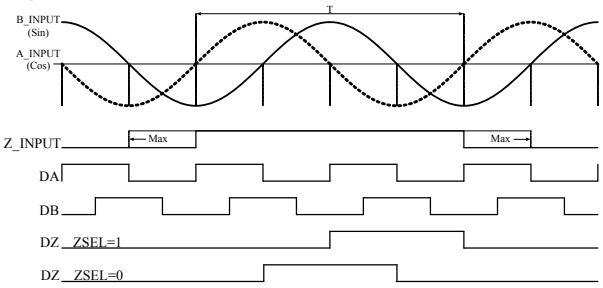
VREF terminal outputs the $V_{DD}/2$ voltage as a reference voltage to use in single-ended input.

## Timing Diagrams

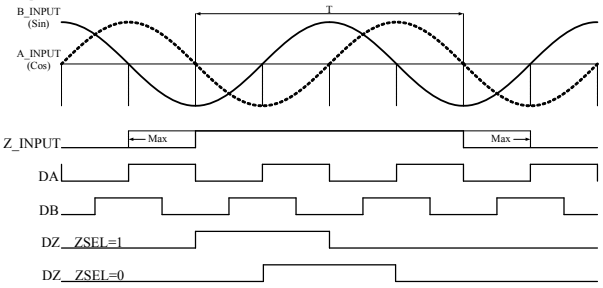
### Interpolation Function and Z-phase Input/Output Timing

DZ signal timing is settable by ZSEL terminal.

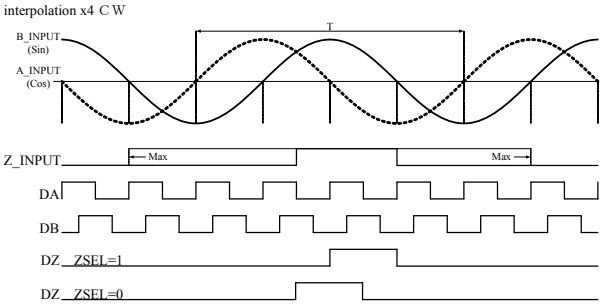
interpolation x2 C W



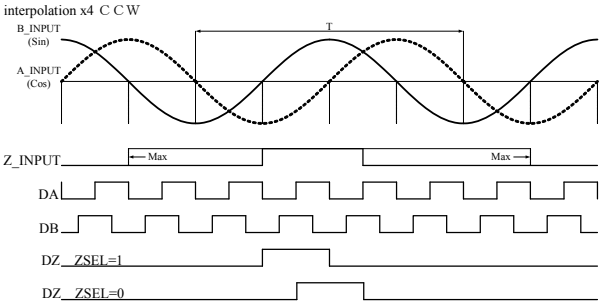

interpolation x2 C C W



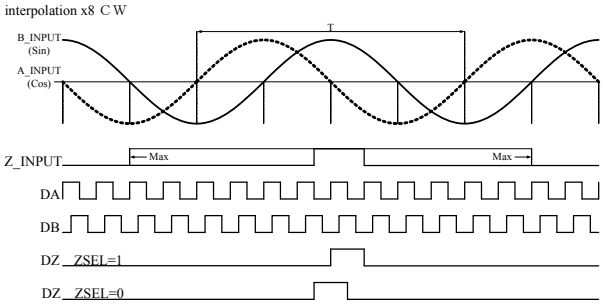

interpolation x4 C W



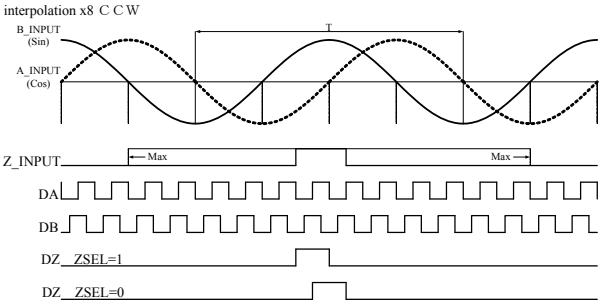

interpolation x4 C C W



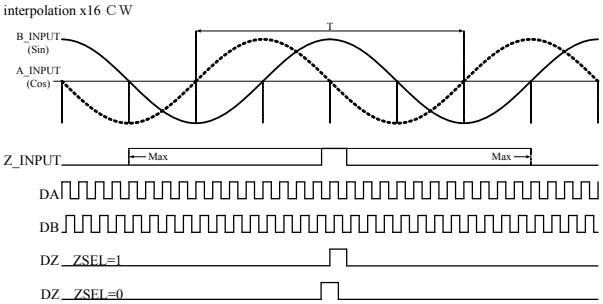

interpolation x8 C W



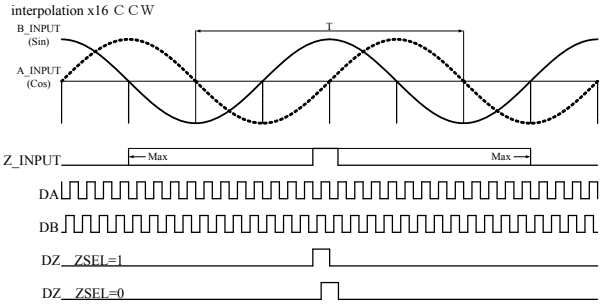

interpolation x8 C C W




interpolation x16 C W



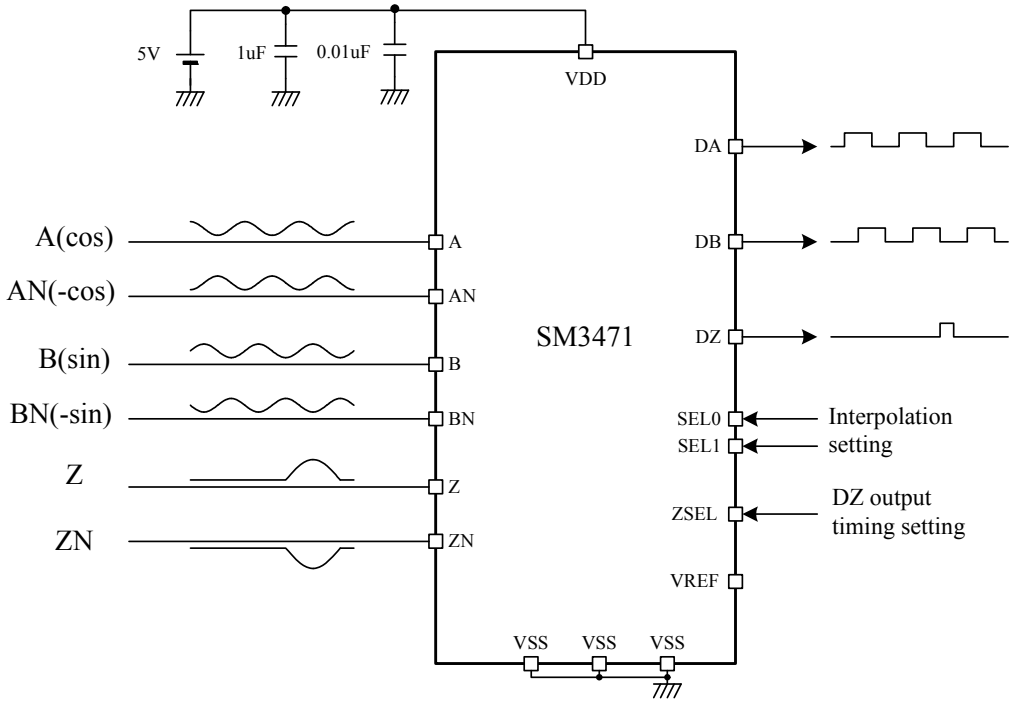

interpolation x16 C C W



# TYPICAL APPLICATION CIRCUITS

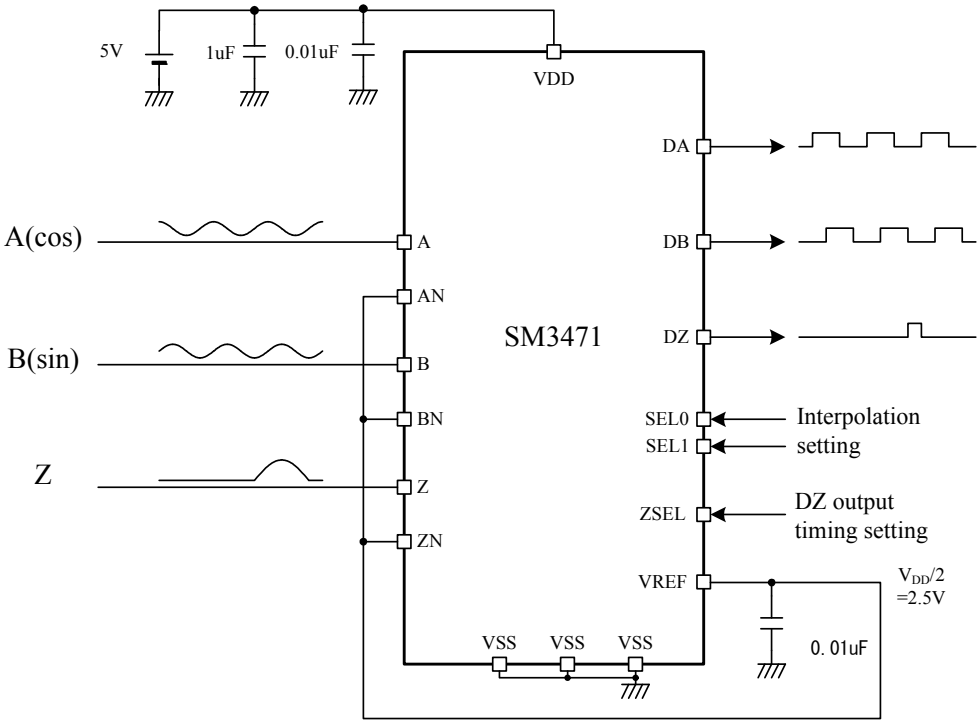
## Typical Application Circuit 1

A/B/Z-phase differential input




## Typical Application Circuit 2

A/B/Z-phase single-ended input (offset voltage=$V_{DD}$/2)



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