■ OVERVIEW

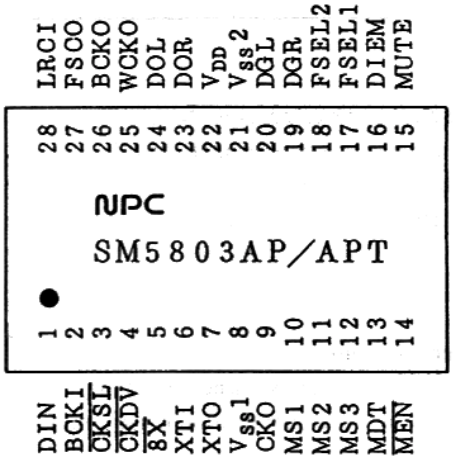
The SM5803AP/APT is a multi-function digital filter for digital audio fabricated using NPC's original molybdenum-gate CMOS technology. This LSI uses a variety of functions including 4-times/8-times oversampling, digital de-emphasis, digital attenuator, jitter-free mechanism and soft mute. The I/O interface allows 16- or 18-bit input data and 16-, 18- or 20-bit output data, so a wide range of system configurations can be realized.

■ FEATURES

- Filter configuration
  - Two-channel 4-times/8-times oversampling
  - Three-stage linear-phase FIR filter configuration (153th order + 29th order + 17th order)
  - 22-bit filter coefficient to reduce round-off error
  - 20 × 22-bit parallel multiplier
  - High-precision operation by 25-bit accumulator
  - Digital attenuation
  - Built-in overflow limiter
  - Built-in quartz oscillator circuitry
- Filter characteristics (fs: sampling frequency)
  - Passband ripple 0 to 0.4535 fs
    ..... Within 0.00005 dB
  - Stopband attenuation
    0.5465 to 7.4535 fs (8 fs mode)
    0.5465 to 3.4535 fs (4 fs mode)
    ..... 110 dB or more
  - Linear phase (group delay distortion: zero)
- Input/output
  - 16/18-bit serial data input (2's complement, MSB first)
  - 16/18/20-bit serial data output (2's complement or COB, MSB first)
- Clock
  - System clock: 512 fs, 256 fs, 384 fs and 192 fs
- Supply voltage 5 V ± 0.25 V
- Package 28-pin plastic DIP
- Molybdenum-gate CMOS construction

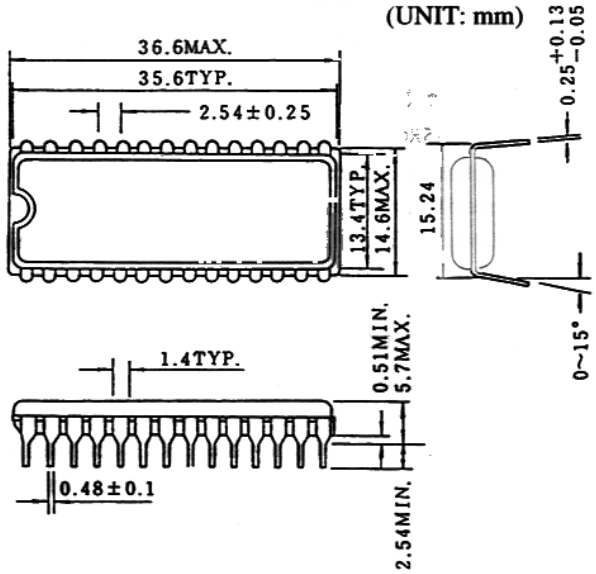
- Filter functions
  - Noise shaper (can be turned on or off)
    Reduction of re-quantization noise component in the audio band
  - Soft mute
    Smooth changes of attenuation level
  - Digital attenuation
    0.188-dB step attenuation in the 0 to -96 dB range
    Floating output prevents reduction of dynamic range.
    Floating output (0/1/2/3/4/5/6-bit selection)
    Control possible with external analog attenuator control output digital attenuator setting
  - Jitter-free mode
    Operation unaffected by input clock jitters
  - Digital de-emphasis
- Free running mode (Jitter-free)
- INPUT/OUTPUT
  - 16 bit serial data input
    (2's complement code, MSB first)
  - 16/18/20bit serial data output
    (2's complement/Complemented offset binary, MSB first)
- SYSTEM CLOCK
  (512fs/256fs/384fs/192fs)
- PACKAGE
  28-pin plastic DIP

■ PINOUT (TOP VIEW)



■ PACKAGE DIMENSION

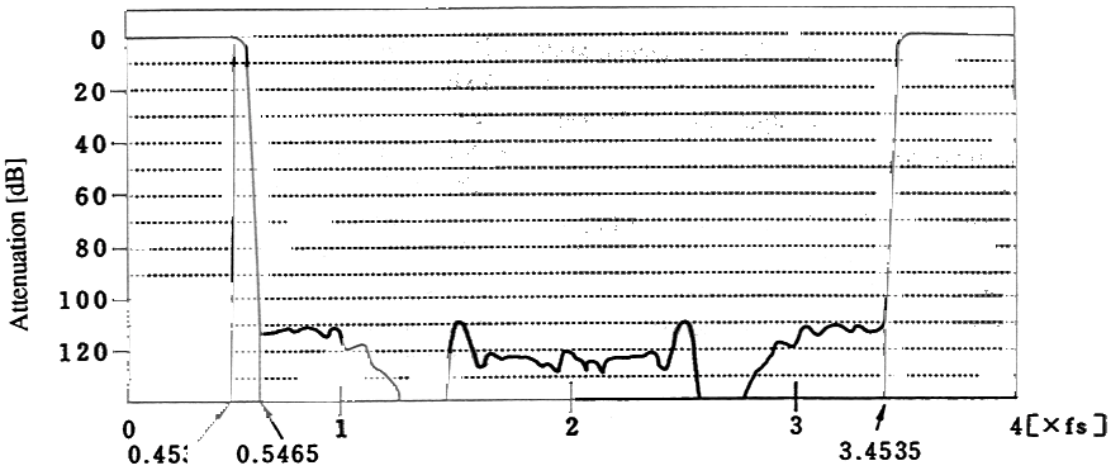
(UNIT: mm)



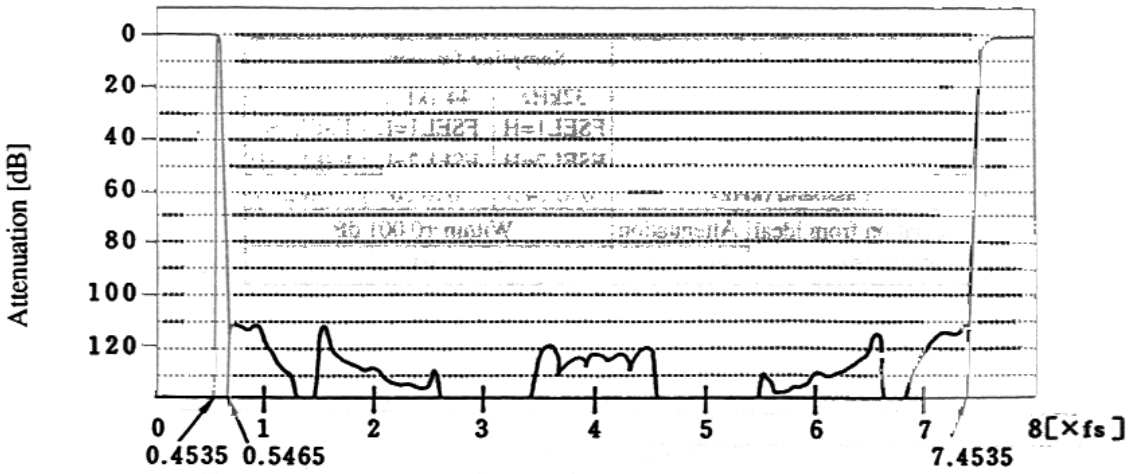
■ FILTER CHARACTERISTICS

1. Oversampling filter

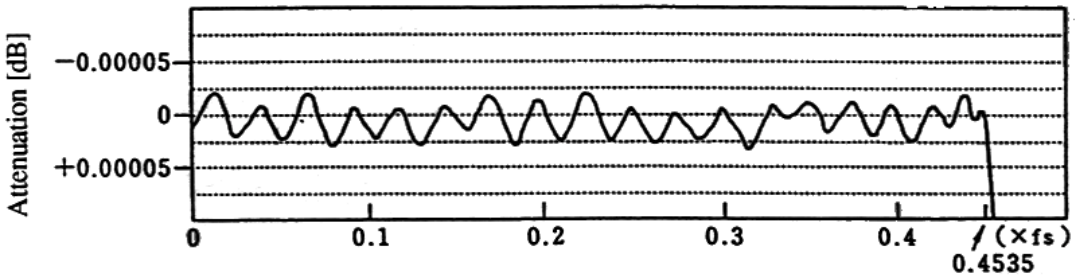
Parameter	8fs mode	4fs mode
Passband	0 to 0.4535fs	
Stopband	0.5465 to 7.4535fs	0.5465 to 3.4535fs
Passband ripple	Within ±0.00005 dB	
Stopband attenuation	110 dB minimum	
Group delay time	Constant	



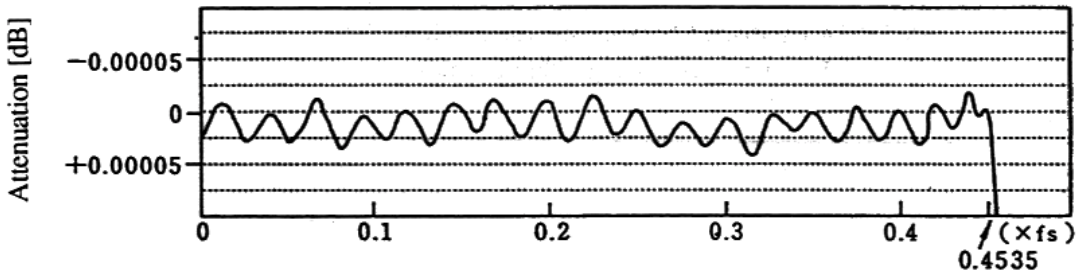
SM5803A Frequency Characteristic (4fs mode, de-emphasis OFF)



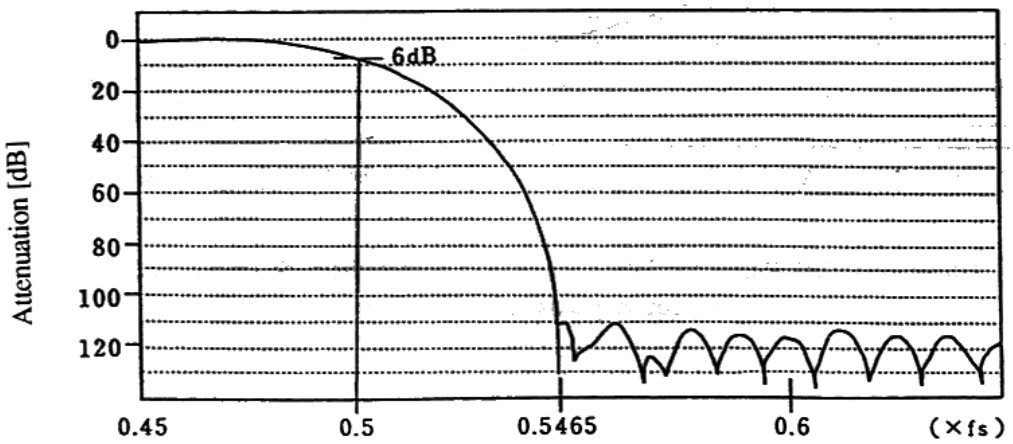
SM5803A Frequency Characteristic (8fs mode, de-emphasis OFF)



SM5803A Passband Characteristic (4fs mode, de-emphasis OFF)



SM5803A Passband Characteristic (8fs mode, de-emphasis OFF)



SM5803A Transition-band Characteristics (4fs/8fs mode, de-emphasis OFF)

■ PIN DESCRIPTION

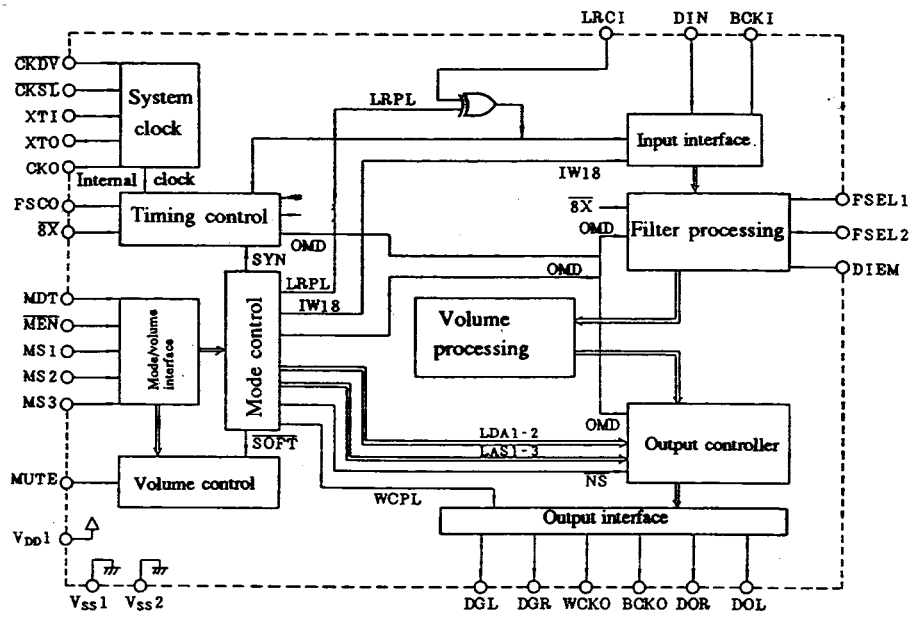
No.	NAME	DESCRIPTION
1	DIN	Input data
2	BCKI	Input data bit clock (data input on the rising edge)
3	$\overline{\text{CKSL}}$	XTI pin input frequency selection (See 6: XTI pin.)
4	$\overline{\text{CKDV}}$	
5	$\overline{\text{8X}}$	Output sampling rate selection H: 4fs mode, L: 8fs mode
6	XTI	Oscillator input (192fs: $\overline{\text{CKSL}}$ = H, $\overline{\text{CKDV}}$ = H) (384fs: $\overline{\text{CKSL}}$ = H, $\overline{\text{CKDV}}$ = L) (256fs: $\overline{\text{CKSL}}$ = L, $\overline{\text{CKDV}}$ = H) (512fs: $\overline{\text{CKSL}}$ = L, $\overline{\text{CKDV}}$ = L)
7	XTO	Oscillator output
8	Vss1	GND 1
9	CKO	Oscillator output clock (same frequency as XTI)
10	MS1	Mode set control 1
11	MS2	Mode set control 2
12	MS3	Mode set control 3
13	MDT	Mode set data
14	$\overline{\text{MEN}}$	Mode set enable
		Set the digital attenuator and mode flag register.
15	MUTE	Mute ON/OFF selection H: no sound output, L: normal output
16	DIEM	De-emphasis ON/OFF selection H: de-emphasis ON, L: de-emphasis OFF
17	FSEL1	De-emphasis filter type (fs) selection
18	FSEL2	

	fs=32kHz	fs=44.1kHz	fs=48kHz
FSEL1	H	L	L
FSEL2	H	L	H

19	DGR	8fs LR parallel output mode: de-glitched negative output 4fs LR alternate output mode: Rch de-glitched output 4fs LR parallel output mode: de-glitched negative output
20	DGL	8fs LR parallel output mode: de-glitched positive output 4fs LR alternate output mode: Lch de-glitched output 4fs LR parallel output mode: de-glitched positive output
21	Vss2	GND pin 2
22	VDD	Power supply (5 V)
23	DOR	8fs LR parallel output mode: Rch data output 4fs LR alternate output mode: LR clock output 4fs LR parallel output mode: Rch data output
24	DOL	8fs LR parallel output mode: Lch data output 4fs LR alternate output mode: Lch/Rch data output 4fs LR parallel output mode: Lch data output
25	WCKO	Output word clock
26	BCKO	Output bit clock
27	FSCO	fs-period internal operation and output timing clock
28	LRCI	Input data sampling rate (fs) clock

(fs stands for the input data sampling frequency.)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Vss=0V)

Item	Symbol	Rating	Unit
Supply voltage	V_{DD}	-0.3 ~ 7.0	V
Input voltage	V_{IN}	-0.3 ~ V_{DD} + 0.3	V
Storage temperature range	T_{STG}	-40 ~ 125	°C
Power dissipation	PW'	250 (AP)	mW
		300 (APT)	
Soldering temperature	T_{SLD}	255 (APT)	°C
Soldering time	T_{SLD}	10	Sec

■ RECOMMENDATORY OPERATING CONDITIONS

(Vss=0V)

Item	Symbol	Rating	Unit
Supply voltage	V_{DD}	4.75 ~ 5.25	V
Operating temperature	T_{OPR}	-20 ~ 70	°C

■ DC ELECTRIC CHARACTERISTICS

V_{DD}=4.75 to 5.25V, Ta=-20 to70°C,Vss=0V unless otherwise specified.

Item	Pin	Symbol	Condition	Rating			
				MIN	TYP	MAX	UNIT
Current consumption	V_{DD}	I_{DD}	V_{DD}=5V,fsys*3 = 10MHz			45 (AP)	mA
			V_{DD}=5V,fsys*3 = 13MHz			50 (APT)	
Input voltage	XTI	V_{IH1}		0.7V_{DD}			V
		V_{IL1}				0.3V_{DD}	
	(*1)	V_{IH2}		2.4			
		V_{IL2}				0.5	
Output voltage	(*2)	V_{OH}	I_{OH}=-0.4mA	2.5			V
		V_{OL}	I_{OL}=1.6mA			0.4	
Input leak current	XTI	I_{LH}	V_{IN}=V_{DD}		10	20	μA
		I_{LL}	V_{IN}=0V		10	20	
	(*1)	I_{LH}	V_{IN}=V_{DD}			1.0	
Input current	(*1)	I_{IN}	V_{IN}=0V		10	20	μA

< Pin type>

*1	LRCI, DIN, BCKI, $\overline{CKSL}$, $\overline{CKDV}$
	MS1, MS2, MS3, MDT, $\overline{MEN}$
	MUTE, DIEM, FSEL1, FSEL2, $\overline{8X}$
*2	CKO, DGR, DGL, DOR, DOL,
	WCKO, BCKO, FSCO

Internal pull-up resistors are attached to all input pins (*1) except XTI.

(*3) fsys: system clock frequency
$\overline{CKDV}$ = L : fXTI/2
$\overline{CKDV}$ = H : fXTI
(fXTI is the XTI input clock frequency.)

SM5803AP

• AC CHARACTERISTICS

(Ta = -20 ~ 70°C, V_{DD} = 4.75 ~ 5.25V, V_{SS} = 0V)

1. XTI TERMINAL

a. Quartz oscillation

ITEM	SYM-BOL	RATING MIN	RATING TYP	RATING MAX	UNIT	CONDITION CKSL	CONDITION CKDV	NOTE
Oscillating frequency	f_{MAX}	1.0		9.5	MHz	H	H	192fs
		2.0		19.0		H	L	384fs
		1.0		9.5		L	H	256fs
		2.0		19.0		L	L	512fs

b. External clock input

ITEM	SYM-BOL	RATING MIN	RATING TYP	RATING MAX	UNIT	CONDITION CKSL	CONDITION CKDV	NOTE
Width of clock pulse (H level)	t_{CWH}	38		500	nSec	H	H	192fs
		24		250		H	L	384fs
		38		500		L	H	256fs
		24		250		L	L	512fs
Width of clock pulse (L level)	t_{CWL}	48		500	nSec	H	H	192fs
		24		250		H	L	384fs
		48		500		L	H	256fs
		24		250		L	L	512fs
Cycle time of clock pulse	t_{XI}	105		1000	nSec	H	H	192fs
		52		500		H	L	384fs
		105		1000		L	H	256fs
		52		500		L	L	512fs

2. SERIAL INPUT TIMING

a. BCKI, DIN, LRCI terminal

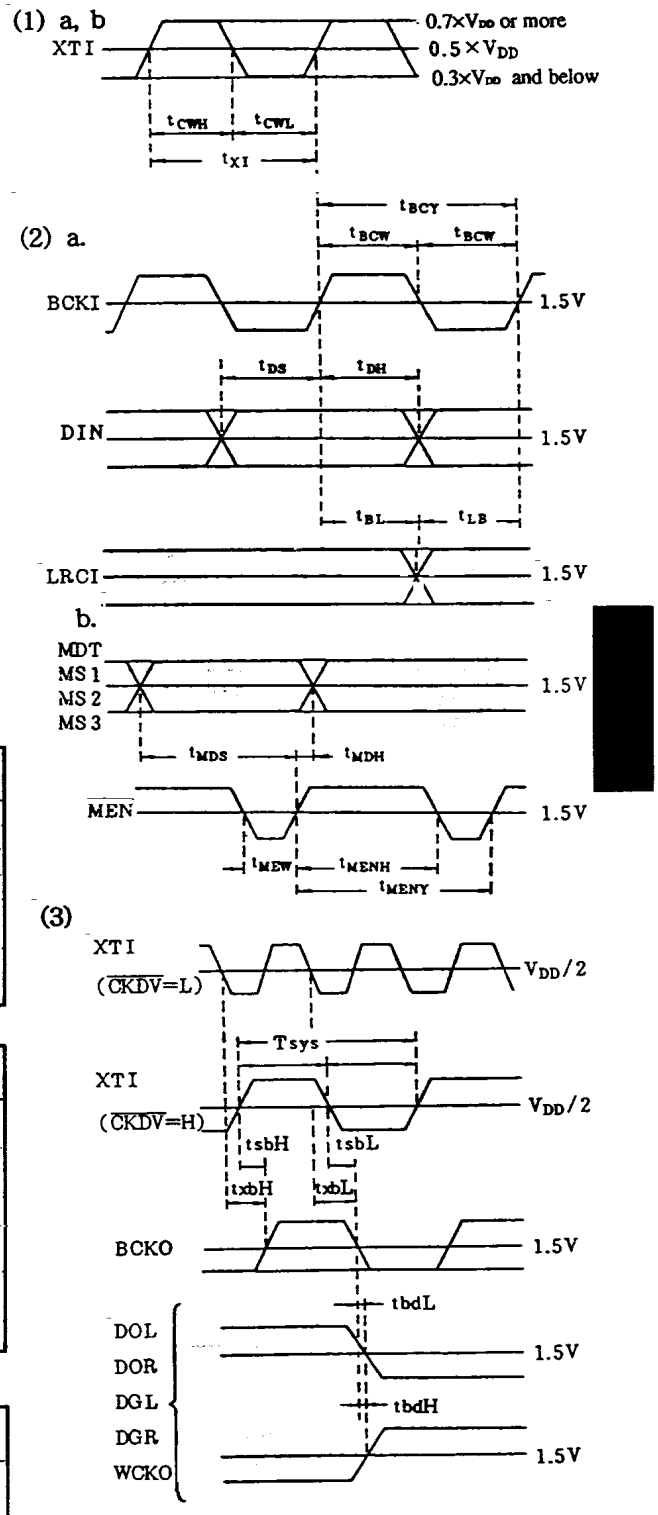
ITEM	SYMBOL	RATING MIN	RATING TYP	RATING MAX	UNIT
BCKI, Pulse width	t_{BCW}	100			nSec
BCKI, Cycle time	t_{BCY}	200			nSec
DIN, Set up time	t_{DS}	75			nSec
DIN, Hold time	t_{DH}	75			nSec
Rising edge of last BCKI to Edge of LRCI	t_{BL}	75			nSec
Edge of LRCI to Rising edge of first BCKI	t_{LB}	75			nSec

b. MS1, MS2, MS3, MDT, MEN terminal

ITEM		SYMBOL	RATING MIN	RATING TYP	RATING MAX	UNIT
MDT, MS1, MS2, MS3 setup time		t_{MDS}	20			nSec
MDT, MS1, MS2, MS3 hold time		t_{MDH}	20			nSec
MEN	L-level period	t_{MEW}	20			
	H-level period	t_{MENH}	5Tsys +20nS			
	Interval with next pulse (MC0, MC3-MC7)	t_{MEMY}	6			Tsys (*1)
	(MC1, MC2)		34			

3. OUPUT TIMING

ITEM		SYMBOL	RATING MIN	RATING TYP	RATING MAX	UNIT	NOTE
BCKO delay time from XTI	CKDV =L	txbH	35		95	nSec	
		txbL	35		95		
	CLDV =H	txbH	35		95		
		txbL	35		95		
Output delay time		tbdL	-10	0	+10	nSec	15pF Load
		tbdH	-10	0	+10		



(*1) Tsys: System clock period $\overline{CKDV}$ = L: txi x 2
$\overline{CKDV}$ = H: txi
where txi is the period of the clock input on XTI.

SM5803APT

• AC CHARACTERISTICS

(Ta = -20 ~ 70°C, V_{DD} = 4.75 ~ 5.25V, V_{SS} = 0V)

1. XTI TERMINAL

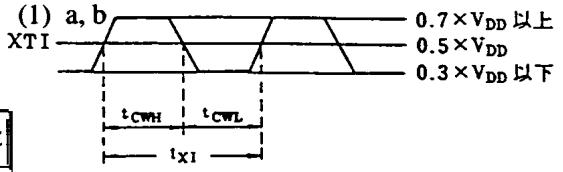
a. Quartz oscillation

ITEM	SYM-BOL	RATING MIN	RATING TYP	RATING MAX	UNIT	CONDITION CKSL	CONDITION CKDV	NOTE
Oscillating frequency	f_{MAX}	1.0		130	MHz	H	H	192fs
		2.0		260		H	L	384fs
		1.0		130		L	H	256fs
		2.0		260		L	L	512fs

b. External clock input

ITEM	SYM-BOL	RATING MIN	RATING TYP	RATING MAX	UNIT	CONDITION CKSL	CONDITION CKDV	NOTE
Width of clock pulse (H level)	t_{CWH}	35*1		500	nSec	H	H	192fs
		15		250		H	L	384fs
		35*1		500		L	H	256fs
		15		250		L	L	512fs
Width of clock pulse (L level)	t_{CWL}	35*1		500	nSec	H	H	192fs
		15		250		H	L	384fs
		35*1		500		L	H	256fs
		15		250		L	L	512fs
Cycle time of clock pulse	t_{XI}	76		1000	nSec	H	H	192fs
		38		500		H	L	384fs
		76		1000		L	H	256fs
		38		500		L	L	512fs

(1) a, b



*1 The clock duty ratios on t_{CWH} and t_{CWL} (i.e., $t_{CWH}/t_{XI} \times 100$) are as follows:

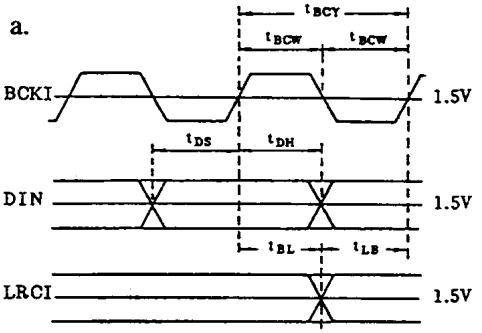
XTI clock frequency	Duty ratio
13MHz	45.5% to 54.5%
12.288MHz (48kHz × 256)	43% to 57%

2. SERIAL INPUT TIMING

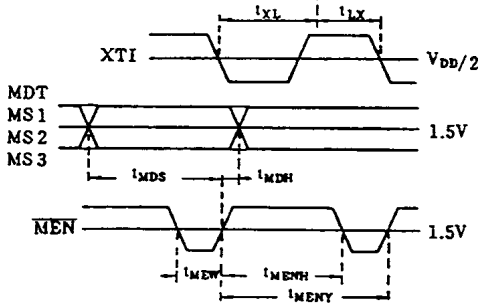
a. BCKI, DIN, LRCI terminal

ITEM	SYMBOL	RATING MIN	RATING TYP	RATING MAX	UNIT
BCKI, Pulse width	t_{BCW}	100			nSec
BCKI, Cycle time	t_{BCY}	200			nSec
DIN, Set up time	t_{DS}	75			nSec
DIN, Hold time	t_{DH}	75			nSec
Rising edge of last BCKI to Edge of LRCI	t_{BL}	75			nSec
Edge of LRCI to Rising edge of first BCKI	t_{LB}	75			nSec
XTI rising edge to Start edge of LRCI (*) (only in forced synchronous mode)	t_{XL}	20			nSec
Start edge of LRCI (*) to XTI rising edge (only in forced synchronous mode)	t_{LX}	0			nSec

(2) a.



b.

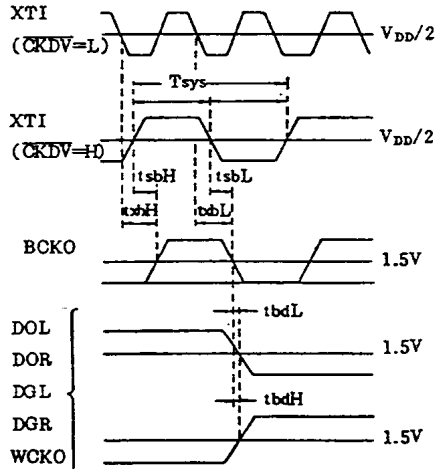


b. MS1, MS2, MS3, MDT, $\overline{MEN}$ terminal

ITEM	SYMBOL	RATING MIN	RATING TYP	RATING MAX	UNIT
MDT, MS1, MS2, MS3 setup time	t_{MDS}	20			nSec
MDT, MS1, MS2, MS3 hold time	t_{MDH}	20			nSec
$\overline{MEN}$ L-level period	t_{MEW}	20			
H-level period	t_{MEMH}	5Tsys +20nS			
Interval with next pulse (MC0, MC3-MC7)	t_{MEMY}	6			Tsys (*1)
(MC1, MC2)		34			

Note) See the table on p.12 for MC0-MC7.

(3)



3. OUPUT TIMING

ITEM		SYMBOL	RATING MIN	RATING TYP	RATING MAX	UNIT	NOTE
BCKO delay time from XTI	$\overline{CKDV}$=L	txbH	35		95	nSec	
		txbL	35		95		
	$\overline{CLDV}$=K	tsbH	35		95		
		tsbL	35		95		
Output delay time		tbdL	-10	0	+10	nSec	15pF Load
		tbdH	-10	0	+10		

(*) Start edge of LRCI:
LRPL flag = L Rising edge
LRPL flag = H Falling edge

(*1) Tsys: system clock period $\overline{CKDV}$ = L: $t_{XI} \times 2$,
$\overline{CKDV}$ = H: t_{XI}.
t_{XI} is the period of the clock input on XTI.

■ FUNCTION DESRIPTION

1. Output mode selection ($\overline{8X}$ input, OMD flag)

$\overline{8X}$ input	OMD flag	Output mode
L	L	8fs LR parallel
H	L	4fs LR alternate
H	H	4fs LR parallel
L	H	Test mode (*1)

(*1) The test mode is the same as [8fs LR parallel output mode] except that the attenuation change operation is accelerated in the soft mute mode.

2. Oversampling filter function

- 8fs oversampling
  Signal input at the sample rate fs is output as data at the oversampling rate 8fs. This filter eliminates sampling noise of 0.5465fs to 7.4535fs.
- 4fs oversampling
  Signal input at the sample rate fs is output as data at the oversampling rate 4fs. This filter eliminates sampling noise of 0.5465fs to 3.4535fs.

3. Digital de-emphasis filter

An IIR filter is used to revive the gain and phase characteristics of the de-emphasis filter.

- De-emphasis mode selection (DIEM input)
  De-emphasis ON (DIEM input = H or open)
  De-emphasis OFF (DIEM input = L)
- Filter coefficient selection (FSEL1 input, FSEL2 input)

	fs coefficient selection		
	fs=32kHz	44.1kHz	48kHz
FSEL1	H	L	L
FSEL2	H	L	H

- Features of the digital de-emphasis filter
  The IIR achieves almost ideal gain and phase characteristics, so there is no distortion and variation due to component parameters. The primary objective of de-emphasis is to reduce quantization noise in the high-frequency band and widen the dynamic range. However, de-emphasis in the digital stage narrows the dynamic range. This digital filter ensures a sufficiently wide dynamic range by minimizing the level of requantization noise by the following measures:
  1) 8fs or 4fs oversampling output
  2) Noise shaper
  3) 18-bit or longer output word length

4. Digital attenuator

Attenuation is possible in 0.188 dB steps from 0 to -96 dB. Lch and Rch outputs can be attenuated independently. The attenuation level is given by the following equations:

Attenuation (L) = attenuation setting (L) × 0.188 dB; Lch

Attenuation (R) = attenuation setting (R) × 0.188 dB; Rch

- Relation with soft mute mode
  When the soft mute mode is ON ($\overline{SOFT}$ flag = L):
  When an attenuation value is set, attenuation changes gradually in 0.188 dB steps until it reaches the level given by the above equation. (See Figure 1.)
  When the soft mute mode is OFF ($\overline{SOFT}$ flag = H):
  When an attenuation value is set, attenuation immediately changes to the level given by the above equation.

5. Mute

The maximum attenuation value (511) is set in the mute mode (i.e., attenuation of 95.9 dB). When the mute mode is reset, attenuation returns to the previous setting. (When the setting is changed externally while in the mute mode, attenuation changes to the new value.)

- Mute mode selection (MUTE input)
  Mute mode ON (MUTE input = H or open)
  Mute mode OFF (MUTE input = L)
- Relation with soft mute mode
  When the soft mute mode is ON ($\overline{SOFT}$ flag = L):
  Gradual attenuation in 0.188 dB steps (See Figure 2.)
  When the soft mute mode is OFF ($\overline{SOFT}$ flag = H):
  Direct attenuation to the specified level

6. Soft mute

When the soft mute mode is ON, noise generated by the attenuator setting (MC4, MC5, MC6) or mute ON/OFF is prevented by gradual attenuation.

- Soft mute mode selection ($\overline{SOFT}$ flag)
  Soft mute mode ON ($\overline{SOFT}$ flag = L)
  Soft mute mode OFF ($\overline{SOFT}$ flag = H)

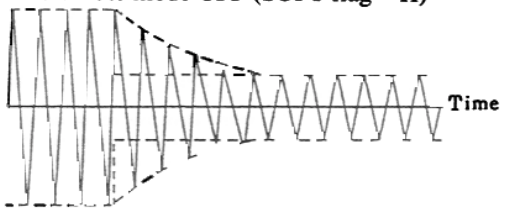


Figure When the attenuator setting is changed

flag)

- Output data format
  MSB first
  Switching between 2's complement and COB (complemented offset binary) (COB flag)
  2's complement format (COB flag = L)
  COB format (COB flag = H)
- Floating output system
  In the floating output system, a 6 dB-step analog attenuator is provided after D/A conversion and controlled (switched) according to the digital attenuator setting. Ordinary digital attenuators use only the low-order bits of the DA converter when a large attenuation value is set, which narrows the dynamic range.
  The floating output system does not suffer this problem. The 6-dB step attenuator is switched statically according to the digital attenuator setting, so errors in the analog attenuator stage do not adversely affect sound quality.
  In floating output, a word is configured from the DA data and analog shift words. (See Figure 5.)

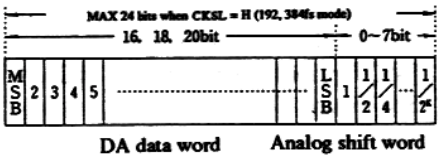


Figure 5 Configuration of Output Word

- DA data word
  This data word is input to the DA converter for analog conversion. Data value Nda is expressed as follows:
  Nda = Nreal/Nas
  where Nreal is the true data value, and Nas is the value (1, 1/2, 1/4, ...) of the analog shift part.

* DA data word bit selection (LDA1 flag, LDA2 flag)
Selection can be made from 16, 18 and 20 bits.

DA output part, No. of bits	LDA1 flag	LDA2 flag
16	L	L
18	H	L
20	L	H

- Analog shift word
  Word for controlling the analog attenuator stage following the DA converter

* Maximum shift bit (Las) selection (LAS1, LAS2, LAS3 flag)
When the configuration of the analog attenuator is 1, 1/2, 1/4 ... $1/2^K$ ($K \leq 6$), set the following:
Las = K
When Las is set from 1 to 6, bits 2 to 7 are output as the analog shift word. Each bit is output MSB first and weighed with 1, 1/2, 1/4 ... 1/2K. Only 1 bit corresponding to the digital attenuator value is active (H) while the rest are set to 0 (L).

Note:
When the CKSL input is H (192fs/384fs clock mode), the sum of DA word bits and analog shift word bits must not exceed 24 (Lda + Las ≤ 23).

Las setting flag			Analog shift bit	Digital attenuator value								DA data word length that can be used when CKSL = H (*1)
LAS3	LAS2	LAS1	LAS	0 ~ -0dB	32 ~ -6dB	64 ~ -12dB	96 ~ -18dB	128 ~ -24dB	160 ~ -30dB	192 ~ -36dB		
L	L	L	0	No analog shift part								
L	L	H	1	1	1/2	1/2	1/2	1/2	1/2	1/2		20 bits
L	H	L	2	1	1/2	1/4	1/4	1/4	1/4	1/4		18
L	H	H	3	1	1/2	1/4	1/8	1/8	1/8	1/8		16
H	L	L	4	1	1/2	1/4	1/8	1/8	1/16	1/16		18 bits
H	L	H	5	1	1/2	14	1/8	1/16	1/32	1/32		16
H	H	L	6		1/2	1/8	1/8	1/16	1/32	1/64		16 bits

(*1) The DA data length is not limited when CKSL = L, so any combinations of 16, 18 and 20 bits are possible.

- Output timing

Item	Symbol	Output mode		
		8fs LR parallel	4fs LR alternate	4fs LR parallel
Bit clock period	Tb	Tsys	Tsys	2 × Tsys
Data word length	Tw			
CKSL = H		24 × Tsys	24 × Tsys	48 × Tsys
CKSL = L		32 × Tsys	32 × Tsys	64 × Tsys

Tsys; Internal system clock period (See 8. System clock.)
Tb, Tw; See the figure below.

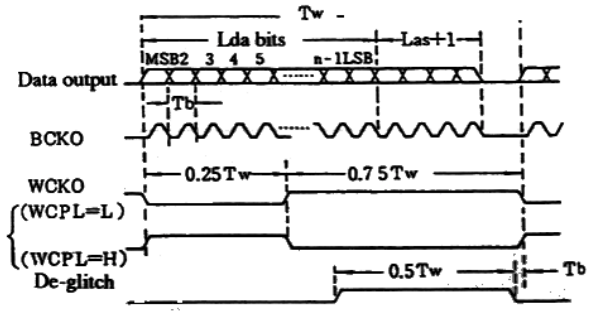


Figure 6 Output word

When the floating system is not in use
(Las = 0: LAS1, LAS2, LAS3 flags = L)

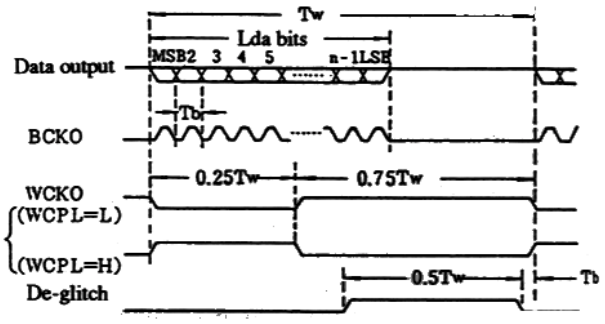


Figure 7 Output word
When the floating system is in use (Las ≥ 1)

12. Attenuation register (RattL, RattR) and mode flag register (Rmod) setting
(MS1 to MS3 input, MDT input, $\overline{MEN}$ input)

Mode set control input					Operation
Mode	MS1	MS2	MS3	$\overline{MEN}$	
MC0	L	L	L		Read MDT input to MSIPO and simultaneously shift MSIPO by 1 bit (READ).
MC1	H	L	L		Increment the attenuation register (L, R) by 1 (INC RattL, RattR).
MC2	L	H	L		Decrement the attenuation register (L, R) by 1 (DEC, RattL, RattR)
MC3	H	H	L		Set the attenuation register (L, R) to 0 (Reset RattL, RattR).
MC4	L	L	H		Transfer the MSIPO contents to the attenuation register (L) (MSIPO to RattL).
MC5	H	L	H		Transfer the MSIPO contents to the attenuation register (R) (MSIPO to RattR).
MC6	L	H	H		Transfer the MSIPO contents to the mode flag register (Rmod) (MSIPO to Rmod).
MC7	H	H	H		Reset the mode flag register Rmod (set all flags to L). Reset the attenuation register (L, R) (Reset RattL, RattR). Reset the operation output timing counter.

MSIPO; serial → parallel conversion register
; rising edge

- Attenuation register (Ratt(L) and Ratt(R)) setting
Of all the functions listed in the table above, 6 functions have an effect on the attenuation registers.

(MC1) Increment the attenuation register by 1 (this increases the attenuation by 0.188 dB).
Ratt (L) + 1 → Ratt (L)
Ratt (R) + 1 → Ratt (R)
The register value will not change when it is the maximum value (511).

(MC2) Decrement the attenuation register by 1 (this decreases the attenuation by 0.188 dB).
Ratt (L) - 1 → Ratt (L)
Ratt (R) - 1 → Ratt (R)
The register value will not change when it is the minimum value (0).

(MC3) Reset the attenuation register (attenuation 0 dB).
0 → Ratt (L)
0 → Ratt (R)
Figure 8 and Figure 9 show examples of the attenuation register settings using MC1 to MC3.

(MC4) (MC5) Transfer MSIPO register contents to the attenuation register.
MSIPO → Ratt (L) (with MC4)
MSIPO → Ratt (R) (with MC5)
The MSIPO register must be set with [MC0] prior to using MC4 or MC5.
See Figure 10 and Figure 11.

(MC7) Reset the attenuation register.
0 → Ratt (L)
0 → Ratt (R)
This function also resets the mode flag register (Rmod) and the operation output timing counter at the same time.

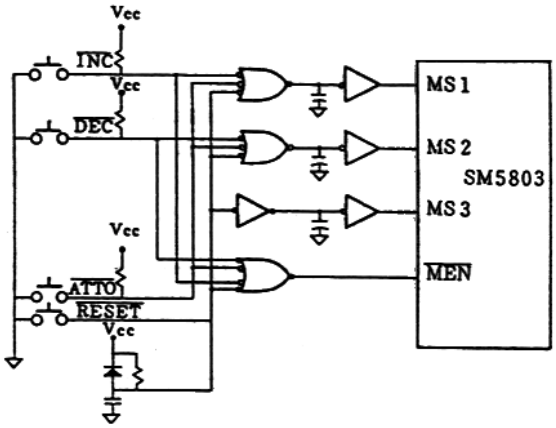


Figure 8 Example of attenuation register setting circuit using MC1, MC2 and MC3

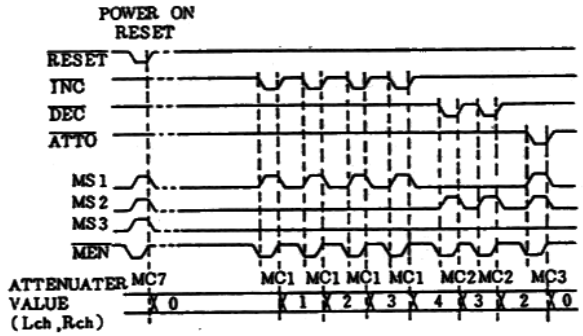


Figure 9 (Figure 8) Operation timing

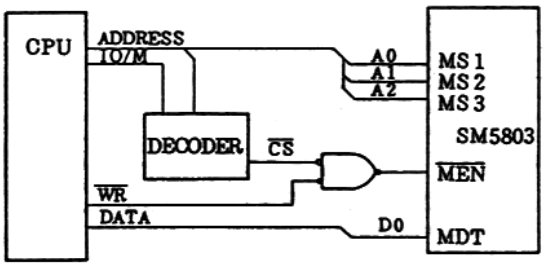


Figure 10 Example of attenuation register setting circuit using MC0, MC4 and MC5

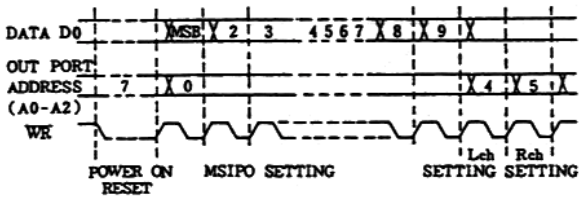


Figure 11 Operation timing of (Figure 10)

- Mode flag register (Rmod) setting
  Of all the functions listed in the above table, 2 functions have an effect on the mode flag register.

(MC6) Transfer MSIPO register contents to the mode flag register (Rmod).
MSIPO → Rmod
The MSIPO register must be set with (MC0) prior to using this function.
See Figure 12 and Figure 13.

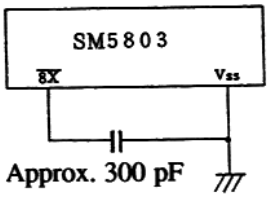
(MC7) Reset the MSIPO register (Rmod) (i.e. set all flags to L). This function also resets the attenuation register and operation output timing at the same time.
See the table below on the right.

- Internal operation timing reset

(MC7) When this function is input, the internal operation and output timing counter is synchronously reset with the start edge of LRCI. This is useful for synchronizing the external input clock (LRCI) with the internal operation/output timing at the start of the jitter-free mode (SYN flag = L).
This function also resets the mode flag register and the attenuation register at the same time.

Notes:

1. This IC must be reset entirely in the (MC7) mode after power-on.
2. To perform 4-times oversampling, the IC must operate once in the 8-times mode at power-up or thereafter. The circuit shown below activates 8-times oversampling at power-up.



The time required for taking $\overline{8X}$ L must be at least half (1/2) the LRCI clock period when the XTI clock is ON.

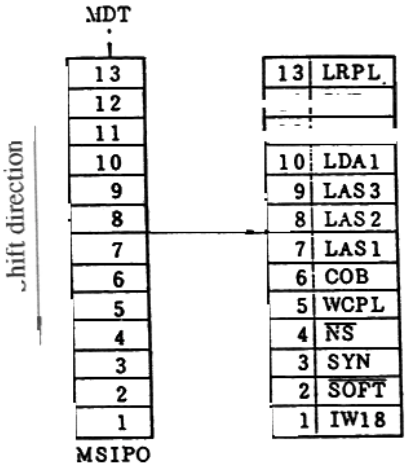


Figure 12 Mode flag register contents

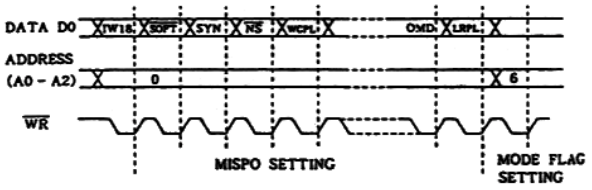


Figure 13 Mode flag setting using MC0 and MC6 (circuit of Figure 10 is in use)

List of mode flag settings (*Note 1)

Mode flag	Value	State
LRPL	L	Start on the rising edge of LRCI
	H	Start on the falling edge of LRCI
OMD	L	8fs LR parallel output operation (when $\overline{8X}$ = L) 4fs LR alternate output operation (when $\overline{8X}$ = H)
	H	Test mode (when $\overline{8X}$ = L) 4fs LR parallel output operation (when $\overline{8X}$ = H)
LDA1 LDA2 (*Note 1)		Lda = DA data length (bit) 16 : 18 : 20 LDA1 L : H : L LDA2 L : L : H
LAS1 LAS2 LAS3 (*Note 2)		Maximum analog shift setting Las = LAS1 +2×LAS2 +4×LAS3
COB	L	Output data in 2's complement format
	H	Output data in COB format
WCPL	L	Word delimit on the falling edge of the WCKO clock
	H	Word delimit on the rising edge of the WCKO clock
NS	L	Noise shaper ON
	H	Noise shaper OFF
SYN	L	Jitter-free mode
	H	Forced synchronization mode
SOFT	L	Soft mute ON
	H	Soft mute OFF
IW18	L	Input data word length, 16 bits
	H	Input data word length, 18 bits

(*Note 1) All flags are reset to "L" upon reset.
(*Note 2) The sum of Lda and Las values must be 23 or less when $\overline{CKSL}$ = H (192fs/384fs mode).

■ TIMING CHART

1. INPUT TIMING (DIN, BCKI, LRCI)

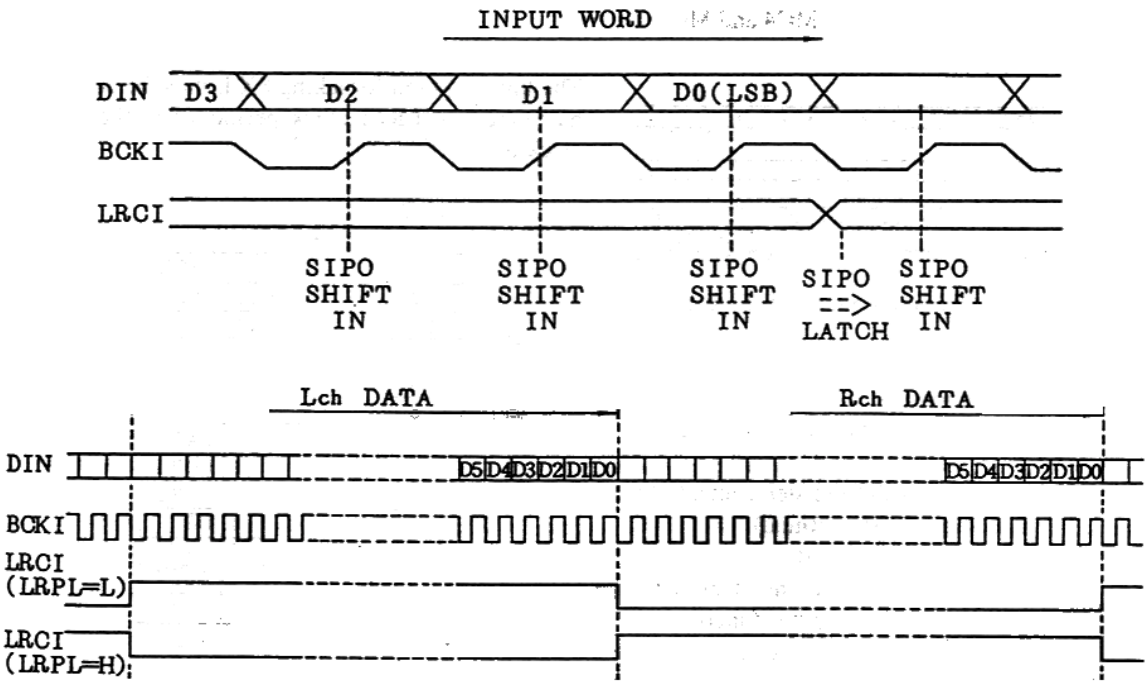


Figure A Audio data input timing

The 16 bits (when IW18 flag = L) or 18 bits (IW18 flag = H) immediately preceding the changing edge of the LRCI input clock are latched as input data.

Output timing (DOL, DOR, BCKO, WCKO, DGL, DGR)

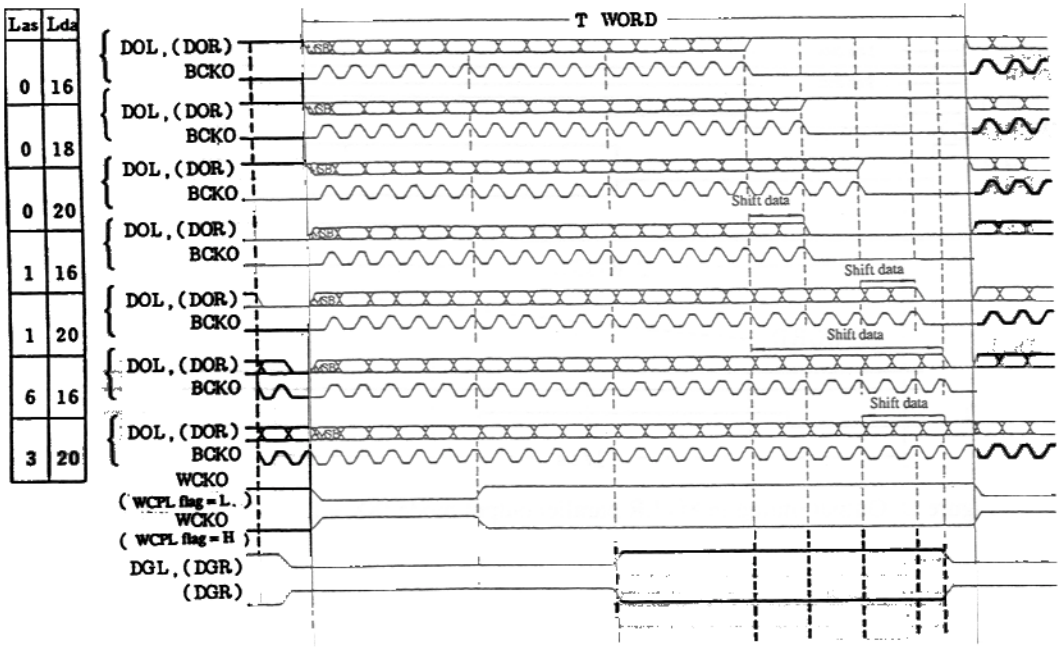


Figure B Unit output word timing (when $\overline{CKSL}$ = H)
Lda: Number of DAC bits
Las: Number of analog shift bits

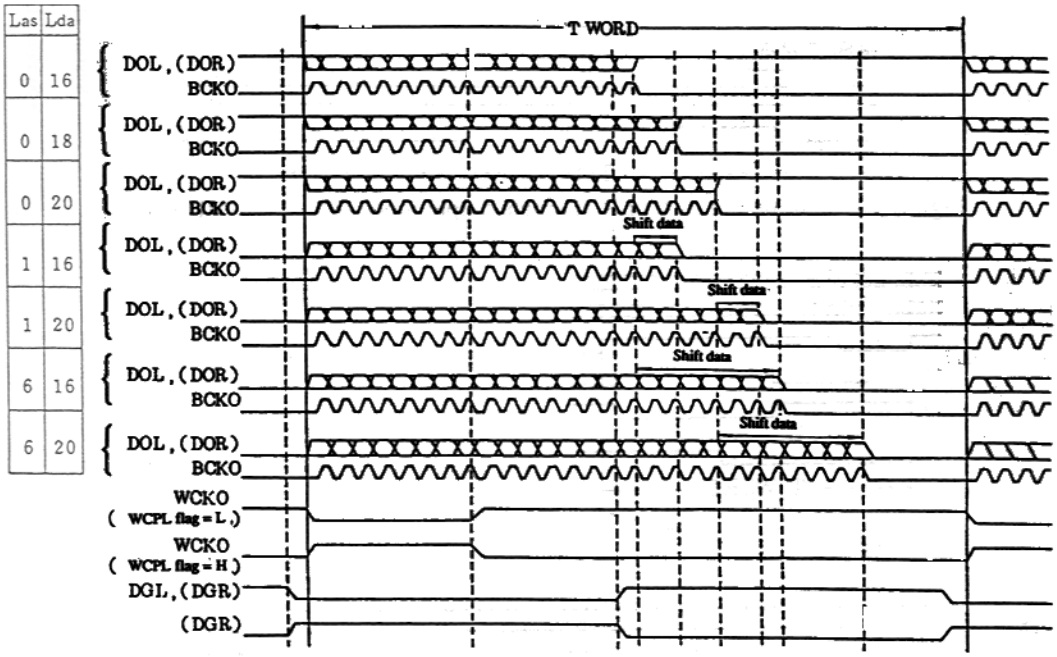


Figure C Unit output word timing (when $\overline{CKSL}$ = L)
Lda: Number of DAC bits
Las: Number of analog shift bits

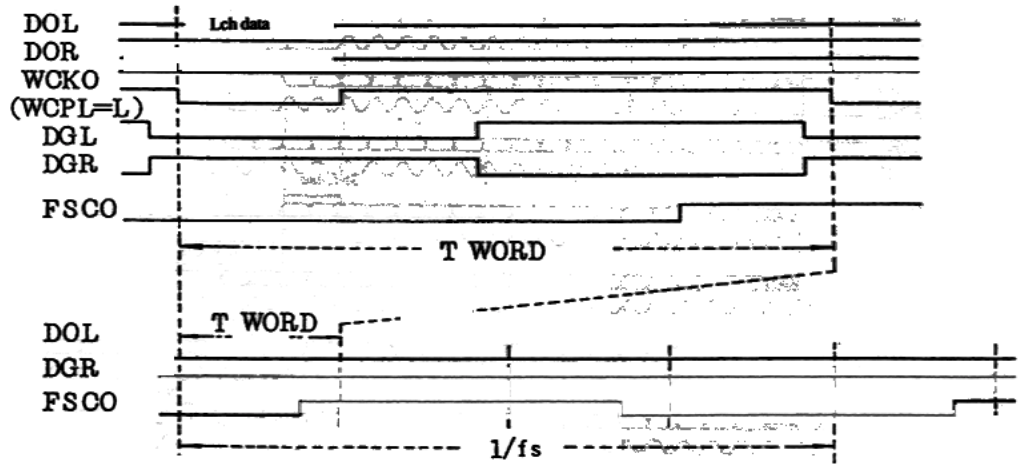


Figure D Output timing in 8fs LR parallel output mode ($\overline{8X}$ = L, OMD flag = L or H)

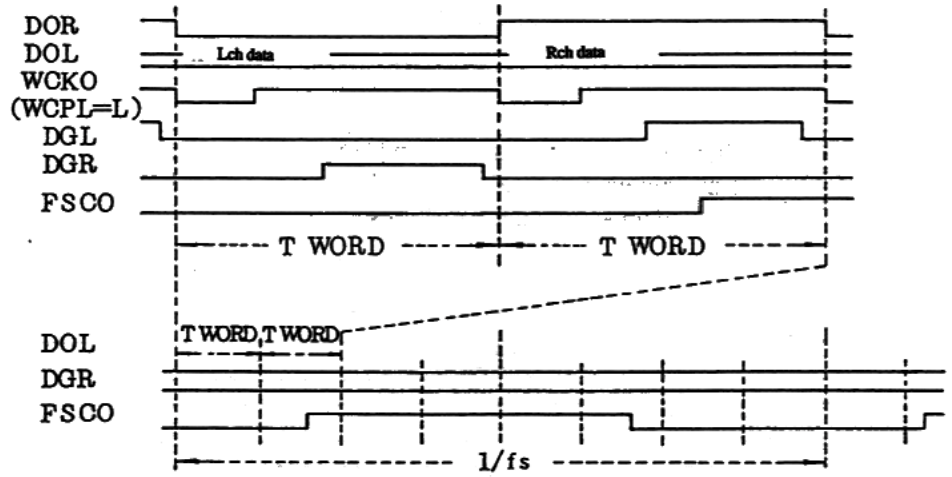


Figure F Output timing in 4fs LR alternate output mode ($\overline{8X}$ = H, OMD flag = L)

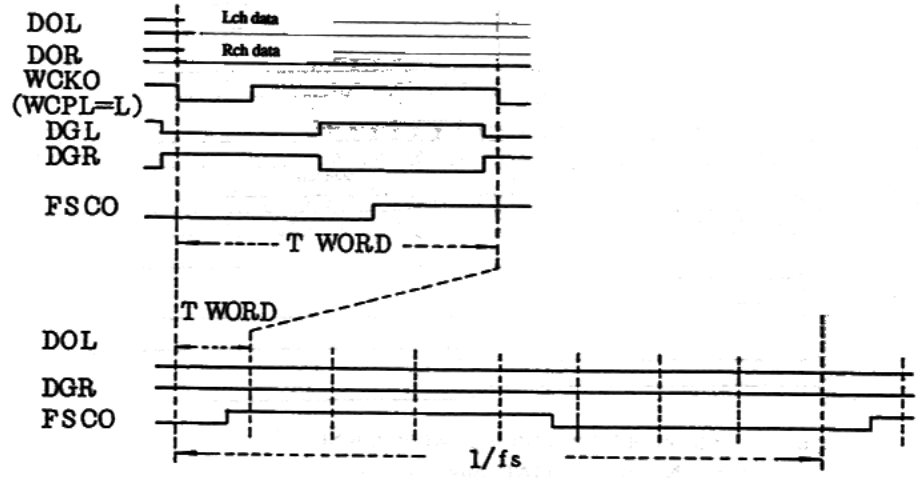
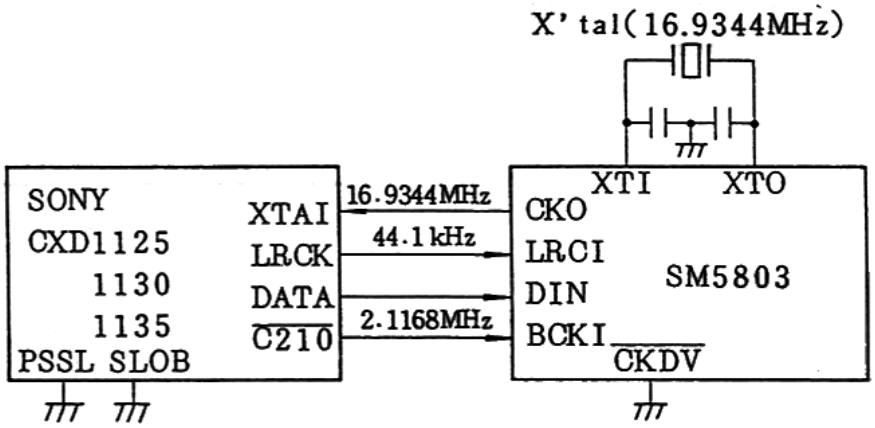
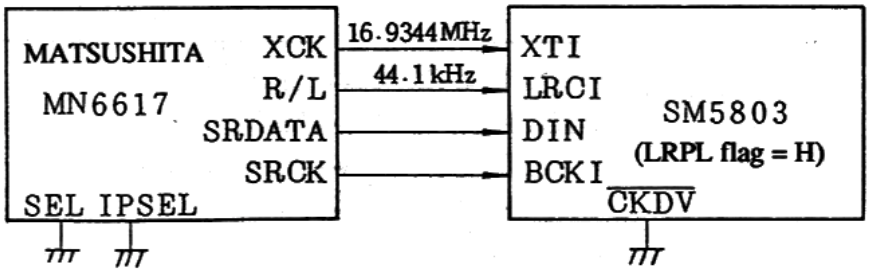


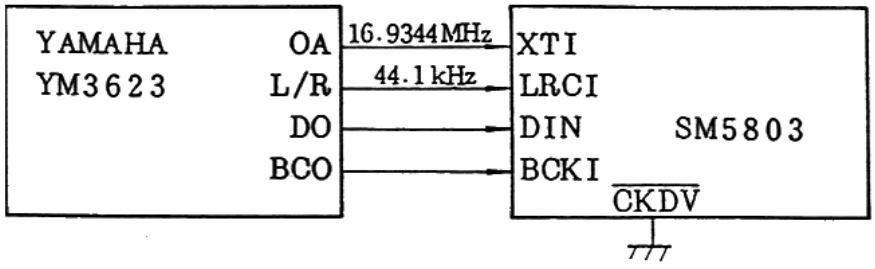
Figure G Output timing in 4fs LR parallel output mode ($\overline{8X}$ = H, OMD flag = H)

■ TYPICAL APPLICATION

1. Input connection examples

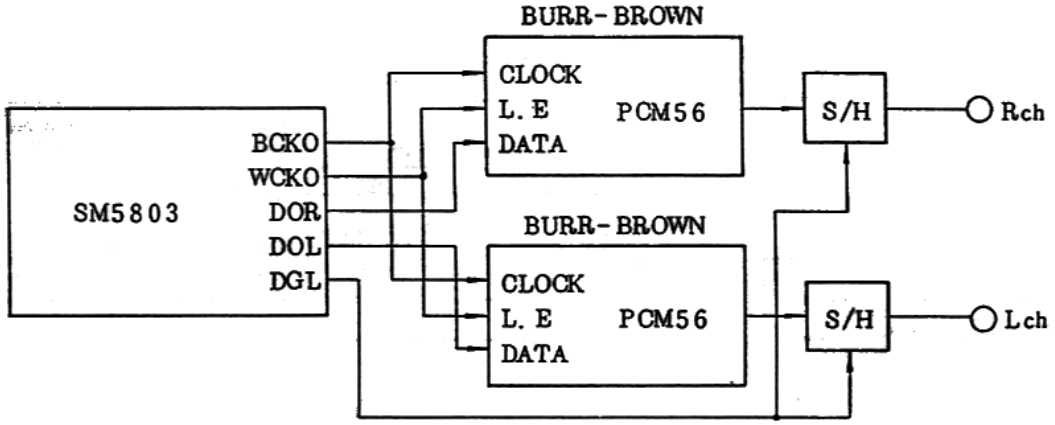






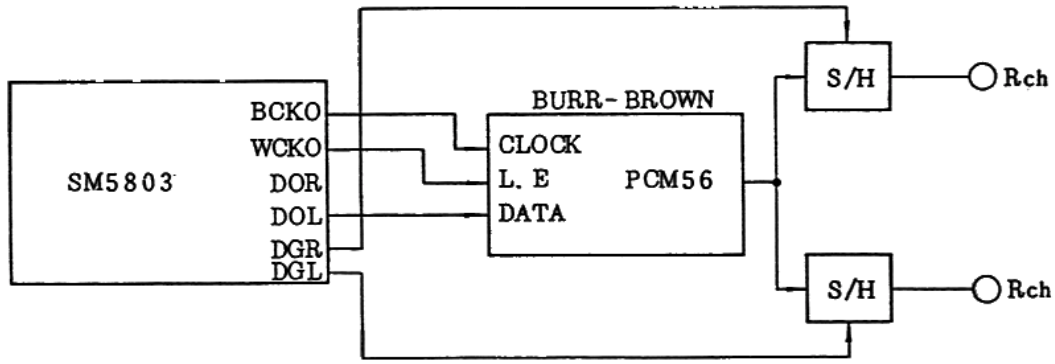
Output connection examples

(1) Example of using 16-bit 2DAC (8fs, 4fs LR parallel output mode)



- 8fs LR parallel output $\overline{8X}$ input = L, OMD flag = L
- 4fs LR parallel output $\overline{8X}$ input = H, OMD flag = H

(2) Example of using 16-bit 1DAC (4fs LR alternate output mode)



- 4fs LR parallel output 8X output = H, OMD flag = L