SM511/SM512 4-Bit Microcomputer (LCD Driver)

■ Description

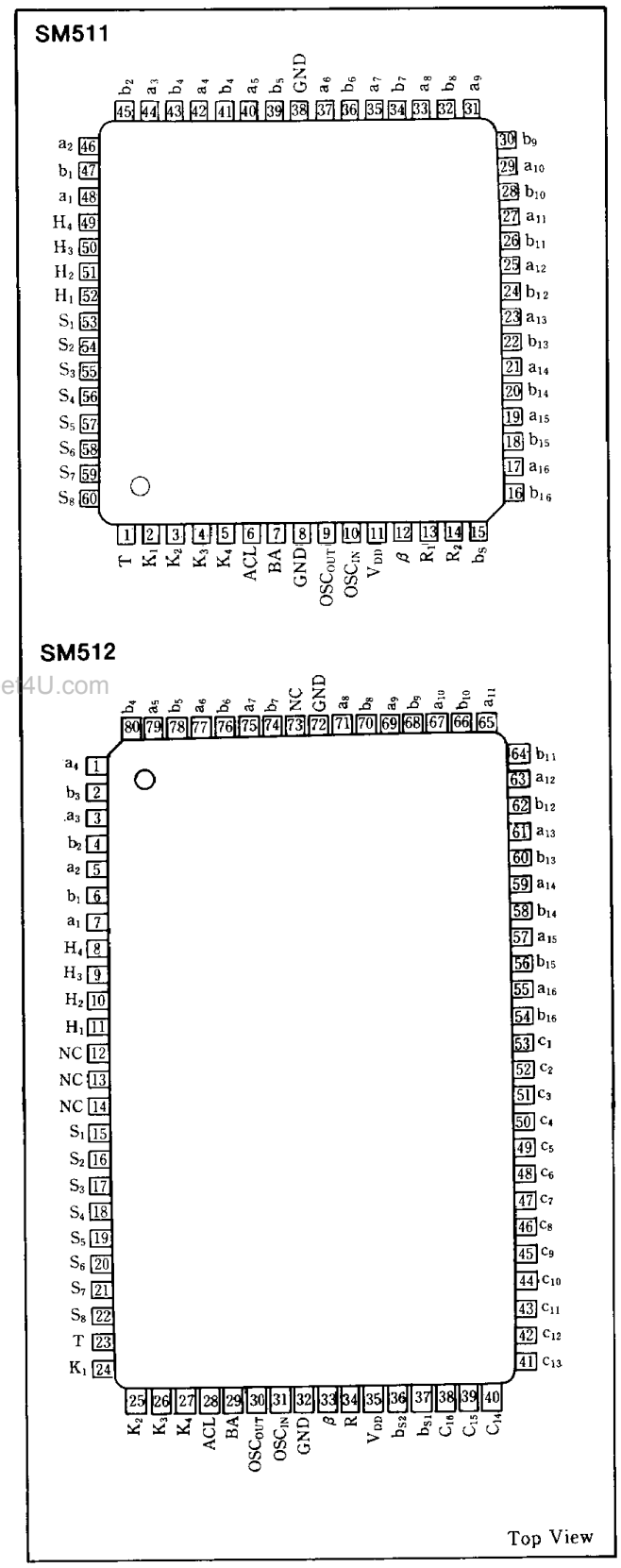
The SM511/SM512 is a CMOS 4-bit microcomputer which integrates a 4-bit parallel processing function, a 4,032×8-bit ROM, a 128/142×4-bit RAM, a 15 stage divider and a 136/200-segment LCD driver circuit.

This microcomputer is applicable to many applications having multiple LCD segments with low-power consumption.

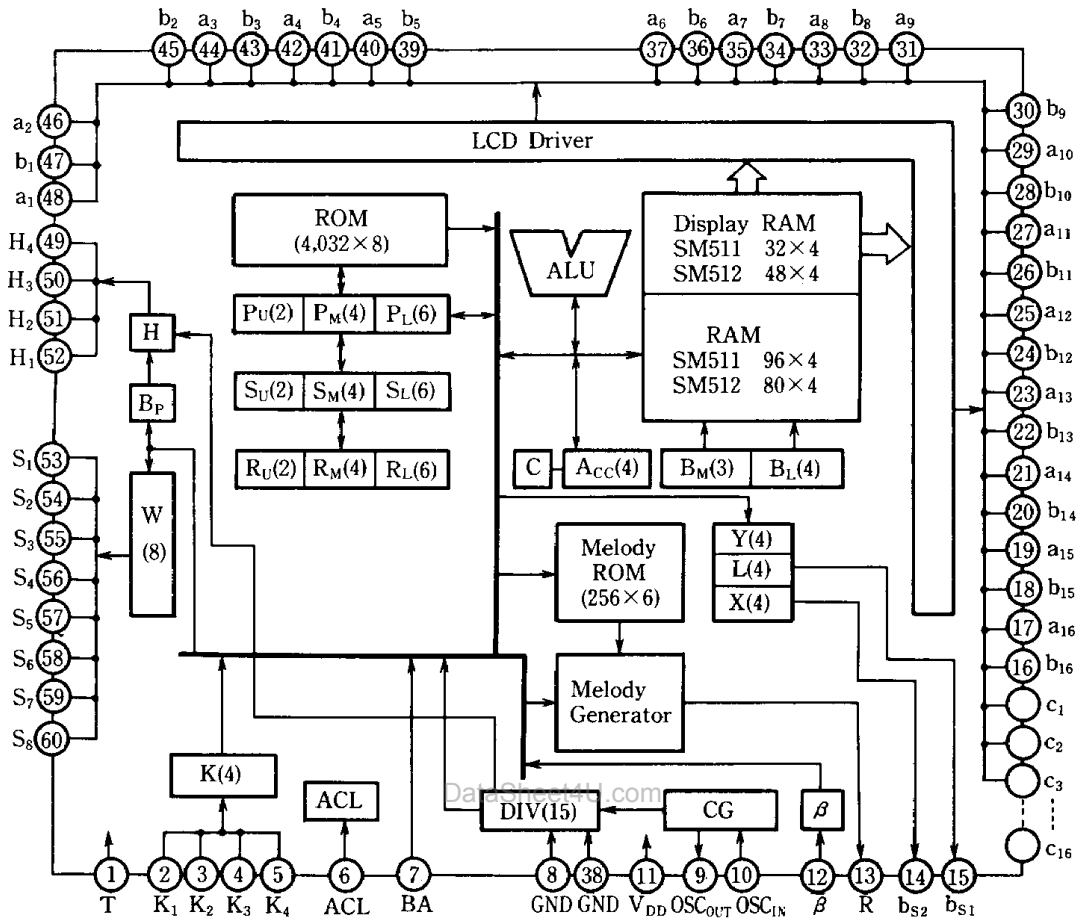
■ Features

1. CMOS process
2. ROM capacity: 4,032×8 bits
3. RAM capacity:
   Data RAM: 96×4 bits (SM511)
   80×4 bits (SM512)
   Display RAM: 32×4 bits (SM511)
   48×4 bits (SM512)
4. Instruction set: 55
5. Subroutine nesting: 2 levels
6. Instruction cycle: 61 μs (TYP.)
7. I/O ports
   Input ports: 6 bits
   Output ports: 9 bits
   LCD output ports
   Segment: 34 bits for SM511
   : 50 bits for SM512
   Common: 4 bits
8. 15-stage divider with reset
9. Melody generator circuit
   (Output time for up to 32 sec.)
10. LCD drive circuit
    3V, 1/4 duty, 1/3 bias,
    136 segments (MAX.) for SM511
    200 segments (MAX.) for SM512
11. Crystal oscillator circuit (32.768kHz)
12. Standby mode: 20 μA
    (Current consumption at clock halt)
13. Single −3V (TYP.) power supply
14. 60-pin QFP (QFP60-P-1414) for SM511
    80-pin QFP (QFP80-P-1420) for SM512

■ Pin Connections



Block Diagram



Symbol description

ALU	: Arithmetic logic unit	W	: 8-bit shift register
Acc	: Accumulator	B_M, B_L	: RAM address register
C	: Carry F/F	B_P	: Backplate signal generator circuit
P_U, P_M, P_L	: Program counter	H, L, X, Y	: 4-bit F/F
S_U, S_M, S_L	: Stack register of program counter	K	: Key input F/F
R_U, R_M, R_L	: Stack register of program counter	CG	: Clock generator
DIV	: Divider		

Note: Pin numbers apply to the SM511. Signals C_1-C_{16} apply to the SM512 only.

Pin Description

Symbol	I/O	Circuit type	Function
ai, bi, ci*	O		Segment output ports (i=1 to 16)
b_{S1}, b_{S2}			
H_1-H_4	O		Common output ports
S_1-S_8	O		Strobe output ports
T	I		Test input port (normally connected to V_{DD})
K_1-K_4	I	Pull down	Key input ports
OSC_{IN}			Crystal oscillator
OSC_{OUT}			
BA, β	I	Pull up	Independent input ports
GND, V_{DD}			Power supply
R	O		Melody output port
ACL	I	Pull down	Auto clear

*The Ci port applies to the SM512 only.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Pin voltage	V_{DD}	−3.5 to +0.3	V	1
	V_{IN}	V_{DD} to +0.3	V	
Operating temperature	Topr	0 to 50	℃	
Storage temperature	Tstg	−55 to +150	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND (GND=0V).

Recommended Operating Conditions

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	−3.2 to −2.6	V
Oscillator frequency	f_{OSC}	32.768 (TYP.)	kHz

■ Electrical Characteristics

(V_{DD} = −3V ± 10%, Ta = 25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH1}		−0.6			V	1
	V_{IL1}				V_{DD}+0.6	V	
	V_{IH2}		−0.3			V	2
	V_{IL2}				V_{DD}+0.3	V	
Input current	I_{IH1}	V_{IN} = 0V	1		15	μA	3
	I_{IH2}	V_{IN} = V_{DD}	1		15	μA	4
Output voltage	V_{OH}	I_{OUT} = 50 μA to V_{DD}	−0.5			V	5
	V_{OL}	I_{OUT} = 5 μA to GND			V_{DD}+0.5	V	
	V_{OA}	V_{DD} = −3.0V No load	−0.3	0		V	6
	V_{OB}		−1.3	−1.0	−0.7	V	
	V_{OC}		−2.3	−2.0	−1.7	V	
	V_{OD}		−3.0	−3.0	−2.7	V	
Output current	I_{SO}	V_{OUT} = −0.2V	100			μA	7
	I_{SIN}	V_{OUT} = V_{DD}+0.2V	100			μA	
Supply current	I_{DA1}	During full-range operation		50		μA	8
	I_{DS1}	When system clock is stationary		20		μA	
	I_{DA2}	During full-range operation		35		μA	9
	I_{DS2}	When system clock is stationary		17		μA	

Note 1: Applied to pins K_1-K_4, β
Note 2: Applied to pins ACL, BA
Note 3: Applied to pins K_1-K_4
Note 4: Applied to pin β
Note 5: Applied to pins S_1-S_8
Note 6: Applied to pins a_1-a_{16}, b_1-b_{16}, c_1-c_{16}, b_{S1}, b_{S2}, H_1-H_4 (c_1-c_{15} apply to the SM512 only)
Note 7: Applied to pin R
Note 8: When melody circuit is inoperative with V_{DD} at −3.0V and system clock at 16.384kHz.
Note 9: When melody circuit is inoperative with V_{DD} at −3.0V and system clock at 8.192kHz.

■ Pin Functions

(1) K_1-K_4 (Inputs)

The K_1-K_4 ports normally pulled down are connected to, and loaded into the accumulator (Acc) by instructions.

A matrix composed of K input ports and strobe output ports (S_1-S_8) enables up to 32 kinds of keys to be connected.

In this case, be sure to take the interval at least 1 step between strobe outputs and K inputs.

(2) BA, β (Individual inputs)

The individual input ports BA and β normally pulled up can be tested using the TAL and TB instructions.

Applying a High level signal to these ports skips the next instruction.

(3) S_1-S_8 (Strobe outputs)

The strobe outputs (S_1-S_8) are used to output an 8-bit W register, and compose a key input matrix in combination with the input ports K_1-K_4.

The W register is an 8-bit register transferred by the PTW instruction in parallel.

The W′register is an 8-bit shift register of which the least significant bit W_1 is set and reset by WS and WR instructions, and the entire contents of W′register are shifted by one bit.

(4) a_1-a_{16}, b_1-b_{16}, c_1-c_{16}, bs_1, bs_2

The segment outputs a_1-a_{16}, b_1-b_{16}, including c_1-c_{16} (for SM512 only) are connected to display RAM. By transferring appropriate data to the display RAM, alphanumeric characters are automatically displayed.

The bs_1 and bs_2 are used to output the contents of L F/F and X F/F.

Segment output ports are designed to drive an LCD with 1/4 duty cycle.

The bs_1 is used to flash the display such as a colon under the control of Y F/F.

(5) H_1-H_4 (Common outputs)

The H_1-H_4 are used to drive an LCD with 1/4 duty cycle and 1/3 bias, and provide a 4 level output.

The common outputs control the BP F/F, BC F/F to select a display mode or blanking mode.

Below shows the conditions of a display mode to be selected.

BP=1 and BC=0

(6) R (Melody output)

An internal melody generator circuit provides a variety of sound signals.

■ Hardware Configuration

(1) Program counter and stack

The program counter consists of a 2-bit register P_U, a 4-bit register R_M and a 6-bit polynomial counter P_L. The P_U and P_M specify the pages and the P_L specifies the steps within a page.

The stack consists of registers S_U, S_M, S_L and R_U, R_M, R_L, and has 2 levels of nesting.

(2) Program memory (ROM)

An on-chip 4,032-bit ROM is organized as 64 pages×63 steps. Fig. 1 shows the ROM configuration.

- When power on, the system starts execution from the address $P_U=3$, $P_M=7$, $P_L=0$ specified by an ACL circuit.
- When the system starts execution from the system clock halt state by a 1S signal or a key input signal, the address starts at $P_U=1$, $P_M=0$, $P_L=0$.
- For the instructions except for a jump instruction, the polynomial counter P_L is shifted by 1 step according to a polynomial code.
- The combination of jump instructions including T, TL, TM, TML, RTN0, RTN1 and ATPL enables to jump to any page or any subroutine. Fig. 2 shows the relationship between jump instructions and jump addresses on a ROM map.

P_M \ P_U	0	1	2	3
0	0 Subroutine cover page	10 Start from CEND	20	30
1	1	11	21	31
2	2	12	22	32
3	3	13	23	33
4	4	14	24	34
5	5	15	25	35
6	6	16	26	36
7	7	17	27	37 Power on
8	8	18	28	38
9	9	19	29	39
A	A	1A	2A	3A
B	B	1B	2B	3B
C	C	1C	2C	3C
D	D	1D	2D	3D
E	E	1E	2E	3E
F	F	1F	2F	3F

Note: 1 page consists of 63 steps.

Fig. 1 ROM configuration

P_M \ P_U	0	1	2	3
0	0 IDX	10 [START]	20	30
1	1	11	21	31
2	2	12	22	32
3	3 TM	13	23	33
4	4	14	24	34
5	5 T	15 TL (Note2)	25	35 TML (Note1)
6	6	16	26	36
7	7	17	27	37 [ACL]
8	8	18	28	38
F	F	1F	2F	3F

Note 1: Jump address of TML should be PM=0 to 3
Note 2: Jump address of TL should be all address.

Fig. 2 Jump instructions and jump address

B_L \ B_M	X 000	Y 001	Z 010	M 011	P 100	Q 101	R 110	S 111
0000								
0001								
0010								
0011								
0100								
0101								
0110								
0111								
1000								
1001								
1010								
1011								
1100								
1101								
1110								
1111								

The area (R, S) enclosed by a thick frame is allocated for a display RAM of the SM511.
The area (Q, R, S) with oblique lines is allocated for a display RAM of the SM512.

Fig. 3 RAM configuration

(3) Data memory RAM

A 512-bit data RAM consists of 8×16×4 bits.

The RAM is specified by a 3-bit B_M and a 4-bit B_L. The B_M is used to specify the files and the B_L specify the words. Note that 1 word consists of 4-bits.

The SM511 has 2×16×4-bits and the SM512 has 3×16×4 bits of display RAM area out of the entire RAM, and the display RAM is connected to external pins for segment outputs.

Writing data to the display RAM directly drives an LCD with 1/4 duty and 1/3 bias scheme.

Fig. 3 shows the RAM map.

(4) Divider circuit for clock function

An internal 15-stage divider circuit is used to make a clock system.

The divider outputs the signal at 1 sec. unit (1S), and γ F/F is set at the rising edge of 1S signal. γ F/F can be tested by an instruction, and reset by the test. A 1 sec. count is notified upon execution of this instruction.

(5) Standby function

The SM511/SM512 is a low power consumption design due to CMOS process. Further low power feature can also be obtained by halting almost all the system clocks by executing the CEND instruction for low power requirements.

γ F/F must be reset or one or more inputs of K_1-K_4 must go High in order to restart the system clock from the halt state. Then the program starts at the ROM address 1000 (P_U=1, P_M=0, P_L=0).

(6) Selection of system clock

Either system clock of 16.384kHz or 8.192kHz can be selected by instructions. Selecting 8.192kHz of clock offers low power consumption with low speed of execution time. The rest of functions are the same with the case when 16.384kHz clock is selected.

The system clock immediately after executing ACL is set to 8.192kHz of clock.

(7) ACL circuit

Resistors and Capacitors are mounted in an ACL circuit which does not normally require any external circuits.

The ACL will be cleared in about 0.5 sec from a crystal oscillator circuit starts oscillation after power on, and the program starts at P_U=3, P_M=7, P_L=0.

The ACL operations can be obtained by transferring signals into the ACL pin after power on. Note that it takes about 0.5 sec to start execution of program after the ACL signal is released.

In case noise may harm the ACL operation, apply a 0.01 to 0.1 μF of capacitor between ACL pin and GND pin.

Fig. 4 shows the sample circuit.

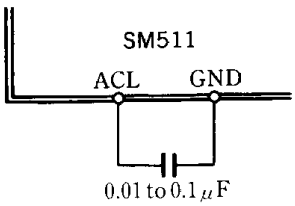


Fig. 4 Compensator for ACL

(8) Melody ROM

A melody ROM is organized as 256 steps×6 bits which executes musical notes, pause and stop instructions.

The melody ROM is used to output 12 musical scales (555 to 2097Hz) in two octaves and select tone length either 125ms or 62.5ms.

It also generates melodies, effect sound, alarms and repeats any part of melodies.

	m_3 m_2 m_1 m_0	Output frequency (Hz)	Clock cycle*	(Note)
do	0 0 1 0	2114.1	15.5	7 8 8 8
si	0 0 1 1	1985.9	16.5	8 8 8 9
la #	0 1 0 0	1872.4	17.5	8 9 9 9
la	0 1 0 1	1771.2	18.5	9 9 9 10
so #	0 1 1 0	1680.4	19.5	9 10 10 10
so	0 1 1 1	1560.4	21.0	10 11 10 11
fa #	1 0 0 0	1489.5	22.0	11 11 11 11
fa	1 0 0 1	1394.4	23.5	11 12 12 12
mi	1 0 1 0	1310.7	25.0	12 13 12 13
re #	1 0 1 1	1236.5	26.5	13 13 13 14
re	1 1 0 0	1170.3	28.0	14 14 14 14
do #	1 1 0 1	1110.8	29.5	14 15 15 15

* : Clock cycle of 32.768kHz

Note: The numerics within waveforms show the clock cycle count of the crystal oscillation frequency 32.768kHz.
As shown in table 1, the melody output waveform is generated with the controlled frequency by amplifying the numerics.

Fig. 5 Melody output frequency

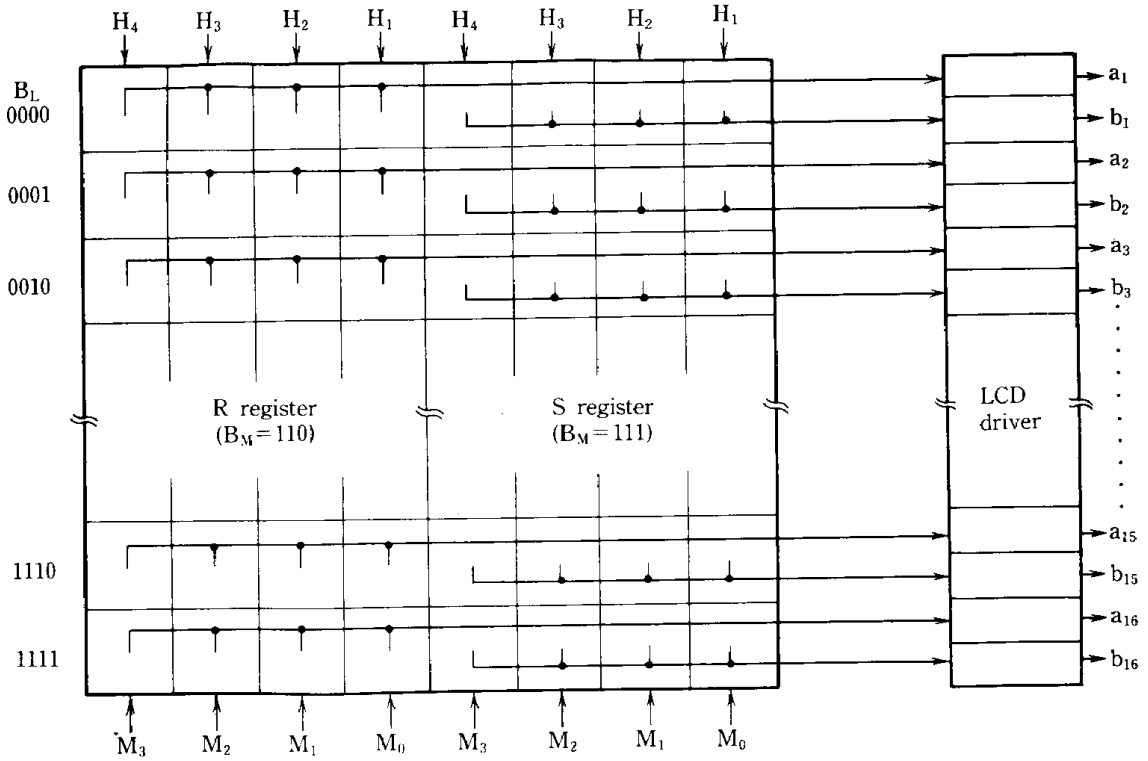


Fig. 6 Display RAM of the SM511 and LCD segment output

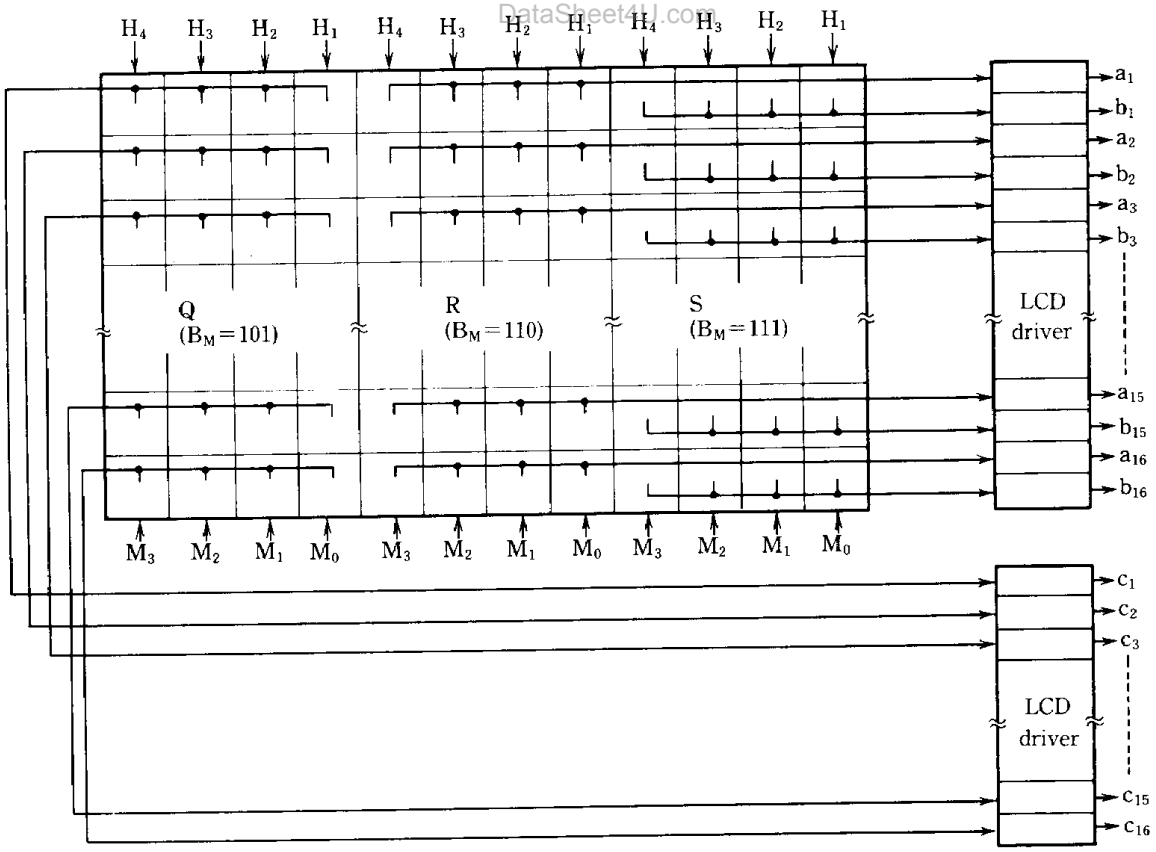


Fig. 7 Display RAM of the SM512 and LCD segment output

(9) LCD driver

• LCD segment

The SM511/SM512 has an on-chip LCD driver circuit which can directly drive an LCD with a 3V, 1/4 duty and 1/3 bias scheme.

The display RAM is connected to segment outputs of a_1-a_{16}, b_1-b_{16} for the SM511 and a_1-a_{16}, b_1-b_{16}, c_1-c_{16} for the SM512 according to LCD common outputs of H_1-H_4 as shown in Fig. 6 and 7.

The segment outputs provide 1-digit data (M_0-M_3) of the display RAM in synchronizing with H_1-H_4 outputs.

Each segment of the LCD can be turned on or off by controlling the corresponding bit data "1" or "0" in the display RAM area.

The LCD driving waveform relative to the display mode is automatically generated. The SM511 provides the maximum of 136 segments, and the SM512 provides 200 segments. Fig. 8 shows the segment display example.

• Display waveform

Fig. 9 shows the display waveforms required to display the number "5" on the LCD pattern of the SM511 and "PM 5" on that of the SM512 shown in Fig. 8 (segment outputs a_1, b_1 for SM511 and a_1, b_1, c_1 for SM512 are used).

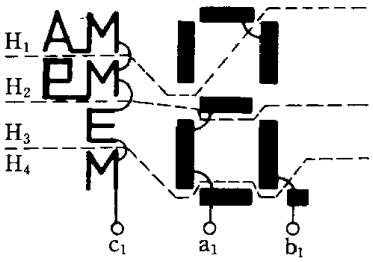


Fig. 8 7-segment numeric LCD digit

• LCD flashing output (bs_1)

The bs_1 output is used to flash symbols displayed on the LCD screen.

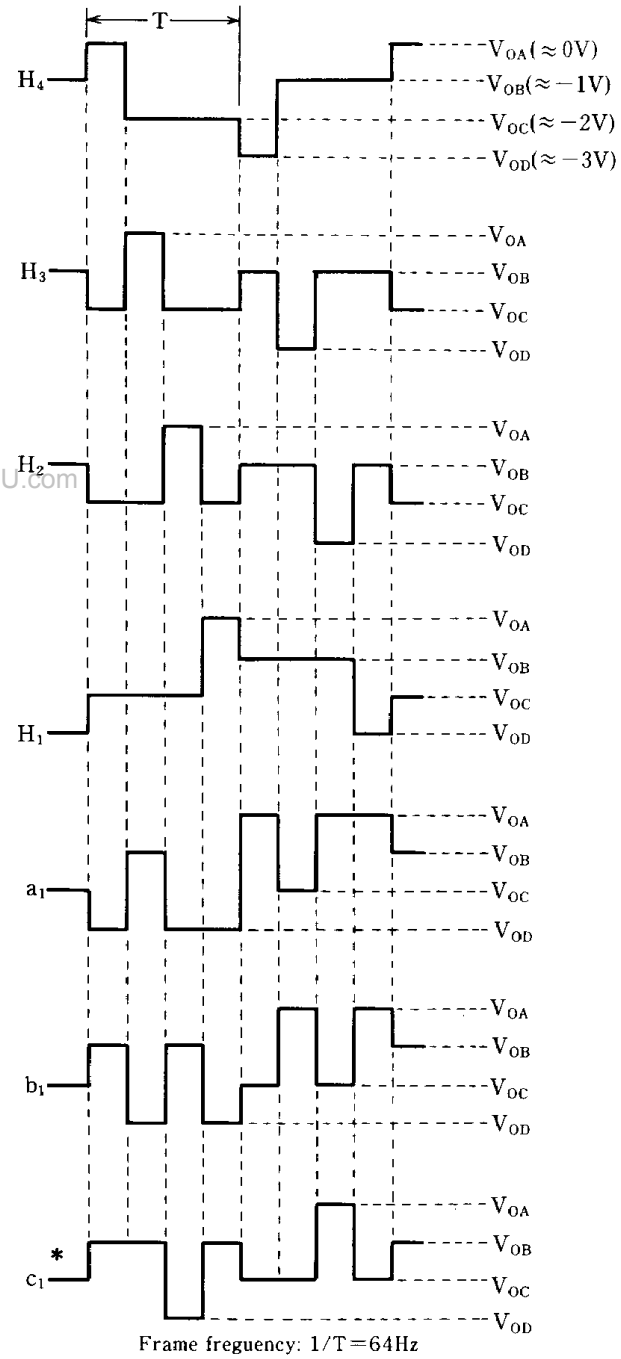
For the 4 segments determined by the combination of the segment output bs_1 and common outputs H_1-H_4, each segment can be turned on and off or flashed.

The flashing time should be on for 0.5 sec and off for 0.5 sec.

• Blanking the display

There are two ways for blanking the entire display depending on applications.

1. When blanking the display for a short period of time, control the common signal generator circuit by the ATBP instruction.
2. When blanking the display for a long period of time to decrease power consumption, use the BDC instruction to turn on and off the liquid crystal bleeder current. In this case, to cut off the bleeder current decreases great amount of power consumption.



Frame freguency: 1/T=64Hz

* C_1 is applicable to the SM512 only

Fig. 9 LCD driving signal waveform

■ Comparison Table of The SM510 Series

		SM510	SM511	SM512	
Process		CMOS	CMOS	CMOS	
ROM capacity		2,772×8	4,032×8	4,032×8	bit
RAM capacity		96×4+32×4	96×4+32×4	80×4+48×4	bit
Supply voltage		−3.2 to −2.6	−3.2 to −2.6	−3.2 to −2.6	V
Instruction set		49	55	55	
Subroutine nesting		2	2	2	level
Input port		6	6	6	
Output port		47	47	63	
Instruction cycle (MIN.)		61	61	61	μs
System clock generator circuit		Yes	Yes	Yes	
Current consumption	CEND	15 μA (TYP.) (Note 1)	20 μA (TYP.) (Note 1) 17 μA (TYP.) (Note 2)	20 μA (TYP.) (Note 1) 17 μA (TYP.) (Note 2)	μA
	Operation	40 μA (TYP.) (Note 1)	50 μA (TYP.) (Note 1) 35 μA (TYP.) (Note 2)	50 μA (TYP.) (Note 1) 35 μA (TYP.) (Note 2)	μA
Operating temperature		0 to 50	0 to 50	0 to 50	℃
Package		60QFP	60QFP	80QFP	
Number of LCD segment		132 (MAX.)	136 (MAX.)	200 (MAX.)	
Melody output		No (4,096kHz sound output)	Yes	Yes	

Note 1: System clock: 16.384kHz
Note 2: System clock: 8.192kHz

■ Instruction Set

(1) RAM address instructions

Mnemonic	Machine code	Operation
LB xy	40-4F	B_{L1}, B_{L0}←x(I_3, I_2) B_{M1}, B_{M0}←y(I_2, I_0)
LBL xy (2-byte)	5F 00-FF	B_M←x(I_6 -I_4), B_L←y(I_3 -I_0)
SBM	02	B_{M2}←1 (only next step)
EXBLA	0B	Acc↔B_L
INCB	64	Skip if B_L=F_H, B_L←B_L+1
DECB	6C	Skip if B_L=0, B_L←B_L−1

(2) ROM address instructions

Mnemonic	Machine code	Operation
ATPL	03	P_{L3}-P_{L0}←Acc
RTN0	6E	P_U←S_U←R_U, P_M←S_M←R_M P_L←S_L←R_L
RTN1	6F	P_U←S_U←R_U, P_M←S_M←R_M P_L←S_L←R_L, Skip next step
TL xyz (2-byte)	70-7F 00-FF	P_M←x(I_3-I_0), P_U←y(I_7-I_6) P_L←z(I_5-I_0)
TML xyz (2-byte)	68-6B 00-FF	R←S←PC+1, P_{M3}, P_{M2}←(0, 0) P_{M1}, P_{M0}←x(I_1, I_0), P_U←y(I_7, I_6) P_L←z(I_5-I_0)
TM x IDX yz (2-byte)	C0-FF 00-FF	R←S←PC+1, P_U←0, P_M←0 P_L←x(I_5-I_0), P_U←y(I_7, I_6) P_L←z(I_5-I_0), P_M←$(0100)_2$
T xy	80-BF	P_L←x(I_5-I_0)

(3) Data transfer instructions

Mnemonic	Machine code	Operation
EXC x	10-13	Acc↔M B_{M1}, B_{M0}←B_{M1}, B_{M0}⊕x(I_1, I_0)
BDC	60-34	BC←C Display on if C=0 Display off if C=1
EXCI x	14-17	Acc↔M B_{M1}, B_{M0}←B_{M1}, B_{M0} ⊕ x(I_1, I_0) Skip if B_L=F_H, B_L←B_L+1
EXCD x	1C-1F	Acc↔M B_{M1}, B_{M0}←B_{M1}, B_{M0} ⊕ x(I_1, I_0) Skip if B_L=0, B_L←B_L−1
LDA x	18-1B	Acc↔M B_{M1}, B_{M0}←B_{M1}, B_{M0} ⊕ x(I_1, I_0)
LAX x	20-2F	Acc←x(I_4-I_1) Skip when in succession
PTW	6D	W_i←W_i (i=7 to 0)
WR	62	W_0←0, W_{i+1}←W_i (i=6 to 0)
WS	63	W_0←1, W_{i+1}←W_i (i=6 to 0)

(4) I/O instructions

Mnemonic	Machine code	Operation
KTA	50	Acc←K
ATBP (2-byte)	60 35	BP←Acc
ATX	5C	X←Acc
ATL	59	L←Acc
ATFC (2-byte)	60 33	Y←Acc

(5) Arithmetic instructions

Mnemonic	Machine code	Operation
ADD	08	Acc←Acc+M
ADD11	09	Acc←Acc+M+C, C←CY Skip if CY=1
ADX x	30-3F	Acc←Acc+x(I_3-I_0) Skip if CY=1
COMA	0A	Acc←$\overline{\text{Acc}}$
DC	3A	Acc←Acc+$(1010)_2$
ROT	00	C←Acc_0, Acc_i←Acc_{i+1} (i=2 to 0), Acc_3←C
RC	66	C←0
SC	67	C←1

(6) Test instructions

Mnemonic	Machine code	Operation
TB	51	Skip if β=1
TC	52	Skip if C=0
TAM	53	Skip if Acc=M
TMI x	54-57	Skip if M_i=1, (i=x(I_1, I_0))
TA0	5A	Skip if Acc=0
TABL	5B	Skip if Acc=B_L
TIS	58	Skip if IS=0, r←0
TAL	5E	Skip if BA=1

(7) Bit manipulation instructions

Mnemonic	Machine code	Operation
RM x	04-07	M_i←0 (i=x(I_1, I_0))
SM x	0C-0F	M_i←I (i=x(I_1, I_0))

(8) Melody control instructions

Mnemonic	Machine code	Operation
PRE x (2-byte)	61 00-FF	Melody ROM pointer preset
SME (2-byte)	60 31	ME←1
RME (2-byte)	60 30	ME←0
TMEL (2-byte)	60 32	Skip if MES=1, MES←0

■ System Configulation Example